**User manual** 



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# 1 Introduction

This document is the user guide for the KITFS26SKTEVM programming board. This document is intended for the engineers involved in the evaluation, design, implementation, and validation of FS26 Fail-safe system basis chip with multiple SMPS and LDO.

The scope of this document is to provide the user with information to evaluate the FS26 Fail-safe system basis chip with multiple SMPS and LDO. This document covers connecting the hardware, installing the software and tools, configuring the environment and using the kit.

The board contains a socket for LQFP48 package in order to allow functional testing and programming of different samples.

# 2 Finding kit resources and information on the NXP web site

NXP Semiconductors provides online resources for this evaluation board and its supported device(s) on <u>http://www.nxp.com</u>.

The information page for KITFS26SKTEVM evaluation board is at <a href="http://www.nxp.com/KITFS26SKTEVM">http://www.nxp.com/KITFS26SKTEVM</a>. The information page provides overview information, documentation, software and tools, parametrics, ordering information and a **Getting Started** tab. The **Getting Started** tab provides quick-reference information applicable to using the KITFS26SKTEVM evaluation board, including the downloadable assets referenced in this document.

# 2.1 Collaborate in the NXP community

The NXP community is for sharing ideas and tips, ask and answer technical questions, and receive input on just about any embedded design topic.

The NXP community is at <u>http://community.nxp.com</u>.

# 3 Getting ready

Working with the KITFS26SKTEVM requires the kit contents, additional hardware and a Windows PC workstation with installed software.

# 3.1 Kit contents

- Assembled and tested evaluation board and preprogrammed FRDM-KL25Z microcontroller board in an anti-static bag
- 3.0 ft USB-STD A to USB-B-mini cable
- Two connectors, terminal block plug, 2 pos., str. 3.81 mm
- Three connectors, terminal block plug, 3 pos., str. 3.81 mm
- · Jumpers mounted on board
- Quick start guide

# 3.2 Additional hardware

In addition to the kit contents, the following hardware is necessary or beneficial when working with this kit.

• Power supply with a range of 8.0 V to 40 V and a current limit set initially to 1.0 A

# 3.3 Windows PC workstation

This evaluation board requires a Windows PC workstation. Meeting these minimum specifications should produce great results when working with this evaluation board.

• USB-enabled computer with Windows 7 or Windows 10

# 3.4 Software

Installing software is necessary to work with this evaluation board.

• NXP GUI installation package

# 4 Getting to know the hardware

# 4.1 Kit overview

The KITFS26SKTEVM provides flexibility to play with all the features of the device and make measurements on the main part of the application. The KL25Z Freedom connected to the board, combined with the FS26 NXP GUI software allows to fully configure and control FS26 SBC. The LQFP48 Socket on board allows to test or to program different samples.

An FS26 SBC sample must be inserted in the socket to enable OTP programming, emulation or evaluation. The performance on this board is limited and KITFS26SKTEVM must be used for further evaluation.

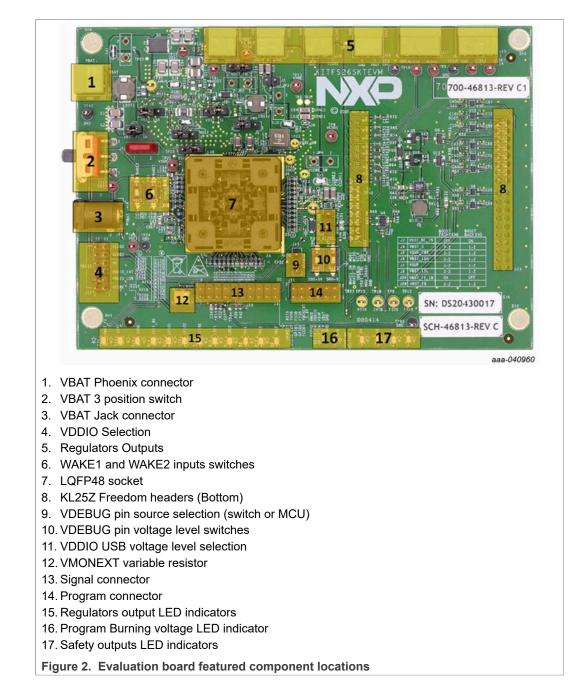
# 4.1.1 KITFS26SKTEVM features

- VBAT power supply connectors (Jack and Phoenix)
- LQFP48 burn in open top Socket
- VPRE output 3.2 V to 6.35 V
- VBOOST in Independent mode or in Front end topology to support battery cranking profiles
- VCORE output 0.8 V to 3.3 V
- LDO1 and LDO2, from 3.3 V or 5.0 V, up to 400 mA
- VTRK1 and VTRK2, from 3.3 V or 5.0 V, up to 125 mA
- VREF 1% accuracy regulator for external ADC reference
- FS0B, FS1b external safety pins
- USB to SPI protocol for easy connection to software GUI.
- LEDs that indicate signal or regulator status
- Manual or Automated OTP fuse programming.
- Advance system monitoring via AMUX or external ADC.
- · Analog variable resistor to test external VMON

# 4.2 Kit featured components

Figure 2 identifies the location of some of the main KIT features.

# KITFS26SKTEVM evaluation board



# 4.2.1 LQFP48 open top socket

This KIT is equipped with an LQFP48 open socket. This socket enables FS26 family OTP emulation and OTP programming on several samples with easy insertion or replacement. Socket part number is NP584-048-113 Yamaichi (maximum current per pin 1 A).

In order to insert or change a device you must push the top of the socket and keep it pressed, then carefully insert the IC with aligned pins. Pin 1 is on the top left of the socket.

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### KITFS26SKTEVM evaluation board

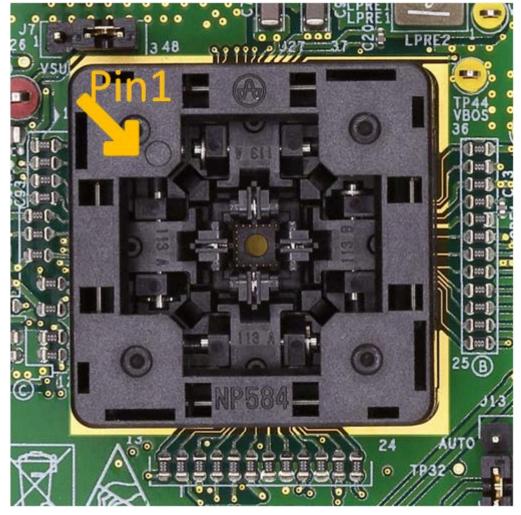


Figure 3. IC insertion on socket

# 4.2.2 VBAT connectors

There are two ways of supplying the board: either by a Phoenix Connector (J2) or a Jack connector (J2). The selection of the supplying connector is done thanks to a three-position switch (SW1). Figure 4 shows related schematic. Nominal VBAT voltage is 12 V and can support up to 40 V.

Table 1. VBAT Phoenix connector (J20)

| Schematic label | Signal name | Description                  |
|-----------------|-------------|------------------------------|
| J20-1           | VBAT        | Battery voltage supply input |
| J20-2           | GND         | Ground                       |

Table 2. VBAT three position connector (SW1)

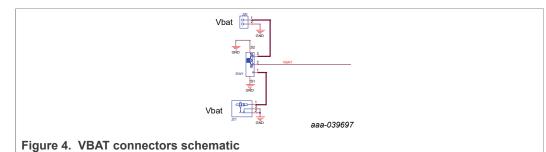
| Schematic label | Signal name  | Description                         |
|-----------------|--------------|-------------------------------------|
| SW1 pin 2-3     | VBAT Phoenix | Board supplied by Phoenix connector |

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| Schematic label             |           | Description                      |
|-----------------------------|-----------|----------------------------------|
| SW1 pin 2 (Middle position) | VBAT      | Board not supplied               |
| SW1 pin 2-1                 | VBAT jack | Board supplied by jack connector |

Table 2. VBAT three position connector (SW1)...continued



# 4.2.3 Power topology configuration

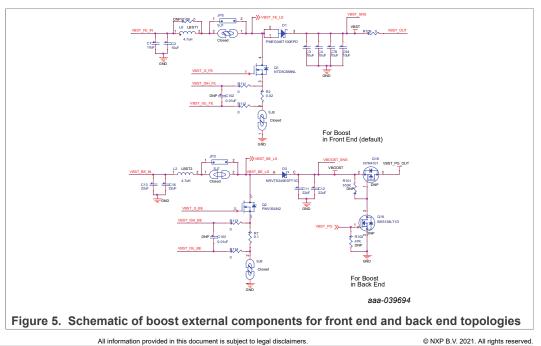
There are two power topologies available depending on the application and OTP configuration. The device can be supplied directly by the battery after diode and pi filter; on the other side, the boost regulator can be connected in Front end topology to support cold cranking profiles.

It is possible to evaluate both power topologies with this board since external boost components for each topology are soldered separately as shown in <u>Figure 5</u>.

A set of jumper configurations allows you to select between the two options. See <u>Figure 6</u> and <u>Table 3</u>. Default jumper configuration is boost in front end topology.

In front end topology boost is connected to the battery after reverse diode; the output of the boost supplies the device during cold cranking profiles. Otherwise, boost stops switching, and it is bypassed. See reference [1] for more information.

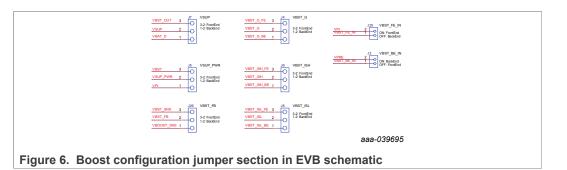
In back end topology or independent boost, the device is supplied by the battery, and the boost is supplied by the buck regulator VPRE.



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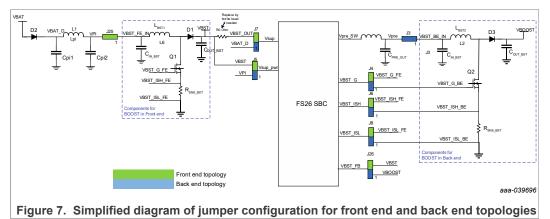
# KITFS26SKTEVM evaluation board



| Table 3  | lumpor | configuration | for front o | nd and ha | ck and r | ower topologies  |
|----------|--------|---------------|-------------|-----------|----------|------------------|
| Table 5. | Jumper | configuration | ior mont e  | nu anu ba | ck enu p | lower topologies |

| Schematic label | Signal Name | BOOST Front end<br>(Default positions) | BOOST Back end |
|-----------------|-------------|--|----------------|
| J25             | VBST_FE_IN  | ON                                     | OFF            |
| J3              | VBST_BE_IN  | OFF                                    | ON             |
| J7              | VSUP        | 3-2                                    | 1-2            |
| J5              | VSUP_PWR    | 3-2                                    | 1-2            |
| J4              | VBST_G      | 3-2                                    | 1-2            |
| J6              | VBST_ISH    | 3-2                                    | 1-2            |
| J8              | VBST_ISL    | 3-2                                    | 1-2            |
| J26             | VBST_FB     | 3-2                                    | 1-2            |

Figure 7 shows a simplified diagram of jumper configuration to associated device pins.

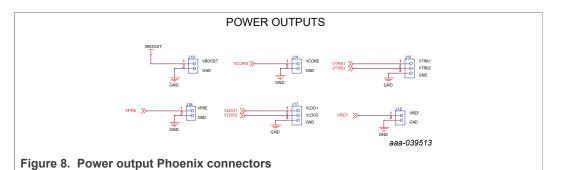


When testing the FS26 SBC with a front end configuration at very low battery level and loading product at its maximum rating, make sure that the power supply is capable of providing at least 4 A.

# 4.2.4 Output power supply connectors

Output regulators are accessible through test points or Phoenix connectors in order to make measurement or plug loads. Male connectors are included on this kit to plug or unplug wires easily. All output regulators are located at the top edge of the board as shown in Figure 2.

# KITFS26SKTEVM evaluation board



#### Table 4. VBOOST connector (J19)

| Schematic label | Signal name | Description                |
|-----------------|-------------|----------------------------|
| J19-1           | VBOOST      | VBOOST power supply output |
| J19-2           | GND         | Ground                     |

#### Table 5. VPRE connector (J16)

| Schematic label | Signal name | Description              |  |
|-----------------|-------------|--------------------------|--|
| J16-1           | VPRE        | VPRE power supply output |  |
| J16-2           | GND         | Ground                   |  |

#### Table 6. VCORE connector (J14)

| Schematic label | Signal name | Description               |
|-----------------|-------------|---------------------------|
| J16-1           | VCORE       | VCORE power supply output |
| J16-2           | GND         | Ground                    |

#### Table 7. VLDO1/VLDO2 connector (J17)

| Schematic label | Signal name | Description              |
|-----------------|-------------|--------------------------|
| J17-1           | LDO1        | LDO1 power supply output |
| J17-2           | LDO2        | LDO2 power supply output |
| J17-3           | GND         | Ground                   |

#### Table 8. VTRK1/VTRK2 connector (J15)

| Schematic label | Signal name | Description               |
|-----------------|-------------|---------------------------|
| J15-1           | VTRK1       | VTRK2 power supply output |
| J15-2           | VTRK2       | VTRK1 power supply output |
| J15-3           | GND         | Ground                    |

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#### Table 9. VREF connector (J18)

| Schematic label | Signal name | Description           |
|-----------------|-------------|-----------------------|
| J18-1           | VREF        | VREF reference output |
| J18-2           | GND         | Ground                |

### 4.2.5 Signal and program connectors

Signal and program connectors allow access to most of the device signals in order to program the device externally or to perform debug and diagnosis.

| Schematic label | Signal name  | Description   |
|-----------------|--------------|---|
| J23_1           | VMONEXT      | External monitoring, resistor bridge side   |
| J23_2           | RSTB         | RSTB IC safety output   |
| J23_3           | VDDIO_EXT    | Optional external supply for VDDIO, make sure that there is a jumper between J12 5-6 pins |
| J23_4           | INTB         | INTB interruption output  |
| J23_5           | GPIO1        | GPIO1 IC side, for signal access; disconnect R87 before use as an output                  |
| J23_6           | FS0B         | FS0B IC safety output   |
| J23_7           | GPIO2        | GPIO2 IC side, for signal access; disconnect R87 before use as an output                  |
| J23_8           | FS1B         | FS1B IC safety output   |
| J23_9           | FCCU1        | FCCU1   |
| J23_10          | VMONEXT_0.8V | VMONEXT IC side, for access or disconnect R39 to apply 0.8 V externally                   |
| J23_11          | FCCU2        | FCCU2   |
| J23_12          | AMUX         | AMUX pin read   |
| J23_13          | GPIO1_IN     | GPIO1 input side  |
| J23_14          | VDDIO        | VDDIO IC side access  |
| J23_15          | GPIO2_IN     | GPIO2 input side  |
| J23_16          | VSUP         | VSUP pin access   |
| J23_17          | DBG_OTP      | DBG_OTP power supply(8V) access   |
| J23_18          | VBAT         | VBAT access   |
| J23_19          | GND          | GND   |
| J23_20          | GND          | GND   |

Table 10. Signal connector (J23)

# KITFS26SKTEVM evaluation board

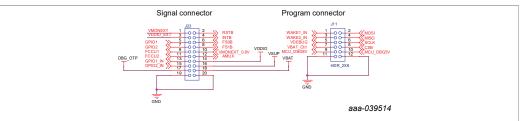


Figure 9. Signal and debug headers connectors

| Schematic label | Signal name | Description  |
|-----------------|-------------|--|
| J11_1           | WAKE1_IN    | WAKE1 input access   |
| J11_2           | MOSI        | MOSI signal access   |
| J11_3           | MISO        | MOSI signal access   |
| J11_4           | WAKE2_IN    | WAKE2 input access   |
| J11_5           | VDEBUG      | VDEBUG pin   |
| J11_6           | SCLK        | SCLK signal access   |
| J11_7           | VBAT_Ctrl   | VBAT_Ctrl KL25Z output access; to control VBAT power by MCU, JP1 must be OFF |
| J11_8           | CSB         | CSB signal access  |
| J11_9           | MCU_DBG8V   | MCU_DBG8V KL25Z output access  |
| J11_10          | MCU_DBG5V   | MCU_DBG5V KL25Z output access  |
| J11_11          | GND         | GND  |
| J11_12          | GND         | GND  |

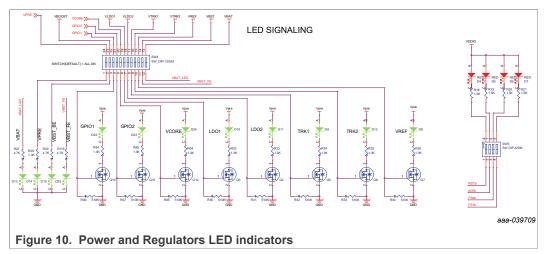
#### Table 11. Program connector (J11)

# 4.2.6 Indicators

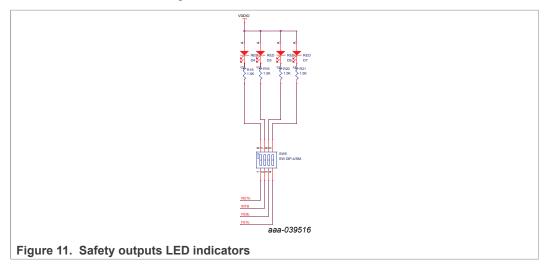
On this board there are LEDs to display VBAT regulators, safety outputs, and GPIO status. For VBAT, regulators and GPIOs there are GREEN LEDs indicating that the output is powered on. The power supply of these indicators is usually VPRE, and it is controlled by a low voltage MOSFET by the corresponding signal or regulator.

These regulators can be turned off manually at any time with the switch SW4 in order to avoid undesired losses and obtain more accurate current consumption measurements.

# KITFS26SKTEVM evaluation board



The color of the Safety outputs LED indicators is RED. When the safety output is asserted, LED indicators are turned on and off when the safety output is released. LEDs can be disabled as well using switch SW5.

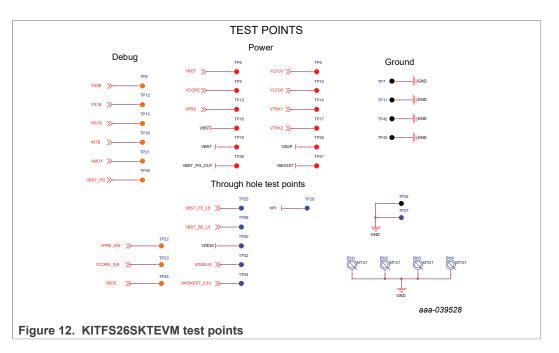


# 4.2.7 Test points

The KITFS26SKTEVM evaluation board has several test points for easy access and measurements. The test points are color coded, and can be different part numbers or without a part number, as shown in Figure 12.

- Orange: Test loop access to device signals such as safety outputs, analog pins and regulator switch nodes.
- Red: Test loop access for power supplies
- Black: Test loop access to GND
- Blue: Not a part; through hole small test points on board close to the signal

# KITFS26SKTEVM evaluation board

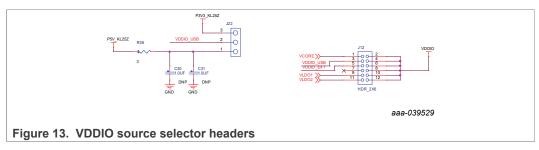


# 4.2.8 VDDIO selection

VDDIO reference can be supplied by 3.3 V or 5 V depending on the system. The supply can be generated on board, from a voltage regulator, or from an external source.

J12 allows selection of the supply source, as shown in <u>Table 12</u>.

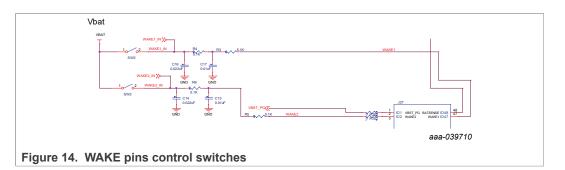
| Table 12. VDDIO connector (J12) |             |                                   |  |  |
|---------------------------------|-------------|-----------------------------------|--|--|
| Schematic label                 | Signal name | Description                       |  |  |
| J12_1-2                         | VCORE       | VDDIO supply is VCORE             |  |  |
| J12_3-4(Default)                | VDDIO_USB   | VDDIO supply is VDDIO_USB(J22_2)  |  |  |
| J12_5-6                         | VDDIO_EXT   | VDDIO supply is VDDIO_EXT (J23_3) |  |  |
| J12_7-8                         | NC          | VDDIO Not connected               |  |  |
| J12_9-10                        | VLDO1       | VDDIO supply is VLDO1             |  |  |
| J12_11-12                       | VLDO2       | VDDIO supply is VLDO2             |  |  |



# 4.2.9 Wake input switches

Wake inputs can be exercised by switches SW2 for WAKE1\_IN and SW3 for WAKE2\_IN. These interrupts are supplied by the battery to VBAT signal.

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# 4.2.10 VDebug pin voltage control

VDEBUG pin allows FS26 SBC to enter the different operating modes to perform debug or programming by applying different voltage thresholds or sequences. These thresholds can be generated on board and debug pin can be controlled manually or fully automated by KL25Z.

The selection for manual (default) or automatic is done by J13.

 Table 13.
 Debug control selector (J13)

| Schematic label | Signal name      | Description                                |
|-----------------|------------------|--|
| J13_1-2         | Manual (default) | Debug threshold are control by SW6 and SW7 |
| J13_2-3         | Automatic        | Debug thresholds are controlled by KL25Z   |

Different voltage levels and sequences can be used to enter debug mode, emulate an OTP configuration, or burn an OTP configuration to the fuses. The threshold levels are:

- VDEBUG < VDBG4TH (VDEBUG < 4.2 V): Waive debug entry at power up or after low power modes exit.
- VDEBUG > VDBG4TH (VDEBUG > 4.2 V): Enter debug mode at power up or after low power modes exit.
- VDEBUG VDBG65TH (VDEBUG > 6.9 V): Burning level for OTP programming.

The power supply to generate the debug entry voltage threshold comes from KL25Z USB. This means that Freedom and USB must be plugged in. Burning voltage for OTP is generated by an on-board boost IC that is also powered by KL25Z Freedom.

For Manual mode use SW6 to allow connection to 5 V power supply, and SW7 to connect to 8 V power supply; when VDBG65TH is reached a blue LED (D19) turns on. <u>Table 14</u> shows the possible output voltage level to apply to VDebug pin depending on SW6 and SW7 positions.

| SW6 | SW7 | VDebug (J13-2) voltage level |
|-----|-----|------------------------------|
| OFF | OFF | 0 V                          |
| OFF | ON  | 7.8 V                        |
| ON  | OFF | 4.5 V                        |
| ON  | ON  | 7.8 V                        |

 Table 14. SW6 and SW7 VDebug output configuration

When automatic mode is selected on connector J13 and KL25Z is plugged in and used, 5 V and 8 V thresholds can be controlled on the NXP GUI by KL25Z signals. It is

#### KITFS26SKTEVM evaluation board

also possible to control VBAT by an MCU signal to generate automated sequences for program and emulations; these signals are:

- VBAT\_Ctrl: Open or close VBAT power supply
- MCU\_DBG5V: 5 V on VDebug pin
- MCU\_DBG8V: 8 V on VDebug pin

#### Debug mode entry

To enter debug mode, follow the below sequence:

- 1. VBAT OFF (SW1)
- 2. VDebug (J13) > VDBG4TH
- 3. VBAT ON (SW1)
- At this step debug mode is enabled and you can emulate an OTP configuration or access the SPI register map. You can read FS\_STATES register to verify you are in debug mode.

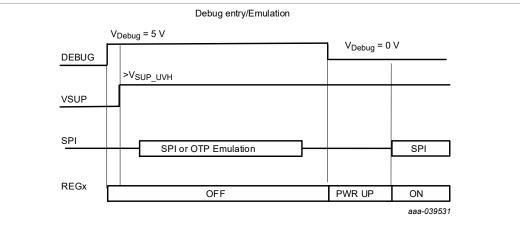


Figure 15. Debug entry voltage sequence

#### OTP programming

To burn an OTP configuration on the fuses permanently, the following sequence must be applied. More detailed instructions are explained in <u>Section 8.5 "Program an OTP configuration"</u>.

- 1. VBAT OFF (SW1)
- 2. VDebug (J13) > VDBG4TH (SW6 ON).
- 3. VBAT ON (SW1)
- At this step debug mode is enabled and you can emulate an OTP configuration or access the SPI register map. You can read FS\_STATES register to verify you are in debug mode.
- VDebug (J13) > VDBG65TH (SW7 ON). If the threshold is applied D19 blue LED turns on.
- 6. Load an OTP configuration file and wait until all commands are sent.
- 7. Put VDebug (J13) to 0 V (first SW7 and then SW6)
- 8. The device should power up with selected OTP configuration or you can restart the device power supply to load the burned OTP configuration from fuses.

# KITFS26SKTEVM evaluation board

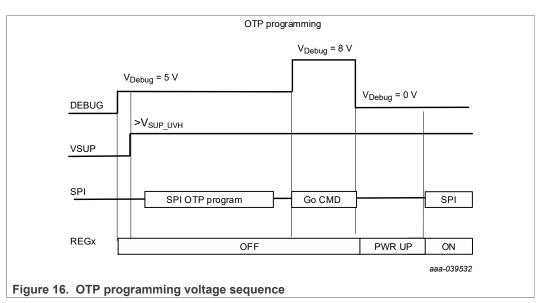
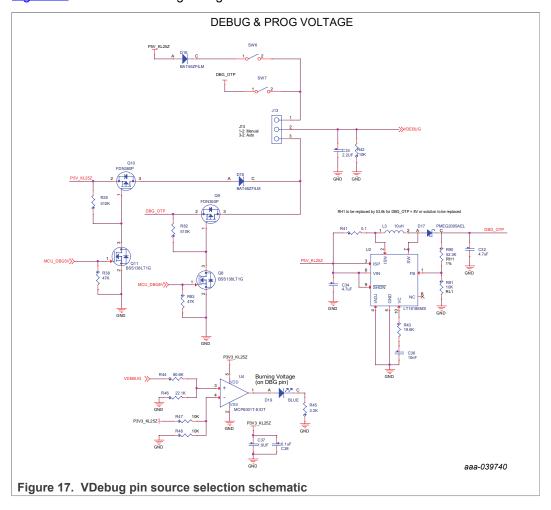


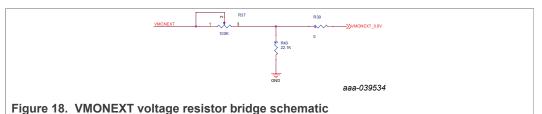
Figure 17 shows the VDebug voltage sources and its selection.



### 4.2.11 VMONEXT monitoring

FS26 VMONEXT monitoring pin can be accessed in different ways. VMONEXT value should always be 0.8 V if used. VMONEXT signal can be supplied by any source or regulator and VMONEXT\_0.8V value can be adjusted by using a screwdriver on R37 potentiometer. Default bridge resistor is 22.2 k $\Omega$ .

To apply 0.8 V directly to VMONEXT\_0.8V, remove R39 and apply 0.8 V to connector J10\_1.



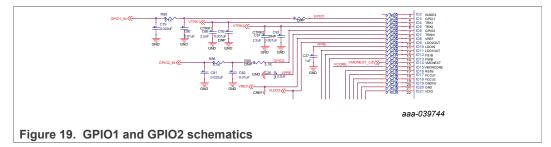
# 4.2.12 GPIO1 and GPIO2

GPIO1 and GPIO2 FS26 pins are connected by default as outputs, and can be accessed by J10 connector.

- J10\_5 for GPIO1
- J10\_7 for GPIO2.

To exercise GPIO pins as inputs, R87 and R89 must be populated in order to apply voltage before RC filter. GPIO input supply can be applied through J10 header.

- GPIO1\_IN can be access through J10\_13, R87 must be populated.
- GPIO2\_IN can be access through J10\_15, R89 must be populated.



**Note:** There are no external pull-ups or pull-downs for the GPIO. If the internal pull-ups or pull-downs are not enabled by OTP you can add external PU/PD through J10.

# 4.3 Default jumper configuration

KIT is provided with the below default jumper configuration. This configuration is suited for a Boost in front end topology.



Figure 20. Default jumper configuration on KITFS26SKTEVM

# 4.4 Schematic, board layout and bill of materials

The schematic, board layout and bill of materials for the KITFS26SKTEVM evaluation board are available at <u>http://www.nxp.com/KITFS26SKTEVM</u>.

# 5 Installing and configuring software and tools

# 5.1 Flashing or updating the GUI firmware

The KITFS26SKTEVM is delivered with the GUI firmware flashed. If MCU firmware is flashed, ignore this section. If it is specified to update the firmware or it is malfunctioning, follow these instructions:

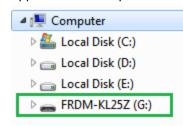
### 5.1.1 Flashing Freedom board firmware for Windows 7

Steps 1 and 2 are not required if BOOTLOADER is already loaded in the Freedom board and a start is required from Step 3.

- 1. Press the RST push button and connect the USB cable into the SDA port on the Freedom board.
  - A new "BOOTLOADER" device should appear on the left pane of the File explorer.
- 2. Drag and drop the file "MSD-DEBUG-FRDM-KL25Z\_Pemicro\_v118.SDA" into the BOOTLOADER drive.
  - **Note:** Make sure to allow enough time for the firmware to be saved in the Boot loader.

# KITFS26SKTEVM evaluation board

- 3. Disconnect and reconnect the USB cable into the SDA port.
  - This time WITHOUT pressing the RST push button, FRDM\_KL25Z device should appear on the left pane of the File explorer as pictured below.



- 4. Locate the file "nxp-gui-fw-frdmkl25z-usb\_hid-fs2630\_vX.Y.bin" from the package and drag and drop the file into the FRDM\_KL25Z device.
  - Note: Make sure to allow enough time for the firmware to be saved.
- 5. Freedom board Firmware is successfully loaded. Disconnect and reconnect the USB cable into the KL25Z USB port.

#### 5.1.2 Flashing Freedom board firmware from Windows 10

1. Disable the storage services: Run the services, double click on the storage service from the list and press the stop button.

|  | Q Services       |   |   |   | - 🗆                | ×                          |
|--|------------------|---|---|---|--------------------|----------------------------|
|  | File Action View | w Help  |   |   |                    |                            |
|  | <b>* *</b> 📷 🗐   | ā 🗟 📘 🖬 🕨 🖬 🖬 🕨   |   |   |                    |                            |
|  | Services (Local) | Services (Local)  |   |   |                    |                            |
|  |                  | Storage Service   | Name  | Description                                   | Status             | Start *                    |
| Run  | ×                | Stop the service<br>Restart the service   | Snow Inventory Client<br>Software Protection<br>Spot Verifier   | This is the S<br>Enables the<br>Verifies pote |                    | Autc<br>Autc<br>Man        |
|  |                  | Description:<br>Provides enabling services for storage<br>settings and external storage | SSDP Discovery     State Repository Service     State Repository Service     Still Image Acquisition Events | Discovers n<br>Provides re<br>Launches a      | Running<br>Running | Man<br>Man<br>Man          |
| Type the name of a program, folder, document, or     |                  | expansion   | Storage Service   | a contract of the second states of            | Running            |                            |
| Internet resource, and Windows will open it for you. | ~                |   | Storage Tiers Management Superfetch Symantec Endpoint Protecti Symantec Network Access                      |   | Running<br>Running | Man<br>Auto<br>Auto<br>Man |
|  |                  |   | Synaptics FP WBF Policy Ser   |   | Running            | Auto<br>Auto               |
|  |                  |   | SynTPEnh Caller Service   |   | Running            | Aute *                     |
| OK Cancel Browse.                                    |                  | Extended / Standard /   |   |   |                    |                            |

Steps 2 and 3 are not required if BOOTLOADER is already loaded in the Freedom board and a start is required from Step 4.

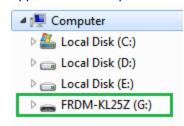
2. Press the RST push button and connect the USB cable into the SDA port on the Freedom board.

a. A new "BOOTLOADER" device should appear on the left pane of the File explorer.

- 3. Drag and drop the file "MSD-DEBUG-FRDM-KL25Z\_Pemicro\_v118.SDA" into the BOOTLOADER drive.
  - a. **Note:** Make sure to allow enough time for the firmware to be saved in the Boot loader.

# KITFS26SKTEVM evaluation board

- 4. Disconnect and reconnect the USB cable into the SDA port.
  - This time WITHOUT pressing the RST push button, FRDM\_KL25Z device should appear on the left pane of the File explorer as pictured below.



- 5. Locate the file "nxp-gui-fw-frdmkl25z-usb\_hid-fs2630\_vX.Y.bin" from the package and drag and drop the file into the FRDM\_KL25Z device.
  - Note: Make sure to allow enough time for the firmware to be saved.
- 6. Freedom board Firmware is successfully loaded. Disconnect and reconnect the USB cable into the KL25Z USB port.

# 5.2 Installing GUI software package

To install the FS26 NXP GUI Download or obtain the NXP GUI package, unzip an open 1-NXP\_GUI\_Setup folder:

| Name                | Status  | Date modified     | Туре          | Size |
|---------------------|---------|-------------------|---------------|------|
| 🔒 0 - Documentation | $\odot$ | 6/8/2020 10:57 AM | File folder   |      |
| 1 - NXP_GUI_Setup   | g       | 6/8/2020 5:26 PM  | File folder   |      |
| 2 - KL25Z_FW        | $\odot$ | 6/4/2020 1:42 PM  | File folder   |      |
| LICENSE.txt         | $\odot$ | 6/4/2020 11:14 AM | Text Document | 3 KB |

Then double click on the NXP\_GUI\_version-Setup.exe and follow the instructions.

| Name                         | Status | Date modified    | Туре        | Size      |  |
|------------------------------|--------|------------------|-------------|-----------|--|
| ( ■ NXP_GUI-3.1.45-Setup.exe | g      | 6/6/2020 6:55 PM | Application | 64,336 KB |  |

Proceed with the following pop-up windows to install the application on Windows PC:

# KITFS26SKTEVM evaluation board

|            | 당 NXP_GUI 3.1.45 Setup   |   |  | _   |                                | × |
|------------|--|---|--|---|--------------------------------|---|
|            |  | Welcome to N<br>Setup will guide you thr<br>3.1.45.<br>It is recommended that<br>before starting Setup.<br>relevant system files wi<br>computer.<br>Click Next to continue. | ough the ir<br>you close<br>This will ma | nstallation of M<br>all other applic<br>ike it possible i | IXP_GUI<br>ations<br>to update | 2 |
|            |  |   |  | Next >  | Cance                          | 8 |
| Figure 21. | Application setup initial  | window  |  |   |                                |   |
|            | NXP_GUI 3.1.45 Setup<br>License Agreement<br>Please review the license terms   | before installing NXP GL  | II 3.1.45.                               | _   | -                              | × |
|            |  |   |  |   |                                |   |
|            | Press Page Down to see the res   | t of the agreement.   |  |   |                                |   |
|            | /* * Copyright 2019 TESSOLVE * All rights reserved. * * Redistribution and use in sou * are permitted provided that * * o Redistributions of source c * of conditions and the follow * | the following conditions a<br>ode must retain the abov<br>ing disclaimer.   | are met:<br>ve copyrigh                  | nt notice, this   | list                           | × |
|            | If you accept the terms of the a<br>agreement to install NXP_GUI 3.  |   | to continue                              | e. You must ac  | cept the                       |   |
|            | Nullsoft Install System v3.05 ——   |   |  |   |                                |   |
|            |  | < Ba  | ck                                       | I Agree   | Cance                          | 9 |
| Figure 22. | License agreement wind   | dow   |  |   |                                |   |

User manual

# KITFS26SKTEVM evaluation board

|            | ₩XP_GUI 3.1.45 Setup   |  |  |  |  |  |  |
|------------|--|--|--|--|--|--|--|
|            | Choose Components<br>Choose which features of NXP_GUI 3.1.45 you want to install.  |  |  |  |  |  |  |
|            | Check the components you want to install and uncheck the components you don't want to install. Click Next to continue.   |  |  |  |  |  |  |
|            | Select components to install:       ✓ MainSection       Position your mouse         ✓ Optional       Position your mouse         Optional       See its description.             |  |  |  |  |  |  |
|            | Space required: 164.4 MB   |  |  |  |  |  |  |
|            | Nullsoft Install System v3.05  |  |  |  |  |  |  |
|            | < Back Next > Cancel   |  |  |  |  |  |  |
| Figure 23. | . Select FS2630_GUI feature  |  |  |  |  |  |  |
|            | (¬¬¬¬¬¬¬¬¬¬¬¬¬¬¬¬¬¬¬¬¬¬¬¬¬¬¬¬¬¬¬¬¬¬¬¬  |  |  |  |  |  |  |
|            | Choose Install Location<br>Choose the folder in which to install NXP_GUI 3.1.45.   |  |  |  |  |  |  |
|            | Setup will install NXP_GUI 3.1.45 in the following folder. To install in a different folder, click<br>Browse and select another folder. Click Install to start the installation. |  |  |  |  |  |  |
|            | Destination Folder   |  |  |  |  |  |  |
|            | C:\Program Files (x86)\WXPGUI\ Browse  |  |  |  |  |  |  |
|            | Space required: 164.4 MB<br>Space available: 26.9 GB   |  |  |  |  |  |  |
|            | Nullsoft Install System v3.05       < Back       Install       Cancel  |  |  |  |  |  |  |

#### Figure 24. Choose the folder to install

Select the below options before completing the installation of the setup

- Run NXP\_GUI
- Show Readme

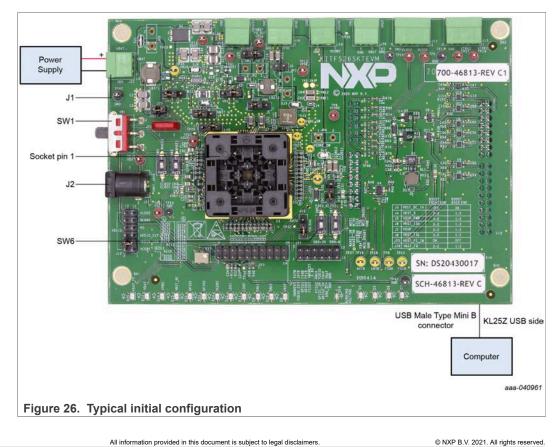
Select Finish to complete the installation

### **KITFS26SKTEVM** evaluation board

| 당 NXP_GUI 3.1.45 Setup | – 🗆 X  |
|------------------------|--|
|                        | Completing NXP_GUI 3.1.45 Setup<br>NXP_GUI 3.1.45 has been installed on your computer.<br>Click Finish to dose Setup.<br>✓ Run NXP_GUI 3.1.45<br>✓ Show Readme |
| Figure 25. Run NXP_GUI | < <u>B</u> ack <u>F</u> inish Cancel   |

When installation is finished the application can be found in the windows search bar as "NXPGUI". Click to launch

#### Configuring the hardware 6



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To configure the hardware and workstation, complete the following procedure:

- 1. With board disconnected, push and insert an FS26 device into the socket. Pin 1 is on the top left of the socket.
- 2. With SW1 in middle position, set DC power supply to 12 V and current limit to 1.0 A. Attach the DC power supply positive and negative output to KITFS26SKTEVM VBAT Phoenix connector (J1). Or connect 12 V power supply to VBAT Jack (J2).

| Table 15. | VBAT | Phoenix | connector | (J1) |
|-----------|------|---------|-----------|------|
|-----------|------|---------|-----------|------|

| Schematic label | Signal name | Description                  |
|-----------------|-------------|------------------------------|
| J1-1            | VBAT        | Battery voltage supply input |
| J1-2            | GND         | Ground                       |

| Schematic label             | Signal name  | Description                         |
|-----------------------------|--------------|-------------------------------------|
| SW1 pin 2-3                 | VBAT Phoenix | Board supplied by Phoenix connector |
| SW1 pin 2 (middle position) | VBAT         | Board not supplied                  |
| SW1 pin 2-1                 | VBAT jack    | Board supplied by jack connector    |

- 3. Connect the Windows PC USB port to the KL25Z USB side of the freedom board included in KIT, using the provided USB 2.0 cable.
- 4. Turn On SW6 to apply 5.0 V to the VDebug pin.
- 5. Turn on the power supply
- 6. Close SW1

**Note:** At this step, the product is in debug mode and all regulators are turned off. The user can then power up with OTP configuration or configure the mirror registers before power up. Power up is effective as soon as SW6 is turned off.

# 7 FS26 NXP GUI

Once the KIT is ready and the NXP GUI is installed launch the KIT from the Windows search bar.



### Launching FS26\_GUI Application

Once the NXP GUI is open, the **Kit Selection** window is displayed. Check for the following settings and select **OK**.

# KITFS26SKTEVM evaluation board

| Select the kit on board de    | evice(s), target MCU and USB int | erface |
|-------------------------------|----------------------------------|--------|
| Kit and Devices               |                                  | cirace |
| PF5020                        |                                  | ^      |
| PF5023                        |                                  |        |
| PF5024                        |                                  |        |
| ✓ KITPF7100                   |                                  |        |
| PF7100                        |                                  |        |
| ✓ KITFS26                     |                                  |        |
| FS26                          |                                  |        |
| ✓ KITFS5600                   |                                  | ~      |
| A kit for NXP PMIC evaluation | n                                |        |
| Advanced Settings             |                                  |        |
| Feature Set                   | SPI                              |        |
| Target MCU                    | FRDM-KL25Z                       |        |
| USB Interface                 | usb-hid                          |        |
| Use this configuration and    | Donot ask again!                 |        |
|                               | ОК                               | Cancel |

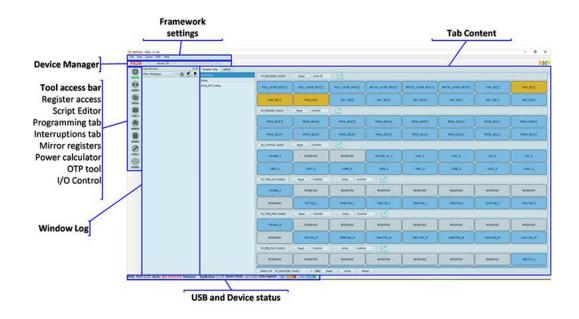
To avoid the Kit Selection window on every launch, check the box "Use this configuration and do not ask again".

The below window opens.



# 7.1 Framework

# KITFS26SKTEVM evaluation board



**Device Manager:** Start communication with device. Enter or exit test mode. Quick access to execute system scripts.

Framework settings: Import or export files, configure framework.

Window log: USB and Device communication events.

**USB and Device status:** Displays if USB or Device is connected or disconnected. Displays Firmware and GUI version. Display current state of FS state machine; click on display button to refresh.

Tool access bar: Quick access to the FS26 evaluation tools and features.

**Tab content:** Content of each tool or tab; there can be more tabs, boxes, or windows inside.

# 7.1.1 Framework settings

The NXP GUI Main Menu has five GUI Elements: File, View, Export, NXP, and Help

|                         | NXP GUI - FS2630 - 2.0.70 |
|-------------------------|---------------------------|
|                         | File View Export NXP Help |
|                         | FS2630 Start 12C -        |
| Figure 28. GUI elements |                           |

# 7.1.2 File

Load or save a configuration OR exit the application. Load and Save are only enabled when OTP tool tab is active.

| Ņ | 1.1.45 MXP GUI - FS26 - 3.1.45 |      |        |     |      |  |  |
|---|--------------------------------|------|--------|-----|------|--|--|
|   | File                           | View | Export | NXP | Help |  |  |
|   |                                | Load |        |     |      |  |  |
| _ | Save                           |      |        |     |      |  |  |
|   | Use Default Configuration      |      |        |     |      |  |  |
|   | Exit                           |      |        |     |      |  |  |

- Load: Loads an existing configuration file previously exported from OTP tool to continue to modify it on the OTP tool. This file has a .cfg extension. It is usually named as: FS26\_ProgIDASILlevel\_CONFIG.cfg. Example: FS26\_A0D\_CONFIG.cfg.
- Save: Saves the current configuration of the OTP tool as a .cfg file.
- Use default configuration: Load default values into the OTP tool.
- Exit: Exits NXP GUI application

### 7.1.3 View

This main menu has options that are related to GUI display options and menu, and contains the following subitems:

- 1. Display
- 2. Show
- 3. Naming Conventions
- **Display:** It consists of Connection Tool Bar (enabled by default) option. To show or hide, go to **View>>Display** and select **Connection Tool Bar**

| 腔 NXP GUI - FS26 - 1.0     |                               |
|----------------------------|-------------------------------|
| File View Export NXP Help  | 2                             |
| ES Display                 | Connection Tool Bar           |
| Show                       | >                             |
| Naming Conventions         | Witching Regulator Regulators |
| Blo                        | ock Diagram                   |
| Figure 29. Display options |                               |



| NXP GUI -               | FS26 - 1.0                                       |                    |  |
|-------------------------|--|--------------------|--|
| File View               | Export NXP Help                                  |                    |  |
| FS Dis                  | splay 🕨  | Exit test mode Po  |  |
|                         | iow 🔸  | OTP Tool           |  |
|                         | aming Conventions 🔹 🕨                            | Power Calculator   |  |
| ACCESS                  | iller messages                                   | Registry Map       |  |
|                         | S26 [M_MIRRORDATA:0x3<br>S26 [WIO_DIS_VOTP:0x2   |                    |  |
| <> F                    | S26 [M_MIRRORCMD:0x39                            | Mirror Editors     |  |
|                         | S26 [M_MIRRORDATA:0x3<br>S26 [ID_VOTP:0x21]R:0x( |                    |  |
| Party F.                | S26 [FS_MIRRORCMD:0xb]                           | Device Programming |  |
| F                       | S26 [FS_MIRRORDATA:0x<br>S26 [CFG_OVUV_1_OTP:(   | Log Window         |  |
| PPOC -                  |  |                    |  |
| Figure 30. Show options |  |                    |  |

• **Naming Conventions:** Select Friendly or Register name display for OTP tool. Option enabled only when OTP tool is active.

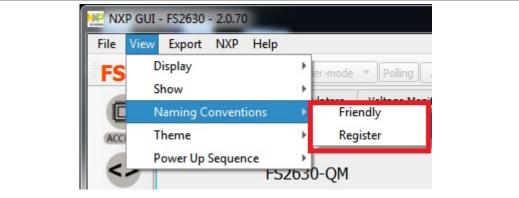


Figure 31. Naming conventions options

**Friendly:** Go to View >>Naming Conventions >>Friendly. This mode helps to view the registers names as user friendly names throughout the OTP Tool.

| VSUP UV threshold            | 4.8 V/4.3 V                |
|------------------------------|----------------------------|
| Exit DFS on WAKE1 event      | Enabled                    |
| Auto-retry power up from DF: | Enabled                    |
| Auto-retry mode              | Limited retry              |
| Auto-retry timer limit       | 100 ms                     |
| Clock frequency selection    | 16 MHz                     |
| VBOS input selection         | Auto Transition on VPRE_UV |

**Register:** Go to View >>Naming Conventions >>Register. This mode helps to view the register names as Register's Technical names throughout the OTP Tool. Example: VSUP UV threshold -> VSUP\_UVTH\_OTP

#### 7.1.4 Export

This option allows user to export the current OTP from the OTP tool into different script formats.

- OTP: Exports OTP configuration into OTP script file for programming.
- TBB: Exports OTP configuration into a TBB script file for emulation
- I-HEX: Exports to Intel Hex script file
- S-HEX: Exports to Simple Hex script file

# KITFS26SKTEVM evaluation board

| NX NX               | (P GUI - | FS2630 | - 2.0.70 | )    |                     |
|---------------------|----------|--------|----------|------|---------------------|
| File                | View     | Export | NXP      | Help |                     |
| ES                  | 263      | ОТ     | P        |      | user-mode 🔻 Polling |
|                     |          | TB     | В        |      |                     |
|                     |          | HE     | х        |      | S-HEX               |
| ACC                 | ESS      |        |          | BIOC | I-HEX               |
| e 33. Export option | ns       |        |          |      |                     |

This option will be enabled only in OTP Tool and will remain disabled in other sections of the GUI.

# 7.2 Device manager

The device manager allows start/stop of communication with device as well as enter/exit of the test mode; it also allows quick access to execute useful system scripts.

| NXP GUI - FS26 - 1.0       |                         |                             |               |           |
|----------------------------|-------------------------|-----------------------------|---------------|-----------|
| File View Export NXP Help  |                         |                             |               |           |
| FS26 Start Device ID: FS26 | Apply test mode Polling | <b>SPI Freq (KHz):</b> 6000 | Go to Standby | ▼ execute |
| Figure 34. Device manag    | er                      | -                           |               |           |

#### 7.2.1 Device connection

If USB is detected from USB and device status bar, USB status changes from **NOT DETECTED** to **DISCONNECTED**. Start button is enabled.

MCU: FRDM-KL25Z State: DISCONNECTED

Click on start button to start communication with FS26 device.

| \rm MXP GU | Л - FS26 - 3 | 1.38                                     |  |
|------------|--------------|--|--|
| File View  | v Export     | NXP Help                                 |  |
| FS26       | Start        | Device ID: FS26 - Apply test mode Poling |  |

When connected successfully, FS26 color changes to green and other buttons are enabled. USB status changes to **CONNECTED**.

| File | View   | Export | NXP   | Help   |       |     |                         |
|------|--------|--------|-------|--------|-------|-----|-------------------------|
| FS   | 26     | Stop   | Devi  | ce ID: | FS26  | -   | Apply test mode Polling |
|      | 1      |        |       |        |       |     |                         |
| мси  | I: FRD | M-KL25 | Z Sta | ate: C | ONNEC | TED |                         |

### KITFS26SKTEVM evaluation board

Apply test mode to send MAIN and Failsafe Test mode entry keys. If test mode is entered correctly, button will change to "Exit test

|        | File View   | Export NXP Help      |                                    |         |
|--------|-------------|----------------------|------------------------------------|---------|
|        | <b>FS26</b> | Stop Device ID: FS26 | <ul> <li>Exit test mode</li> </ul> | Polling |
| mode". |             |                      |                                    | , ,     |

When test mode is entered, tabs requiring test mode are enabled, such as Mirrors tabs and device programming.

Click on polling to do a continuous check of test mode entry.

If the Device versioning bits are already programmed with an existing part number, the NXP GUI decodes and displays the assigned Device ID. The below example displays FS2633D.

| File | View | Export  | NXP  | Help                     |                     |  |
|------|------|---------|------|--------------------------|---------------------|--|
| FS   | 263  | 3D [    | Stop | Device ID: FS2633D 🔻 Exi | t test mode Polling |  |
|      |      | on Wind | law  | a 🛛 🗌                    | 0101                |  |

# 7.2.2 Script shortcuts

To find a section with system script shortcuts, select the script and click on execute to the device. Notice that it does not warrant the entry or acknowledge of the device. Device must be in INIT FS state in most cases.

|     | Go to Standby          | execute |
|-----|------------------------|---------|
| or  | Go to LPOFF            | AMUX    |
|     | Simple-WD              |         |
|     | Challenger-WD          |         |
| ICI | OpenWD-Window          |         |
| ۱S  | Safety outputs release |         |

# 7.3 Access

# 7.3.1 Register map

The register access tab allows read/write to the FS26 Main and Failsafe register maps and is divided in the following sections:

|                               | 🔤 Register Map    | MUX |
|-------------------------------|-------------------|-----|
|                               | Functional        |     |
|                               | Safety            |     |
|                               | Write_INIT_Safety |     |
| Figure 35. Register access ta | ıb                |     |

- Functional: MAIN functional SPI registers (Diagnostics, configuration and controls)
- Safety: Safety SPI registers (Diagnostics and configuration)

| FULL_LAYER_REV[2] | FULL_LAYER_REV[1]  | FULL_LAYER_REV[0]  | METAL_LAYER_REV[2]   | METAL_LAYER_REV[1]   | METAL_LAYER_REV[0]   | FAM_ID[3]  | FAM_ID[2]  |
|-------------------|--|--|--|--|--|--|--|
| FAM_ID[1]         | FAM_ID[0]  | DEV_ID[5]  | DEV_ID[4]  | DEV_ID[3]  | DEV_ID[2]  | DEV_ID[1]  | DEV_ID[0]  |
| M_PROGID (0x02)   | Read 0x0000  |  |  |  |  |  |  |
| PROG_IDH[7]       | PROG_IDH[6]  | PROG_IDH[5]  | PROG_IDH[4]  | PROG_IDH[3]  | PROG_IDH[2]  | PROG_IDH[1]  | PROG_IDH[0]  |
| PROG_IDL[7]       | PROG_IDL[6]  | PROG_IDL[5]  | PROG_IDL[4]  | PROG_IDL[3]  | PROG_IDL[2]  | PROG_IDL[1]  | PROG_IDL[0]  |
| M_STATUS (0x04)   | Read 0x0000  |  |  |  |  |  |  |
| TWARN_S           | RESERVED   | RESERVED   | VBSTFB_UV_S  | WK2_S  | WK1_S  | 102_5  | IO1_S  |
| VREF_S            | VBST_S   | VPRE_S   | TRK2_S   | TRK1_S   | CORE_S   | LDO2_S   | LD01_S   |
| M_TSD_FLG (0x06)  | Read 0x0000  | Write 0x000  |  |  |  |  |  |
| TWARN_I           | RESERVED   | RESERVED   | RESERVED   | RESERVED   | RESERVED   | RESERVED   | RESERVED   |
| RESERVED          | IO1TSD_I   | VPRETSD_I  | TRK2TSD_I  | TRK1TSD_I  | CORETSD_I  | LD02TSD_I  | LDO1TSD_I  |
| M_TSD_MSK (0x08)  | Read 0x0000  | Write 0x000  | • 🚺  |  |  |  |  |
| TWARN_M           | RESERVED   | RESERVED   | RESERVED   | RESERVED   | RESERVED   | RESERVED   | RESERVED   |
| RESERVED          | IO1TSD_M   | VPRETSD_M  | TRK2TSD_M  | TRK1TSD_M  | CORETSD_M  | LDO2TSD_M  | LDO1TSD_M  |
| M_REG_FLG (0x0A)  | Read 0x0000  | Write 0x000  | . []   |  |  |  |  |
| RESERVED          | RESERVED   | RESERVED   | RESERVED   | RESERVED   | RESERVED   | RESERVED   | VBSTOV_I   |
|                   | H, FROG D(0x02)  PROG_DH(7)  PROG_DH(7)  PROG_DH(7)  PROG_DH(7)  PROG_DH(7)  PROG_DH(7)  PROG_CH(7)  P | M, FROGD (0x02)         Read         (0x0000)           PROG_DH(7)         PROG_DH(6)         PROG_DH(6)           PROG_DH(7)         PROG_DH(6)         M.           M_STATUS (0x64)         Read         0x0000           TWARN_S         RESERVED         VREF_S           VREF_S         VRST_S         M.           TWARN_I         RESERVED         0x150_J           M_TSD_HG (0x60)         Read         0x0000           TWARN_J         RESERVED         0x150_J           M_TSD_HG (0x60)         Read         0x0000           TWARN_M         RESERVED         0x150_J           M_TSD_MG (0x80)         Read         0x0000           TWARN_M         RESERVED         0x150_J           M_TESERVED         0x150_M         M.           M_TESERVED         0x150_M         M. | H, FROGD (0x02)         Read         0x0000           PROG_DH(7)         PROG_DH(6)         PROG_DH(5)           PROG_DL(7)         PROG_DL(6)         PROG_DL(5)           M_STATUS (0x04)         Read         0x0000         Image: Comparison of the comparison of | H, PROG_DK(202)         Read         0x0000           PROG_DH(7)         PROG_DH(8)         PROG_DH(4)           PROG_DH(7)         PROG_DH(6)         PROG_DH(3)         PROG_DH(4)           PROG_DL(7)         PROG_DL(6)         PROG_DL(2)         PROG_DL(4)           M_STATUS (b04)         Read         0x0000         Image: Comparison of the | H, PROG_D(xx02)         Read         0x0000         Image: Control of C | H, PROGD (xx22)       Read       0x0000       Image: Constraint of the second of the | H, PROGD (xx22)       Read       0x0000       Image: Control of |

• Write\_INIT\_Safety: Safety registers that can be configured during INIT FS state (ex. WD configuration, WD window).

#### Figure 36. Main register maps

There are three types of registers: read only (only read button), write only (only write button) or read/write (read and write buttons).

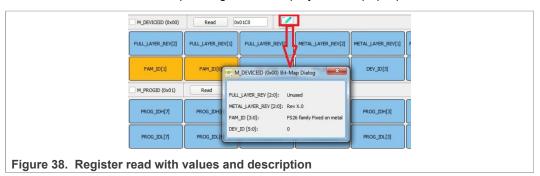
#### 7.3.1.1 Register read only

To read the values of a register, click on **READ** button; the value is read from the device and displayed on label near **READ** button, and is displayed on the log window.

| M_DEVICEID (0x00) | Read              | 01C0              |                    |                    |                    |           |           |
|-------------------|-------------------|-------------------|--------------------|--------------------|--------------------|-----------|-----------|
| FULL_LAYER_REV[2] | FULL_LAYER_REV[1] | FULL_LAYER_REV[0] | METAL_LAYER_REV[2] | METAL_LAYER_REV[1] | METAL_LAYER_REV[0] | FAM_ID[3] | FAM_ID[2] |
| FAM_ID[1]         | FAM_ID[0]         | DEV_ID[5]         | DEV_ID[4]          | DEV_ID[3]          | DEV_ID[2]          | DEV_ID[1] | DEV_ID[0] |

Figure 37. Read only register

To view the values of all the bits from a register after read operation, click on **Edit button**. Bits are read with their corresponding values displayed as a pop-up window.



User manual

### 7.3.1.2 Register write only

To write the bit values individually, click on the desired bit and corresponding bit button changes color. The value is updated on the log window. Click on WRITE button to write on the register.

| TWARN_I         RESERVED         RESERVED | M_TSD_FLG (0x03) | Read 0x   | 0000 W    | rite 0x0089 |           |           |           |            |
|--|------------------|-----------|-----------|-------------|-----------|-----------|-----------|------------|
| RESERVED IOITSD_I VPRETSD_I TRKITSD_I CORETSD_I LDOITSD_I LDOITSD_I LDOITSD_I  | TWARN_I          | RESERVED  | RESERVED  | RESERVED    | RESERVED  | RESERVED  | RESERVED  | RESERVED   |
|  | RESERVED         | IO 1TSD_I | VPRETSD_I | TRK2TSD_I   | TRK1TSD_I | CORETSD_I | LDO2TSD_I | LDO 1TSD_I |

Figure 39. Write only registers

To write the values through text box near WRITE button, input the appropriate write value then click on **WRITE** button to write to the register.

|                  | Read 0x   | <0000 W   | ite Dx0088 |            |           |           |            |  |  |
|------------------|-----------|-----------|------------|------------|-----------|-----------|------------|--|--|
| TWARN_M          | RESERVED  | RESERVED  | RESERVED   | RESERVED   | RESERVED  | RESERVED  | RESERVED   |  |  |
| RESERVED         | IO 1TSD_M | VPRETSD_M | TRK2TSD_M  | TRK ITSD_M | CORETSD_M | LDOZTSD_M | LDO 1TSD_M |  |  |
| M REG FLG (0x05) | Read 0x   | x0000 Wr  | ite 0x00ff |            |           |           |            |  |  |
|                  | 1         |           |            |            |           |           |            |  |  |
| RESERVED         | RESERVED  | RESERVED  | RESERVED   | RESERVED   | RESERVED  | RESERVED  | VBSTOV_I   |  |  |

Figure 40. Write only register with input data box

The value can be written as well by selecting the edit option near **WRITE** button; the bits and corresponding values are displayed as a pop window. Select the options of all write bits, close the input dialog box and select the **WRITE** button.

Selected input combinations are written to the register.

| RESERVED            | MR M_REG_FL                          | G (0x05) Bit-Map Dialog   | 1         |  | RESERVED | VBSTOV_I  |
|---------------------|--------------------------------------|---|-----------|--|----------|-----------|
| VPREUVH_I           | VBSTOV_I:<br>VPREUVH_I:<br>VBSTOC_I: | VBST has not cross VBST_OV_TH threshold<br>VPRE crossed VPRE_UVH threshold<br>Over current event occurred   | -         | VBST has not cross VBST_OV_TH threshold<br>VPRE has not cross VPRE_UVH threshold<br>No Over current event detected | LD020C_I | LDO 10C_I |
| M_REG_MSK (0x06)    | VBSTOC_I:<br>VPREOC_I:               | Over current event occurred   | -         | No Over current event detected   |          |           |
| RESERVED            | TRK2OC_I:<br>TRK1OC_I:               | Over current event occurred   | -         | No Over current event detected<br>No Over current event detected   | RESERVED | VBSTOV_M  |
| VPREUVH_M           | COREOC_I:<br>LDO2OC_I:               | Over current event occurred <ul> <li>Over current event occurred</li> <li>Image: Second secon</li></ul> | -         | No Over current event detected   | LDO2OC_M | LDO10C_M  |
| ielect All M_DEVICE | LD010C_I:                            | Over current event occurred   | LDO10C_I: | No Over current event detected   |          |           |

#### 7.3.1.3 Register read/write

To read or write the bit values individually, click on each bit button; the value is read from the bit or written to the bit based on its properties and displayed on the log window and in the label near **READ** and textbox near **WRITE** button correspondingly. The bit button color changes accordingly.

#### 7.3.1.4 Global read/write

The global read/write and reset option is located at the left bottom section of the register tab.

| The SELECT ALL o | option selects all the | registers on the tab. |
|------------------|------------------------|-----------------------|
|                  |                        |                       |

| Register Map AMUX                     |                       |                       |                       |                        |                        |                        |             |             |
|---------------------------------------|-----------------------|-----------------------|-----------------------|------------------------|------------------------|------------------------|-------------|-------------|
| Functional                            | M_DEVICEID (0x00      | Read                  | 0x01C0                | <                      |                        |                        |             |             |
| Safety<br>Write_INIT_Safety<br>M_VOTP | FULL_LAYE<br>R_REV[2] | FULL_LAYE<br>R_REV[1] | FULL_LAYE<br>R_REV[0] | METAL_LAYE<br>R_REV[2] | METAL_LAYE<br>R_REV[1] | METAL_LAYE<br>R_REV[0] | FAM_ID[3]   | FAM_ID[2]   |
| OTP_TRIM_MAIN<br>OTP_CONF_MAIN        | FAM_ID[1]             | FAM_ID[0]             | DEV_ID[5]             | DEV_ID[4]              | DEV_ID[3]              | DEV_ID[2]              | DEV_ID[1]   | DEV_ID[0]   |
| OTP_TRIM_FAILSAFE                     | M_PROGID (0x01)       | Read                  | 0x0000                | 1                      |                        |                        |             |             |
| OTP_CONF_FAILSAFE                     | PROG_IDH[7]           | PROG_IDH[6]           | PROG_IDH[5]           | PROG_IDH[4]            | PROG_IDH[3]            | PROG_IDH[2]            | PROG_IDH[1] | PROG_IDH[0] |
| FS_TestMode                           | PROG_IDL[7]           | PROG_IDL[6]           | PROG_IDL[5]           | PROG_IDL[4]            | PROG_IDL[3]            | PROG_IDL[2]            | PROG_IDL[1] | PROG_IDL[0] |
| SED .                                 | M_STATUS (0x02)       | Read                  | 0x0000                | 5                      |                        |                        |             |             |
|                                       | TWARN_S               | RESERVED              | RESERVED              | VBSTFB_UV_S            | WK2_S                  | WK1_S                  | 102_S       | IO1_S       |
|                                       | VREF_S                | VBST_S                | VPRE_S                | TRK2_S                 | TRK1_S                 | CORE_S                 | LDO2_S      | LDO1_S      |
|                                       | M_TSD_FLG (0x03)      | Read                  | 0x0000                | Write 0x0000           |                        |                        |             |             |
|                                       | TWARN_I               | RESERVED              | RESERVED              | RESERVED               | RESERVED               | RESERVED               | RESERVED    | RESERVED    |
| FRDM-KL25Z State: NOT DETECTED F      | Select Al M_DEV       |                       | • (26) Read           | Write Reset            |                        |                        |             |             |

Figure 42. Global read/write

WRITE: Writes data to all selected registers at once

READ: Reads data back from the selected register at once

**RESET:** Resets all input textboxes to 0x00. Write bits are set to 0 and change register bit buttons to default setting.

| Select All M_DEVICEID (0x00) 🔻 (26) Read Write Res | et |
|--|----|

### 7.3.2 INIT FS tab

Configure reaction of safety outputs for VMON, FCCU, ERRMON, and configure Fault Monitor. It is required to be in INIT FS to configure registers. Click on read all button to get current configuration, then modify it.

Click on the combo box controls to select configuration, then click on write button.

Click on Read or Read all button to get configuration; read values appear to the right of controls.

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|   | INIT Safety | Ø FS Config    | C Regulators   | and AMUX                 |                         |  |
|---|-------------|----------------|----------------|--------------------------|-------------------------|--|
| INIT Safety   |             | VMON Reaction  |                |                          |                         | Safety Inputs  |
| VMON PRE OV FS RE   | ACTION VM   |                |                | serts RSTb and FS0b      | FCCU12 FILT             | б µs • 6 µs  |
| VMON_PRE_UV_FS_RE   |             | ON PRE UV a 🔻  | VMON_PRE UV as | serts FS0b only          | ERRMON_FS_REACTION      | RSTb and FS0b c + RSTb and FS0b only is asserted low in case of fault detected on ERRM |
| VMON CORE OV FS R   |             | -              | VMON_CORE OV a | asserts RSTb and FS0b    | ERRMON_ACK_TIME         | 8 ms - 8 ms  |
| VMON_CORE_UV_FS_R   |             | ON CORE UV -   | VMON_CORE UV a | asserts FS0b only        | ERRMON_FLT_POLARITY     | Level is a fault offerer exercise a destruction  |
| VMON_LDO1_OV_FS_R   |             | -              | VMON_LDO1 OV   | asserts RSTb and FS0b    | WAKE2_LP_POLARITY       | Go to LP modes when WAKE2 goes low   |
| VMON_LDO1_UV_FS_R   |             |                | VMON_LDO1 UV a | asserts FS0b only        | FCCU2_FS_REACTION       | RSTB and FS0b c + RSTB and FS0b only is asserted low in case of fault on FCCU2         |
| VMON_LDO2_OV_FS_R   |             |                | VMON_LDO2 OV   | asserts RSTb and FS0b    | FCCU1_FS_REACTION       | RSTB and FS0b c + RSTB and FS0b only is asserted low in case of fault on FCCU1         |
| VMON_LDO2_UV_FS_R   |             | -              | VMON_LDO2 UV a | asserts FS0b only        | FCCU12_FS_REACTION      | RSTB and FS0b c * RSTB and FS0b only is asserted low in case of fault on FCCU1 and FCC |
| /MON_TRK1_OV_FS_R   | EACTION VM  | ON_TRK1 OV +   | VMON_TRK1 OV a | asserts RSTb and FS0b    | FCCU2_FLT_POL           | LOW LEVEL IS A FAULT   |
| VMON_TRK1_UV_FS_R   | EACTION VM  | ON_TRK1 UV -   | VMON_TRK1 UV a | isserts FSOb only        | FCCU1_FLT_POL           | LOW LEVEL IS A + LOW LEVEL IS A FAULT  |
| VMON_TRK2_OV_FS_R   | EACTION VM  | ON_TRK2 OV 👻   | VMON_TRK2 OV a | asserts RSTb and FS0b    | FCCU12_FLT_POL          | FCCU1=0 or FCCU = FCCU1=0 or FCCU2=1 level is a fault                                  |
| VMON_TRK2_UV_FS_R   | EACTION VM  | ON_TRK2 UV 🔻   | VMON_TRK2 UV a | isserts FS0b only        | FCCU_CFG                | FCCU1 and FCCU: + FCCU1 and FCCU2 inputs monitoring activated by pair                  |
| MON_REF_OV_FS_RE  | ACTION VM   | ON_REF OV a 🔻  | VMON_REF OV as | serts RSTb and FS0b      |                         |  |
| VMON_REF_UV_FS_RE/  | ACTION VM   | ON_REF UV a: + | VMON_REF UV as | serts FS0b only          |                         | Write Read   |
| VMON_EXT_OV_FS_RE   | ACTION VM   | ON_EXT OV a 🔻  | VMON_EXT OV as | serts RSTb and FS0b      |                         |  |
| VMON_EXT_UV_FS_RE   | ACTION VM   | ON_EXT UV a 🔻  | VMON_EXT UV as | serts FS0b only          |                         |  |
|   |             |                |                |                          |                         |  |
|   |             | Write Re       | ad             |                          |                         |  |
| Fault Monitor   |             |                |                |                          |                         | FS1B Configuration   |
| FLT_ERR_CNT 1 T   |             |                |                |                          |                         | FS1B_TDELAY 0 ms  0 ms   |
| DIS8S RSTb LOW 8s Co + RSTb LOW 8s Counter enabled  |             |                |                |                          |                         | FS1B_TDUR 100 ms + 100 ms  |
| CLK_MON_DIS CLK Monitoring A + CLK Monitoring Active  |             |                |                | e                        |                         | Write Read   |
| BACKUP_SAFETY_PATH_FS1B RSTb assertion  RSTb assertion  |             |                |                | l                        | VVIICe Keau             |  |
| BACKUP_SAFETY_PATH  | H_FSOB RSTb | asseruori      | STb assertion  |                          |                         |  |
| RSTB_DUR 10 ms + 10 ms  |             |                |                |                          |                         |  |
| FLT_ERR_REACTION RSTb and FS0b a ▼ RSTb and FS0b are asserted low if FLTERRCNT ≥ intermediate value |             |                |                | asserted low if FLTERRCM | IT ≥ intermediate value |  |
| FLT_ERR_CNT_LIMIT   | 6           | - 6            |                |                          |                         |  |
|   |             | Write          | Read           |                          |                         |  |
|   |             |                |                |                          |                         |  |

Figure 43. INIT FS tab

To get current state, click on FS\_STATES display from USB and Device status bar on the bottom.

# 7.3.3 FS config tab

This tab helps to configure safety features such as Watchdog and fault error counter. Click on Read all button to get current configuration.

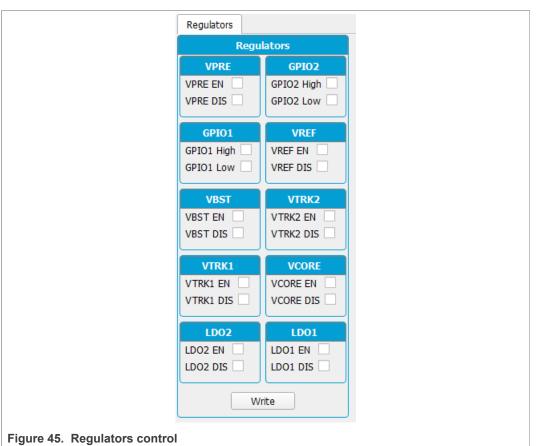
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| F5 Confg       Read Al       Wite Al       Epot         Release F5 Outputs       Claar Errors       WatchDog Confg         Release F508       Release F508       WD Chalenger       WD Chalenger       WD D_RFL_QUT       0       0       0         Release F518       Release F518       Release F518       Release F518       Release F518       F10       0 <t< th=""><th>🗱 Register Map 🛛 INIT Safety 🖓 FS Config 🕚 Regulators 🖬 AMUX</th><th></th></t<>   | 🗱 Register Map 🛛 INIT Safety 🖓 FS Config 🕚 Regulators 🖬 AMUX   |   |
|--|--|---|
| Release FS08       Release FS08       WD Challenger       WD Challenger       WD_ERR_CNT       0       0         Release FS18       Release FS18       Release FS18       Release FS18       Release FS18       Release FS18       WD_Simple         Release FS08.FS18       Release FS08.FS18       Release FS08.FS18       Release FS08.FS18       Release FS08.FS18       Release FS08.FS18         Release FS08.FS18       Release FS08.FS18       Release FS08.FS18       Release FS08.FS18       Release FS08.FS18         VD_RER_LINIT       6       6         WD_RER_LINIT       6       6         WD_FS_REACTION       RSTb and FS0b are asserted low if WD Envor counter value = WDERRCHT[1:0]         WDW_RECOVERY       64 ms       % 64 ms         WDM_DCDUbty Cycle       Closed Window : 50% / Open Window : 50%       Open Window : 50%         WDM_DECIDIty Cycle       Closed Window : 50% / Open Window : 50%       ABIST_URA ABIST *         ABIST2_TRK1       No ABIST *       ABIST2_TRK1       No ABIST *         ABIST2_TRK1       No ABIST *       ABIST2_TKN       No ABIST *         ABIST2_REF       No ABIST *       ABIST *       ABIST *         ABIST2_TRK1       No ABIST *       ABIST *       ABIST *         Write       Read       Write  | FS Config  | Read All Write All Export   |
| Release FS1B       WD Simple       WD_SIMPLe         WD_BRE_CNT       0       0         Release FS0B-FS1B       EnfMon Ack       ERRMON ACK         PRT_ERR_CNT       1       1         WD_BRE_LIMIT       6       6         WD_FS_REACTION       RSTb and FS0b are asserted low if WD Error counter value = WDERRCNT[1:0]         Write       Read         WDW_RECOVERY       64 ms         WDM_DC(Duty Cycle)       Closed Window: : 50% / Open Window : 50%         WDM_DC(Duty Cycle)       3 ms         Write       Read         Wirte       Read         Write       Read  | Release FS Outputs Clear Errors  | WatchDog Config   |
| WD Window         MD Window         WDW_RECOVERY       64 ms         MDM_DC(Duty Cycle)       Cosed Window : 50% / Open Window : 50%         MDM_DC(Duty Cycle)       Cosed Window : 50% / Open Window : 50%         WDM_PERIOD       3 ms       Content of the state of  | Release FS1B     Release FS1B     WD Simple     WD_R       Release FS0B-FS1B     Release FS0B-FS1B     EmMon Ack     ERRMON ACK     FLT_E       WD_R     WD_R     WD_R     WD_R     WD_R | RFR_CNT     0     0       ERR_CNT     1     1       RFR_LIMIT     6     6       ERR_LIMIT     6     6     |
| WDM_DCC(Duty Cycle)       Closed Window : • Closed Window : 50% / Open Window : 50%       ABIST2_CORE No ABIST • ABIST2_CORE No ABIST • ABIST2_LDO1 No ABIST • ABIST2_LDO2 No ABIST • ABIST2_RX1 No ABIST • ABIST2_RX1 No ABIST • ABIST2_RX2 No ABIST • ABIST2_RX2 No ABIST • ABIST2_RX1 | WD Window  |   |
| WDM_PERIOD     3 ms     ABIST2_CURIN NABIST       WDM_PERIOD     3 ms     ABIST2_LOLO IN ABIST       Write     Read       ABIST2_TRK1     No ABIST       ABIST2_RK1     No ABIST       ABIST2_RK2     No ABIST       ABIST2_RK2     No ABIST       ABIST2_RK2     No ABIST       ABIST2_RK2     No ABIST       Write     Read  | WDW_RECOVERY 64 ms + 64 ms   | ABIST2_VPRE No ABIST   STBY_WAKE_UP Device has wake   |
| Write     Read       Write     Read       Write     Read       Write     Read         Write     Read         Write     Read         Write     Read         Write     Read         Write     Read         Write     Read         Write     Read   | WDM_DC(Duty Cycle) Closed Window : - Closed Window : 50% / Open Window : 50%   | ABIST2_CORE No ABIST  |
|  |  | ABIST2_LDO2 No ABIST  ABIST2_TKL No ABIST  ABIST2_TKL No ABIST  ABIST2_TKL2 No ABIST  ABIST2_REF No ABIST |
|  | Figure 44. FS config tab   | Write Read  |

### 7.3.4 Regulators control

Enable or disable FS26 regulators. Check Enable or Disable box then click on write button. These registers do not provide regulator status; it writes '1' to apply the command then restart to 0. Write '0' has no effect. VPRE can be only enabled or disabled in test mode.

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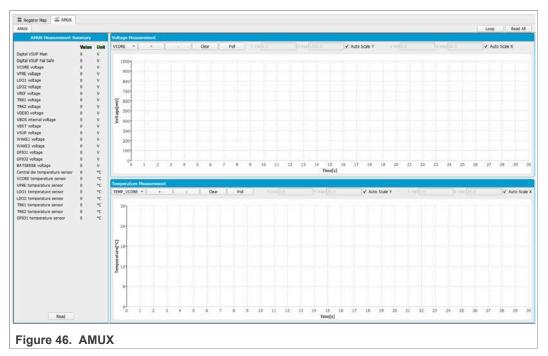
# 7.3.5 AMUX

This Menu can be accessed from Tool Bar >REG ACCESS or View >>Show>> Register Map >>AMUX Registers.

This tab allows selection of AMUX pin channel and gets its current value by using KL25Z AMUX ADC pin. The voltage or temperature graph can do a single read or dynamically display various channels.

The displayed values apply to the divider and temperature formulas.

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To do a single read of all channels click on Read button.

To use the dynamic graph, select the channel then click on "+" button to add to the graph and then start polling with **Poll** button.

Click again on Poll button to stop measurements.

# 7.4 Script editor

The script editor allows you to create or send existing sequences to the device. You can read/write individually to a register, to an I/O or to an analog pin. You can emulate an OTP configuration as well with this tab.

This Menu can be accessed from Tool Bar >>SCRIPT or View >>Show>> Script Editor.

| 526   | 30 Start        | I2C * User-mode * Poling Apply | ADDR: 0x0 * ADDR: 0x1 * |                       | N |
|-------|-----------------|--------------------------------|-------------------------|-----------------------|---|
| CCESS | Device<br>Alias | F52630<br>Alias                | Script Commands Window  | Script Results Window |   |
| <>    | Digital Pins    |                                |                         |                       |   |
| CRIPT | Analog Pins     |                                |                         |                       |   |
|       | Registers       |                                |                         |                       |   |
| PROG  | Mode            |                                |                         |                       |   |
|       | Generator       |                                |                         |                       |   |
| INT   |                 |                                |                         |                       |   |
| AFROR |                 |                                |                         |                       |   |
|       |                 |                                |                         |                       |   |
| ROWER |                 |                                |                         |                       |   |
| 2     |                 |                                |                         |                       |   |
| OTP   |                 |                                |                         |                       |   |

Figure 47. Script editor window

The script can be written by selecting and configuring the pins and registers that are available on the script commands section, or by loading a previously exported .txt file.

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| Device<br>Alias | FS26<br>Alias |  |
|-----------------|---------------|--|
| Digital Pins    |               |  |
| Analog Pins     |               |  |
| Registers       |               |  |
| ▷ Mode          |               |  |
| Generator       |               |  |
|                 |               |  |

Click on one type of command to access more options, until the command to build the sequence is found.

• Digital pins: Select the pin name, then pin value (High or Low). Command is automatically added to the script.

| <ul> <li>Digital Pir</li> </ul> | ns        |   |
|---------------------------------|-----------|---|
| Pin Name:                       | MCU_DBG5V | • |
| Pin Value:                      | HIGH      | • |

• Analog pins: Select the pin name then write the pin value. If the pin is read only, pin value will not be enabled and it will be added to script editor automatically.

| Analog P   | ins      |   |
|------------|----------|---|
| Pin Name:  | AMUX_ADC | • |
| Pin Value: | Select   | - |
|            |          |   |

- Registers: Select the Operation (Read/Write).
  - Read: Select the register group then the register name. Register is added to script editor automatically.

| Read 💌       |
|--------------|
| functional 🔹 |
| M_DEVICEID - |
| 0x0000       |
|              |

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• Write: Select the register group then the register name. Write value and click on enter key. Value must be written in HEX. Push Enter key to add to the editor.

| <ul> <li>Registers</li> </ul> |            |   |   |   |  |
|-------------------------------|------------|---|---|---|--|
| Operation:                    | Write      | Ŧ | ) |   |  |
| Reg Group:                    | functional |   | Ŧ | ] |  |
| Reg Name/Addr:                | M_TSD_FLG  |   |   | • |  |
| Value:                        | 0x0000     | _ |   |   |  |
|                               |            |   |   |   |  |

- Mode: Write command to exit or enter different device modes.
  - Test mode: Send Main and Failsafe test mode entry keys
  - User mode: Exit test mode if device is in test mode.
- Generator: Select an existing script to add to the script editor. Please consider that some options may require to be in a specific mode or state.

| <ul> <li>Generator</li> </ul> |                   |
|-------------------------------|-------------------|
| Generator:                    | Select            |
| Part numbers:                 | functional-config |
|                               | safety-config     |
|                               | otp-config        |
|                               | otp-emulation     |
|                               | VOTP-config       |
|                               |                   |
|                               | Go to Standby     |
|                               | Go to LPOFF       |
|                               | Simple-WD         |
|                               | Challenger-WD     |
|                               | OpenWD-Window     |
|                               | FS0B-Release      |

The script operations can be found in the bottom of the script editor window. This section is responsible for:

- Execution of script.
- Script management : Create, Open, Save, Run
- Logging feature : Load, Save, Clear



Figure 48. Script editor options

Run: Runs the script once

Loop: Runs the script continuously in loop

Save: Saves the script that is present in the script command window in text file

Open: Opens a saved script from the desired location

**ATE:** Saves the script in ATE format

Clear: Clears the script command window

**Script Editor Help Window**: This section describes the commands available in Script editor and their formats. This Menu can be accessed from Menu >> SCRIPT >> Help or View >>**Show**>> Script Editor >> Help

### 7.5 OTP mirror registers

To enable this tab, test mode must be applied. This tab is divided in Main and Failsafe OTP registers.

Each bit group box can be read or written, or the whole page can be read. OTP configuration can be imported or exported from this tab.

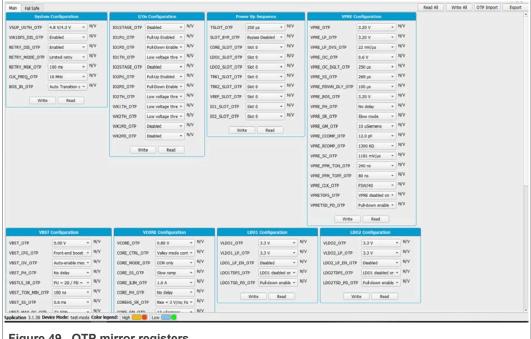


Figure 49. OTP mirror registers

### 7.5.1 Read/write operation

To read a bit group, click on the read button from a box. Read values are displayed to the right of each register.

### KITFS26SKTEVM evaluation board

| Main  | Fail Safe  |                 |   |            |
|-------|------------|-----------------|---|------------|
|       | Syste      | m Configuration |   |            |
| VSUP_ | UVTH_OTP   | 4.8 V/4.3 V     | - | 4.8 V/4.   |
| WK1D  | FS_DIS_OTP | Enabled         | * | Enabled    |
| RETRY | _DIS_OTP   | Disabled        | * | Disabled   |
| RETRY | _MODE_OTP  | Infinite retry  | - | Infinite r |
| RETRY | _MSK_OTP   | 819200 ms       | - | 819200     |
| CLK_F | REQ_OTP    | 16 MHz          | * | 16 MHz     |
| BOS_I | N_OTP      | Auto Transition | • | Auto Tra   |
|       | Write      | e Read          |   |            |

#### Figure 50. Read bit group

To write to a bit group, modify the controls of each register, then click on write button.

| Syste          | m Configuratio | DN     | 1            |
|----------------|----------------|--------|--------------|
| VSUP_UVTH_OTP  | 4.8 V/4.3 V    |        | 4.8 V/4.     |
| WK1DFS_DIS_OTP | 6.3 V/5.8 V    |        | Enabled      |
| RETRY_DIS_OTP  | Disabled       | VSUP   | UV threshold |
| RETRY_MODE_OTP | Infinite retry | *      | Infinite r   |
| RETRY_MSK_OTP  | 819200 ms      | *      | 819200       |
| CLK_FREQ_OTP   | 16 MHz         | *      | 16 MHz       |
| BOS_IN_OTP     | Auto Transitio | on c 🔻 | Auto Tri     |
| Write          | Read           | j      |              |

#### 7.5.2 Read/write all and write all operation

Read all will read all the bits of each block from all mirror registers.

Read values will appear at the right of each register as well on the window log.



To write all OTP bit groups configuration click on Write all button.

#### 7.5.3 Mirror registers export option

This operation generates and saves as text file in local device which can be imported later into this tab. <u>Figure 53</u> shows the generate .txt configuration file.

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| E FS26 - Mirror Editor  |   |                    |  |     |  |  | ×  | Read Al Write Al                                 | OTP Import  | Expo |
|---|---|--------------------|--|-----|--|--|----|--|-------------|------|
| 🛧 📙 « EN  | C TESTING > OTP Configurat                  | ons > FS2633D back | end 455Khz WD enabled  | ~ 0 | Search FS263                                     | 30 back end 455                                  | P  | NEED OF THIS OF                                  | OTP alipois | Expo |
| Organize - New fold   | # )   |                    |  |     |  | 10 <b>•</b>                                      | 0  |  |             |      |
| Courie access     Documents     Documents     Documents     Documents     Pictures     Pictures     FAST_Platfor     FS2633D front er     Function 1     Miss scripts     S32R3 No Safety | Name,                                       | 5                  | anus Date modified Ty  | pe  | Size   |  |    | bd   |             |      |
| File name: 530<br>Save as type: .ctg (  | 32104                                       |                    |  |     |  |  |    | guration   | ,           |      |
| <ul> <li>Hide Folders</li> </ul>  |   |                    |  |     | Save   | Canci  | el | alley mode control                               |             |      |
|   | VBST_OV_OTP<br>VBST_PH_OTP<br>VBSTLS_SR_OTP |                    | Auto-enable mode<br>1 Clock Cycle<br>PU = 2Ω / PD = 1.7Ω<br>180 ns | COR | E_MODE_OTP<br>E_SS_OTP<br>E_ILIM_OTP<br>E_PH_OTP | CCM only<br>Fast ramp<br>2.5 A<br>2 Clock Cycles | •  | CCH only<br>Fast ramp<br>2.5 A<br>2 Clock Cycles |             |      |

### 7.5.4 OTP import to mirror registers

This option is used to import the configuration file previously saved. Click on OTP import button and select the the.txt configuration file previously saved from this tab.

|                   | System Configuration                          |                      | I/Os Configuration                   | Power Up Sequence   |
|-------------------|---|----------------------|--------------------------------------|---|
| VSUP_UVTH_OTP 4.  | V/4.3 V + 4.8 V/4.3 V                         | I01STAGE_OTP Low Sid | te Driver + Low Side Driver          | TSLOT_OTP 250 µs + 250 µs                                     |
| WK1DF5_DI5_OTP En | abled + Enabled                               | 101PU_OTP PuHUp      | Disabled * Pull-Up Disabled          | SLOT_BYP_OTP Bypass Deabled * Bypass Deabled                  |
| RETRY_DIS_OTP En  | abled = Enabled                               | 101PD_OTP Pul-Dov    | wn Disable * Pull-Down Disabled      | CORE_SLOT_OTP OFF . OFF                                       |
| RETRY_MODE_OTP LI | ited retry + Limited retry                    | ID1TH_OTP Low vol    | tage thre + Low voltage threshold    | LD01_SLOT_OTP OFF + OFF                                       |
| RETRY_MSK_OTP 80  | 0 ms = 800 ms                                 | IO2STAGE_OTP Low Sid | fe Driver * Low Side Driver          | LD02_SL0T_0TP OFF * OFF                                       |
| OLK_FREQ_OTP 18   | MH2 * 16 MH2                                  | JO2PU_OTP Pul-Up I   | Disabled · Pull-Up Disabled          | TRK1_SLOT_OTP OFF * OFF                                       |
| BOS_IN_OTP AU     | to Transition c + Auto Transition on VPRE_UVH | 102PD_OTP Pul-Dov    | wn Deable • Pul-Down Deabled         | TRIQ_SLOT_OTP OFF + OFF                                       |
|                   | Write Read                                    | IO2TH_OTP Low vol    | tage thre + Low voltage threshold    | VREF_SLOT_OTP OFF + OFF                                       |
|                   |   | WKITH_OTP High vol   | tage thre + High voltage threshold   | 101_SLOT_0TP 0FF + 0FF  |
|                   |   | WK2TH_OTP Low vol    | tage thre + Low voltage threshold    | 102_SLOT_OTP OFF + OFF  |
|                   |   | WK1PD_OTP Disabled   | f - Disabled                         | Write Read  |
|                   |   | WK2PD_OTP Disabled   | f + Dsabled                          |   |
|                   |   | -                    | Write Read                           |   |
|                   |   |                      |                                      |   |
|                   | VPRE Configuration                            |                      | VBST Configuration                   | VCORE Configuration   |
| VPRE_OTP          | 5.40 V + 5.40 V                               | VBST_OTP             | 8.00 V + 8.00 V                      | VCORE_OTP 1.50 V * 1.50 V                                     |
| VPRE_LP_OTP       | 3.70 V + 3.70 V                               | VBST_CFG_OTP         | Front-end boost * Front-end boost    | CORE_CTRL_OTP Valley mode cont * Valley mode control          |
| VPRE_LP_DVS_OTP   | 22 mV/us * 22 mV/us                           | VEST_OV_OTP          | Auto-enable moc * Auto-enable mode   | CORE_MODE_OTP CCH only - CCH only                             |
| VPRE_OC_OTP       | 2.0 A • 2.0 A                                 | VBST_PH_OTP          | 1 Clock Cycle + 1 Clock Cycle        | CORE_SS_OTP Fast ramp * Fast ramp                             |
| VPRE_OC_DGLT_OTP  | 250 µs * 250 µs                               | VBSTLS_SR_OTP        | PU = 20 / PD = - PU = 20 / PD = 1.70 | CORE_113M_0TP 2.5 A + 2.5 A                                   |
| VPRE_SS_OTP       | 269 µs + 269 µs                               | VEST_TON_MEN_OTF     | P 160 ns + 160 ns                    | CORE_PH_OTP 2 Clock Cycles * 2 Clock Cycles                   |
| VPRE_POWN_DLY_OTP |   | VBST_SS_OTP          | 0.6 ms + 0.6 ms                      | COREHS_SR_OTP Rise = 3 V/ns; Fa = Rise = 3 V/ns; Fal = 2 V/ns |
| VPRE_BOS_OTP      | 5.00 V + 5.00 V                               | VEST_MAX_DC_OTP      |                                      | CORE_GM_OTP 53 uSemens * 53 uSemens                           |
| VPRE_PH_OTP       | No delity - No delity                         | VEST_CCOMP_OTP       | 200 pF + 200 pF                      | CORE_CCOMP_OTP 60 pF - 60 pF                                  |
| VPRE_SR_OTP       | Slow mode * Slow mode                         | VBST_GMCOMP_OTP      |                                      | CORE_RCOMP_OTP 200 kg + 200 kg                                |
| VPRE_GM_OTP       | 10 uSiemens • 10 uSiemens                     | VEST_RCOMP_OTP       | 1000 kD + 1000 kD                    | CORE_LSEL_OTP 1 µH + 1 µH                                     |
| VPRE_CCOMP_OTP    | 12.0 pF + 12.0 pF                             | VBST_BLM_OTP         | 60 mV/RSNS + 60 mV/RSNS              | CORETDFS_OTP VCORE disabled ( * VCORE disabled only           |
| VPRE_RCOMP_OTP    | 1300 KD • 1300 KD                             | VBST_SC_OTP          | 0 mV/µs • 0 mV/µs                    | CORETSD_PD_OTP Pull-down enable * Pull-down enabled in TSD    |
| VPRE_SC_OTP       | 1181 mV/µs • 1181 mV/µs                       |                      | Write Read                           | Witte Road  |
|                   |   |                      |                                      |   |

#### Figure 54. OTP Import for reference

### 7.6 Device programming

This section is used to burn permanently an OTP configuration on the OTP fuses. To enable this window device must be in test mode.

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| Device Programm       | ing Configuration |                  |          |             | Fuse    | Box Status        |            |             |            |
|-----------------------|-------------------|------------------|----------|-------------|---------|-------------------|------------|-------------|------------|
| Config Source         | Script -          | Main Programming | ) Status | Main Sector | r Flags | FailSafe Programm | ing Status | FailSafe Se | ctor Flags |
| Select Config Script  | Browse            | BUSY             | 0        | CRCSTS0     | 1       | BUSY              | 0          | CRCSTS0     | 1          |
| Config Script         | Not Selected      | ERROR            | 0        | CRCSTS1     | 0       | ERROR             | 0          | CRCSTS1     | 0          |
| Part number Selection | Select 🔻          | ONE_ERR          | 0        | CRCSTS2     | 0       | ONE_ERR           | 0          | CRCSTS2     | 0          |
| Status                | Not Ready         | TWO_ERR          | 0        | SECTBE0     | 1       | TWO_ERR           | 0          | SECTBE0     | 1          |
|                       |                   | MAX_PGM_EXCEED   | 0        | SECTBE1     | 0       | MAX_PGM_EXCEED    | 0          | SECTBE1     | 0          |
|                       |                   | VRR_CHECK_TRIES  | 1        | SECTBE2     | 0       | VRR_CHECK_TRIES   | 1          | SECTBE2     | 0          |
|                       |                   | PGM_FAIL_WP      | 0        | SECTWP0     | 1       | PGM_FAIL_WP       | 0          | SECTWP0     | 1          |
|                       |                   | BOOT_ERROR       | 0        | SECTWP1     | 0       | BOOT_ERROR        | 0          | SECTWP1     | 0          |
|                       |                   | VRR_ERROR        | 0        | SECTWP2     | 0       | VRR_ERROR         | 0          | SECTWP2     | 0          |
| Program               | Reset             |                  |          |             |         | Read              |            |             |            |

Figure 55. Device programming

To program an OTP configuration Vdebug pin must be higher than VDBG65TH. To apply this voltage, turn on SW7 (Apply 8 V to Vdebug).

Click on Browse to select an OTP script file, then click on program button to run the script. If Vdebug not set to 8 V a pop-up appears asking to turn on SW7, or it turns on automatically if jumper J13 is on Automatic mode J13 3-2.

If the required conditions are met (sectors available), the programming starts. Otherwise the execution is cancelled. To verify sectors are available click on read button from Fuse Box Status.

OTP is programmed into SECTBE2 of Main and Failsafe. SECTBE1 and SECTBE0 are reserved for NXP users only.

Blue or '0': Available

Yellow or '1': Not available

When programming is complete, a pop-up appears to request to turn off SW7 and SW6 (Put Vdebug to 0 V).

If the device was programmed correctly the power-up sequence starts. Fuse box status can be read to verify if sectors are burned. In some conditions a power up could be required.

### 7.7 INT tab

This tab allows access to monitor the regulators and safety events. To access the Interrupt Editor window, Menu >> INT **OR** View >>Show>> Interrupt Editor

It is separated in two tabs: interrupt tab and safety diagnostic tab.

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| ARP OV Ø Het Maked   Car all Rad Pol <b>Registron Status Registron Status</b> <  |                        | onfiguration | Safety          | Dagnostic   | s               |                    |        |                       |      |                |        |             |                 |      |                | <i></i>          |          |  |      |                |   | Read A |
|--|------------------------|--------------|-----------------|-------------|-----------------|--------------------|--------|-----------------------|------|----------------|--------|-------------|-----------------|------|----------------|------------------|----------|--|------|----------------|---|--------|
| RIP UVN       B       Int K Haded       LO1 Shutdown       B       Int K Haded       VIR       VIR       VIR       B       Int K Haded       VIR       VIR       VIR       B       Int K Haded       VIR       VIR       B       Int K Haded       VIR       VIR       VIR       B       Int K Haded       B       VIR       VIR       B       Int K Haded       B       VIR       B       Int K Haded       B       DI       DI </th <th>s</th> <th>ystem Sup</th> <th></th> <th>Inder Volt</th> <th></th> <th></th> <th>Over T</th> <th>and the second second</th> <th></th> <th></th> <th></th> <th></th> <th></th> <th>int</th> <th></th> <th>ē</th> <th></th> <th>Contraction of the local division of the loc</th> <th></th> <th></th> <th></th> <th></th> | s                      | ystem Sup    |                 | Inder Volt  |                 |                    | Over T | and the second second |      |                |        |             |                 | int  |                | ē                |          | Contraction of the local division of the loc |      |                |   |        |
| R2P OV 0 Het Makel   R2P OV 0 Het Makel <th></th> <th>Clear</th> <th>Clear<br/>Status</th> <th>Mask</th> <th>Mask<br/>Status</th> <th></th> <th>Clear</th> <th>Clear<br/>Status</th> <th>Mask</th> <th>Mask<br/>Status</th> <th></th> <th>Clear</th> <th>Clear<br/>Status</th> <th>Mask</th> <th>Mask<br/>Status</th> <th></th> <th>Clear</th> <th>Clear<br/>Status</th> <th>Mask</th> <th>Hask<br/>Status</th> <th></th> <th></th>  |                        | Clear        | Clear<br>Status | Mask        | Mask<br>Status  |                    | Clear  | Clear<br>Status       | Mask | Mask<br>Status |        | Clear       | Clear<br>Status | Mask | Mask<br>Status |                  | Clear    | Clear<br>Status  | Mask | Hask<br>Status |   |        |
| RR UVG       B       Int K Maked       B   | ISUP UVH               |              |                 |             | Not Masked      | LDO1 Shutdown      |        | 0                     |      | Not Masked     | VPRE   |             |                 |      | Not Masked     | WARE1 Event      |          | 1  |      | Not Masked     |   |        |
| NOS UVIN _ B _ Inct Maked<br>SEUVIN _ V _ B _ Inct Maked<br>ST_OV _ B _ Inct Maked<br>Coar all Rod Poll  | SUP OV                 |              | 0               |             | Not Masked      | LDO2 Shutdown      |        | 0                     |      | Not Masked     | VBST   |             |                 |      | Not Masked     | WARE2 Event      |          | 1  |      | Not Masked     |   |        |
| RE UNI V       Incl Makel       VTM2 Shudowi       Incl Makel       LDQ2       Incl  | UP UV6                 |              | 0               |             | Not Masked      | VCORE Shutdown     |        |                       |      | Not Masked     | VCORE  |             |                 |      | Not Masked     | 101 Event        |          | 0  |      | Not Masked     |   |        |
| ST_OV         8         Int Hade         Int I         8         Int Hade         Int Hade           Clear al         Read         Pol         Int Hade         Int H   | IOS UVH                |              | ٥               |             | Not Masked      | VTRK1 Shutdown     |        | 0                     |      | Not Masked     | LD01   |             | ٥               |      | Not Masked     | 102 Event        |          | 0  |      | Not Masked     | 0 |        |
| Cor al         Red         Pol           TP2         8         Not Madel         91 Occ         8         91 Occ         91 Occ         91 Occ         91 Occ   | PRE UVH                | X            |                 |             | Not Masked      | VTRK2 Shutdown     |        | 0                     |      | Not Masked     | LD02   |             | 0               |      | Not Masked     | LOT Event        |          | 0  |      | Not Masked     |   |        |
| Regulators Status         Series         Read         Pol         Series         Read         Pol           V0057         0  | BST_OV                 |              | ٥               |             | Not Masked      | Clear al           | 1      | Read                  | Pol  |                | TRK1   |             |                 |      | Not Masked     | Invalid register |          | 0  |      | Not Masked     |   |        |
| Cor al Read Pol         Sense<br>Status         Status         Sense<br>Status         Status  | 14                     | Clear all    | Read            | Po          | al 👘            |                    |        |                       |      |                | TRK2   |             | 0               |      | Not Masked     | SPI Clock        |          | 0  |      | Not Masked     |   |        |
| Angelators Status           Satus           V6         0           00057         0           98E_5         0           101_5         0           902_5         0           92_5         0           15711_0V_5         0   |                        |              |                 |             |                 |                    |        |                       |      |                |        | Clear all   | Read            | Pd   | 4              | SPI ORC          |          | 0  |      | Not Masked     |   |        |
| State           #4         0           #5         0           #6.5         0           0.5.4         0           0.5.4         0           8.5         0           5.4         0           5.5         0           5.5         0           5.5         0           5.5         0   |                        |              |                 |             |                 |                    |        |                       |      |                |        |             |                 |      |                | 0                | lear all | Re   | ad   | Pol            |   |        |
| Read Pol   | RK1_S<br>RK2_S<br>RF_S | s            |                 | 0<br>0<br>0 |                 |                    |        |                       |      |                |        |             |                 |      |                |                  |          |  |      |                |   |        |
|  | IS THE UV              | Read         | Pol             | ]           | J               |                    |        |                       |      |                |        |             |                 |      |                |                  |          |  |      |                |   |        |
|  |                        |              |                 |             |                 |                    |        |                       |      |                |        |             |                 |      |                |                  |          |  |      |                |   |        |
|  |                        |              |                 |             |                 |                    |        |                       |      |                |        |             |                 |      |                |                  |          |  |      |                |   |        |
|  |                        |              |                 |             |                 |                    |        |                       |      |                |        |             |                 |      |                |                  |          |  |      |                |   |        |
| Fernware: 0.11 Application 3.1.145 Device Hode: user mode Color learned: Tech 🥣 Lev 🥌 PS STATES : 4 Debug entry  |                        |              | elication 1     | 1.1.146 De  | Nice Mode: Lut  | r-mode Color Incur | at Hei |                       | Low  | FS STATE       | 5; 42  | Vebug entry |                 |      |                |                  |          |  |      |                |   |        |
| Financians: 0.11 Application 3.1.145 Device Hode: user-mode Color legend: High 🦰 Low 🥽 FS_STATES : 4-Debug entry   |                        |              | plication 3     | 1.1.146 De  | tvice Mode: use | ermode Color leger | dt Hg  | h 🧰 [                 | Low  | FS_STATES      | 5: 4-C | hebug entry |                 |      |                |                  |          |  |      |                |   |        |

The below legend and functions apply to both tabs:

- Blue means Low or not activated.
- Yellow means High or activated.
- To clear flags, click on each check box from clear column or click on clear all button.
- To **mask** the interruption, check the box of each interruption from mask column.
- Click on **Read** button of each box to read the current status or on **Read all** button to update the whole tab.
- Use Poll button to read each box periodically.

Sense status can be read only.

#### 7.7.1 Interruptions

This tab allows the user to monitor the regulators, Wake inputs, I/O and communication events or status. It allows read, write and poll over/under voltage, over temperature and over current of device. You can read, clear or mask an interruption.

If an event occurs flag changes to red. When regulators are red or '1' they are turned ON.

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| Over Temperature Over Current |       |           |                 |      |                |              | Miscella  | aneous           |        |                |               |
|-------------------------------|-------|-----------|-----------------|------|----------------|--------------|-----------|------------------|--------|----------------|---------------|
| Mask<br>Status                |       | Clear     | Clear<br>Status | Mask | Mask<br>Status |              | Cle       | ar Clea<br>Statu | r Mask | Mask<br>Status | Sens<br>State |
| N/V                           | VPRE  |           |                 |      | N/V            | WAKE1 EV     | ent 🗌     |                  |        | N/V            |               |
| N/V                           | VBST  |           |                 |      | N/V            | WAKE2 EV     | ent 🗌     |                  |        | N/V            |               |
| N/V                           | VCORE |           |                 |      | N/V            | IO1 Event    |           |                  |        | N/V            |               |
| N/V                           | LDO1  |           |                 |      | N/V            | IO2 Event    |           |                  |        | N/V            |               |
| N/V                           | LDO2  |           |                 |      | N/V            | LDT Event    |           |                  |        | N/V            |               |
|                               | TRK1  |           |                 |      | N/V            | Invalid regi | ster 🗌    |                  |        | N/V            |               |
| ·                             | TRK2  |           |                 |      | N/V            | SPI Clock    |           |                  |        | N/V            |               |
|                               |       | Clear all | Read            | Poll |                | SPI CRC      |           |                  |        | N/V            |               |
|                               |       |           |                 |      |                |              | Clear all | Re               | ad     | Pol            |               |
|                               |       |           |                 |      |                |              |           |                  |        |                |               |
|                               |       |           |                 |      |                |              |           |                  |        |                |               |

### 7.7.2 Safety diagnostics

Safety diagnostics tab allows the monitoring of safety events such as VMON status, bad WD, SPI communication errors, FCCU pins, safety outputs, ABIST1 and ABIST2 status.

|         | F         | S VMON Sta      | atus |                |               | Safe  | ty Diagr        | ostics |                |                 |            |        | Safe IO         |                 | Flags       | and Status      |                 |
|---------|-----------|-----------------|------|----------------|---------------|-------|-----------------|--------|----------------|-----------------|------------|--------|-----------------|-----------------|-------------|-----------------|-----------------|
|         | Clear     | Clear<br>Status | Mask | Mask<br>Status |               | Clear | Clear<br>Status | Mask   | Mask<br>Status | Sense<br>Status |            | Clear  | Clear<br>Status | Sense<br>Status | Clear       | Clear<br>Status | Sense<br>Status |
| EXT_UV  |           |                 |      | N/V            | BAD_WD_DATA   |       |                 |        | N/V            |                 | EXT_RSTB   |        |                 |                 | OTP_CORRUPT |                 |                 |
| EXT_OV  |           |                 |      |                | BAD_WD_TIMING |       |                 |        |                |                 | RSTB_EVENT |        |                 |                 | REG_CORRUPT |                 |                 |
| REF_UV  |           |                 |      | N/V            | FS_DIGREF_OV  |       |                 |        |                |                 | RSTB_DIAG  |        |                 |                 | TM_ACTIVE   |                 |                 |
| REF_OV  |           |                 |      |                | ABIST2_PASS   |       |                 |        |                |                 | RSTB_REQ   |        |                 |                 | DBG_MODE    |                 |                 |
| TRK2_UV |           |                 |      | N/V            | ABIST2_DONE   |       |                 |        |                |                 | FS0B_DIAG  |        |                 |                 | FS_COM      |                 |                 |
| TRK2_OV |           |                 |      |                | SPI_FS_CLK    |       |                 |        |                |                 | FS0B_REQ   |        |                 |                 | FS_WD       |                 |                 |
| TRK1_UV |           |                 |      | N/V            | SPI_FS_REQ    |       |                 |        |                |                 | FS1B_DIAG  |        |                 |                 | FS_IO       |                 |                 |
| TRK1_OV |           |                 |      |                | SPI_FS_CRC    |       |                 |        |                |                 | FS1B_REQ   |        |                 |                 | FS_REG_OVUV |                 |                 |
| LDO2_UV |           |                 |      | N/V            | FS_OSC_DRIFT  |       |                 |        |                |                 | GOTO_INIT  |        |                 |                 | FS_BIST     |                 |                 |
| LDO2_OV |           |                 |      |                | FCCU1         |       |                 |        | N/V            |                 | RSTB_DRV   |        |                 |                 | Clear all   | Read P          | Poll            |
| LDO1_UV |           |                 |      | N/V            | FCCU2         |       |                 |        | N/V            |                 | RSTB_SNS   |        |                 |                 |             |                 |                 |
| LDO1_OV |           |                 |      |                | FCCU12        |       |                 |        |                |                 | FS0B_DRV   |        |                 |                 |             |                 |                 |
| CORE_UV |           |                 |      | N/V            | ERRMON        |       |                 |        | N/V            |                 | FS0B_SNS   |        |                 |                 |             |                 |                 |
| CORE_OV |           |                 |      |                | ABIST1_PASS   |       |                 |        |                |                 | FS1B_DRV   |        |                 |                 |             |                 |                 |
| VPRE_UV |           |                 |      | N/V            | ERRMON_PIN    |       |                 |        |                |                 | FS1B_SNS   |        |                 |                 |             |                 |                 |
| VPRE_OV |           |                 |      |                | FCCU1_RT      |       |                 |        |                |                 | Clea       | ar all | Read            | Poll            |             |                 |                 |
|         | Clear all | Read            | Poll |                | FCCU2_RT      |       |                 |        |                |                 |            |        |                 |                 |             |                 |                 |
|         |           |                 |      |                | Clear         | all   | Read            |        | Pol            |                 |            |        |                 |                 |             |                 |                 |

Figure 58. Safety diagnostics tab

ABIST1\_PASS Yellow means that it is done and PASS, since we can read '1' from its register. 0 or blue after execution means fail.

### 7.8 OTP tool

This tool allows user to configure OTP registers, to save configurations and to generate scripts in different file formats which can be burnt (OTP script) or emulated (TBB script) into the FS26 SBC.

To access the FS26 OTP tool, launch NXP GUI Application and Navigate to the **OTP** Tool **OR** Access OTP Tool from Menu: View >> Show/Hide >>OTP Tool

It is possible to save a configuration to visualize or to modify it later. Click on save config to export or File then Save. To import Click on Import button or from File then Load.

### 7.8.1 OTP tool application menu

All blocks in the OTP tool have default values configured on launch. It consists of the following configuration sections:

- System configuration
- · Switching regulators
- Regulators
- Voltage monitoring
- System safety configuration

|  | tion Switching Regulat   | cor neg | ulators Voltage M |                |             |               |                 | _ | Import | Save Config | Customer De  | Carls  |
|--|--|---------|-------------------|----------------|-------------|---------------|-----------------|---|--------|-------------|--|--|
|  | Block Diagram  |         | System            | n Configuratio | n           | Pow           | er-up Sequence  |   |        | ·           | Company Name*  | [Company Name]   |
|  | FS26-D   |         | VSUP_UVTH_OTP     | 4.8 V/4.3 V    | •           | TSLOT_OTP     | 250 µs          | * |        |             | Location   | [Company Location]   |
|  | I  |         | WK1DFS_DIS_OTP    | Enabled        | *           | SLOT_BYP_OTP  | Bypass Disabled | * |        |             | Contact Name*  | Pro  |
| VBST   | → J ++ s   | 5.00 V  | RETRY_DIS_OTP     | Enabled        | -           | CORE_SLOT_OTP | Slot 0          |   |        |             | Contact Name*  | (concace name)   |
| VPRE   |  | 3.20 V  | RETRY_MODE_OTP    | Limited retry  | •           | LD01_SLOT_OTP | Slot 0          | • |        |             | Contact E-mail*  | [Contact E-mail]   |
|  |  |         | RETRY_MSK_OTP     | 100 ms         | -           | LD02_SLOT_OTP | Slot 0          | - |        |             | Phone Number*  | [Contact Phone Number  |
| VCOR   |  | 0.80 V  | CLK_FREQ_OTP      | 16 MHz         | -           | TRK1_SLOT_OTP | Slot 0          | - |        |             | Address#1"   | [Company Address]  |
| LDOI   | <b>1</b> → 3   | 3.3 V   | BOS_IN_OTP        | Auto Transitio | n on VPRE * | TRK2_SLOT_OTP | Slot 0          | * |        |             |  |  |
| LDO  | 2 3  | 1.3 V   |                   |                |             | VREF_SLOT_OTP | Slot 0          | * |        |             | Address#2  |  |
| TRK  | 1  | 1% VRI  |                   |                |             | IO1_SLOT_OTP  | Slot 0          | • |        |             | City*  | [Cty]  |
| TRKZ   |  | % VRI   |                   |                |             | IO2_SLOT_OTP  | Slot 0          | • |        |             | Zip Code*  | [Zip/ Postal Code]   |
| VREF   |  | .3 V    |                   |                |             | 199           |                 |   |        |             | Country*   | [Country]  |
|  |  |         |                   |                |             |               |                 |   |        |             |  | [control ]]  |
|  |  |         |                   |                |             |               |                 |   |        |             | Other Info   | -  |
| 1/0  | ) Configuration  |         |                   |                | Seque       | ence Diagram  |                 |   |        |             | C Program Det  | alla -   |
|  |  |         |                   |                |             |               |                 |   |        |             |  |  |
| DISTAGE_OTP  | Disabled   | •       |                   |                |             |               |                 |   |        |             |  |  |
|  | Disabled<br>Pull-Up Enabled  | •       |                   |                |             |               |                 |   |        |             |  | [Program Name]   |
| DIPU_OTP   |  |         |                   |                |             |               |                 |   |        |             | Program Name*<br>Application*<br>Production Date   | [Program Name]<br>[Application Description]<br>[Targeted Production Date   |
| DIPU_OTP<br>DIPD_OTP   | Pull-Up Enabled  |         | VPRE              |                |             |               |                 |   |        |             | Program Name*<br>Application*<br>Production Date<br>Sample Date*   | [Program Name]<br>[Application Description]  |
| DIPU_OTP<br>DIPD_OTP<br>DITH_OTP   | Pul-Up Enabled<br>Pul-Down Enabled   | •       | VERE              |                |             |               |                 |   |        |             | Program Name*<br>Application*<br>Production Date<br>Sample Date*<br>Other Info   | [Program Name]<br>[Application Description]<br>[Targeted Production Da<br>[Require Sample Date]                                  |
| DIPU_OTP<br>DIPD_OTP<br>DITH_OTP<br>DISTAGE_OTP  | Pul-Up Enabled<br>Pul-Down Enabled<br>Low voltage threshold  |         |                   |                |             |               |                 |   |        |             | Program Name*<br>Application*<br>Production Date<br>Sample Date*<br>Other Info<br>Device Type<br>OTP ID                | [Program Name]<br>[Application Description]<br>[Targeted Production Da<br>[Require Sample Date]<br>[F526-0<br>A0                 |
| DIPU_OTP<br>DIPD_OTP<br>DITH_OTP<br>D2STAGE_OTP<br>D2PU_OTP  | Pul-Up Enabled<br>Pul-Down Enabled<br>Low voltage threshold<br>Disabled  |         | VCORE             |                |             |               |                 |   |        |             | Program Name*<br>Application*<br>Production Date<br>Sample Date*<br>Other Info<br>Device Type<br>OTP ID<br>Part Number | [Program Name]<br>[Appkation Description]<br>[Targeted Production Da<br>[Require Sample Date]<br>FS26-0<br>A0<br>PFS26AMDA0ES    |
| DIPU_OTP<br>DIPD_OTP<br>DITH_OTP<br>DISTAGE_OTP<br>DIPU_OTP<br>DIPU_OTP  | Pull-Up Enabled<br>Pull-Down Enabled<br>Low voltage threshold<br>Disabled<br>Pull-Up Enabled   |         |                   |                |             |               |                 |   |        |             | Program Name*<br>Application*<br>Production Date<br>Sample Date*<br>Other Info<br>Device Type<br>OTP ID                | [Program Name]<br>[Appkation Description]<br>[Targeted Production Da<br>[Require Sample Date]<br>[F526-D<br>A0<br>PF526AMDA0ES   |
| 019U_0TP<br>019D_0TP<br>01TH_0TP<br>025TAGE_0TP<br>025U_0TP<br>025D_0TP<br>025D_0TP<br>021H_0TP  | Pul-Up Enabled<br>Pul-Down Enabled<br>Low voltage threshold<br>Disabled<br>Pul-Up Enabled<br>Pul-Up Enabled  |         | VCORE             |                |             |               |                 |   |        |             | Program Name*<br>Application*<br>Production Date<br>Sample Date*<br>Other Info<br>Device Type<br>OTP ID<br>Part Number | [Program Name]<br>[Appkation Description]<br>[Targeted Production Da<br>[Require Sample Date]<br>[F526-D<br>A0<br>PF526AMDA0ES   |
| O1PU_OTP<br>O1PD_OTP<br>O1TH_OTP<br>O2STAGE_OTP<br>O2PU_OTP<br>O2PD_OTP<br>O2PD_OTP<br>O2TH_OTP<br>WK1TH_OTP                                       | PuE-Up Enabled<br>PuE-Down Enabled<br>Low voltage threshold<br>Disabled<br>PuE-Up Enabled<br>PuE-Down Enabled<br>Low voltage threshold   |         |                   |                |             |               |                 |   |        |             | Program Name*<br>Application*<br>Production Date<br>Sample Date*<br>Other Info<br>Device Type<br>OTP ID<br>Part Number | [Program Name]<br>[Appkation Description]<br>[Targeted Production Da<br>[Require Sample Date]<br>[F526-D<br>A0<br>PF526AMDA0ES   |
| DIPU_OTP<br>OIPD_OTP<br>OITH_OTP<br>D2STAGE_OTP<br>D2STAGE_OTP<br>D2PD_OTP<br>D2PD_OTP<br>D2PD_OTP<br>D2TH_OTP<br>WK1TH_OTP<br>WK2TH_OTP           | PuE-Up Enabled<br>PuE-Down Enabled<br>Low voltage threshold<br>Disabled<br>PuE-Up Enabled<br>PuE-Down Enabled<br>Low voltage threshold<br>Low voltage threshold                          |         | VCORE             |                |             |               |                 |   |        |             | Program Name*<br>Application*<br>Production Date<br>Sample Date*<br>Other Info<br>Device Type<br>OTP ID<br>Part Number | [Program Name]<br>[Appkation Description]<br>[Targeted Production Da<br>[Require Sample Date]<br>[F526-D<br>A0<br>PF526AMDA0ES   |
| 01PU_0TP<br>01PU_0TP<br>01PD_0TP<br>02TH_0TP<br>02STAGE_0TP<br>02PU_0TP<br>02PD_0TP<br>02PD_0TP<br>02TH_0TP<br>0XETH_0TP<br>0KLTH_0TP<br>0KLTH_0TP | Put-Up Enabled<br>Put-Down Enabled<br>Low voltage threshold<br>Disabled<br>Put-Up Enabled<br>Put-Down Enabled<br>Low voltage threshold<br>Low voltage threshold<br>Low voltage threshold |         | VCORE             |                |             |               |                 |   |        |             | Program Name*<br>Application*<br>Production Date<br>Sample Date*<br>Other Info<br>Device Type<br>OTP ID<br>Part Number | [Program Name]<br>[Application Description]<br>[Targeted Production Di<br>[Require Sample Date]<br>[F526-D<br>A0<br>PF526AMDA0ES |
| 01PU_0TP<br>01PU_0TP<br>01TH_0TP<br>02STAGE_0TP<br>02PU_0TP<br>02PD_0TP<br>02PD_0TP<br>02TH_0TP<br>0XLTH_0TP<br>0KLTH_0TP<br>0KL2TH_0TP            | PuI-Up Enabled<br>PuI-Down Enabled<br>Low voltage threshold<br>Disabled<br>PuI-Down Enabled<br>Low voltage threshold<br>Low voltage threshold<br>Low voltage threshold<br>Disabled       |         | VCORE             |                |             |               |                 |   |        |             | Program Name*<br>Application*<br>Production Date<br>Sample Date*<br>Other Info<br>Device Type<br>OTP ID<br>Part Number | [Program Name]<br>[Application Description]<br>[Targeted Production Di<br>[Require Sample Date]<br>[F526-D<br>A0<br>PF526AMDA0ES |
| 0410,200,200,200,200,200,200,200,200,200,2   | PuI-Up Enabled<br>PuI-Down Enabled<br>Low voltage threshold<br>Disabled<br>PuI-Down Enabled<br>Low voltage threshold<br>Low voltage threshold<br>Low voltage threshold<br>Disabled       |         | VCCRE             |                |             |               |                 |   |        |             | Program Name*<br>Application*<br>Production Date<br>Sample Date*<br>Other Info<br>Device Type<br>OTP ID<br>Part Number | [Program Name]<br>[Appkation Description]<br>[Targeted Production Da<br>[Require Sample Date]<br>[F526-D<br>A0<br>PF526AMDA0ES   |

### 7.8.2 OTP configuration sections

#### 7.8.2.1 System config

This block consists of the parameter (bits) settings that are related to the System configuration registers of FS26. It displays block diagram with the selected regulators output values from Regulators section. It contains the Power up sequence configuration which is displayed in the sequence diagram. You can configure the I/O and Wake inputs as well.

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|  | gram         | Syster         | n Configuration           | Pow           | er-up Sequence  | I/             | 0 Configuration       |
|--|--------------|----------------|---------------------------|---------------|-----------------|----------------|-----------------------|
| FS26-D   |              | VSUP_UVTH_OTP  | 4.8 V/4.3 V 👻             | TSLOT_OTP     | 250 µs          | ▼ IO1STAGE_OTP | Disabled              |
| F320-L   | T            | WK1DFS_DIS_OTP | Enabled 👻                 | SLOT_BYP_OTP  | Bypass Disabled | IO1PU_OTP      | Pull-Up Enabled       |
| VBST   | 5.00 \       | RETRY_DIS_OTP  | Enabled 👻                 | CORE_SLOT_OTP | Slot 0          | IO1PD_OTP      | Pull-Down Enabled     |
|  | - <u></u> -  | RETRY_MODE_OTP | Limited retry -           | LDO1_SLOT_OTP | Slot 0          | ▼ IO1TH_OTP    | Low voltage threshold |
| VPRE   | - □-→ 3.20 \ | RETRY_MSK_OTP  | 100 ms 👻                  | LDO2_SLOT_OTP | Slot 0          | IO2STAGE_OTP   | Disabled              |
| VCORE  | - □> 0.80 \  | CLK_FREQ_OTP   | 16 MHz 👻                  | TRK1_SLOT_OTP | Slot 0          | IO2PU_OTP      | Pull-Up Enabled       |
| LD01   | → 3.3 V      | BOS_IN_OTP     | Auto Transition on VPRE - | TRK2_SLOT_OTP | Slot 0          | IO2PD_OTP      | Pull-Down Enabled     |
| LDO2   | → 3.3 V      |                |                           | VREF_SLOT_OTP | Slot 0          | ▼ IO2TH_OTP    | Low voltage threshold |
| TRK1   | → 1% V       | RI             |                           | IO1_SLOT_OTP  | Slot 0          | ▼ WK1TH_OTP    | Low voltage threshold |
| TRK2   | → 1% V       | RI             |                           | IO2_SLOT_OTP  | Slot 0          | WK2TH_OTP      | Low voltage threshold |
| VREF   | → 3.3 V      |                |                           |               |                 | WK1PD_OTP      | Disabled              |
|  | 010 1        |                |                           |               |                 | WK2PD_OTP      | Disabled              |
| VPRE   |              |                |                           |               |                 |                |                       |
| VORE   |              |                |                           |               |                 |                |                       |
| VCORE  |              |                |                           | _             |                 |                |                       |
|  |              |                |                           |               |                 |                |                       |
| LDO1   |              |                |                           |               |                 |                |                       |
| LD01   |              |                |                           |               |                 |                |                       |
|  |              |                |                           |               |                 |                |                       |
| LDO2   |              |                |                           | -             |                 |                |                       |
| LDO2<br>TRK1<br>TRK2                           |              |                |                           |               |                 |                |                       |
| LDO2   |              |                |                           |               |                 |                |                       |
| LDO2<br>TRK1<br>TRK2                           |              |                |                           |               |                 |                |                       |
| LD02<br>TRK1<br>TRK2<br>VREF<br>GPI01<br>GPI02 |              |                |                           |               |                 |                |                       |
| LDO2<br>TRK1<br>TRK2<br>VREF<br>GPI01          | 72644        | rtosti-        | 22904<br>2504             | uks.cs        |                 |                |                       |

#### 7.8.2.2 Regulators

The FS26 regulators are separated in two tabs, Switching regulator and Regulators (LDOs).

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| VPRE C            | onfiguration            |     | VBST             | Configuration                   | VCORE Configuration |                |                             |  |
|-------------------|-------------------------|-----|------------------|---------------------------------|---------------------|----------------|-----------------------------|--|
| /PRE_OTP          | 3.20 V                  | •   | VBST_OTP         | 5.00 V                          | •                   | VCORE_OTP      | 0.80 V -                    |  |
| PRE_LP_OTP        | 3.20 V                  | -   | VBST_CFG_OTP     | Front-end boost                 | •                   | CORE_CTRL_OTP  | Valley mode control         |  |
| VPRE_LP_DVS_OTP   | 22 mV/µs                | -   | VBST_OV_OTP      | Auto-enable mode                | -                   | CORE_MODE_OTP  | CCM only -                  |  |
| VPRE_OC_OTP       | 0.6 V                   | -   | VBST_PH_OTP      | No delay                        | -                   | CORE_SS_OTP    | Slow ramp -                 |  |
| VPRE_OC_DGLT_OTP  | 250 µs                  | -   | VBSTLS_SR_OTP    | $PU = 2\Omega / PD = 1.7\Omega$ | -                   | CORE_ILIM_OTP  | 1.0 A -                     |  |
| VPRE_SS_OTP       | 269 µs                  | -   | VBST_TON_MIN_OTP | 180 ns                          | -                   | CORE_PH_OTP    | No delay                    |  |
| VPRE_PDWN_DLY_OTP | 100 µs                  | -   | VBST_SS_OTP      | 0.6 ms                          | -                   | COREHS_SR_OTP  | Rise = 3 V/ns; Fall = 2 V - |  |
| VPRE_BOS_OTP      | 3.20 V                  | -   | VBST_MAX_DC_OTP  | 72.50%                          | -                   | CORE_GM_OTP    | 13 uSiemens                 |  |
| VPRE_PH_OTP       | No delay                | -   | VBST_CCOMP_OTP   | 200 µF                          | -                   | CORE_CCOMP_OTP | 50 pF                       |  |
| VPRE_SR_OTP       | Slow mode               | -   | VBST_GMCOMP_OTP  | 3.9 µS                          | -                   | CORE_RCOMP_OTP | 150 kΩ -                    |  |
| VPRE_GM_OTP       | 10 uSiemens             | -   | VBST_RCOMP_OTP   | 1000 kΩ                         | -                   | CORE_LSEL_OTP  | 1 µH -                      |  |
| VPRE_CCOMP_OTP    | 12.0 pF                 | -   | VBST_ILIM_OTP    | 60 mV/RSNS                      | -                   | CORETDFS_OTP   | VCORE disabled only         |  |
| VPRE_RCOMP_OTP    | 1300 ΚΩ                 | -   | VBST_SC_OTP      | 0 mV/µs                         | -                   | CORETSD_PD_OTP | Pull-down enabled in TS     |  |
| VPRE_SC_OTP       | 1181 mV/µs              | -   |                  |                                 |                     |                |                             |  |
| VPRE_PFM_TON_OTP  | 240 ns                  | -   |                  |                                 |                     |                |                             |  |
| VPRE_PFM_TOFF_OTP | 80 ns                   | •   |                  |                                 |                     |                |                             |  |
| VPRE_CLK_OTP      | FSW/40                  | •   |                  |                                 |                     |                |                             |  |
| VPRETDFS_OTP      | VPRE disabled only      | •   |                  |                                 |                     |                |                             |  |
| VPRETSD_PD_OTP    | Pull-down enabled in TS | - 2 |                  |                                 |                     |                |                             |  |

In the switching regulators you can configure VPRE, VBST and VCORE output values and its internal parameters. You can select the Power topology by configuring the

| VBST_ | _CFG_ | OTP | bit | group. |  |
|-------|-------|-----|-----|--------|--|

| VBST         | Configuration     |
|--------------|-------------------|
| VBST_OTP     | 7.00 V 👻          |
| VBST_CFG_OTP | Front-end boost   |
| VBST_OV_OTP  | Independent boost |

In the Regulators tab, you will find: VLDO1, VLDO2, VTRK1, VTRK2, VREF output values and its TSD behavior.

#### 7.8.2.3 System safety configuration

This tab allows user to configure ABIST1 for each regulator, configure system reaction in case of Fault or enable and disable Watchdog timer.

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| System Configuration | Switching Regulator | Regulators | Voltage Monitoring  | System Safety Configuration | OTP ID |
|----------------------|---------------------|------------|---------------------|-----------------------------|--------|
| ABIST1               | Configuration       |            | System Saf          |                             |        |
| ABIST1_VPRE_EN_OTP   | Disabled            | -          | WAKE2_LP_EN_OTP     | Disabled 👻                  |        |
| ABIST1_VCORE_EN_OTF  | Disabled            | -          | FAULT_DFS_EN_OTP    | Go to DFS when FLT_EF 🔻     |        |
| ABIST1_LDO1_EN_OTP   | Disabled            | -          | FS1B_FS0B_EN_OTP    | Delayed Assertion Enable 🔻  |        |
| ABIST1_LDO2_EN_OTP   | Disabled            | -          | PRE_RSTB_DLY_EN_OTP | 0 us 👻                      |        |
| ABIST1_TRK1_EN_OTP   | Disabled            | -          | DIS8S_DIS_OTP       | 8 Second Timer Enabled 🔻    |        |
| ABIST1_TRK2_EN_OTP   | Disabled            | -          | WD_DIS_OTP          | WD Timer Enable 🔹           |        |
| ABIST1_VREF_EN_OTP   | Disabled            | -          | LBIST_STDBY_OTP     | Always perform LBIST 🔹      |        |
| ABIST1_EXT_EN_OTP    | Disabled            | -          |                     |                             |        |
|                      |                     |            |                     |                             |        |

#### 7.8.2.4 Voltage monitoring

This tab allows user to configure FS26 voltage monitoring and consists of the following:

- VMONPRE Configuration
- VMONLDO1 Configuration
- VMONCORE Configuration
- VMONLDO2 Configuration
- VMONEXT Configuration
- VMONREF Configuration

Make sure that each VMON is assigned with the same voltage output value configured on regulators tab, then select its fault OV/UV threshold and filtering time.

| System Configuration R | egulators  | Voltage Monitoring | System Safety Configuration |                  |   |                      | Import           | Save Co |
|------------------------|------------|--------------------|-----------------------------|------------------|---|----------------------|------------------|---------|
| VMONPRE                | Configura  | tion               | VMONLDO                     | 1 Configuration  |   | VMONTRK1             | Configuration    |         |
| PRE_V_OTP              | 3.2 V      | •                  | LDO1_V_OTP                  | 3.3 V            | • | TRK1_V_OTP           | 1.2 V            | •       |
| MON_PRE_OVTH_OTP       | 104.5 %    | •                  | VMON_LDO1_OVTH_OTP          | 104.5 %          | - | VMON_TRK1_OVTH_OTP   | 104.5 %          | -       |
| MON_PRE_UVTH_OTP       | 88 %       | •                  | VMON_LDO1_UVTH_OTP          | 88 %             | - | VMON_TRK1_UVTH_OTP   | 88 %             | •       |
| MON_PRE_OVDGLT_OTP     | 25 us      | •                  | VMON_LDO1_OVDGLT_OTP        | 25 us            | - | VMON_TRK1_OVDGLT_OTP | 25 us            | -       |
| MON_PRE_UVDGLT_OTP     | 5 us       | •                  | VMON_LDO1_UVDGLT_OTP        | 5 us             | • | VMON_TRK1_UVDGLT_OTP | 5 us             | •       |
| VMONCOF                | RE Configu | ration             | VMONLD                      | 02 Configuration |   | VMONTR               | (2 Configuration |         |
| CORE_V_OTP             | 0.8 V      | •                  | LDO2_V_OTP                  | 3.3 V            | • | TRK2_V_OTP           | 1.2 V            | •       |
| MON_CORE_OVTH_OTP      | 104.5 %    | •                  | VMON_LDO2_OVTH_OTP          | 104.5 %          | • | VMON_TRK2_OVTH_OTP   | 104.5 %          | •       |
| MON_CORE_UVTH_OTP      | 88 %       | •                  | VMON_LDO2_UVTH_OTP          | 88 %             | - | VMON_TRK2_UVTH_OTP   | 88 %             | •       |
| MON_CORE_OVDGLT_OTF    | 25 us      | •                  | VMON_LDO2_OVDGLT_OT         | P 25 us          | - | VMON_TRK2_OVDGLT_OTP | 25 us            | -       |
| MON_CORE_UVDGLT_OTP    | 5 us       | •                  | VMON_LDO2_UVDGLT_OT         | 5 us             | • | VMON_TRK2_UVDGLT_OTP | 5 us             | -       |
| VMONEXT                | Configura  | tion               | VMONREF                     | Configuration    |   |                      |                  |         |
| MON_EXT_OVTH_OTP       | 104.5 %    | •                  | VREF_V_OTP                  | 3.3 V            | • |                      |                  |         |
| MON_EXT_UVTH_OTP       | 88 %       | •                  | VMON_VREF_OVTH_OTP          | 104.5 %          | • |                      |                  |         |
| MON_EXT_OVDGLT_OTP     | 25 us      | •                  | VMON_VREF_UVTH_OTP          | 88 %             | • |                      |                  |         |

#### 7.8.2.5 OTP ID

Displays OTP ID. Only NXP users can create a new OTP ID.

|              | Program ID |
|--------------|------------|
| PROG_IDH_OTP | A          |
| PROG_IDL_OTP | 0          |

## 7.9 I/O pins tab

This section can control some I/Os connected to the KL26Z plugged freedom. It can read the device safety outputs externally or to control different voltage sources in order to apply sequences to apply debug mode without moving any switches.

The input pins are the pins that can be read from the MCU, they are input pins from MCU point of view. This section contains the safety outputs FS0B, FS1B and RSTB. You can read it once with Read button. Or you can select at which frequency you want to the read the pins, select the duration then start polling with Poll button.

| Log Window      |                   |           |          | Inpu   | t Pins |      |      | Output Pins              |
|-----------------|-------------------|-----------|----------|--------|--------|------|------|--------------------------|
| Filter Messages | SAVE CLEAR RUN FS | OB_MCU :  | Duration | 100 ms | •      | Poll | Read | MCU_DBG8V: OLow OHigh    |
| >               | FS                | IB_MCU :  | Duration | 100 ms | \$     | Poll | Read | MCU_DBG5V: OLow OHigh    |
| PT              | RS                | STB_MCU : | Duration | 100 ms | \$     | Poll | Read | VBAT_ctrl : O Low O High |
| 3               |                   |           |          |        |        |      |      |                          |
| ×               |                   |           |          |        |        |      |      |                          |
|                 |                   |           |          |        |        |      |      |                          |
| 2               |                   |           |          |        |        |      |      |                          |
| OR              |                   |           |          |        |        |      |      |                          |
| D               |                   |           |          |        |        |      |      |                          |
| ER)             |                   |           |          |        |        |      |      |                          |
|                 |                   |           |          |        |        |      |      |                          |
| 2               |                   |           |          |        |        |      |      |                          |
| P               |                   |           |          |        |        |      |      |                          |
|                 |                   |           |          |        |        |      |      |                          |

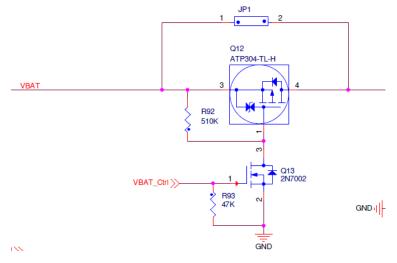
The output pins are thresholds that can be controlled with MCU. These pins are described in <u>Section 4.2.10 "VDebug pin voltage control"</u>.

- VBAT\_Ctrl: Open or close VBAT power supply
- MCU\_DBG5V: 5 V on VDebug pin
- MCU\_DBG8V: 8 V on VDebug pin

They can be used instead of the Manual switches SW6 and SW7. In order to use MCU\_DBG5V and MCU\_DBG8V for debug pin control, J13 must be on "Auto mode" J13 position 3-2. Select high or low to control the pins, default is low.

To use VBAT\_Ctrl the red jumper JP1 next to the VBAT switch must be OFF. Once you remove JP1 you can start using VBAT\_Ctrl instead of SW1 to turn on or off power supply.

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These pins are also accessible from script editor; you could use those pins to create script sequences.

## 8 Using FS26 NXP GUI

Once you have installed the NXP GUI (<u>Section 5.2 "Installing GUI software package"</u>) you can follow these instructions for a quick power up, debug, programming or enter the different operating modes of the FS26 SBC.

### 8.1 Power up

If your FS26 device already contains an OTP configuration, you only need to connect a power supply to the VBAT Phoenix connector or the VBAT jack connector. See <u>Section 4.2.2 "VBAT connectors"</u>.

It is recommended to set your power supply to an initial value of 12 V and current limited to 1 A.

Make sure your board has the right jumper configuration. Every KIT is delivered with a default jumper configuration as in <u>Section 4.3 "Default jumper configuration"</u>. This configuration is enabled for a boost in front end topology. For back end see <u>Section 4.2.3</u> "<u>Power topology configuration</u>".

Verify the KL25Z freedom is plugged, as well as the USB cable on KL25Z USB connector side. It is important that the USB cable is connected since in addition to enabling the communication with the NXP GUI, it provides voltages and references to some circuits on board as well as generates the VDDIO reference for the IC.

Since all the previous statements are valid or considered, you may use the switch SW1 to power on your board.

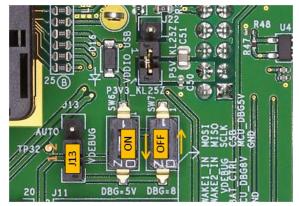
If your OTP configuration has many safety features enabled, your device may restart or turn off after a few seconds. Enter debug mode to waive some of those features.

### 8.2 Debug mode entry

To modify any parameters or to communicate with the IC, you may enter the debug mode. To enter debug mode, you should consider the power and connection statements from <u>Section 8.1 "Power up"</u>.

Once your KIT is ready, follow the next steps:

- 1. Make sure the device is powered off (SW1 middle position).
- Turn ON SW6 to apply 5 V to the VDebug pin. Make sure the jumper of J13 has the right configuration; default is Manual. See <u>Section 4.2.10 "VDebug pin voltage control"</u> for more details.



- 3. Power on VBAT, and the device will enter debug mode. This allows access to the register map, to emulate, or to program an OTP configuration on the NXP GUI.
- To verify you are in debug mode, you can use NXP GUI Register map window to Read FS\_STATES (0x17) or you can click on FS\_STATES display from USB and Device status bar.

FS\_STATES : 4-Debug entry

It is possible to start power up sequence and stay in debug mode. In order to start power up sequence, turn SW6 off to put VDebug pin to 0 V.

#### 8.3 Test mode entry

To enter the test mode, the chip needs to be in the Debug mode. Then test mode can be accessed by writing the appropriate key sequences.

You can access test mode from NXP GUI device manager or write the keys to the script editor

**From Device Manager:** Click on "Apply test mode" button to send the Main and Failsafe test mode entry keys.



#### From Script Editor:

Copy and paste the keys in the script editor:

// Main Test mode entry

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- SET\_REG:FS26:M\_TestMode:M\_TM\_ENTRY:0x0000
- SET REG:FS26:M TestMode:M TM ENTRY:0xD5A7
- SET\_REG:FS26:M\_TestMode:M\_TM\_ENTRY:0xB8EE
- SET\_REG:FS26:M\_TestMode:M\_TM\_ENTRY:0x0F37

//Fail Safe Test mode entry

SET\_REG:FS26:FS\_TestMode:FS\_TM\_ENTRY:0x0000

- SET\_REG:FS26:FS\_TestMode:FS\_TM\_ENTRY:0xD5A7
- SET\_REG:FS26:FS\_TestMode:FS\_TM\_ENTRY:0xB8EE
- SET\_REG:FS26:FS\_TestMode:FS\_TM\_ENTRY:0x0F37

GET\_REG:FS26:FS\_TestMode:FS\_TM\_STATUS1

| Script Commands Window  |
|---|
| // Main Test mode entry<br>SET_REG:FS26:M_TestMode:M_TM_ENTRY:0x0000<br>SET_REG:FS26:M_TestMode:M_TM_ENTRY:0xD5A7<br>SET_REG:FS26:M_TestMode:M_TM_ENTRY:0xB8EE<br>SET_REG:FS26:M_TestMode:M_TM_ENTRY:0x0F37   |
| //Fail Safe Test mode entry<br>SET_REG:FS26:FS_TestMode:FS_TM_ENTRY:0x0000<br>SET_REG:FS26:FS_TestMode:FS_TM_ENTRY:0xD5A7<br>SET_REG:FS26:FS_TestMode:FS_TM_ENTRY:0xB8EE<br>SET_REG:FS26:FS_TestMode:FS_TM_ENTRY:0x0F37<br>GET_REG:FS26:FS_TestMode:FS_TM_STATUS1 |

Then click on Run Script.



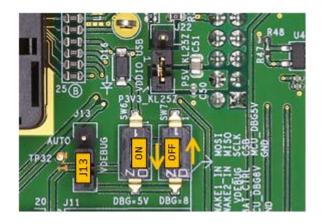
## 8.4 Emulate an OTP configuration

Before starting, make sure that the power conditions from <u>Section 8.1 "Power up"</u> are valid.

If you're not in debug mode:

1. Make sure the device is Powered off (SW1 middle position).

 Then turn ON SW6 to apply ~4.5 V to the VDebug pin. Make sure jumper J13 has the right configuration, default is Manual. See <u>Section 4.2.2 "VBAT connectors"</u> for more details.



3. Power on VBAT(SW1), and the device will be in debug mode.

If already in debug entry:

- 1. Open the NXP GUI, connect the device, and open the script editor.
- 2. Load a provided or created OTP configuration script (TBB) to load into the mirror registers.



3. Then click on the Run Script button.

A TBB script typically contains Test mode entry keys, if it doesn't have it. See <u>Section 8.3</u> <u>"Test mode entry"</u> to enter Test mode.

After running the script, you can read the mirror registers to verify the loaded OTP configuration in the OTP Mirrors tab. Turn the VDebug (SW6) switch to 0 V to start the power up sequence.

## 8.5 Program an OTP configuration

This section is intended to burn an OTP configuration permanently into the fuses. You can program device sectors only one time. Make sure sectors are available.

You can program an OTP configuration from Device Programming tab. See <u>Section 7.6</u> "Device programming" OR from the script editor.

1. If not in debug mode, see <u>Section 8.2 "Debug mode entry"</u>.

2. Turn on the SW7 to apply ~8 V to the VDebug pin in order to reach the OTP burning threshold VDBG65TH. If this voltage is turn on, a blue LED will turn on (D19).

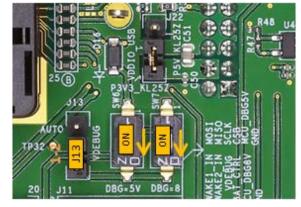




Figure 65. Burning voltage LED indicator (D19)

- 3. Open the NXP GUI, connect the device, and go to the script editor.
- 4. Load a provided or created OTP configuration script to load on the mirror registers. Then click on Run button to run the script.



### KITFS26SKTEVM evaluation board

5. Once the script has been sent, turn off SW7 then SW6.



6. Device should power up with the burned OTP configuration or perform a POR on VBAT to verify the fused OTP configuration.

### 8.6 Go to INIT FS in debug mode

From Power up:

- 1. Put Debug pin to 5 V (SW6 On) to access debug entry.
- 2. Device Power up (SW1)
- 3. If the device does not have an OTP configuration Emulate or program an OTP configuration. See <u>Section 8.4 "Emulate an OTP configuration"</u> for Emulation or <u>Section 8.5 "Program an OTP configuration"</u> for programming.
- 4. Put off SW6 to continue the state machine and access INIT FS. You can verify current state from USB and device status bar; click on display to refresh.

#### FS\_STATES : 9-INIT\_FS

### 8.7 Go to Normal mode

To enter Normal mode from GUI, you must be in debug mode and in INIT FS state. If simple Watchdog, you can use a script to release safety outputs FS0B and FS1B. If Watchdog challenger, sequence must be sent manually.

- 1. Once in INIT FS, verify ABIST1 is pass from Safety diagnostics tab
- 2. Configure or verify Watchdog type from Mirrors tab.
- 3. Use a script to release safety outputs; use script A for watchdog simple or script B for watchdog challenger. Script to release safety outputs is available in device manager

scripts section, orr from script editor > Generator > Safety outputs release script and run.

a. Sequence to enter normal mode with a Watchdog simple:

//INIT FS and simple WD enabled required //Open WD window SET REG:FS26:Safety:FS WDW DURATION:0x008B SET REG:FS26:Safety:FS NOT WDW DURATION:0xF144 //Send 1 good wd refresh to close INIT window SET\_REG:FS26:Safety:FS\_WD\_ANSWER:0x5AB2 //clean fault error counter SET REG:FS26:Safety:FS WD ANSWER:0x5AB2 SET\_REG:FS26:Safety:FS\_WD\_ANSWER:0x5AB2 //Exit dbg mode SET REG:FS26:Safety:FS STATES:0x4000 //release FS0B and FS1B SET REG:FS26:Safety:FS RELEASE FS0B FS1B:0xB2A5 b. Sequence to enter normal mode with a Watchdog Challenger: //INIT FS and WD Challenger required //Open WD window SET\_REG:FS26:Safety:FS\_WDW\_DURATION:0x008B SET REG:FS26:Safety:FS NOT WDW DURATION:0xF144 //Send 1 ZD refresh to close INIT window SET REG:FS26:Safety:FS WD ANSWER:0xa54d //clean fault error counter SET REG:FS26:Safety:FS WD ANSWER:0x4a9a SET REG:FS26:Safety:FS WD ANSWER:0x9535 SET REG:FS26:Safety:FS WD ANSWER:0x2a6a SET\_REG:FS26:Safety:FS\_WD\_ANSWER:0x54d4 SET REG:FS26:Safety:FS WD ANSWER:0xa9a9 SET REG:FS26:Safety:FS WD ANSWER:0x5353 //Exit dbg mode SET REG:FS26:Safety:FS STATES:0x4000

//release FS0B and FS1B SET\_REG:FS26:Safety:FS\_RELEASE\_FS0B\_FS1B:0xA565

#### Release safety outputs without script

To release safety outputs step by step, continue with these instructions:

 Configure WD window. Since it is not possible to send a WD refresh periodically, open WD Window. From FS config tab, go to WD window box, select INFINITE window and click on write button.

| WD Window          |                                |     |  |
|--------------------|--------------------------------|-----|--|
| WDW_RECOVERY       | 64 ms 🔹 64 ms                  |     |  |
| WDM_DC(Duty Cycle) | Closed Window :                | 50% |  |
| WDM_PERIOD         | Disable (INFINITE OPEN WINDOW) | OPE |  |
|                    | 1 ms                           |     |  |
|                    | 2 ms                           |     |  |
|                    | 3 ms                           |     |  |
|                    | 4 ms                           |     |  |
|                    | 6 ms                           |     |  |

Or from device manager select Open WD Window script and click on execute.

2. Send one good WD refresh to move on the state machine. From FS Config tab, click on WD challenger or WD simple one time.

Or execute it from script editor or device manager.

- Send the number selected good WD refresh to clean the Fault error counter. Example: Default number is 6. Click 6 times on WD Challenger or WD simple buttons. You can verify the Fault error count is now 0 (FLT\_ERR\_CNT) in FS config tab.
- 4. Exit debug mode. Write 1 to exit debug mode bit in FS\_STATES. Go to register map, then to safety tab.

| F5_STATES (0x17)         Read         0x0000         Write         0x4000 |           |               |          |              |              |              |              |              |
|---|-----------|---------------|----------|--------------|--------------|--------------|--------------|--------------|
|   | TM_ACTIVE | EXIT_DBG_MODE | DBG_MODE | OTP_CORRUPT  | REG_CORRUPT  | RESERVED     | RESERVED     | RESERVED     |
|   | RESERVED  | RESERVED      | RESERVED | FS_STATES[4] | FS_STATES[3] | FS_STATES[2] | FS_STATES[1] | FS_STATES[0] |

5. Send "FS0b release" or "FS0b and FS1b release" command to move to normal mode. You can find these buttons in FS config tab.



6. After these steps, device should move to Normal mode. To verify current state, click on FS states display from USB and Device status bar.

FS\_STATES : 11-Normal

#### 8.8 Low power modes

Once in INIT FS or Normal mode, select a way to exit the low power modes. Write 1 to the event or events that can wake the product from the low power modes.

KITFS26SKTEVM evaluation board

| M_WID_CFG (0x10) Read 0x0000 Wite 0x0000 C |          |          |          |          |          |          |          |
|--|----------|----------|----------|----------|----------|----------|----------|
| RESERVED                                   | RESERVED | RESERVED | RESERVED | IO2WUPOL | IO1WUPOL | WAKE2POL | WAKE1POL |
| RESERVED                                   | RESERVED | CSBWUEN  | LDTWUEN  | IO2WUEN  | IO1WUEN  | WK2WUEN  | WK1WUEN  |

#### 8.8.1 Go to Standby

Execute Go to Standby script from Device Manager.

| Go to Standby | • | execute |  |
|---------------|---|---------|--|
|---------------|---|---------|--|

Or from Script editor > Generator, select Go to Standby script and run it.

Device should go to standby mode. Only VPRE stays turn ON and LDOs as configured.

| Device FS26                | Script Commands Window   |
|----------------------------|--|
| Alias FS26 r               | //STANDBY MODE, send in less than 10ms<br>SET_REG:FS26:Safety:FS_LP_REQ:0x00AA<br>SET_REG:FS26:Safety:FS_LP_REQ:0x0055 |
| Digital Pins               |  |
| Analog Pins                |  |
| Registers                  |  |
| ▷ Mode                     | 1  |
| / Generator                |  |
| Generator: Go to Standby 🔹 |  |

#### 8.8.2 Go to LPOFF

| Go to LPOFF | - | execute |
|-------------|---|---------|
|-------------|---|---------|

Once in INIT FS or Normal mode, execute Go to LPOFF script from Device Manager. Or from Script editor > Generator, select Go to LPOFF script and run it.

Device should go to LPOFF mode. Only VPRE stays ON.

|         |                   | Script Commands Window  |
|---------|-------------------|---|
| Device  | FS26              | Script Commands Window  |
| Alias   | F526              | //Go to LPOFF<br>SET_REG:FS26:Safety:FS_LP_REQ:0x00A5<br>SET_REG:FS26:Safety:FS_LP_REQ:0x005A |
| Digital | l Pins            |   |
|         |                   |   |
| Analog  | g Pins            |   |
|         |                   |   |
| Regist  | ters              |   |
|         |                   |   |
| Mode    |                   |   |
|         |                   |   |
| Gener   | rator             |   |
| Generat | or: Go to LPOFF 🔹 |   |

## 9 References

#### [1] **FS26 datasheet** — Safety System Basis Chip with Low Power for ASIL D FS26 Datasheet-Product Preview-REV 1.3 — Dec 2020.pdf

| Revision history |          |                 |  |
|------------------|----------|-----------------|--|
| Rev              | Date     | Description     |  |
| v.1.0            | 20210218 | Initial version |  |

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