Electra House, 32 Southtown Road
Great Yarmouth, Norfolk
NR31 0DU, England

Telephone +44 (0)1493 602602
Email:sales@midasdisplays.com
www.midasdisplays.com

MCCOG128064D6W-FPTLW		128 x 64	N/A	LCD Module
Specification				
Version: 1		Date: 30/10/2020		
Revision				
1	30/10/2020	First Issue		

Display Features			
Resolution	128 x 64		
Appearance	Black on White		
Logic Voltage	3V		
Interface	Parallel / SPI		
Font Set	N/A		
Display Mode	Transflective		
LC Type	FSTN		
Module Size	45.00 x 40.00 x 10.40mm		
Operating Temperature	-20°C ~ +70°C		
Construction	COG	Box Quantity	Weight / Display
LED Backlight	White	---	---

*- For full design functionality, please use this specification in conjunction with the ST7565R specification. (Provided Separately)

Display Accessories	
Part Number	**Description**

Optional Variants	
Appearances	**Voltage**

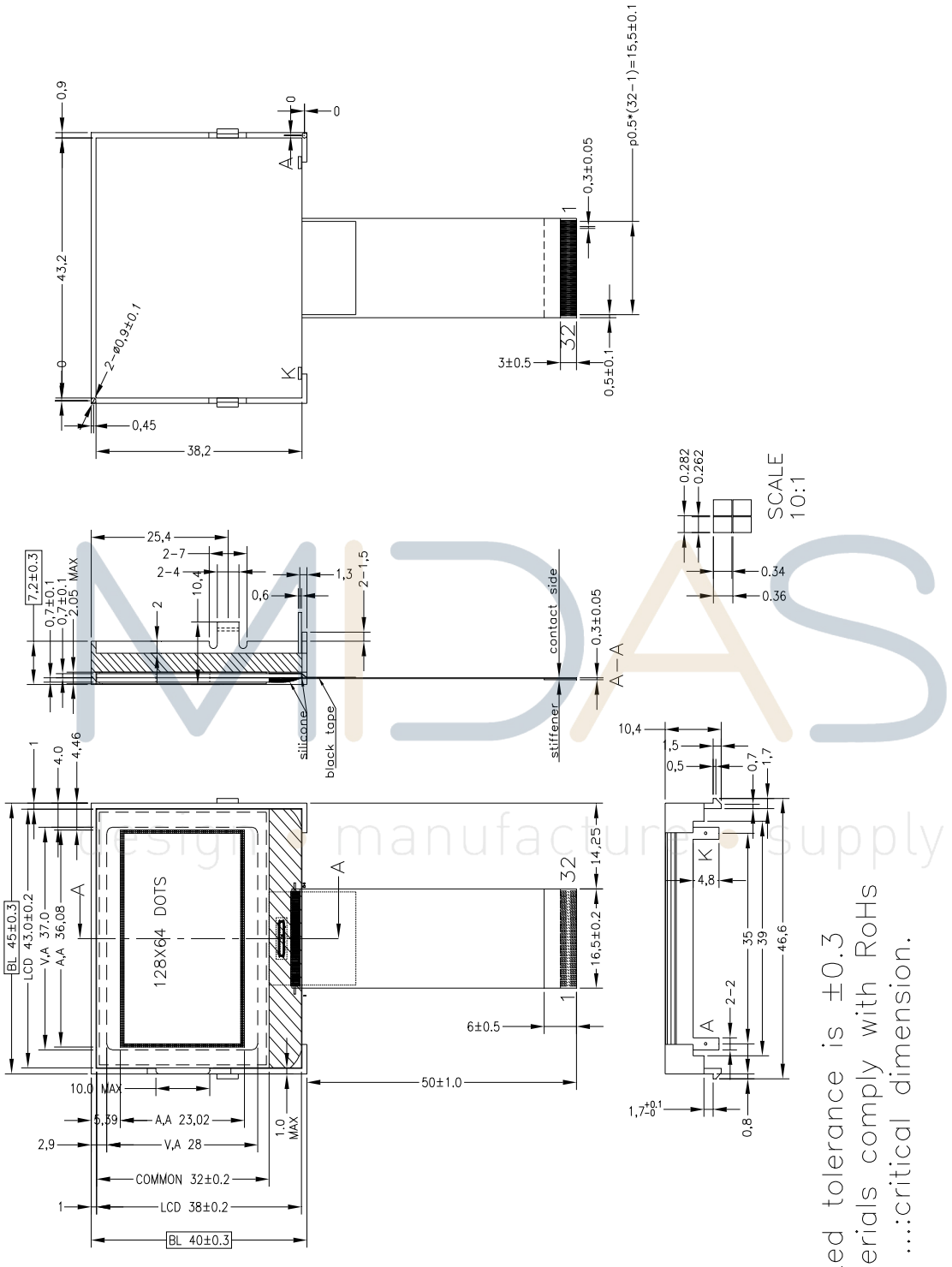
1. FUNCTIONS & FEATURES

- MCCOG128064D6W-FPTLW Series LCD Type :
- Viewing Direction : 6 O'clock
- Driving Scheme : 1/65 Duty Cycle, 1/9 Bias
- Power Supply Voltage(Typ.) : 3.0 V
- LCD Operation Voltage :9.0 V
- Display Contents :128x64 Dots
- Backlight : LED,Lightguide,White
- Operating temperature :-20°C ～ +70°C
- Storage temperature :-30°C ～ +80°C
- RoHS Compliant

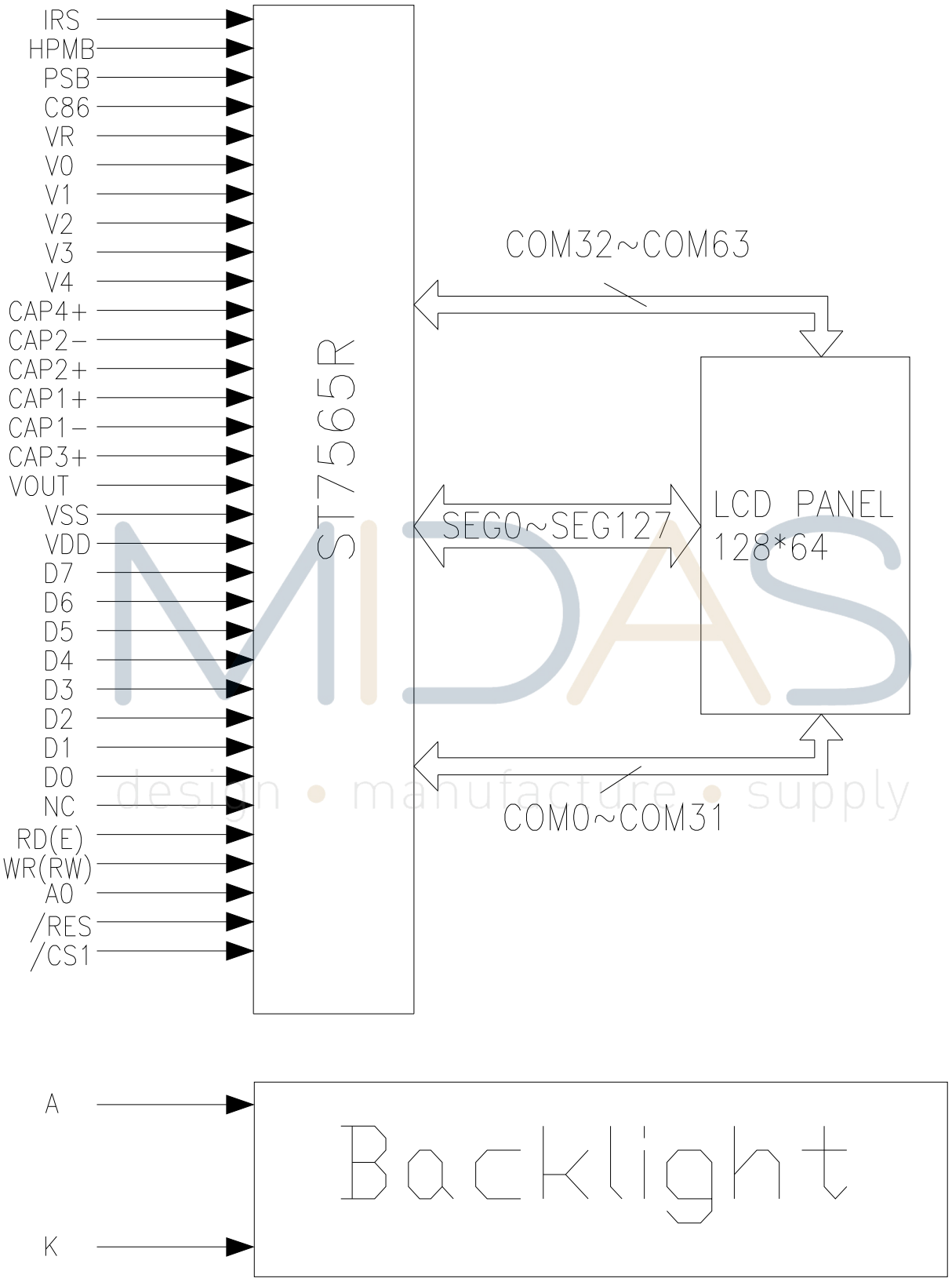
2. MECHANICAL SPECIFICATIONS

- Module Size: : 45.0(L) x 40.00(W) x 10.4(T)mm （without FPC）
- Viewing Area Size: : 37.00(W) x 28.00(H) mm
- Active Area Size : 36.08(W) x 23.02(H)mm
- Dot pitch: : 0.282(W) x 0.36(H)mm
- Dot Size: : 0.262(W) x 0.34(H) mm

EXTERNAL DIMENSIONS



BLOCK DIAGRAM



PIN DESCRIPTION

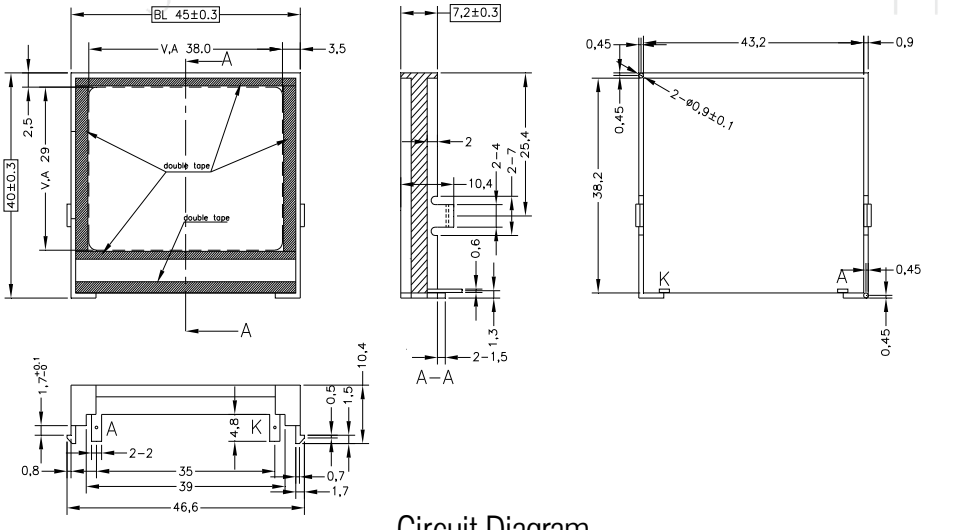
Pin No.	Name	Description
1	IRS	This terminal selects the resistors for the V0 voltage level adjustment. IRS = “H”: Use the internal resistors IRS = “L”: Do not use the internal resistors. The V0 voltage level is regulated by an external resistive voltage divider attached to the VR terminal
2	HPMB	This is the power control terminal for the power supply circuit for liquid crystal drive. /HPM = “H”: Normal mode /HPM = “L”: High power mode (suggested)
3	PSB	This pin configures the interface to be parallel mode or serial mode. P/S = “H”: Parallel data input/output. P/S = “L”: Serial data input.
4	C86	This is the MPU interface selection pin. C86 = “H”: 6800 Series MPU interface. C86 = “L”: 8080 Series MPU interface.
5	VR	This is the internal-output VREG power supply for the LCD power supply voltage regulator.
6	V0	LCD driver supplies voltages
7	V1	
8	V2	
9	V3	
10	V4	
11	CAP4+	DC/DC voltage converter.
12	CAP2-	
13	CAP2+	
14	CAP1+	
15	CAP1-	
16	CAP3+	
17	VOUT	
18	VSS	Ground
19	VDD	Voltage supply
20	D7	This is an 8-bit bi-directional data bus that connects to an 8-bit or 16-bit standard MPU data bus. When the serial interface (SPI-4) is selected (P/S = “L”) : D7 : serial data input (SI) ; D6 : the serial clock input (SCL). D0 to D5 should be connected to VDD or floating. When the chip select is not active, D0 to D7 are set to high impedance.
21	D6	
22	D5	
23	D4	
24	D3	
25	D2	
26	D1	
27	D0	
28	RD(E)	• When connected to 8080 series MPU, this pin is treated as the “/RD” signal of the 8080 MPU and is LOW-active. The data bus is in an output status when this signal is “L”. • When connected to 6800 series MPU, this pin is treated as the “E” signal of the 6800 MPU and is HIGH-active. This is the enable clock input terminal of the 6800 Series MPU.
29	WR(RW)	• When connected to 8080 series MPU, this pin is treated as the “/WR” signal of the 8080 MPU and is LOW-active. The signals on the data bus are latched at the rising edge of the /WR signal. • When connected to 6800 series MPU, this pin is treated as the “R/W” signal of the 6800 MPU and decides the access type : When R/W = “H”: Read. When R/W = “L”: Write.

30	A0	This is connect to the least significant bit of the normal MPU address bus, and it determines whether the data bits are data or command. A0 = “H”: Indicates that D0 to D7 are display data. A0 = “L”: Indicates that D0 to D7 are control data.
31	/RES	The RESET signal
32	/CS1	This is the Chip Select signal.

A	Supply voltage for backlight LED+
K	Supply voltage for backlight LED-

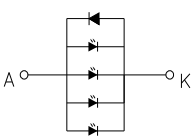
BACKLIGHT CHARACTERISTICS

Item	Symbol	min.	typ.	max.	Unit	Condition
Forward Voltagt	Vf	2.9	3.1	3.3	V	If= 60 mA T=25° C
Power Dissipation	Pd	174	186	198	mW	
Luminous Uniformity	ΔLv	70			%	
Luminance	Lv	420	500		cd/m ^{2}	
Color Coordinate	X	0.260		0.30		
	Y	0.270		0.31		
Lifetime	50000h				Hours	



Circuit Diagram

COLOR:WHITE



Remarks:
1.Unmarked tolerance is ±0.3
2.All materials comply with RoHs
3. ☐ ...:critical dimension.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Unit
Power Supply Voltage	VDD	-0.3 ~ 3.6	V
Power supply voltage (VDD standard)	V0,VOUT	-0.3 ~ 13.5	V
Power supply voltage (VDD standard)	V1, V2, V3, V4	-0.3 to V0	V
Operating temperature	TOPR	–20 to +70	°C
Storage temperature	TSTR	–30 to +80	°C

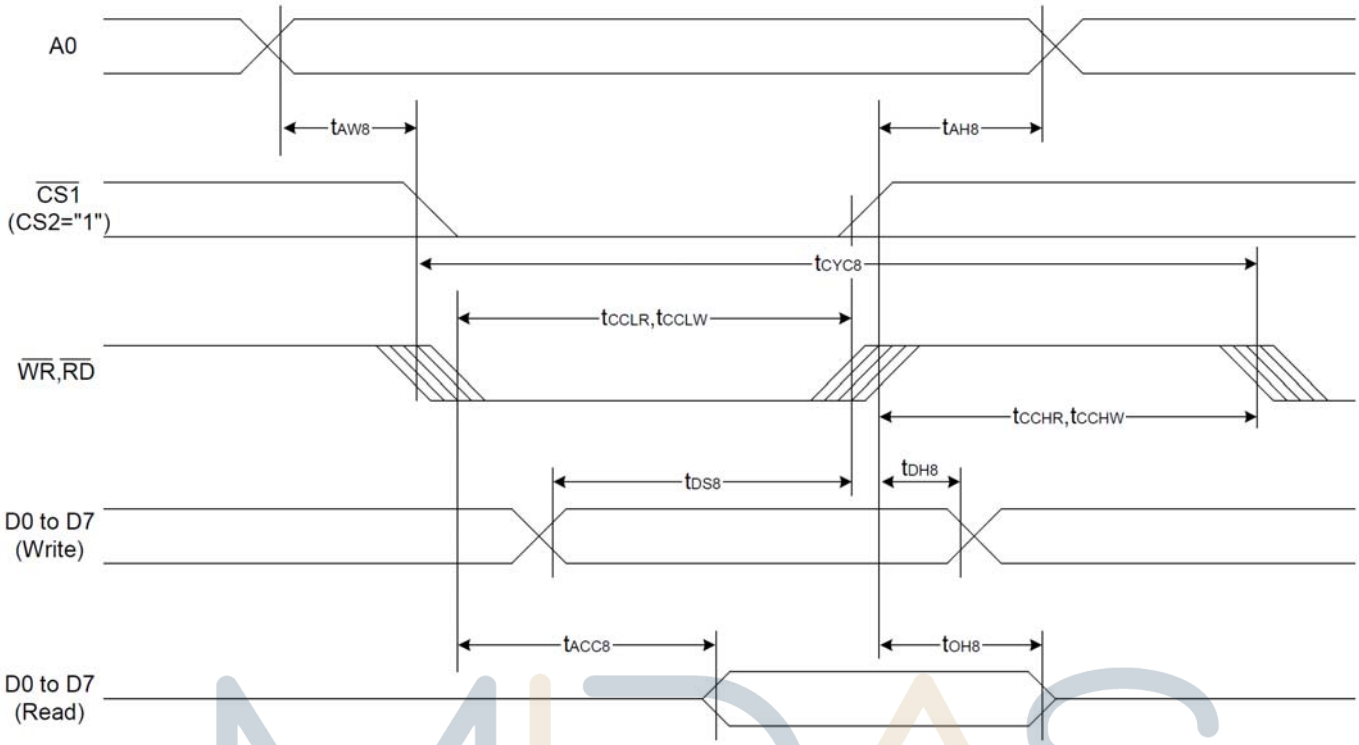
ELECTRICAL CHARACTERISTICS

1. DC CHARACTERISTICS

Item	Symbol	Condition	STANDARD VALUE			units
			Min.	Typ.	Max.	
Operating Voltage	V_{DD}	Relative to VSS	2.7	3.0	3.3	V
LCD driving voltage	V_{LCD}	Relative to VSS	8.7	9.0	9.3	
High-level Input Voltage	V_{IHC}	---	0.8 x VDD	---	VDD	
Low-level Input Voltage	V_{ILC}	---	VSS	---	0.2 x VDD	
High-level Output Voltage	V_{OHC}	IOH = –0.5 mA	0.8 x VDD	---	VDD	
Low-level Output Voltage	V_{OLC}	IOH = –0.5 mA	VSS	---	0.2 x VDD	
Consumption current	I_{DD}	---	---	TBD	---	mA

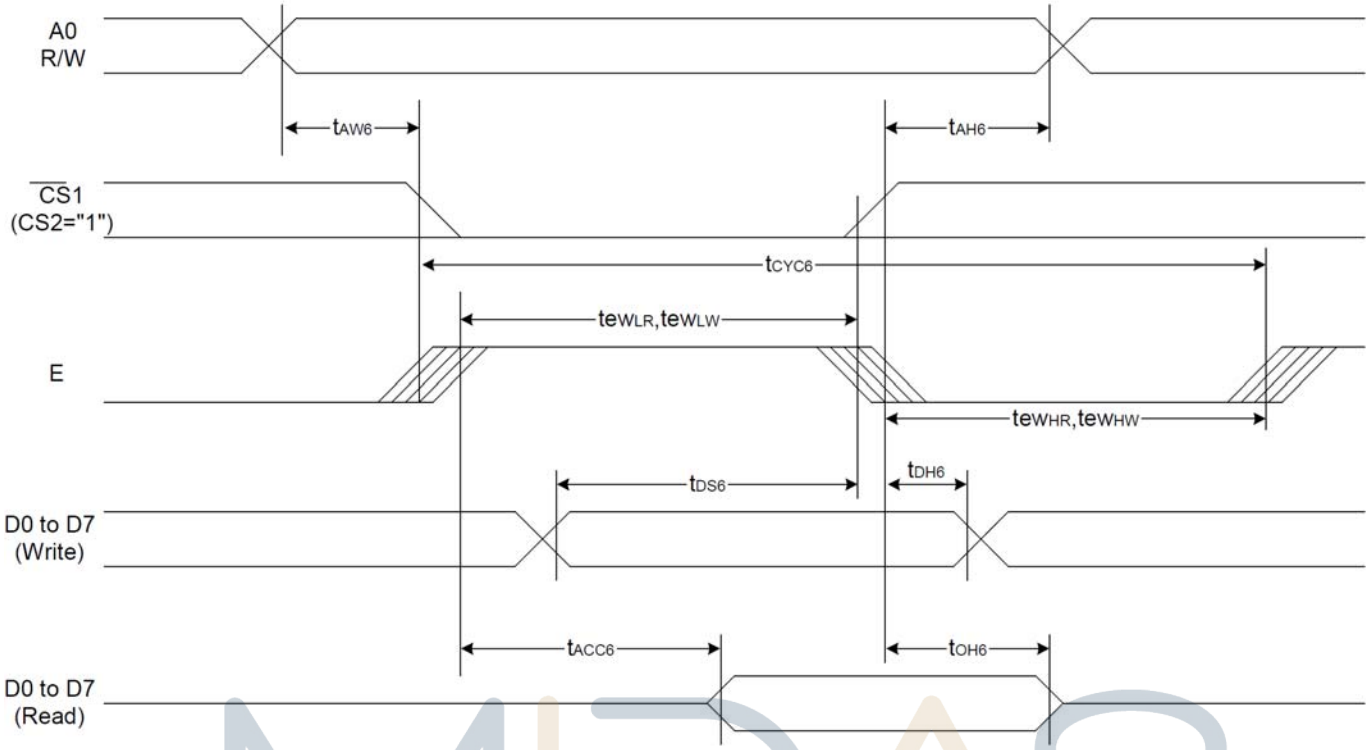
2. AC CHARACTERISTICS

System Bus Read/Write Characteristics 1 (For the 8080 Series MPU)



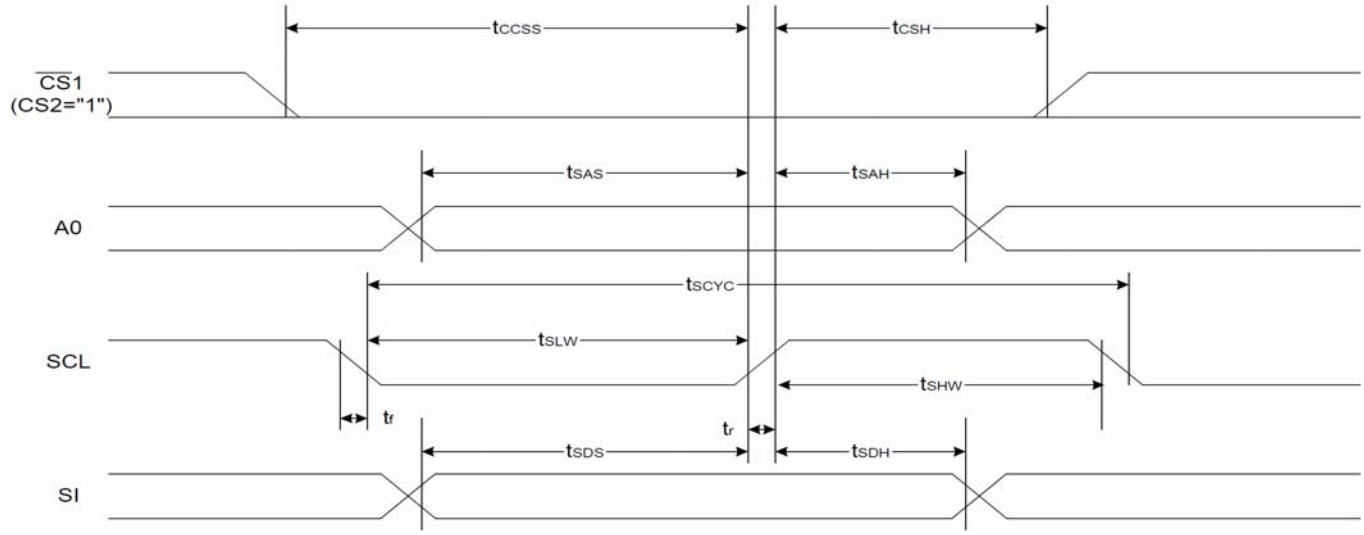
Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	t_{AH8}		0	—	Ns
Address setup time		t_{AW8}		0	—	
System cycle time		t_{CYC8}		240	—	
Enable L pulse width (WRITE)	WR	t_{CCLW}		80	—	
Enable H pulse width (WRITE)		t_{CCHW}		80	—	
Enable L pulse width (READ)	RD	t_{CCLR}		140	—	
Enable H pulse width (READ)		t_{CCHR}		80		
WRITE Data setup time	D0 to D7	t_{DS8}		40	—	
WRITE Address hold time		t_{DH8}		0	—	
READ access time		t_{ACC8}	C_L = 100 pF	—	70	
READ Output disable time		t_{OH8}	C_L = 100 pF	5	50	

System Bus Read/Write Characteristics 2 (For the 6800 Series MPU)



Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	t_{AH6}		0	—	ns
Address setup time		t_{AW6}		0	—	
System cycle time		t_{CYC6}		240	—	
Enable L pulse width (WRITE)	WR	t_{EWLW}		80	—	
Enable H pulse width (WRITE)		t_{EWHW}		80	—	
Enable L pulse width (READ)	RD	t_{EWLR}		80	—	
Enable H pulse width (READ)		t_{EWHR}		140		
WRITE Data setup time	D0 to D7	t_{DS6}		40	—	
WRITE Address hold time		t_{DH6}		0	—	
READ access time		t_{ACC6}	C_L = 100 pF	—	70	
READ Output disable time		t_{OH6}	C_L = 100 pF	5	50	

The 4-line SPI Interface

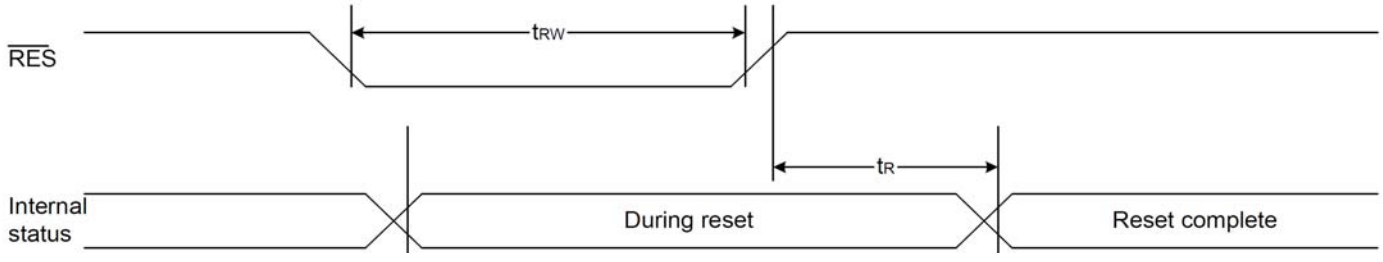


Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
4-line SPI Clock Period	SCL	Tscyc		50	—	ns
SCL "H" pulse width		Tshw		25	—	
SCL "L" pulse width		TSLW		25	—	
Address setup time	A0	TSAS		20	—	
Address hold time		Tsah		10	—	
Data setup time	SI	Tsds		20	—	
Data hold time		TSDH		10	—	
CS-SCL time	CS	Tcss		20	—	
CS-SCL time		Tcsh		40	—	

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
4-line SPI Clock Period	SCL	TSCYC		200	—	ns
SCL "H" pulse width		TSHW		80	—	
SCL "L" pulse width		TSLW		80	—	
Address setup time	A0	TSAS		60	—	
Address hold time		TSAH		30	—	
Data setup time	SI	TSDS		60	—	
Data hold time		TSDH		30	—	
CS-SCL time	CS	TCSS		40	—	
CS-SCL time		TCSH		100	—	

*1 The input signal rise and fall time (tr, tf) are specified at 15 ns or less.
*2 All timing is specified using 20% and 80% of VDD as the standard.

Reset Timing

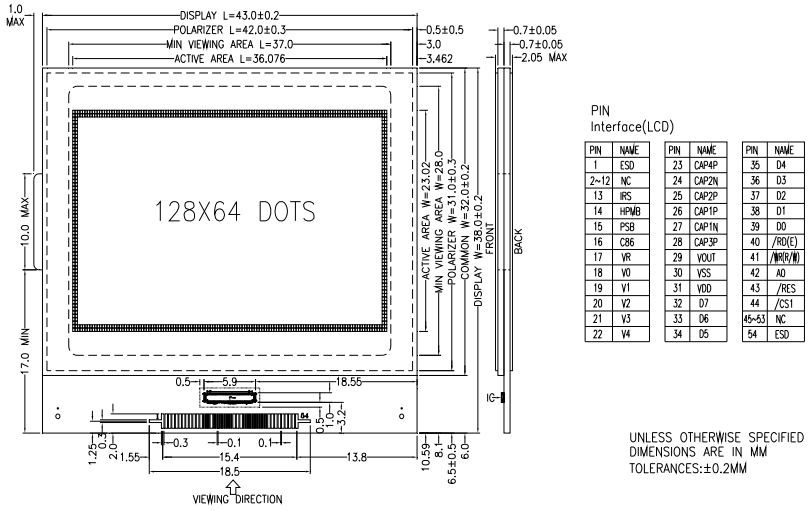


COMMAND TABLE

(COMMAND FOR ST7565R)

Command	Command Code											Function
	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	
(1) Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0 1	LCD display ON/OFF 0: OFF, 1: ON
(2) Display start line set	0	1	0	0	1	Display start address						Sets the display RAM display start line address
(3) Page address set	0	1	0	1	0	1	1	Page address				Sets the display RAM page address
(4) Column address set upper bit Column address set lower bit	0	1	0	0	0	0	1	Most significant column address				Sets the most significant 4 bits of the display RAM column address. Sets the least significant 4 bits of the display RAM column address.
				0	0	0	0	Least significant column address				
(5) Status read	0	0	1	Status				0	0	0	0	Reads the status data
(6) Display data write	1	1	0	Write data								Writes to the display RAM
(7) Display data read	1	0	1	Read data								Reads from the display RAM
(8) ADC select	0	1	0	1	0	1	0	0	0	0	0 1	Sets the display RAM address SEG output correspondence 0: normal, 1: reverse
(9) Display normal/ reverse	0	1	0	1	0	1	0	0	1	1	0 1	Sets the LCD display normal/ reverse 0: normal, 1: reverse
(10) Display all points ON/OFF	0	1	0	1	0	1	0	0	1	0	0 1	Display all points 0: normal display 1: all points ON
(11) LCD bias set	0	1	0	1	0	1	0	0	0	1	0 1	Sets the LCD drive voltage bias ratio 0: 1/9 bias, 1: 1/7 bias (ST7565R)
(12) Read-modify-write	0	1	0	1	1	1	0	0	0	0	0	Column address increment At write: +1 At read: 0
(13) End	0	1	0	1	1	1	0	1	1	1	0	Clear read/modify/write
(14) Reset	0	1	0	1	1	1	0	0	0	1	0	Internal reset
(15) Common output mode select	0	1	0	1	1	0	0	0 1	*	*	*	Select COM output scan direction 0: normal direction 1: reverse direction
(16) Power control set	0	1	0	0	0	1	0	1	Operating mode			Select internal power supply operating mode
(17) V_0 voltage regulator internal resistor ratio set	0	1	0	0	0	1	0	0	Resistor ratio			Select internal resistor ratio(Rb/Ra) mode
(18) Electronic volume mode set Electronic volume register set	0	1	0	1	0	0	0	0	0	0	1	Set the V_0 output voltage electronic volume register
				0	0	Electronic volume value						
(19) Static indicator ON/OFF Static indicator register set	0	1	0	1	0	1	0	1	1	0	0 1	0: OFF, 1: ON Set the flashing mode
				0	0	0	0	0	0	0	Mode	
(20) Booster ratio set	0	1	0	1	1	1	1	1	0	0	0	select booster ratio 00: 2x,3x,4x 01: 5x 11: 6x
				0	0	0	0	0	0	step-up value		
(21) Power save	0	1	0									Display OFF and display all points ON compound command
(22) NOP	0	1	0	1	1	1	0	0	0	1	1	Command for non-operation
(23) Test	0	1	0	1	1	1	1	*	*	*	*	Command for IC test. Do not use this command

LCD ARTWORK



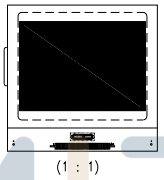
PIN
Interface(LCD)

PIN	NAME
1	ESD
2~12	NC
13	IRS
14	HPMB
15	PSB
16	C86
17	VR
18	V0
19	V1
20	V2
21	V3
22	V4

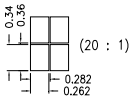
PIN	NAME
23	CAP4P
24	CAP2N
25	CAP2P
26	CAP1P
27	CAP1N
28	CAP3P
29	VOUT
30	VSS
31	VDD
32	D7
33	D6
34	D5

PIN	NAME
35	D4
36	D3
37	D2
38	D1
39	D0
40	/RD(E)
41	/WR(R/W)
42	A0
43	/RES
44	/CS1
45~53	NC
54	ESD

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN MM
TOLERANCES:±0.2MM

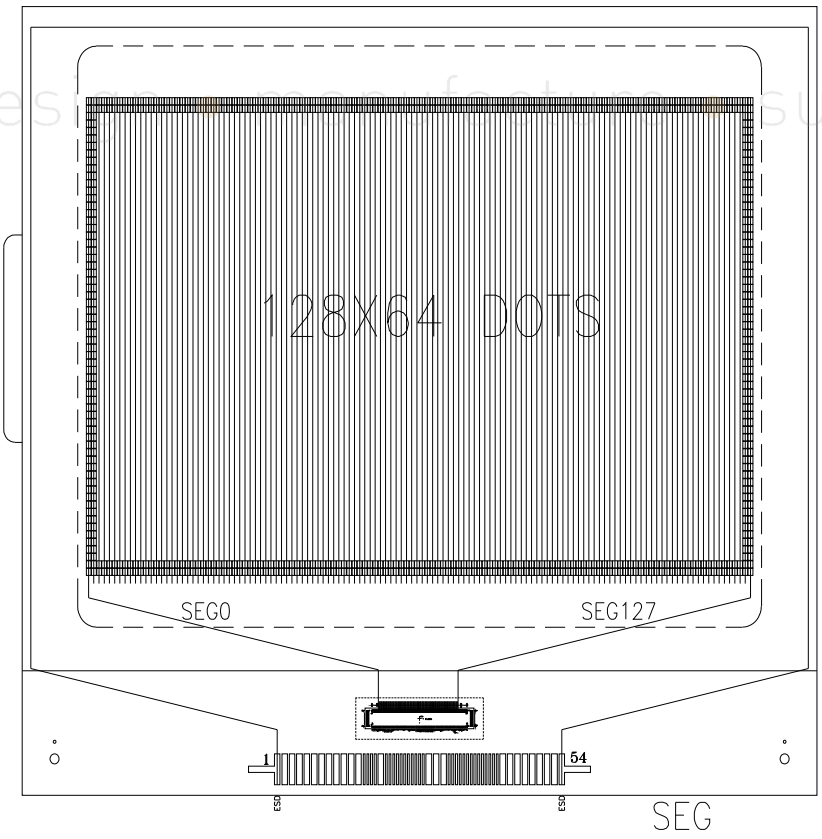


(1 : 1)

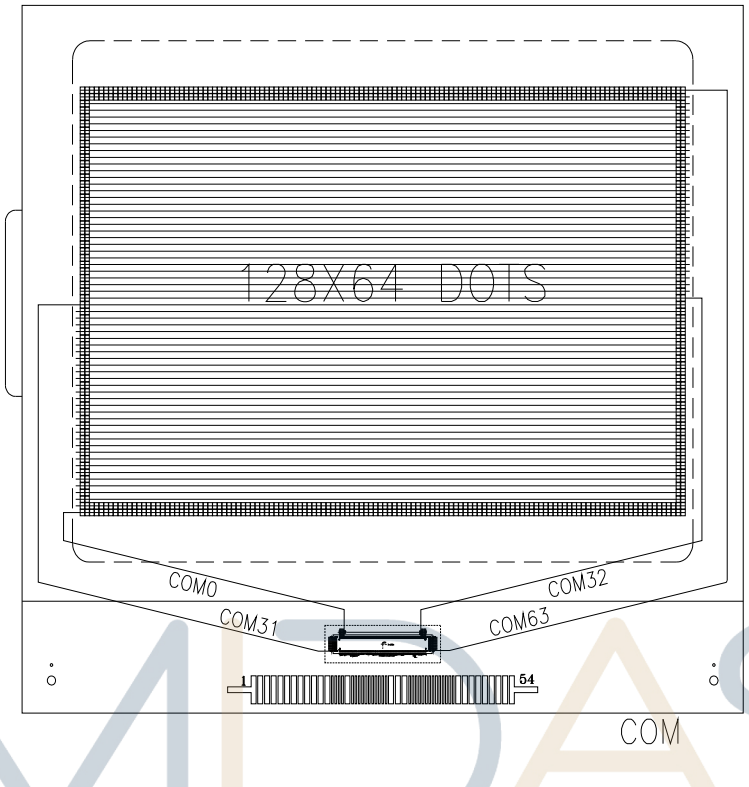


UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN MM
TOLERANCES:±0.1MM

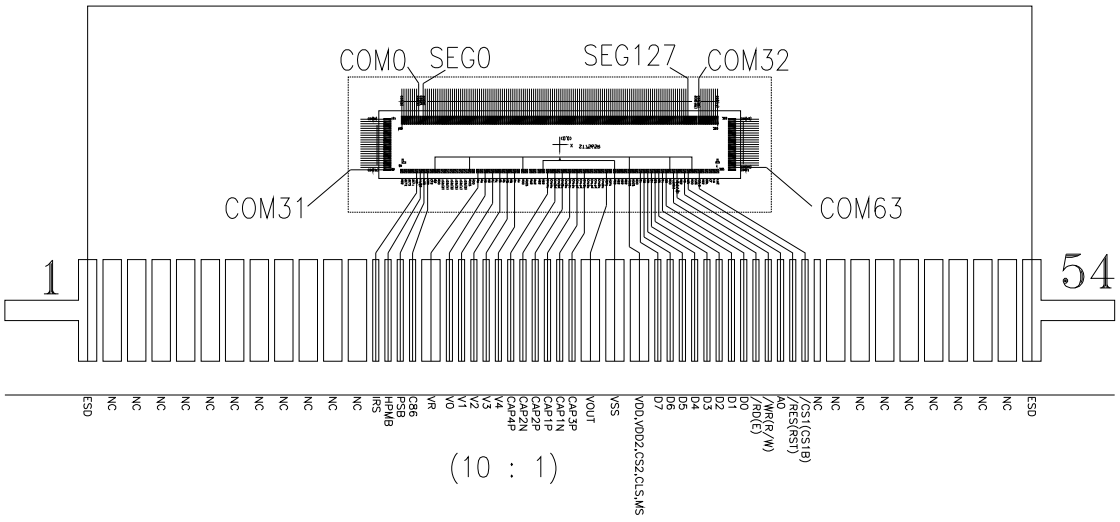
SEG LAYOUT



COM LAYOUT



IC LAYOUT



RELIABILITY TEST

Operating life time: Longer than 50000 hours

(at room temperature without direct irradiation of sunlight)

Reliability characteristics shall meet following requirements.

TEMPERATURE TESTS	NORMAL GRADE
High temperature storage	+80℃ * 96HR
Low temperature storage	-30℃ * 96HR
High temperature operation	+70℃ * 96HR
Low temperature operation	-20℃ * 96HR
High temperature, High humidity	+60℃ 90%RH 96HR
Thermal shock	-20℃ * 30 min 10s 5Cycles 70℃ * 30 min
Vibration test	Frequency * Swing * Time 40Hz * 4mm * 4hrs
Drop test	Drop height * Times 1.0m * 6 times

QUALITY DESCRIPTION & APPLICATION NOTE

Please refer to "General Inspection Criteria" document