NXS0506

SD 3.0-compatible memory card integrated auto-direction control and level translator with EMI filter and ESD protection

Rev. 1 — 31 January 2022 Product data sheet

1. General description

The NXS0506 is an SD 3.0-compatible bidirectional dual supply level translator with auto-direction control. It is designed to interface between a memory card operating at 1.7 V to 3.6 V signal levels and a host with a nominal supply voltage of 1.1 V to 1.95 V. The device supports SD 3.0: SDR104, SDR50, DDR50, SDR25, SDR12 and SD 2.0 High-Speed (50 MHz) and Default-Speed (25 MHz) modes. The device has a built-in EMI filter and robust ESD protection (IEC 61000-4-2, level 4).

2. Features and benefits

- Supports up to 208 MHz clock rate
- SD 3.0 specification-compatible voltage translation to support: SDR104, SDR50, DDR50, SDR25, SDR12, High-Speed and Default-Speed modes
- 1.1 V to 1.95 V host side interface voltage support
- Auto-direction sensing
- Low power consumption
- Integrated pull-up resistors: no external resistors required
- Integrated EMI filters suppress higher harmonics of digital I/Os
- Level shifting buffers keep ESD stress away from the host (zero-clamping concept)
- 16-bumps WLCSP package; pitch 0.35 mm
- ESD protection:
  - HBM ANSI/ESDA/JEDEC JS-001 Class 2 exceeds 2 kV
  - CDM ANSI/ESDA/JEDEC JS-002 Class C3 exceeds 1 kV
  - IEC61000-4-2, level 4, contact discharge on all memory card-side pins exceeds 8 kV
  - IEC61000-4-2, level 4, air discharge on all memory card-side pins exceeds 15 kV
- Specified from -40 °C to +85 °C

3. Applications

- Smartphone
- Mobile handsets
- Digital cameras
- Tablet PCs
- Laptop computers
- SD, MMC or microSD card readers

nexperia

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
NXS0506UP	-40 °C to +85 °C	WLCSP16	wafer level chip-scale package; 16 bumps; 1.455 mm x 1.455 mm x 0.43 mm body	SOT8025-1

5. Marking

Table 2. Marking codes

Type number	Marking code
NXS0506UP	m5

6. Block diagram

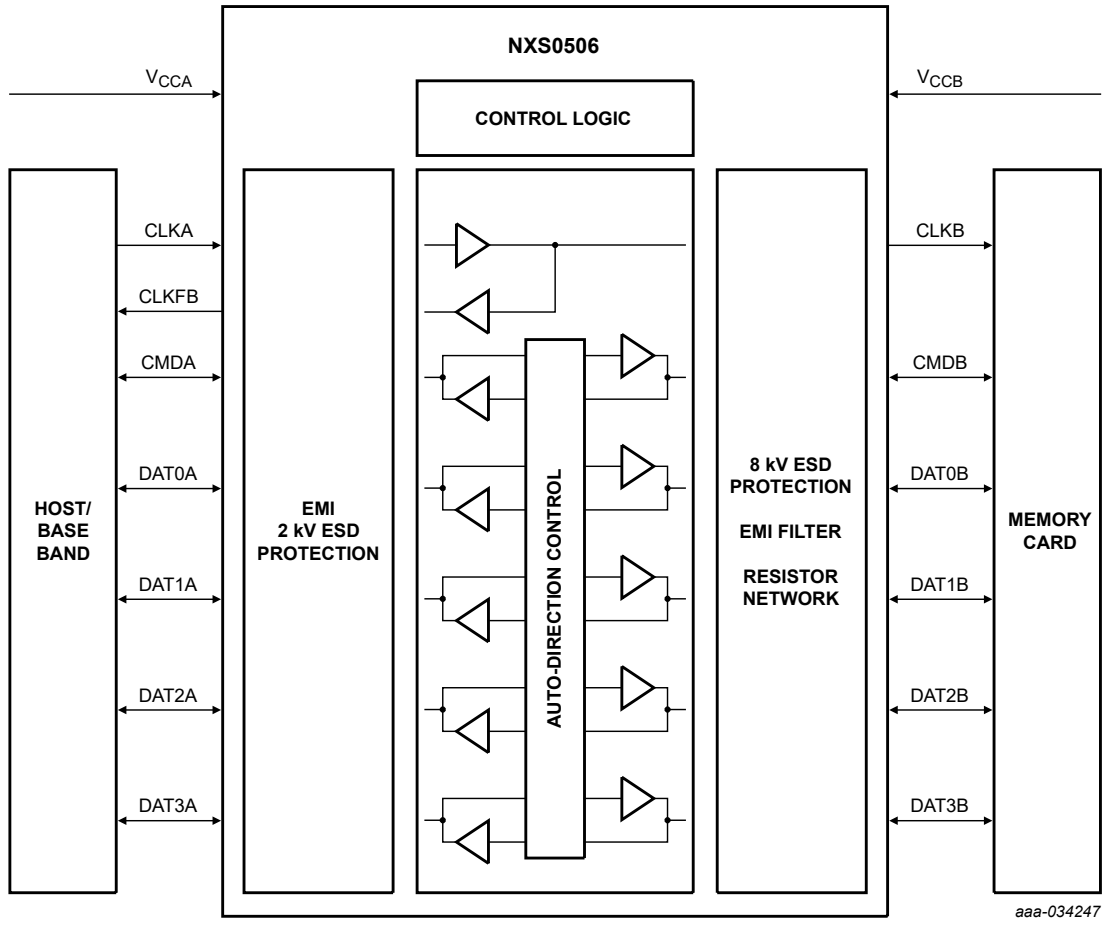


Fig. 1. Block diagram

7. Functional diagram

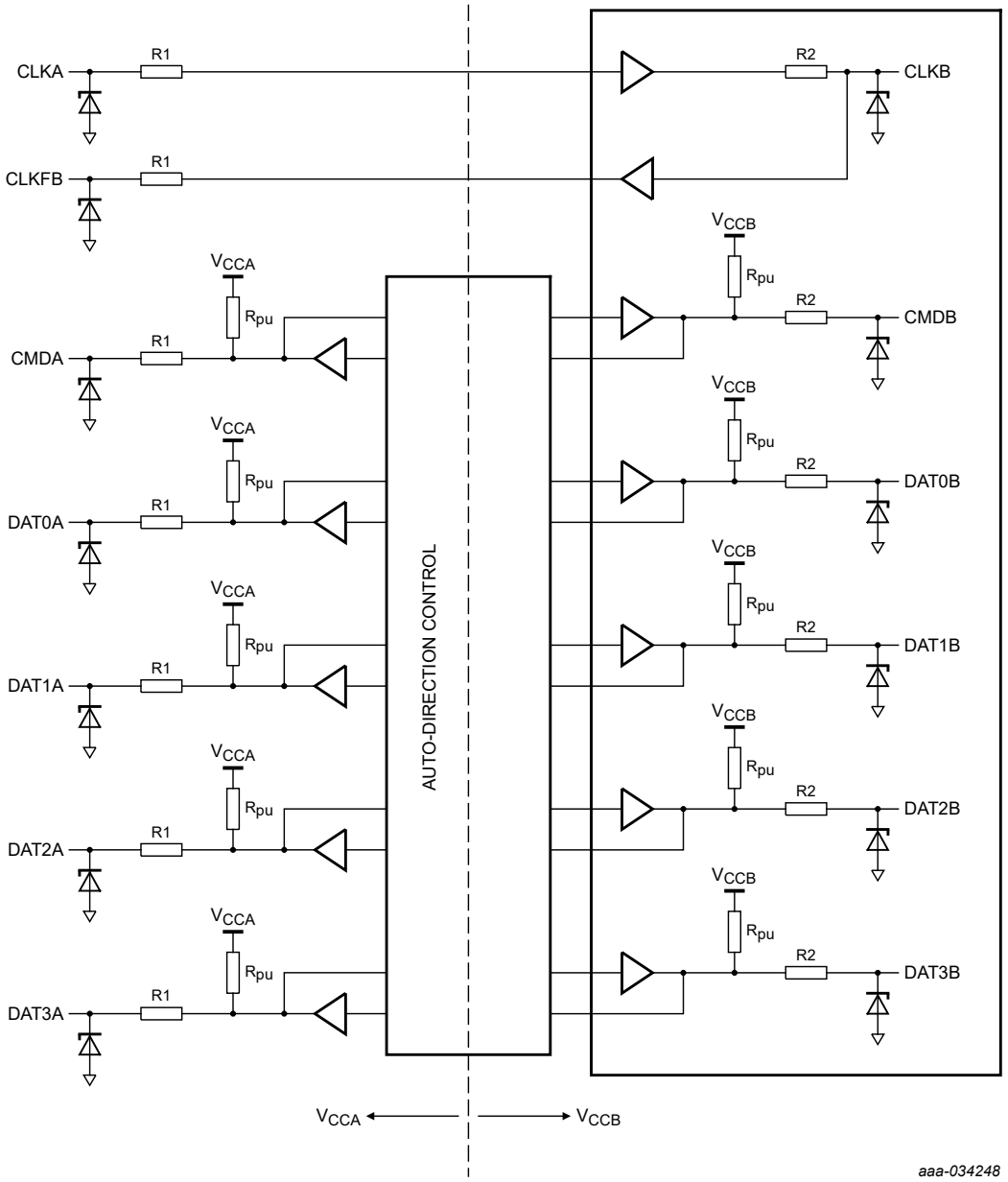
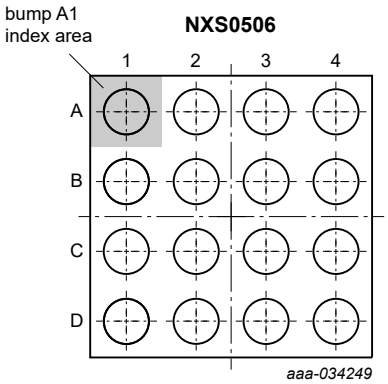


Fig. 2. Functional diagram

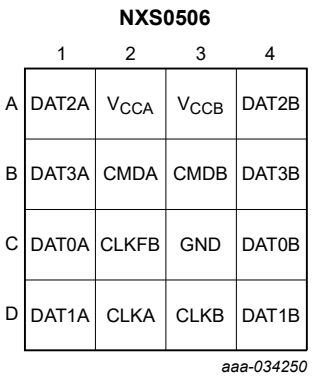
8. Pinning information

8.1. Pinning



Transparent top view

Fig. 3. Bump configuration SOT8025-1 (WLCSP16)



Transparent top view

Bump CLKFB (C2) can be left floating.

Fig. 4. Bump mapping SOT8025-1 (WLCSP16)

8.2. Pin description

Table 3. Pin description

Symbol[1]	Bump	Description
DAT2A	A1	data 2 input or output on host side
DAT3A	B1	data 3 input or output on host side
DAT0A	C1	data 0 input or output on host side
DAT1A	D1	data 1 input or output on host side
V_{CCA}	A2	supply voltage A (host side)
CMDA	B2	command input or output on host side
CLKFB	C2	clock feedback signal on host side, this pin can be left floating
CLKA	D2	clock signal input on host side
V_{CCB}	A3	supply voltage B (memory card side)
CMDB	B3	command input or output on memory card side
GND	C3	supply ground
CLKB	D3	clock signal input on memory card side
DAT2B	A4	data 2 input or output on memory card side
DAT3B	B4	data 3 input or output on memory card side
DAT0B	C4	data 0 input or output on memory card side
DAT1B	D4	data 1 input or output on memory card side

[1] The pin names relate particularly to SD memory cards, but also apply to microSD and MMC memory cards. See Section 9.6 for options to swap identical channels.

9. Functional description

9.1. Level translator

The bidirectional level translator shifts the data between the I/O supply levels of the host and the memory card. Auto direction sensing circuitry determines if a command and data signals are transferred from the memory card to the host (card read mode) or from the host to the memory card (card write mode). The voltage translator has to support several clock and data transfer rates at the signaling levels specified in the SD 3.0 standard specification.

Table 4. Supported modes

Bus speed mode	Signal level (V)	Clock rate (MHz)	Data rate (MB/s)
Default-Speed	3.3	25	12.5
High-Speed	3.3	50	25
SDR12	1.8	25	12.5
SDR25	1.8	50	25
SDR50	1.8	100	50
SDR104	1.8	208	104
DDR50	1.8	50	50

9.2. Enable and direction control

The device contains an auto-enable feature. If V_{CCB} rises above 1.5 V, the level translator logic is enabled automatically. As soon as V_{CCB} drops below 0.65 V, the memory card side drivers and the level translator logic are disabled. All pins on the host side, excluding CLKA are configured as inputs with a 70 kΩ resistor pulled up to V_{CCA}.

The device features an auto correction control for all data channels except CLK. For these pins the direction of data flow is sensed by the direction control logic and the output drivers are controlled accordingly. There is no need for the host interface to indicate the direction of data flow.

9.3. Feedback clock channel

The clock is transmitted from the host to the memory card side. The voltage translator and the Printed-Circuit Board (PCB) tracks introduce some amount of delay. It reduces timing margin for data read back from memory card, especially at higher data rates. Therefore, a feedback path is provided to compensate the delay. The reasoning behind this approach is the fact that the clock is always delivered by the host, while the data in the timing critical read mode comes from the card.

9.4. EMI filter

All input/output driver stages are equipped with EMI filters to reduce interference towards sensitive mobile communication.

9.5. ESD protection

The device has robust ESD protections on all memory card pins. The architecture prevents any stress for the host: the voltage translator discharges any stress to supply ground.

9.6. Pin and channel naming

The channel naming as shown in Fig. 2 and in the Pinning information (Section 8) aims at using NXS0506 for SD-card interfaces. The sequence of the channels is chosen to easily connect to SD-card connectors. As the internal design of channels DAT0 (pins DAT0A and DAT0B), DAT1 (pins DAT1A and DAT1B), DAT2 (pins DAT2A and DAT2B), DAT3 (pins DAT3A and DAT3B) and CMD (pins CMDA and CMDB) is identical, these channels can be exchanged. Swapping channels in the above mentioned group can help ease PCB layout issues. E.g. DAT0 can be swapped with DAT1 or DAT3 with CMD without impact on functionality of NXS0506.

10. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage	4 ms transient; on pin V_{CCA}	-0.5	4.6	V
		4 ms transient; on pin V_{CCB}	-0.5	4.6	V
V_I	input voltage	4 ms transient at I/O pins	-0.5	4.6	V
P_{tot}	total power dissipation	T_{amb} = -40 °C to 85 °C	-	250	mW
T_{stg}	storage temperature		-55	150	°C
$I_{lu(IO)}$	input/output latch-up current	JESD78B: -0.5 x V_{CC} < V_I < 1.5 x V_{CC}; T_j < 125 °C	-100	100	mA

11. Recommended operating conditions

Table 6. Operating conditions

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{CC}	supply voltage	on pin V_{CCA}	[1]	1.1	-	1.95	V
		on pin V_{CCB}	[1]	1.7	-	3.6	V
V_I	input voltage	host side		-0.3	-	V_{CCA} + 0.3	V
		memory card side	[2]	-0.3	-	V_{CCB} + 0.3	V
T_{amb}	ambient temperature			-40	+25	+85	°C

[1] $V_{CCB} \geq V_{CCA}$
[2] The voltage must not exceed 3.6 V.

Table 7. Integrated resistors

Symbol	Parameter	Conditions		T_{amb} = -40 °C to 85 °C			Unit
				Min	Typ[1]	Max	
R_{pu}	pull-up resistance			42	70	100	kΩ
R_s	series resistance	host side; R1	[2]	-	22.5	-	Ω
		card side; R2	[2]	-	15	-	Ω

[1] Typical values are measured at T_{amb} = 25 °C.
[2] Guaranteed by design and characterization

12. Static characteristics

Table 8. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); unless otherwise specified.

Symbol	Parameter	Conditions	T_{amb} = -40 °C to 85 °C			Unit
			Min	Typ[1]	Max	
Automatic enable feature: V_{CCB}						
V_{en}	device enable voltage level	V_{CCA} ≥ 1.0 V; V_{CCB} rising edge	0.9	1.2	1.5	V
V_{dis}	device disable voltage level	V_{CCA} ≥ 1.0 V; V_{CCB} falling edge	0.65	1.0	1.3	V
Host-side input signals: CMDA, DAT0A to DAT3A and CLKA						
V_{IH}	HIGH-level input voltage	1.1 V ≤ V_{CCA} ≤ 1.95 V	0.65V_{CCA}	-	V_{CCA} + 0.3	V
V_{IL}	LOW-level input voltage	1.1 V ≤ V_{CCA} ≤ 1.95 V	-0.3	-	0.35V_{CCA}	V
I_I	input leakage current	CLKA; V_{CCA} = 1.8 V; V_I = 0 V to 1.95 V	-	-	1	µA
Host-side output signals: CMDA and DAT0A to DAT3A						
V_{OH}	HIGH-level output voltage	I_O = -2 µA; V_I = V_{IH} (card side) 1.1 V ≤ V_{CCA} ≤ 1.95 V	0.8V_{CCA}	-	V_{CCA} + 0.3	V
V_{OL}	LOW-level output voltage	I_O = 2 mA; V_I = V_{IL} (card side) 1.1 V ≤ V_{CCA} ≤ 1.95 V	-0.3	-	0.15V_{CCA}	V
Host-side output signals: CLKFB						
V_{OH}	HIGH-level output voltage	I_O = -2 mA; V_I = V_{IH} (host side) 1.1 V ≤ V_{CCA} ≤ 1.95 V	0.8V_{CCA}	-	V_{CCA} + 0.3	V
V_{OL}	LOW-level output voltage	I_O = 2 mA; V_I = V_{IL} (host side) 1.1 V ≤ V_{CCA} ≤ 1.95 V	-0.3	-	0.15V_{CCA}	V
Card-side input signals: CMDB and DAT0B to DAT3B						
V_{IH}	HIGH-level input voltage	1.7 V ≤ V_{CCB} ≤ 3.6 V	0.625V_{CCB}	-	V_{CCB} + 0.3	V
V_{IL}	LOW-level input voltage	1.7 V ≤ V_{CCB} ≤ 1.95 V	-0.3	-	0.35V_{CCB}	V
		2.7 V ≤ V_{CCB} ≤ 3.6 V	-0.3	-	0.30V_{CCB}	V
Card-side output signal: CMDB, DAT0B to DAT3B and CLKB						
V_{OH}	HIGH-level output voltage	CLKB; V_{CCB} = 1.7 V; I_O = -2 mA; V_I = V_{IH} (host side)	0.85V_{CCB}	-	2.0	V
		CLKB; V_{CCB} = 2.7 V; I_O = -4 mA; V_I = V_{IH} (host side)	0.85V_{CCB}	-	V_{CCB} + 0.3	V
		CMDB, DATnB; V_{CCB} = 1.7 V; I_O = -2 µA; V_I = V_{IH} (host side)	0.85V_{CCB}	-	2.0	V
V_{OL}	Low-level output voltage	I_O = 2 mA; V_I = V_{IL} (host side); V_{CCB} = 1.7 V	-0.3	-	0.125V_{CCB}	V
		I_O = 4 mA; V_I = V_{IL} (host side); V_{CCB} = 2.7 V	-0.3	-	0.125V_{CCB}	V

Symbol	Parameter	Conditions	T_{amb} = -40 °C to 85 °C			Unit
			Min	Typ[1]	Max	
Current consumption						
I_{CC}	supply current	host side; all inputs = HIGH $V_I = V_{CCA}$; V_{CCA} = 1.95 V; V_{CCB} = 3.6 V	-	-	4	µA
		card side; all inputs = HIGH $V_I = V_{CCA}$; V_{CCA} = 1.7 V; V_{CCB} = 1.7 V	-	-	7	µA
		card side; all inputs = HIGH $V_I = V_{CCA}$; V_{CCA} = 1.95 V; V_{CCB} = 3.6 V	-	-	20	µA

[1] Typical values are measured at T_{amb} = 25 °C.

13. Dynamic characteristics

13.1. Level translator

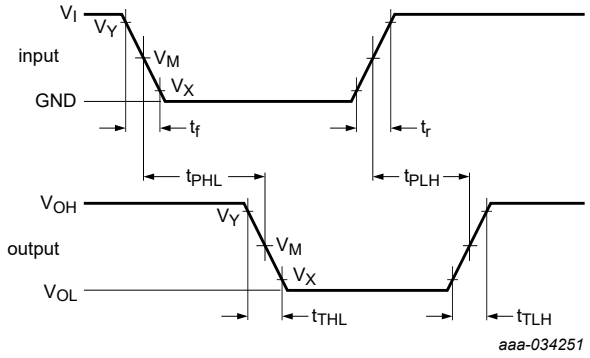
Table 9. Level translator dynamic characteristics

At recommended operating conditions; For waveform and test circuit see Fig. 5 and Fig. 6.

Symbol	Parameter	Conditions	T_{amb} = -40 °C to 85 °C			Unit
			Min	Typ[1]	Max	
Host-side output transition times						
t_t	transition time	V_{CCA} = 1.2 V to V_{CCA} = 1.8 V [2] output transition time between $V_X = 0.35V_{CCA}$ and $V_Y = 0.65V_{CCA}$.	-	0.3	1.0	ns
Host-side input rise and fall times						
t_r, t_f	rise and fall time	V_{CCA} = 1.2 V to 1.8 V; input rise and fall time between $V_X = 0.35V_{CCA}$ and $V_Y = 0.65V_{CCA}$.	-	0.4	1.0	ns
Card-side output transition times						
t_t	transition time	V_{CCB} = 1.8 V; [2] output transition time between V_X = 0.45 V and V_Y = 1.4 V	0.4	0.88	1.32	ns
Card-side input rise and fall times						
t_r	rise time	V_{CCB} = 1.8 V; input rise time between 0.58 V and 1.27 V	0.2	0.5	0.96	ns
t_f	fall time	V_{CCB} = 1.8 V; input fall time between 0.58 V and 1.27 V	0.2	0.45	0.96	ns
Host-side to card-side propagation delay; DATnA to DATnB, CMDA to CMDB and CLKA to CLKB						
t_{pd}	propagation delay	V_{CCA} = 1.2 V; V_{CCB} = 1.8 V [3]	-	3.1	5.4	ns
		V_{CCA} = 1.2 V; V_{CCB} = 3.3 V [3]	-	2.2	4.0	ns
		V_{CCA} = 1.8 V; V_{CCB} = 1.8 V [3]	-	2.7	4.8	ns
		V_{CCA} = 1.8 V; V_{CCB} = 3.3 V [3]	-	1.7	3.1	ns
Card-side to host-side propagation delay; DATnB to DATnA and CMDB to CMDA						
t_{pd}	propagation delay	V_{CCA} = 1.2 V; V_{CCB} = 1.8 V [3]	-	2.7	4.6	ns
		V_{CCA} = 1.2 V; V_{CCB} = 3.3 V [3]	-	1.7	3.0	ns
		V_{CCA} = 1.8 V; V_{CCB} = 1.8 V [3]	-	2.7	4.6	ns
		V_{CCA} = 1.8 V; V_{CCB} = 3.3 V [3]	-	1.6	2.7	ns

Symbol	Parameter	Conditions	T_{amb} = -40 °C to 85 °C			Unit
			Min	Typ[1]	Max	
Host-side to host-side propagation delay; CLKA to CLKFB						
t_{pd}	propagation delay	V_{CCA} = 1.2 V; V_{CCB} = 1.8 V [3]	-	5.8	10	ns
		V_{CCA} = 1.2 V; V_{CCB} = 3.3 V [3]	-	3.9	7.0	ns
		V_{CCA} = 1.8 V; V_{CCB} = 1.8 V [3]	-	5.4	9.4	ns
		V_{CCA} = 1.8 V; V_{CCB} = 3.3 V [3]	-	3.3	5.8	ns
Bus signal equivalent capacitance						
$C_{I/O}$	input/output capacitance	V_I = 0 V; f_i = 1 MHz; V_{CCA} = 1.8 V; host side [4]	-	5	-	pF
		V_I = 0 V; f_i = 1 MHz; V_{CCB} = 1.8 V; card side [4]	-	12	-	pF

[1] Typical values are measured at T_{amb} = 25 °C.
[2] t_t is the same as t_{THL} and t_{TLH}.
[3] t_{pd} is the same as t_{PLH} and t_{PHL}.
[4] EMI filter line capacitance from I/O driver to pin; $C_{I/O}$ is guaranteed by design.



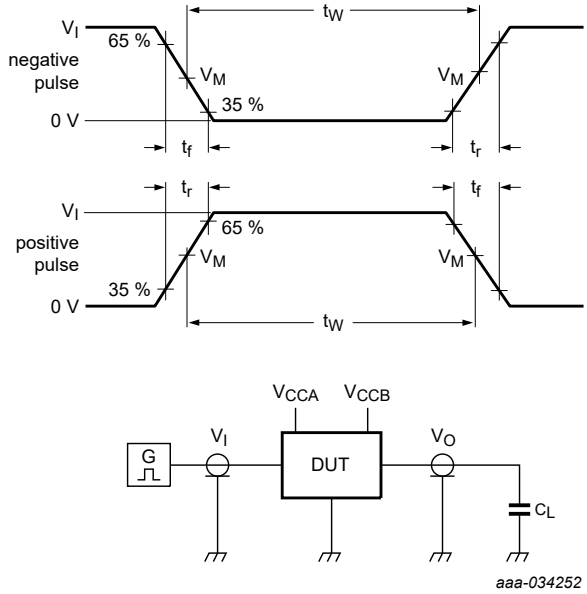
Measurement points are given in Table 10.
V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 5. The input to output propagation delays, input rise and fall times and output transition times

Table 10. Measurement points

Supply voltage		Input		Output
V_{CCA}	V_{CCB}	V_I [1]	V_M [1]	V_M [2]
1.1 V to 1.95 V	1.7 V to 3.6 V	V_{CCI}	$0.5V_{CCI}$	$0.5V_{CCO}$

[1] V_{CCI} is the supply voltage associated with the input.
[2] V_{CCO} is the supply voltage associated with the output.



Test data is given in Table 11.

All input pulses are supplied by generators having the following characteristics:

PRR ≤ 10 MHz; Z_O = 50 Ω; input edges (t_r, t_f) are defined in Section 13.

C_L = Load capacitance including jig and probe capacitance.

Fig. 6. Test circuit for measuring switching time

Table 11. Test data

Supply voltage		Input	Load	
V_{CCA}	V_{CCB}	V_I [1]	C_L (host side)	C_L (card side)
1.1 V to 1.95 V	1.7 V to 3.6 V	V_{CCI}	10 pF	15 pF

[1] V_{CCI} is the supply voltage associated with the input.

14. Application information

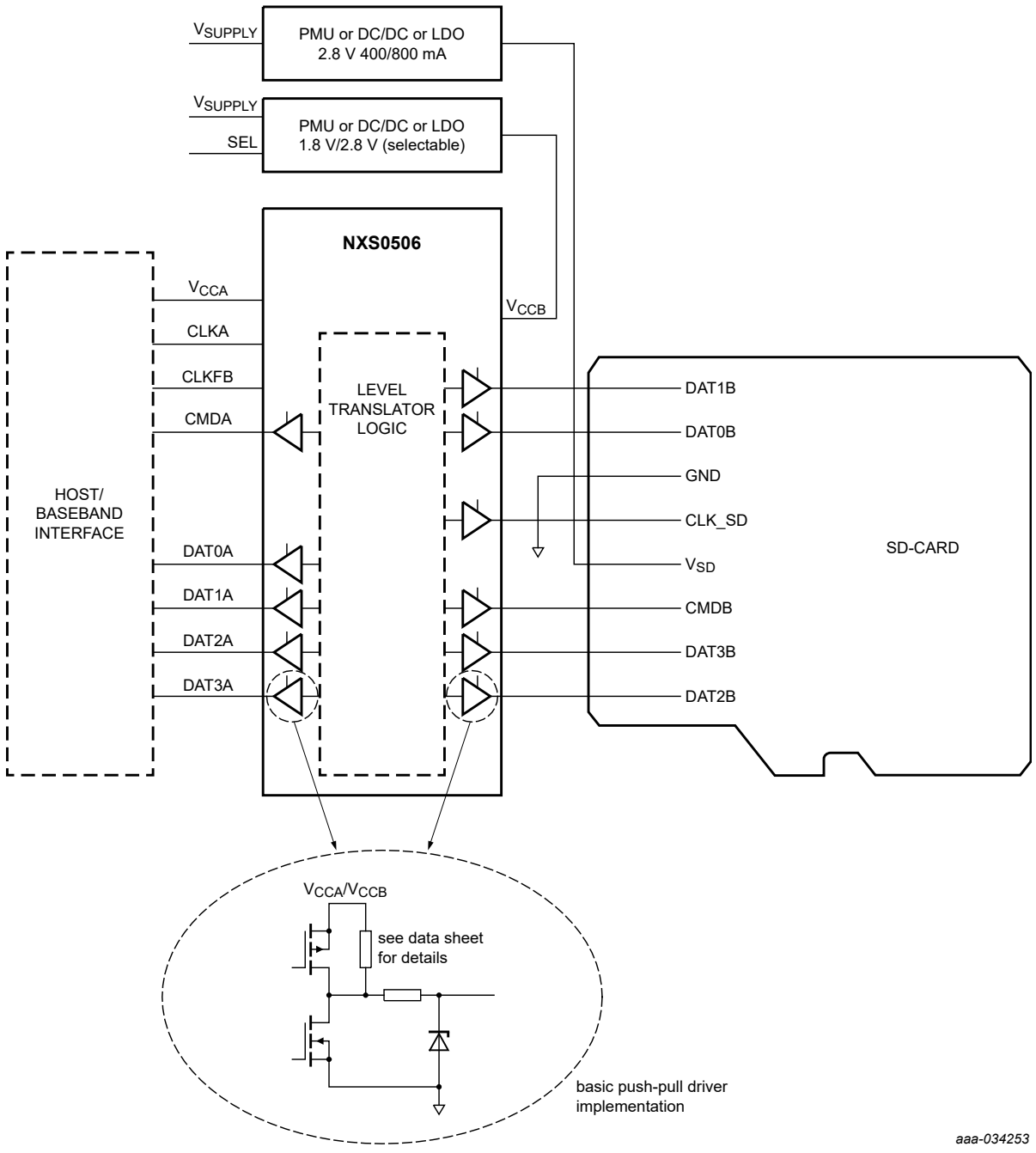


Fig. 7. Application diagram

14.1. PCB design guidelines

The translator can operate with frequencies up to 208 MHz so the PCB connections between host and translator and translator and card can start to act as transmission lines, affecting the signal integrity.

For PCB connections below 8 cm (t_r = 0.4 ns) no degradation of the signal integrity is to be expected. For longer connections it's important to take pre-cautions and check the signal integrity during the development phase of the PCB. If the CLKFB is used to synchronize the data that is read from the card, it is important to place the translator as close as possible to the card connector.

15. Design and assembly recommendations

15.1. PCB design guidelines

For optimum performance, use a Non-Solder Mask PCB Design (NSMD), also known as a copper-definied design, incorporating laser-drilled micro-vias connecting the ground pads to a buried ground-plane layer. This results in the lowest possible ground inductance and provides the best high frequency and ESD performance. For this case, refer to Table 12 for the recommended PCB design parameters.

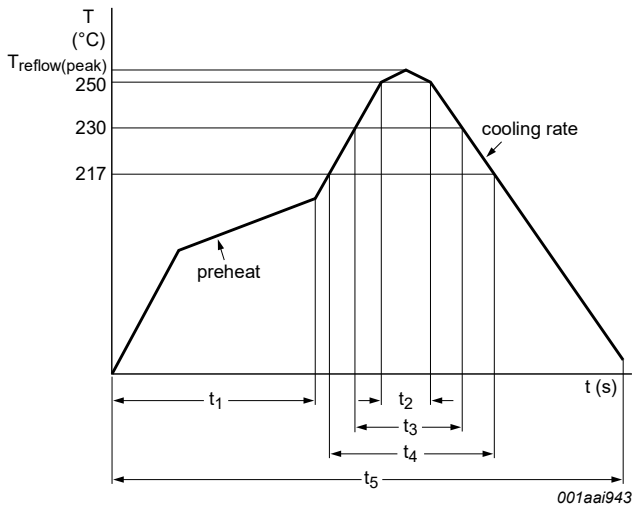
Table 12. Recommended PCB design parameters

Parameter	Value or specification
PCB Cu pad shape	circular
PCB Cu pad diameter	200 µm
PCB solder resist diameter	270 µm
WLCSP pad diameter (UBM)	200 µm

15.2. PCB assembly guidelines for Pb-free soldering

Table 13. Assembly recommendations

Parameter	Value or specification
PCB stencil shape	circular
PCB stencil aperture diameter	200 µm
PCB stencil thickness	80 µm
Solder paste material	$SnAg_4Cu$ (Cu 0.5%) (SAC405)
Solder reflow profile	see Fig. 8



The device can withstand at least three reflows with this profile.

Fig. 8. Pb-free solder reflow profile

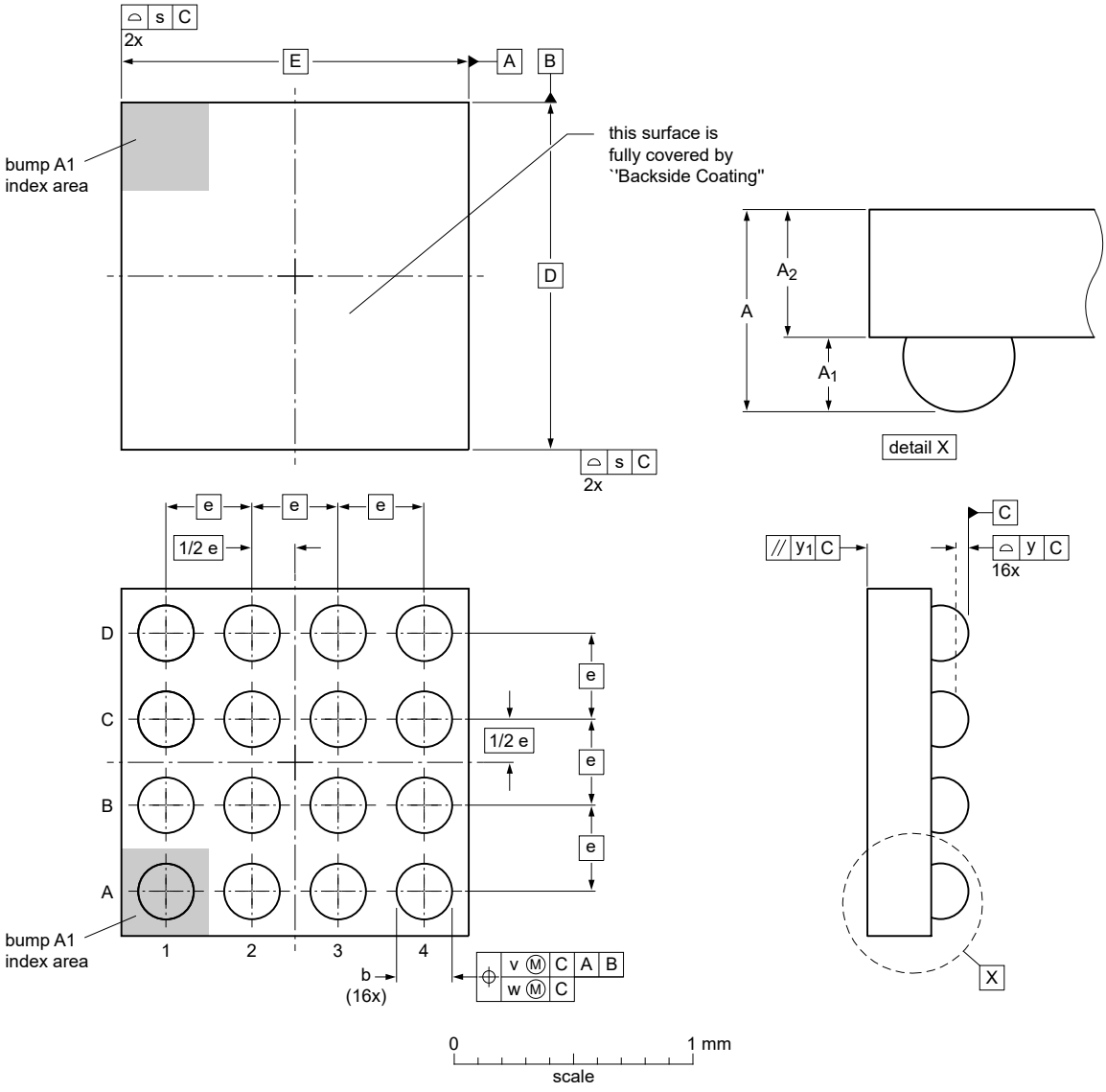
Table 14. Reflow soldering process characteristics

T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{reflow(peak)}$	peak reflow temperature		230	-	260	°C
t_1	time 1	soak time	60	-	180	s
t_2	time 2	time during T ≥ 250 °C	-	-	30	s
t_3	time 3	time during T ≥ 230 °C	10	-	50	s
t_4	time 4	time during T ≥ 217 °C	30	-	150	s
t_5	time 5		-	-	540	s
dT/dt	rate of temperature change	cooling rate	-	-	-6	°C/s
		preheat	2.5	-	4.0	°C/s

16. Package outline

WLCSP16: wafer level chip-scale package; 16 bumps; 1.455 mm x 1.455 mm x 0.43 mm body **SOT8025-1**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	b	D	E	e	s	v	w	y	y_1
mm	max	0.468	0.183	0.285	0.245								
	nom	0.430	0.163	0.267	0.225	1.455	1.455	0.35	0.025	0.015	0.05	0.05	0.06
	min	0.392	0.143	0.249	0.205								

Note
1. Dimension A includes backside coating thickness.

sot8025-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT8025-1						~~21-06-11~~ 21-06-16

Fig. 9. Package outline SOT8025-1 (WLCSP16)

17. Abbreviations

Table 15. Abbreviations

Acronym	Description
DUT	Device Under Test
EMI	Electro Magnetic Interface
ESD	ElectroStatic Discharge
FR4	Flame Retard 4
LDO	Low-Dropout
MMC	MultiMedia Card
NSMD	Non-Solder Mask PCB Design
OSP	Organic Solderability Preservation
PCB	Printed-Circuit Board
PMU	Project Management Unit
PRR	Pulse Rate Repetition
RoHS	Restriction of Hazardous Substances
SD	Secure Digital
UBM	Under Bump Metallization
WLCSP	Wafer-Level Chip-Scale Package

18. Revision history

Table 16. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
NXS0506 v.1	20220131	Product data sheet	-	-

19. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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