

## Key Features

- Voltage Range: 1.65 V – 3.6 V
- Serial Peripheral Interface (SPI) compatible
  - Supports SPI modes 0 and 3
  - Supports single input/output operations (1,1,1)
  - Supports dual input and dual output operations (1,1,2), (1,2,2), (0,2,2)
  - Supports quad input and quad output operations (1,1,4), (1,4,4), (0,4,4)
- 85 MHz Maximum Operating Frequency
- Program
  - Serial-input Page Program up to 256 bytes
  - Program Suspend and Resume
- Erase
  - Page erase (256-byte)
  - Block erase (4/32/64 kbyte)
  - Full Chip erase
  - Erase Suspend and Resume
- Program/Erase Speed
  - Page Program time: 2 ms typical
  - Page Erase time: 8 ms typical
  - Block Erase time: 8 ms typical
  - Chip Erase time: 8 ms typical
- Flexible Architecture: 4/32/64 kbyte blocks
- Hardware Reset ( $\overline{\text{HOLD}}$  /  $\overline{\text{RESET}}$  pin)
- Software-controlled Reset
- Software/Hardware Write Protection
  - 3x512-Byte Security Registers with OTP Lock
  - Enable/Disable protection with WP Pin
  - Write protect all/portion of memory via software protect
  - Top or Bottom Block selection
- Low Power Consumption
  - 1.2 mA active read current (typical)
  - 100 nA deep power-down (DPD) current (typical)
- Temperature Range: -40 °C to +85 °C
- Cycling Endurance/Data Retention
  - 10k program and erase cycles
  - Typical 20-year data retention
- Industry standard green (Pb/Halide-free/RoHS Compliant) Package Options
  - 8-lead SOIC (150-mil)
  - 8-pad 2x3x0.6 UDFN

## 2-Mbit, Ultra-Low Energy Serial Flash Memory

## Contents

<b>Key Features</b> .....	<b>1</b>
<b>1 General Description</b> .....	<b>6</b>
<b>2 Package Types and Pinouts</b> .....	<b>7</b>
2.1 Pin Configuration - SOP 150-mil.....	7
2.2 Pad Configuration - UDFN 2X3 MM.....	7
<b>3 Block Addresses</b> .....	<b>9</b>
<b>4 Functional and Operational Description</b> .....	<b>10</b>
4.1 Dual SPI Commands .....	10
4.2 Quad SPI Commands .....	10
4.3 Supply Voltage.....	10
4.3.1 Operating Supply Voltage .....	10
4.3.2 Power-up Conditions.....	10
4.3.3 Device Reset.....	10
4.3.4 Power-Down.....	10
4.4 Active Power and Standby Power Modes.....	10
4.5 Hold Condition .....	11
4.6 Software Reset and Hardware $\overline{\text{RESET}}$ .....	11
4.6.1 Software Reset.....	11
4.6.2 Hardware Reset (HOLD pin).....	11
<b>5 Status and Configuration Registers</b> .....	<b>12</b>
5.1 Status Register 1 .....	12
5.2 Status Register 2 .....	13
5.3 Status Register 3 .....	13
5.4 Status Register Memory Protection .....	15
5.4.1 Protection Tables .....	15
<b>6 Command Set</b> .....	<b>17</b>
6.1 Configuration and Status Commands .....	19
6.1.1 Write Enable (06h) .....	19
6.1.2 Write Enable for Volatile Status Register (50h).....	19
6.1.3 Write Disable (04h) .....	20
6.1.4 Read Status Register-1 (05h), Status Register-2 (35h), Status Register-3 (15h) .....	20
6.1.5 Active Status Interrupt (25h) .....	21
6.1.6 Write Status Register (01h or 31h or 11h) .....	21
6.2 Read Commands.....	23
6.2.1 Normal Read Data (03h) .....	23
6.2.2 Fast Read (0Bh).....	24
6.2.3 Fast Read Dual Output (3Bh).....	25
6.2.4 Fast Read Dual I/O (BBh) .....	26
6.2.5 Fast Read Quad Output (6Bh) .....	28
6.2.6 Fast Read Quad I/O (EBh).....	29
6.2.7 Set Burst with Wrap (77h) .....	31
6.3 ID and Power Commands.....	31
6.3.1 Release Power-down / Device ID (ABh) .....	32
6.3.2 Read Manufacturer / Device ID (90h) .....	33
6.3.3 Dual I/O Read Manufacture ID/ Device ID (92h).....	34
6.3.4 Quad I/O Read Manufacture ID / Device ID (94h) .....	35
6.3.5 Read JEDEC ID (9Fh).....	36
6.3.6 Read Unique ID Number (4Bh) .....	37
6.3.7 Deep Power-Down (B9h) .....	38
6.4 Program / Erase and Security Commands.....	39
6.4.1 Page Program (02h).....	39
6.4.2 Dual Page Program (A2h).....	40
6.4.3 Quad Page Program (32h).....	41
6.4.4 Page Erase (81h/DBh) .....	42

## 2-Mbit, Ultra-Low Energy Serial Flash Memory

6.4.5 4 kB Block Erase (20h) .....	42
6.4.6 32 kB Block Erase (52h) .....	43
6.4.7 64 kB Block Erase (D8h).....	44
6.4.8 Chip Erase (C7h / 60h) .....	45
6.4.9 Program/Erase Suspend (75h) .....	45
6.4.10 Program/Erase Resume (7Ah).....	47
6.4.11 Erase Security Registers (44h) .....	48
6.4.12 Program Security Registers (42h).....	49
6.4.13 Read Security Registers (48h).....	50
6.4.14 Enable Reset (66h) and Reset Device (99h) .....	51
6.4.15 Read Serial Flash Discoverable Parameter (5Ah) .....	51
<b>7 Electrical Characteristics .....</b>	<b>52</b>
7.1 Absolute Maximum Ratings .....	52
7.2 Operating ranges .....	52
7.3 Power-Up / Power-Down Timing and Requirements .....	53
7.4 DC Characteristics .....	54
7.5 AC Measurement conditions .....	54
7.6 AC Characteristics .....	55
7.7 Serial output timing .....	56
7.8 Serial input timing .....	56
7.9 HOLD Timing .....	56
7.10 WP Timing .....	57
<b>8 Ordering Information .....</b>	<b>58</b>
<b>9 Packaging Information .....</b>	<b>59</b>
9.1 eight-pin SOIC 150-mil.....	59
9.2 eight-pAD 2 x 3 x 0.6 mm UDFN .....	60
<b>Revision History .....</b>	<b>61</b>

## Figure

Figure 1: AT25EU0021A Logic Diagram .....	6
Figure 2: AT25EU0021A Pin Assignments, Eight-pin SOP 150-mil (Top View) .....	7
Figure 3: AT25EU0021A Pad Assignments, Eight-pad UDFN 2x3 mm (Top View).....	7
Figure 4: Hold Condition Activation .....	11
Figure 5: Write Enable Command for SPI Mode .....	19
Figure 6: Write Enable for Volatile Status Register (50h).....	19
Figure 7: Write Disable Command, SPI Mode .....	20
Figure 8: Read Status Register Command .....	20
Figure 9: Active Status Interrupt Command .....	21
Figure 10: Write Status Register Command.....	22
Figure 11: Read Data Command .....	23
Figure 12: Fast Read Command .....	24
Figure 13: Fast Read Dual Output Command.....	25
Figure 14: Fast Read Dual I/O Command (Initial command or previous M5-4≠10) .....	26
Figure 15: Fast Read Dual I/O Command (Previous command M5-4=10) .....	27
Figure 16: Fast Read Quad Output Command .....	28
Figure 17: Fast Read Quad I/O Command (Initial command or previous M5-4≠10).....	29
Figure 18: Fast Read Quad I/O Command (Previous command set M5-4=10).....	30
Figure 19: Set Burst with Wrap Command.....	31
Figure 20: Release Power-Down Command.....	32
Figure 21: Release Power-Down / Device ID Command .....	32
Figure 22: Read Manufacturer / Device ID Command .....	33
Figure 23: Dual I/O Read Manufacture ID/ Device ID Timing .....	34
Figure 24: Quad I/O Read Manufacture ID / Device ID Sequence Diagram .....	35
Figure 25: Read JEDEC ID Command.....	36
Figure 26: Read Unique ID Sequence Diagram.....	37
Figure 27: Deep Power-Down Command .....	38
Figure 28: Page Program Command .....	39
Figure 29: Dual Page Program Command .....	40
Figure 30: Quad Input Page Program Command.....	41
Figure 31: Page Erase Command.....	42
Figure 32: 4 kB Block Erase Command .....	42
Figure 33: 32 kB Block Erase Command .....	43
Figure 34: 64 kB Block Erase Command .....	44
Figure 35: Chip Erase Command.....	45
Figure 36: Program/Erase Suspend Command .....	46
Figure 37: Program/Erase Resume Command .....	47
Figure 38: Erase Security Register Command.....	48
Figure 39: Program Security Register Command .....	49
Figure 40: Read Security Command.....	50
Figure 41: Enable Reset and Reset Command Sequence .....	51
Figure 42: Read Serial Flash Discoverable Parameter Command .....	51
Figure 43: Power-Up Timing and Voltage Levels.....	53
Figure 44: AC Measurement I/O Waveform .....	54
Figure 45: Serial Output Timing .....	56
Figure 46: Serial Input Timing .....	56
Figure 47: HOLD Timing .....	56
Figure 48: WP Timing.....	57

## 2-Mbit, Ultra-Low Energy Serial Flash Memory

## Tables

Table 1: Block Addresses of the AT25EU0021A.....	9
Table 2: Status Register 1 Format .....	12
Table 3: Status Register 2 Format .....	13
Table 4: Status Register 3 Format .....	13
Table 5: Status Register Protect Table .....	14
Table 6: AT25EU0021A Status Register Memory Protection (CMP = 0) .....	15
Table 7: AT25EU0021A Status Register Memory Protection (CMP = 1) .....	16
Table 8: Command Set Table 1 .....	17
Table 9: Wrap Around Length Based on Wrap Bits .....	31
Table 10: AT25EU0021A ID Definition Table.....	31
Table 11: Readable Area of Memory While a Program or Erase Operation is Suspended .....	45
Table 12: Acceptable Commands During Program/Erase Suspend After $t_{PSL}/t_{ESL}$ - .....	46
Table 13: Acceptable Commands During Suspend ( $t_{PSL}/t_{ESL}$ Not Required).....	46
Table 14: Erase Security Coding.....	48
Table 15: Program Security Register Coding.....	49
Table 16: Read Security Register Coding .....	50
Table 17: Absolute Maximum Ratings.....	52
Table 18: Operating Ranges .....	52
Table 19: Timing Requirements for Power-Up/Down.....	53
Table 20: DC Electrical Characteristics.....	54
Table 21: AC Measurement Conditions .....	54
Table 22: AC Electrical Characteristics .....	55
Table 23: Ordering Codes .....	58
Table 24: Package Types .....	58

## 1 General Description

The AT25EU0021A is 2-Mbit Serial Peripheral Interface (SPI) Flash memory, designed for a wide variety of high-volume consumer-based applications in which program code is shadowed from Flash memory into embedded or external RAM for execution. The flexible erase architecture of the device, with its page erase granularity, is ideal for data storage as well, eliminating the need for additional data storage devices.

The erase block sizes of the device have been optimized to meet the needs of today's code and data storage applications. By optimizing the size of the erase blocks, the memory space can be used much more efficiently. Because certain code modules and data storage segments must reside by themselves in their own erase regions, the wasted and unused memory space that occurs with large block erase Flash memory devices can be greatly reduced. This increased memory space efficiency allows additional code routines and data storage segments to be added while still maintaining the same overall device density.

The device uses a single low-voltage power supply, ranging from 1.65 V to 3.6 V, and supports JEDEC standard manufacturer and device ID, a 128-bit Unique Serial Number, and three 512-bytes Security Registers.

Figure 1 shows the logic diagram of the AT25EU0021A device.

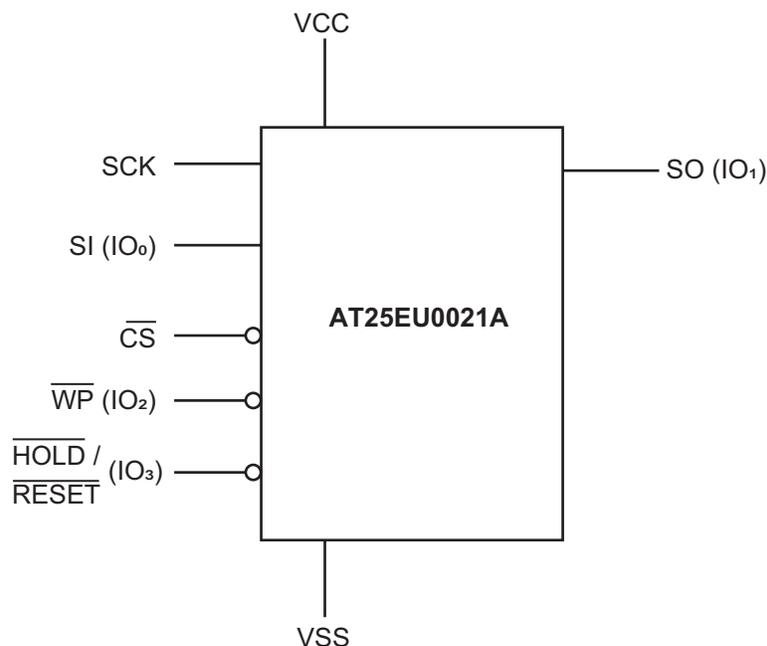


Figure 1: AT25EU0021A Logic Diagram

## 2-Mbit, Ultra-Low Energy Serial Flash Memory

## 2 Package Types and Pinouts

## 2.1 PIN CONFIGURATION - SOP 150-MIL

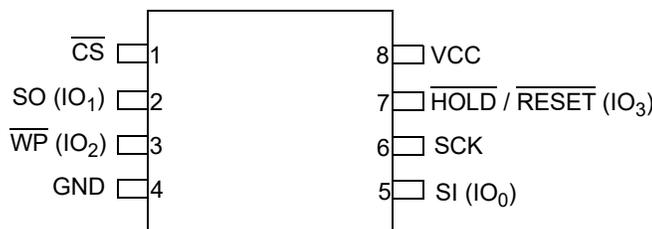


Figure 2: AT25EU0021A Pin Assignments, Eight-pin SOP 150-mil (Top View)

## 2.2 PAD CONFIGURATION - UDFN 2X3 MM

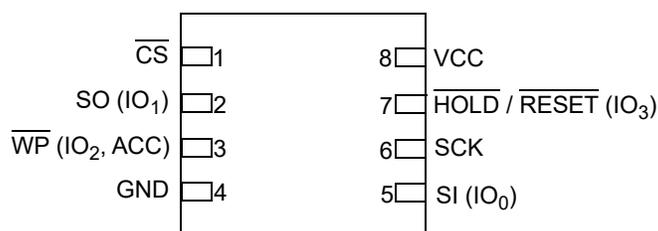


Figure 3: AT25EU0021A Pad Assignments, Eight-pad UDFN 2x3 mm (Top View)

During all operations, VCC must be held stable and within the specified valid range: VCC (min) to VCC (max).

All of the input and output signals must be held high or low (according to voltages of VIH, VOH, VIL, or VOL; see [Section 7.6, AC Characteristics](#)).

Symbol	Name and Function	Asserted State	Type
$\overline{\text{CS}}$	<b>CHIP SELECT:</b> Asserting the CS pin selects the device. When the CS pin is deasserted, the device is deselected and normally be placed in standby mode (all input signals are ignored, and all output signals are high impedance). Unless an internal Program, Erase, or Write Status Registers embedded operation is in progress, the device is in the Standby Power mode. Driving the CS input to low enables the device, placing it in the Active Power mode. After power-up, a falling edge on CS is required before the start of any command. A high-to-low transition on the CS pin is required to start an operation; a low-to-high transition is required to end an operation. When ending an internally self-timed operation, such as a program or erase cycle, the device does not enter the standby mode until the operation is complete.	Low	Input
SCK	<b>SERIAL CLOCK:</b> This pin provides a clock to the device. Command, address, and input data present on the SI pin is latched in on the rising edge of SCK, while output data on the SO pin is clocked out on the falling edge of SCK.	-	Input
SI (IO <sub>0</sub> )	<b>SERIAL INPUT:</b> The SI pin is used for all data input, including command and address sequences. Data on the SI pin is latched in on the rising edge of SCK. Data present on the SI pin is ignored whenever the device is deselected ( $\overline{\text{CS}}$ is deasserted).	-	Input/Output
SO (IO <sub>1</sub> )	<b>SERIAL OUTPUT:</b> Data on the SO pin is clocked out on the falling edge of SCK. The SO pin is in a high-impedance state whenever the device is deselected (CS is deasserted).	-	Input/Output

## 2-Mbit, Ultra-Low Energy Serial Flash Memory

Symbol	Name and Function	Asserted State	Type
$\overline{\text{WP}}$ (IO <sub>2</sub> )	<b>WRITE PROTECT:</b> The $\overline{\text{WP}}$ pin controls the hardware locking feature of the device. When $\overline{\text{WP}}$ is driven low (VIL), while the Status Register Protect bits (SRP1 and SRP0) of the Status Registers (SR2[0] and SR1[7]) are set to 0 and 1, respectively, it is not possible to write to the Status Registers. This prevents any alteration of the Status Registers. As a consequence, all the data bytes in the memory area that are protected by the Block Protect, BP4, BP3 bits in the status registers, are also hardware-protected against data modification while $\overline{\text{WP}}$ remains low.	-	Input/Output
$\overline{\text{HOLD}} / \overline{\text{RESET}}$ (IO <sub>3</sub> )	<b>HOLD:</b> The HOLD function is only available when QE=0, which can be configured either as a $\overline{\text{HOLD}}$ pin or as a $\overline{\text{RESET}}$ pin, depending on the Status Register setting. When QE=0 and $\overline{\text{HOLD}}/\overline{\text{RESET}}=0$ , the HOLD signal goes low to stop any serial communications with the device, but does not stop write status register, programming, or erase operations in progress. To use HOLD, CS must be kept low. It starts on falling edge of the $\overline{\text{HOLD}}$ signal, and SCK must be low. The HOLD condition ends on the rising edge of the HOLD signal when SCK is low. When the QE bit in the Status Register is cleared, the IO <sub>3</sub> pin can be configured either as a HOLD pin or as a RESET pin, depending on the state of the HOLD/RESET bit 7 in Status Register 3. Note that when the QE bit is set, the HOLD or RESET function is not available because this pin is used to transfer data.	-	Input/Output
V <sub>CC</sub>	<b>DEVICE POWER SUPPLY:</b> The V <sub>CC</sub> pin supplies the source voltage to the device.	-	Power
GND	<b>GROUND:</b> The ground reference for the power supply. Connect GND to the system ground.	-	Power

### 3 Block Addresses

Table 1: Block Addresses of the AT25EU0021A

Memory Density	Block (64 kB)	Block (32 kB)	Block No.	Block Size	Address Range	
2 Mbit	Block 0	Half Block 0	Block 0	4	000000h-000FFFh	
			.	.	.	
			.	.	.	
		Block 7	Half Block 1	Block 7	4	007000h-007FFFh
				Block 8	4	008000h-008FFFh
				.	4	.
		Block 15	Half Block 2	Block 15	4	00F000h-00FFFFh
				Block 16	4	010000h-010FFFh
				.	.	.
		Block 23	Half Block 3	Block 23	4	017000h-017FFFh
				Block 24	4	018000h-018FFFh
				.	.	.
	Block 31	Half Block 4	Block 31	4	01F000h-01FFFFh	
			Block 32	4	020000h-020FFFh	
			.	.	.	
	Block 39	Half Block 5	Block 39	4	027000h-027FFFh	
			Block 40	4	028000h-028FFFh	
			.	.	.	
	Block 47	Half Block 6	Block 47	4	02F000h-02FFFFh	
			Block 48	4	030000h-030FFFh	
			.	.	.	
	Block 55	Half Block 7	Block 55	4	037000h-037FFFh	
			Block 56	4	038000h-038FFFh	
			.	.	.	
	Block 63	Half Block 7	Block 63	4	03F000h-03FFFFh	
			.	.	.	
			.	.	.	

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## 2-Mbit, Ultra-Low Energy Serial Flash Memory

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### 4 Functional and Operational Description

The AT25EU0021A features a serial peripheral interface on a four-signals bus: SCK,  $\overline{\text{CS}}$ , SI, and SO. Both SPI bus mode 0 and 3 are supported.

The SPI mode has input bits (including commands, addresses, data, M7~M0, W6~W4, etc.) latched on the rising edge of SCK, as well as output bits transferred out on the falling edge of SCK.

#### 4.1 DUAL SPI COMMANDS

The AT25EU0021A supports Dual SPI operation. when using the Dual Output Fast Read (3Bh) or Dual I/O Fast read (BBh) commands. These commands allow data to be transferred to, and from, the device at two times the rate of the standard SPI. When using the Dual SPI command, the SI and SO pins become bidirectional I/O pins IO0 and IO1, respectively.

#### 4.2 QUAD SPI COMMANDS

The AT25EU0021A supports Quad SPI operation when using the Quad Output Fast Read (6Bh) or Quad I/O Fast Read (EBh) commands. These commands allow the data to be transferred to, and from, the device at four times the rate of standard SPI. When using the Quad SPI command, the SI and SO pins become bidirectional I/O pins, and the  $\overline{\text{WP}}$  and  $\overline{\text{HOLD}}$  pins become IO2 and IO3, respectively. Quad SPI commands require the non-volatile Quad Enable bit (QE) in Status Register 2 to be set to 1.

#### 4.3 SUPPLY VOLTAGE

##### 4.3.1 Operating Supply Voltage

Before selecting the memory and issuing commands to it, a valid and stable VCC voltage within the specified [VCC(min), VCC(max)] range must be applied (see operating ranges). To secure a stable DC supply voltage, it is recommended to decouple the VCC line with a suitable capacitor (usually of the order of 100 nF to 1  $\mu\text{F}$ ) close to the VCC/VSS package pins. This voltage must remain stable and valid until the end of the transmission of the command; for a Write command, it must be stable until the completion of the internal write cycle.

##### 4.3.2 Power-up Conditions

When the power supply is turned on, VCC rises continuously from VSS to VCC. During this time, the  $\overline{\text{CS}}$  line is not allowed to float; it must follow the VCC voltage. Thus, it is recommended to connect the  $\overline{\text{CS}}$  line to VCC through a suitable pull-up resistor. Also, the  $\overline{\text{CS}}$  input offers a built-in safety feature: the  $\overline{\text{CS}}$  input is edge sensitive and level sensitive: after power-up, the device does not become selected until a falling edge has first been detected on  $\overline{\text{CS}}$ . This ensures that  $\overline{\text{CS}}$  must have been high before going low to start the first operation.

##### 4.3.3 Device Reset

To prevent inadvertent Write operations during power-up (continuous rise of VCC), a power-on reset (POR) circuit is included. At power-up, the device does not respond to any command until VCC has reached the power-on reset threshold voltage (this threshold is lower than the minimum VCC operating voltage defined in Power-up Timing). When VCC is lower than VWI, the device is reset.

##### 4.3.4 Power-Down

At power-down (continuous decrease in VCC), as soon as VCC drops from the normal operating voltage to below the power-on reset threshold voltage (VWI), the device stops responding to any command sent to it. During power-down, the device must be deselected ( $\overline{\text{CS}}$  must be allowed to follow the voltage applied on VCC) and in Standby power mode (there must be no internal Write cycle in progress).

#### 4.4 ACTIVE POWER AND STANDBY POWER MODES

When  $\overline{\text{CS}}$  is low, the device is selected, and in the Active Power mode. The device consumes ICC. When  $\overline{\text{CS}}$  is high, the device is deselected. If a Write cycle is not currently in progress, the device then goes in to the Standby Power mode, and the device consumption drops to ICC1.

#### 4.5 HOLD CONDITION

When  $QE=0$ ,  $HOLD/RST=0$ , the  $\overline{HOLD}$  signal is used to pause any serial communications with the device without resetting the clocking sequence, but does not stop the in-progress operation of write status register, programming, or erasing. During the Hold condition, the Serial Data Output (SO) is high impedance, and Serial Data Input (SI) and SCK are don't care. To enter the Hold condition, the device must be selected, with  $\overline{CS}$  low. Normally, the device is kept selected for the whole duration of the Hold condition. Deselecting the device while it is in the Hold condition, has the effect of resetting the state of the device, and this mechanism can be used if it is required to reset any processes that had been in progress. The Hold condition starts when the  $\overline{HOLD}$  signal is driven low at the same time as SCK already being low (Figure 4). The Hold condition ends when the  $\overline{HOLD}$  signal is driven high at the same time as Serial Clock (SCK) is low. Figure 4 also shows what happens if the rising and falling edges are not timed to coincide with SCK being low.

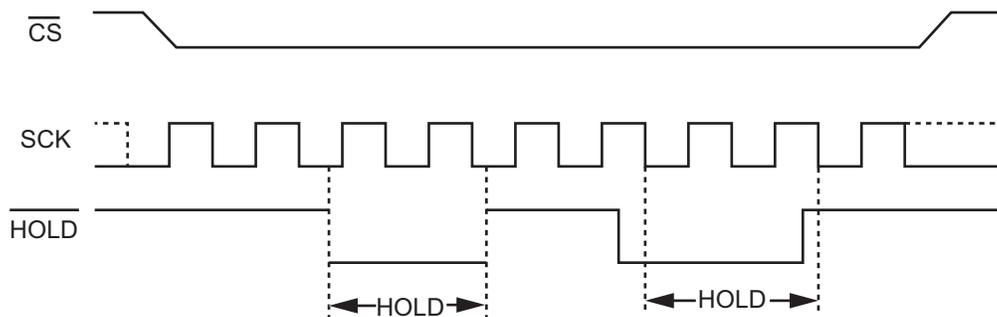


Figure 4: Hold Condition Activation

#### 4.6 SOFTWARE RESET AND HARDWARE RESET

##### 4.6.1 Software Reset

The AT25EU0021A can be reset to the initial power-on state by a software reset sequence. This sequence must include two consecutive commands: Enable Reset (66h) and Reset (99h). If the command sequence is accepted, the device takes approximately 300  $\mu\text{s}$  ( $t_{RST}$ ) to reset. No command is accepted during the reset period.

##### 4.6.2 Hardware Reset ( $\overline{HOLD}$ pin)

The AT25EU0021A can also be configured to use the hardware  $\overline{RESET}$  pin. The  $HOLD/RST$  bit in the Status Register-3 is the configuration bit for the  $\overline{HOLD}$  pin function or the  $\overline{RESET}$  pin function. When  $HOLD/RST=0$  (factory default), the pin acts as a  $\overline{HOLD}$  pin, as described above; when  $HOLD/RST=1$ , the pin acts as a  $\overline{RESET}$  pin. Driving the  $\overline{RESET}$  pin low for a minimum of  $\sim 1 \mu\text{s}$  ( $t_{RESET}(1)$ ) resets the device to its initial power-on state. Any on-going program/erase operation is interrupted, and data corruption can happen. While  $\overline{RESET}$  is low, the device does not accept any command input.

If  $QE$  bit is set to 1, the  $\overline{HOLD}$  or  $\overline{RESET}$  function is disabled, the pin becomes one of the four data I/O pins. (Note that when writing to the Status Register,  $QE$  must be 0.)

Note: While a faster  $\overline{RESET}$  pulse (as short as a few hundred nanoseconds) often resets the device, a 1  $\mu\text{s}$  minimum pulse is recommended to ensure reliable operation.

## 5 Status and Configuration Registers

### 5.1 STATUS REGISTER 1

The following table shows the bit assignments for Status Register 1.

**Table 2: Status Register 1 Format**

Bit #	Acronym	Name	Type	Default	Description
7	SRP0	Status Register Protect 0	R/W	0	The Status Register Protect 0 bit is a non-volatile bit that, along with the SRP1 and WP bits, controls the method of write protection: software protection, hardware protection, power supply lock-down, or one time programmable protection. See <a href="#">Table 5</a> .
6:2	BP4-BP0	Block Protect Size	R/W	0	The Block Protect (BP4, BP3, BP2, BP1, BP0) bits are non-volatile. They define the size of the area to be software-protected against Program and Erase commands. These bits are written with the Write Status Register command. When the Block Protect (BP4, BP3, BP2, BP1, BP0) bits are set to 1, the relevant memory (as defined in <a href="#">Table 6</a> and <a href="#">Table 7</a> ) becomes protected against Page Program, Page Erase, and Block Erase commands. The Block Protect (BP4, BP3, BP2, BP1, BP0) bits can be written provided that the Hardware Protected mode has not been set. The Chip Erase command is executed if the Block Protect (BP2, BP1, and BP0) bits are 0 and CMP=0, or the Block Protect (BP2, BP1 and BP0) bits are 1 and CMP=1. Note that on power-up the device is unprotected.
1	WEL	Write Enable	R	n/a	The Write Enable Latch bit indicates the status of the internal Write Enable Latch. When WEL is 1, the internal Write Enable Latch is set, when WEL is 0, the internal Write Enable Latch is reset, and no Write Status Register, Program or Erase command is accepted.
0	RDY/BSY	Ready/Busy	R	n/a	The Ready/Busy (RDY/BSY) bit indicates whether the memory is busy in with a program, erase, or write status register command. When RDY/BSY is set to 1, the device is busy, when the RDY/BSY bit is cleared to 0, the device is not busy.

## 2-Mbit, Ultra-Low Energy Serial Flash Memory

## 5.2 STATUS REGISTER 2

The following table shows the bit assignments for Status Register 2.

Table 3: Status Register 2 Format

Bit #	Acronym	Name	Type	Default	Description
$\bar{7}$	SUS	Suspend Status	R	n/a	The SUS bit is a read-only bit in Status Register 2 (S15) that is set to 1 after executing a Program/Erase Suspend (75h) command. The SUS bit is cleared to 0 by a Program/Erase Resume (7Ah) command, Software Reset (66h/99h) command, Hardware reset, or power-down, power-up cycle.
6	CMP	Complement Protect	R/W	0	This a non-volatile read/write bit in the status register that is used in conjunction with the BP4, BP3, BP2, BP1, and BP0 bits to provide more flexibility for the array protection. See the <a href="#">Table 5</a> for details.
5:3	LB3-LB1	Write-Protect and Control Status	R	0	The LB bits are non-volatile One-Time Program (OTP) bits in the Status Register (S13-S11) that provide the write protect control and status to the Security Registers. The default state of LB is 0 (the security registers are unlocked). LB can be set to 1 individually using the Write Register command. LB is One-Time Programmable; once it is set to 1, the Security Registers becomes read-only permanently (LB3-1 corresponds to S13-11).
2	Reserved	--	n/a	n/a	Reserved.
1	QE	Quad Enable	n/a	0	This is a non-volatile read/write bit that allows Quad SPI operation. When 0, the WP and HOLD pins are enabled. When set to 1, the quad IO2 and IO3 pins are enabled. Never set the QE pin to 1 during standard SPI or dual SPI operation. If the WP and HOLD pins are connected directly to the power supply or ground.
0	SRP1	Status Register Protect 1	R/W	0	The Status Register Protect 1 is a non-volatile Read/Write bit that, along with the SRP0 and WP bits, controls the method of write protection: software protection, hardware protection, power supply lock-down, or one time programmable protection. See <a href="#">Table 5</a> .

## 5.3 STATUS REGISTER 3

The following table shows the bit assignments for Status Register 3.

Table 4: Status Register 3 Format

Bit #	Acronym	Name	Type	Default	Description
$\bar{7}$	HOLD/RST	$\overline{\text{HOLD}}$ or $\overline{\text{RESET}}$	R/W	0	The $\overline{\text{HOLD}}$ or $\overline{\text{RESET}}$ pin function (HOLD/RST) bit is used to specify whether the HOLD or RESET function must be implemented on the hardware pin. When HOLD/RST=0 (factory default), the pin acts as $\overline{\text{HOLD}}$ ; when HOLD/RST=1, the pin acts as $\overline{\text{RESET}}$ . However, $\overline{\text{HOLD}}$ or $\overline{\text{RESET}}$ functions are only available when QE=0.
6:0	Reserved	--	n/a	n/a	Reserved

Note that the default value is set by the manufacturer during wafer sort, marked as default in following text.

## 2-Mbit, Ultra-Low Energy Serial Flash Memory

Table 5: Status Register Protect Table

SRP1	SRP0	WP	Status Register	Description
$\bar{0}$	0	X	Software Protected	The Status Register can be written to after a Write Enable command, WEL=1 (default).
0	1	0	Hardware Protected	WP=0, the Status Register is locked and cannot be written to.
0	1	1	Hardware Unprotected	WP=1, the Status Register is unlocked and can be written to after a Write Enable command, WEL=1.
1	0	X	Power Supply Lock-Down <sup>1</sup>	Status Register is protected and cannot be written to until the next power-down, power-up cycle.
1	1	X	One-Time Program	Status Register is permanently protected and cannot be written to.

1. When SRP1, SRP0= (1, 0), a power-down, power-up cycle changes SRP1, SRP0 to (0, 0) state.

2. The One-Time Program feature is available upon special order. Contact Dialog Semiconductor for details.

## 2-Mbit, Ultra-Low Energy Serial Flash Memory

## 5.4 STATUS REGISTER MEMORY PROTECTION

## 5.4.1 Protection Tables

Table 6: AT25EU0021A Status Register Memory Protection (CMP = 0)

STATUS REGISTER 1					AT25EU0021A (2M-BIT) MEMORY PROTECTION 3			
BP4	BP3	BP2	BP1	BP0	PROTECTED BLOCK(S)	PROTECTED ADDRESSES	PROTECTED DENSITY	PROTECTED PORTION <sup>2</sup>
0	X	X	0	0	NONE	NONE	NONE	NONE
0	0	X	0	1	3	030000h – 03FFFFh	64 kB	UPPER 1/4
0	0	X	1	0	2 and 3	020000h – 03FFFFh	128 kB	UPPER 1/2
0	1	X	0	1	0	000000h – 00FFFFh	64 kB	LOWER 1/4
0	1	X	1	0	0 and 1	000000h – 01FFFFh	128 kB	LOWER 1/2
0	X	X	1	1	0 to 3	000000h – 03FFFFh	256 kB	ALL
1	X	0	0	0	NONE	NONE	NONE	NONE
1	0	0	0	1	3	03F000h – 03FFFFh	4 kB	U - 1/64
1	0	0	1	0	3	03E000h – 03FFFFh	8 kB	U - 1/32
1	0	0	1	1	3	03C000h – 03FFFFh	16 kB	U - 1/16
1	0	1	0	X	3	038000h – 03FFFFh	32 kB	U - 1/8
1	0	1	1	0	3	038000h – 03FFFFh	32 kB	U - 1/8
1	1	0	0	1	0	000000h – 00FFFFh	4 kB	L - 1/64
1	1	0	1	0	0	000000h – 001FFFh	8 kB	L - 1/32
1	1	0	1	1	0	000000h – 003FFFh	16 kB	L - 1/16
1	1	1	0	X	0	000000h – 007FFFh	32 kB	L - 1/8
1	1	1	1	0	0	000000h – 007FFFh	32 kB	L - 1/8
1	X	1	1	1	0 to 3	000000h – 03FFFFh	256 kB	ALL

1. X = don't care.

2. L = Lower; U = Upper.

3. If any Erase or Program command specifies a memory region that contains protected data portion, this command is ignored.

## 2-Mbit, Ultra-Low Energy Serial Flash Memory

Table 7: AT25EU0021A Status Register Memory Protection (CMP = 1)

STATUS REGISTER 1					AT25EU0021A (2M-BIT) MEMORY PROTECTION 3			
BP4	BP3	BP2	BP1	BP0	PROTECTED BLOCK(S)	PROTECTED ADDRESSES	PROTECTED DENSITY	PROTECTED PORTION <sup>2</sup>
0	X	X	0	0	0 to 3	000000h – 03FFFFh	512 kB	ALL
0	0	X	0	1	0 to 2	000000h – 02FFFFh	448 kB	Lower 3/4
0	0	X	1	0	0 and 1	000000h – 01FFFFh	384 kB	Lower 1/2
0	1	X	0	1	1 to 3	010000h – 03FFFFh	256 kB	Upper 3/4
0	1	X	1	0	2 to 3	020000h – 03FFFFh	448 kB	Upper 1/2
0	X	X	1	1	NONE	NONE	NONE	NONE
1	X	0	0	0	0 to 3	000000h – 03FFFFh	256 kB	ALL
1	0	0	0	1	0 to 3	000000h – 03EFFFh	252 kB	L - 63/64
1	0	0	1	0	0 to 3	000000h – 03DFFFh	248 kB	L - 31/32
1	0	0	1	1	0 to 3	000000h – 03BFFFh	240 kB	L - 15/16
1	0	1	0	X	0 to 3	000000h – 037FFFh	224 kB	L - 7/8
1	0	1	1	0	0 to 3	000000h – 037FFFh	224 kB	L - 7/8
1	1	0	0	1	0 to 3	001000h – 03FFFFh	252 kB	L - 63/64
1	1	0	1	0	0 to 3	002000h – 03FFFFh	248 kB	L - 31/32
1	1	0	1	1	0 to 3	004000h – 03FFFFh	240 kB	L - 15/16
1	1	1	0	X	0 to 3	008000h – 03FFFFh	224 kB	L - 7/8
1	1	1	1	0	0 to 3	008000h – 03FFFFh	224 kB	L - 7/8
1	X	1	1	1	NONE	NONE	NONE	NONE

1. X = don't care.

2. L = Lower; U = Upper.

3. If any Erase or Program command specifies a memory region that contains protected data portion, this command is ignored.

## 2-Mbit, Ultra-Low Energy Serial Flash Memory

## 6 Command Set

All commands, addresses, and data are transferred into and out of the device, beginning with the most significant bit on the first rising edge of SCK after CS is driven low. Then, the one-byte opcode must be transferred into the device on SI, most significant bit first, each bit being latched on a rising edge of SCK.

Every command sequence starts with a one-byte opcode. Depending on the command, this might be followed by address bytes. See Table 8.

For the Read, Fast Read, Read Status Register-1, Read Status Register-2 or Release from Deep Power-Down, or Read Device ID command, the transferred-in command sequence is followed by a data out sequence. CS can be driven high after any bit of the data-out sequence is being transferred out.

For the Page Program, Page Erase, Block Erase, Chip Erase, Write Status Register, Write Enable, Write Disable or Deep Power-Down command, CS must be driven high exactly at a byte boundary; otherwise, the command is rejected. (CS must drive high when the number of clock pulses after CS being driven low is an exact multiple of eight.) For Page Program, if at any time the input byte is not a full byte, nothing happens, and WEL is not reset.

**Table 8: Command Set Table** <sup>1</sup>

Command Name	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	n- Bytes
<b>READ</b>							
Normal Read Data	03h	A23-A16	A15-A8	A7-A0	(D7-D0)	(Next Byte)	(continuous)
Fast Read	0Bh	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)	(continuous)
Dual Output Fast Read	3Bh	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0) <sup>2</sup>	(continuous)
Quad Output Fast Read	6Bh	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0) <sup>3</sup>	(continuous)
Dual I/O Fast Read	BBh	A23-A8 <sup>4</sup>	A7-A0 M7-M0 <sup>4</sup>	(D7-D0)			(continuous)
Quad I/O Fast Read	EBh	A23-A0 M7-M0 <sup>5</sup>	Dummy	(D7-D0) <sup>6</sup>			(continuous)
Set Burst with Wrap	77h	W6-W4					
<b>Program/Erase and Suspend</b>							
Page Program	02h	A23-A16	A15-A8	A7-A0	(D7-D0) <sup>7</sup>	(Next Byte)	
Dual Page Program	A2h	A23-A16	A15-A8	A7-A0	(D7-D0) <sup>7</sup>	(Next Byte)	
Quad Page Program	32h	A23-A16	A15-A8	A7-A0	(D7-D0) <sup>7</sup>	(Next Byte)	
Page Erase	81h/DBh	A23-A16	A15-A8	A7-A0	(D7-D0) <sup>7</sup>	(Next Byte)	
Block Erase (4 kB)	20h	A23-A16	A15-A8	A7-A0	(D7-D0) <sup>7</sup>	(Next Byte)	
Block Erase (32 kB)	52h	A23-A16	A15-A8	A7-A0			
Block Erase (64 kB)	D8h	A23-A16	A15-A8	A7-A0			
Chip Erase	C7h/60h						
Program/Erase Suspend	75h						
Program/Erase Resume	7Ah						
<b>Security</b>							
Erase Security Registers	44h	A23-A16 <sup>8</sup>	A15-A8 <sup>8</sup>	A7-A0 <sup>8</sup>			
Program Security Registers	42h	A23-A16 <sup>8</sup>	A15-A8 <sup>8</sup>	A7-A0 <sup>8</sup>	D7-D0	Next Byte	
Read Security Registers	48h	A23-A16 <sup>8</sup>	A15-A8 <sup>8</sup>	A7-A0 <sup>8</sup>	Dummy	D7-D0	
Read Serial Flash Discoverable Parameter	5Ah	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)	(continuous)

## 2-Mbit, Ultra-Low Energy Serial Flash Memory

Table 8: Command Set Table <sup>1</sup> (Continued)

Command Name	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	n- Bytes
<b>Configuration</b>							
Write Enable	06h						
Volatile SR Write Enable	50h						
Write Disable	04h						
<b>Status Register</b>							
Read Status Register-1	05h	(S7-S0) <sup>9</sup>					(continuous)
Write Status Register <sup>10</sup>	01h	S7-S0	S15-S8				
Read Status Register-2	35h	(S15-S8) <sup>9</sup>					(continuous)
Write Status Register-2	31h	S7-S0					
Read Status Register-3	15h	(S15-S8) <sup>9</sup>					(continuous)
Write Status Register-3	11h	S7-S0					
Active Status Interrupt	25h						
<b>ID and Power</b>							
Deep Power-down	B9h						
Release Power-down / ID	ABh	Dummy	Dummy	Dummy	ID7-ID0		(continuous)
Release Power-down	ABH						
Manufacturer/Device ID	90h	Dummy	Dummy	00/01h	(MF7-MF0)/ (ID7-ID0)	(ID7-ID0) <sup>9</sup> / (MF7-MF0) <sup>9</sup>	(continuous)
Mftr./Device ID Dual IO	92h	A23-A8 <sup>4</sup>	A7-A0 <sup>4</sup> (M7-M0)	(M7-M0) (D7-D0)			(continuous)
Mftr./Device ID Quad IO	94h	A23-A0 (M7-M0) <sup>5</sup>	(M7-M0) (D7-D0) <sup>6</sup>				(continuous)
Read JEDEC ID	9Fh	(MF7-MF0)	(ID15-ID8)	(ID7-ID0) <sup>9</sup>			(continuous)
Read Unique ID Number	4Bh	Dummy	Dummy	Dummy	Dummy	(ID127-ID0)	
<b>Other Commands</b>							
Enable Reset	66h						
Reset Device	99h						

1. Data bytes are transferred with Most Significant Bit first. Byte fields with data in parenthesis ( ) indicate data output from the device.

2. Dual SPI data output format:

IO0 = (D6, D4, D2, D0)

IO1 = (D7, D5, D3, D1)

3. Quad SPI data output format:

IO0 = (D4, D0, .....

IO1 = (D5, D1, .....

IO2 = (D6, D2, .....

IO3 = (D7, D3, .....

4. Dual SPI address input format:

IO0 = A22, A20, A18, A16, A14, A12, A10, A8, A6, A4, A2, A0, M6, M4, M2, M0

IO1 = A23, A21, A19, A17, A15, A13, A11, A9, A7, A5, A3, A1, M7, M5, M3, M1

5. Quad SPI address input format:

IO0 = A20, A16, A12, A8, A4, A0, M4, M0

IO1 = A21, A17, A13, A9, A5, A1, M5, M1

IO2 = A22, A18, A14, A10, A6, A2, M6, M2

IO3 = A23, A19, A15, A11, A7, A3, M7, M3

6. Fast Read Quad I/O data output format:

IO0 = (x, x, x, x, D4, D0, D4, D0)

IO1 = (x, x, x, x, D5, D1, D5, D1)

IO2 = (x, x, x, x, D6, D2, D6, D2)

IO3 = (x, x, x, x, D7, D3, D7, D3)

2-Mbit, Ultra-Low Energy Serial Flash Memory

- 7. At least one byte of data input is required for Page Program, Dual Page Program, Quad Page Program and Program Security Registers, up to 256 bytes of data input. If more than 256 bytes of data are sent to the device, the addressing wraps to the beginning of the page and overwrites previously sent data.
- 8. Security Register Address:  
 Security Register1 A23-16 = 00h A15-9 = 0001000 A8-0 = byte address  
 Security Register2 A23-16 = 00h A15-9 = 0010000 A8-0 = byte address  
 Security Register3 A23-16 = 00h A15-9 = 0011000 A8-0 = byte address
- 9. The Status Register contents and Device ID repeat continuously until  $\overline{CS}$  terminates the command.
- 10. Write Status Register (01h) can also be used to write Status Register-1 and 2, see [Table 6.1.6](#).

6.1 CONFIGURATION AND STATUS COMMANDS

6.1.1 Write Enable (06h)

The Write Enable command sets the Write Enable Latch (WEL) bit in the Status Register to 1. The WEL bit must be set before every Page Program, Page Erase, Block Erase, Chip Erase, Write Status Register, and Erase/Program Security Registers command. The Write Enable command is entered by driving  $\overline{CS}$  low, transferring the opcode 06h into the Data Input (SI) pin on the rising edge of SCK, and then driving  $\overline{CS}$  high.

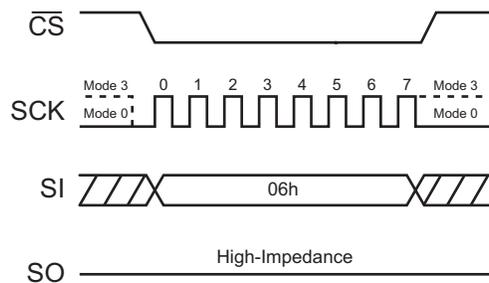


Figure 5: Write Enable Command for SPI Mode

6.1.2 Write Enable for Volatile Status Register (50h)

The non-volatile Status Register bits described in [Section 5](#) can also be written to as volatile bits. This gives more flexibility to change the system configuration and memory protection schemes quickly without waiting for the typical non-volatile bit write cycles or affecting the endurance of the Status Register non-volatile bits. To write the volatile values into the Status Register bits, the Write Enable for Volatile Status Register (50h) command must be issued before a Write Status Register (01h) command. The Write Enable for Volatile Status Register command does not set the Write Enable Latch (WEL) bit; it is only valid for the Write Status Register command to change the volatile Status Register bit values.

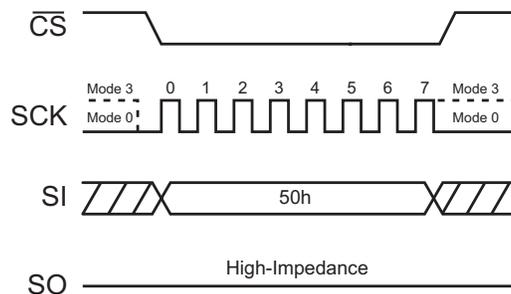


Figure 6: Write Enable for Volatile Status Register (50h)

6.1.3 Write Disable (04h)

The Write Disable command resets the Write Enable Latch (WEL) bit in the Status Register to 0. The Write Disable command is entered by driving  $\overline{CS}$  low, transferring the opcode 04h onto the SI pin, and then driving  $\overline{CS}$  high. Note that the WEL bit is automatically reset after power-up and upon completion of the Write Status Register, Erase/Program Security Registers, Page Program, Page Erase, Block Erase, Chip Erase, and Reset command.

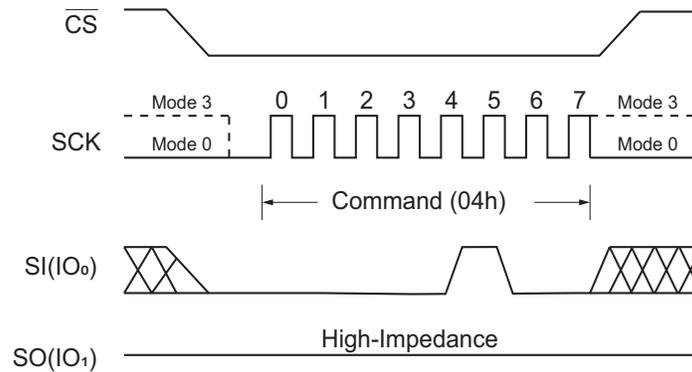


Figure 7: Write Disable Command, SPI Mode

6.1.4 Read Status Register-1 (05h), Status Register-2 (35h), Status Register-3 (15h)

The Read Status Register commands allow the eight-bit Status Registers to be read. The command is entered by driving  $\overline{CS}$  low and transferring the opcode 05h for Status Register-1, 35h for Status Register-2, 15h for Status Register-3 onto the SI pin on the rising edge of SCK. The status register bits are then transferred out on the SO pin at the falling edge of SCK, with most significant bit (MSB) first, as shown in Figure 8. See Section 5 for Status Register descriptions. The Read Status Register command can be used at any time, even while a Program, Erase or Write Status Register cycle is in progress. This allows the RDY/BSY status bit to be checked to determine when the cycle is complete and if the device can accept another command. The Status Register can be read continuously, as shown in Figure 8. The command is completed by driving  $\overline{CS}$  high.

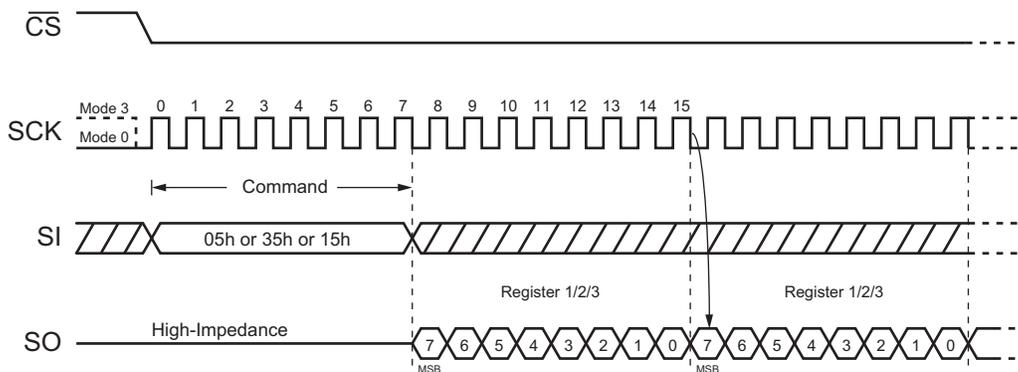


Figure 8: Read Status Register Command

### 6.1.5 Active Status Interrupt (25h)

The Active Status Interrupt improves the ability to determine if the device is busy or not. It is not necessary to continuously read the Status Register; it is sufficient to monitor the value of the SO line. If the SO line is connected to an interrupt line on the host controller, the host controller can be in sleep mode until the SO line indicates that the device is ready for the next command. The RDY/BSY bit can be read at any time, including during an internally self-timed program or erase operation. To enable the Active Status Interrupt command, the  $\overline{CS}$  pin must first be asserted, and the opcode of 25h must be clocked into the device. The value of the SI line after the opcode being clocked in is of no significance to the operation. The value of RDY/BSY is then output on the SO line, and is continuously updated by the device for as long as the  $\overline{CS}$  pin remains asserted. Additional clocks on the SCK pin are not required. That is, whether the additional clock on the SCK pin exists is independent of the correct output of the value of RDY/BSY. (Figure 9 shows a case where additional clocks exist.) If the RDY/BSY bit changes from 1 to 0 while the  $\overline{CS}$  pin is asserted, the SO line changes from 1 to 0. (The RDY/BSY bit cannot change from 0 to 1 during an operation; so, if the SO line already is 0, it does not change.) Deasserting the  $\overline{CS}$  pin terminates the Active Status Interrupt operation and puts the SO pin into a high-impedance state. The sequence of issuing the ASI command is:  $\overline{CS}$  goes low → sending ASI opcode → RDY/BSY data out on SO.

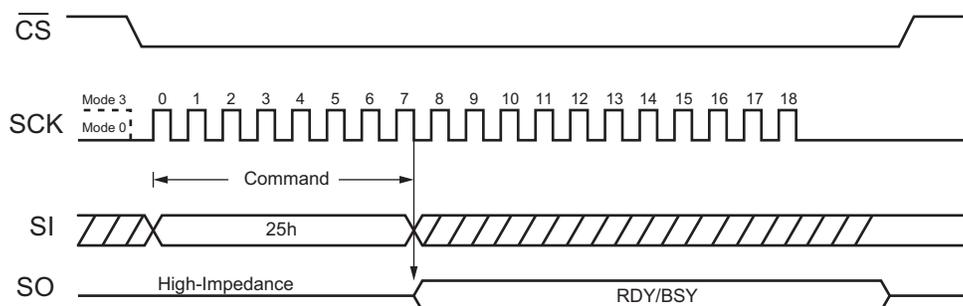


Figure 9: Active Status Interrupt Command

### 6.1.6 Write Status Register (01h or 31h or 11h)

The Write Status Register command allows the Status Registers to be written. Status Register-1 can be written by the Write Status Register 01h command; Status Register-2 be written by the Write Status Register 01h or 31h command; Status Register-3 can be written by the Write Status Register 11h command. When the Write Status Register command 01h writes one byte data, it is written to Status Register-1. When the Write Status Register command 01h writes two bytes of data, the first byte data is written to Status Register-1, and the second byte data is written to Status Register-2. Commands 31h or 11h are used with one byte only (any additional ones are ignored), which is written to the corresponding Status Register: command 31h writes the byte to Status Register 2; command 11h writes the byte to Status Register 3. The writable Status Register bits include: SRP0, BP[4:0] in Status Register-1; CMP, LB[3:1], QE, and SRP1 in Status Register- 2; HOLD/RST in Status Register- 3. All other Status Register bit locations are read-only and are not affected by the Write Status Register command. LB[3:1] are non-volatile OTP bits; once set to 1, they cannot be cleared to 0.

The Write Status Register (WRSR) command allows new values to be written to the Status Register. Before it can be accepted, a Write Enable (WREN) or Write Enable For Volatile SR command must previously have been executed. After the Write Enable (WREN) command has been decoded and executed, the device sets the Write Enable Latch (WEL).

The Write Status Register command has no effect on S15 (SUS), S1 (WEL), and S0 (RDY/BSY) of the Status Register.  $\overline{CS}$  must be driven high after the 8 or 16 bits of data have been latched in. If not, the Write Status Register (WRSR) command is not executed. As soon as  $\overline{CS}$  is driven high, the self-timed Write Status Register cycle (whose duration is  $t_{W}$ ) is initiated. While the Write Status Register cycle is in progress, the Status Register can still be read to check the value of the Write In Progress (RDY/BSY) bit. The RDY/BSY bit is 1 during the self-timed Write Status Register cycle; it is 0 when it is completed. When the cycle is completed, the Write Enable Latch (WEL) is reset.

The Write Status Register command lets the user change the values of the Block Protect (BP4, BP3, BP2, BP1, and BP0) bits, to define the size of the area that is to be treated as read-only, as defined in Table 6 and Table 7. The Write Status Register (WRSR) command also lets the user set or reset the Status Register Protect (SRP1 and SRP0) bits in accordance with the Write Protect ( $\overline{WP}$ ) signal. The Status Register Protect (SRP1 and SRP0) bits and Write Protect ( $\overline{WP}$ ) signal allow the device to be put

2-Mbit, Ultra-Low Energy Serial Flash Memory

in the Hardware Protected Mode. The Write Status Register command is not executed once the Hardware Protected Mode is entered.

The sequence of issuing WRSR command is:  $\overline{CS}$  goes low → sending WRSR opcode → Status Register data on SI →  $\overline{CS}$  goes high.

The  $\overline{CS}$  must go high exactly at the 8-bit or 16-bit data boundary; otherwise, the command is rejected. The self-timed Write Status Register cycle time ( $t_W$ ) is initiated as soon as  $\overline{CS}$  goes high. The Ready/Busy (RDY/BSY) bit can be checked during the Write Status Register cycle is in progress. The RDY/BSY is set 1 during the  $t_W$  timing, and is set to 0 when the Write Status Register Cycle is completed and the Write Enable Latch (WEL) bit is reset.

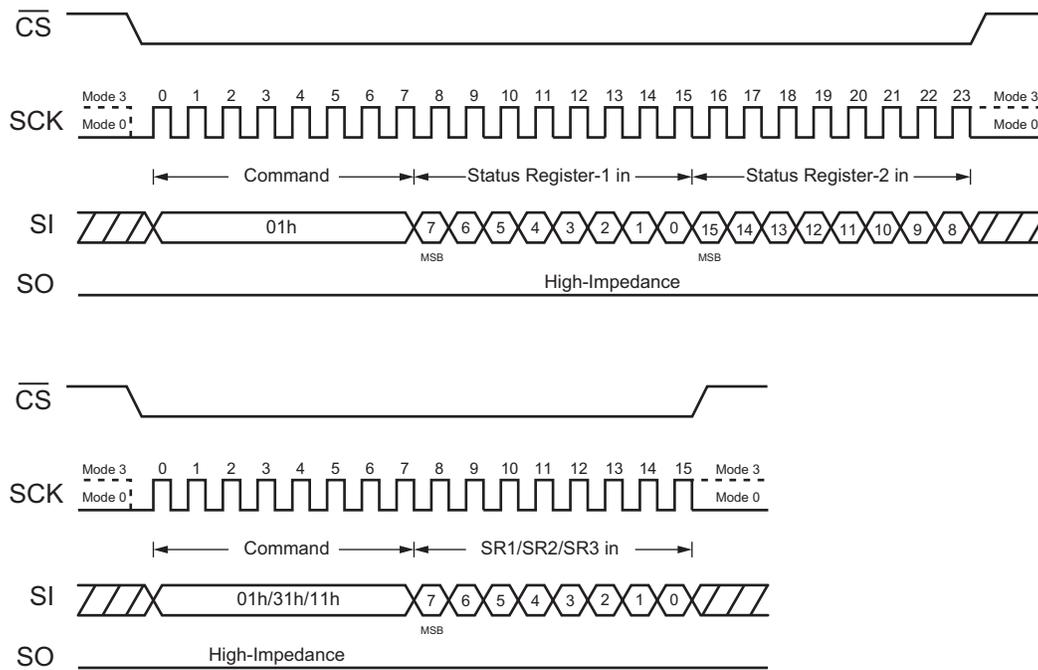


Figure 10: Write Status Register Command

6.2 READ COMMANDS

6.2.1 Normal Read Data (03h)

The Read Data command allows one or more data bytes to be sequentially read from the memory. The command is initiated by driving the  $\overline{CS}$  pin low, then transferring the opcode 03h, followed by a 24-bit address (A23-A0), onto the SI pin. The code and address bits are latched on the rising edge of the SCK pin. After the address is received, the data byte of the addressed memory location is transferred out on the SO pin at the falling edge of SCK, with most significant bit (MSB) first. The address is automatically incremented to the next higher address after each byte of data is transferred out, allowing for a continuous stream of data. This means that the entire memory can be accessed with a single command as long as the clock continues. The command is completed by driving  $\overline{CS}$  high. The Read Data command sequence is shown in Figure 11. If a Read Data command is issued while an Erase, Program, or other Write cycle is in progress (RDY/BSY=1), the command is ignored and has no effect on the current cycle. The Read Data command allows a clock frequency up to a maximum of  $f_R$  (see Section 7.6, AC Characteristics).

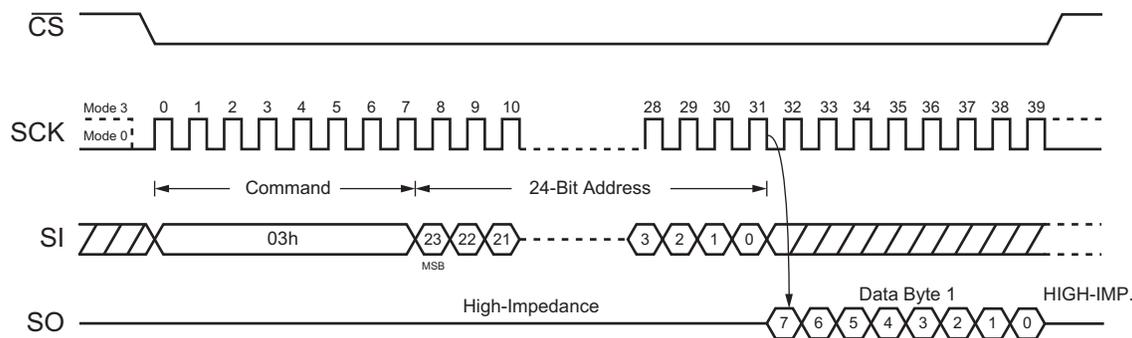


Figure 11: Read Data Command

2-Mbit, Ultra-Low Energy Serial Flash Memory

6.2.2 Fast Read (0Bh)

The Fast Read command is similar to the Read Data command except that it can operate at the highest possible frequency of  $f_C$  (see Section 7.6, AC Characteristics). In standard SPI mode, this is done by adding eight dummy clocks after the 24-bit address, as shown in Figure 12. The dummy clocks allow the devices internal circuits additional time for setting up the initial address. During the dummy clocks the data value on the SO pin is a don't care.

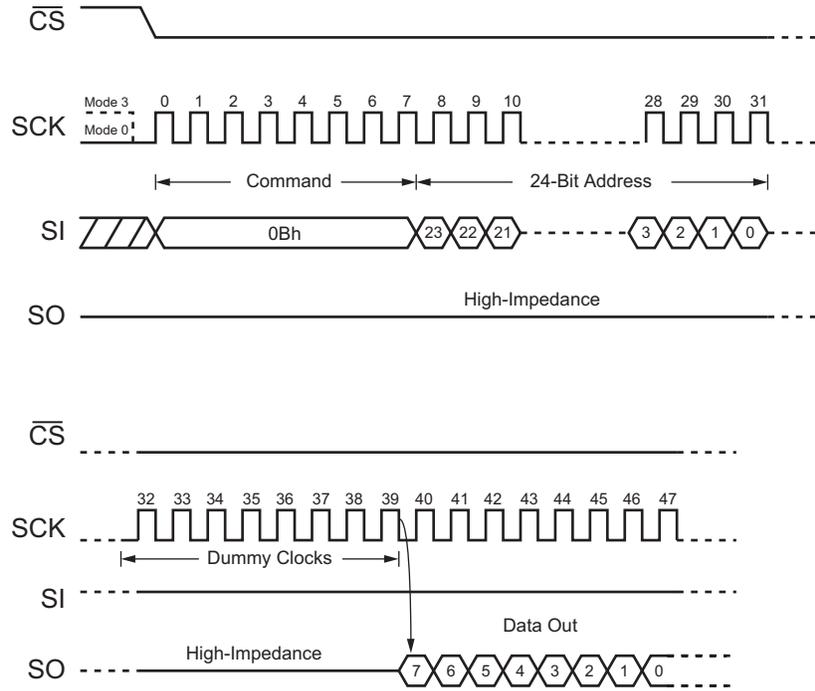


Figure 12: Fast Read Command

6.2.3 Fast Read Dual Output (3Bh)

The Dual-Output Read Array command is similar to the standard Read Array command and can be used to sequentially read a continuous stream of data from the device by providing the clock pin once the initial starting address has been specified. Unlike the standard Read Array command, the Dual-Output Read Array command allows two bits of data to be clocked out of the device on every clock cycle, rather than just one.

To perform the Dual-Output Read Array operation, the  $\overline{CS}$  pin must first be asserted; then, the opcode 3Bh must be clocked into the device. After the opcode has been clocked in, the three address bytes must be clocked in to specify the location of the first byte to read within the memory array. Following the three address bytes, a single dummy byte also must be clocked into the device.

After the three address bytes and the dummy byte have been clocked in, additional clock cycles output data on both the SO and SI pins. The data is output with the MSB of a byte first, and the MSB is output on the SO pin. During the first clock cycle, bit seven of the first data byte is output on the SO pin, while bit six of the same data byte is output on the SI pin. During the next clock cycle, bits five and four of the first data byte are output on the SO and SI pins, respectively. The sequence continues with each byte of data being output after every four clock cycles. When the last byte (0FFFFFFh) of the memory array has been read, the device continues reading from the beginning of the array (000000h). There are no delays when wrapping around from the end of the array to the beginning of the array. Deasserting the  $\overline{CS}$  pin terminates the read operation and puts the SO and SI pins into a high-impedance state. The  $\overline{CS}$  pin can be deasserted at any time and does not require that a full byte of data be read.

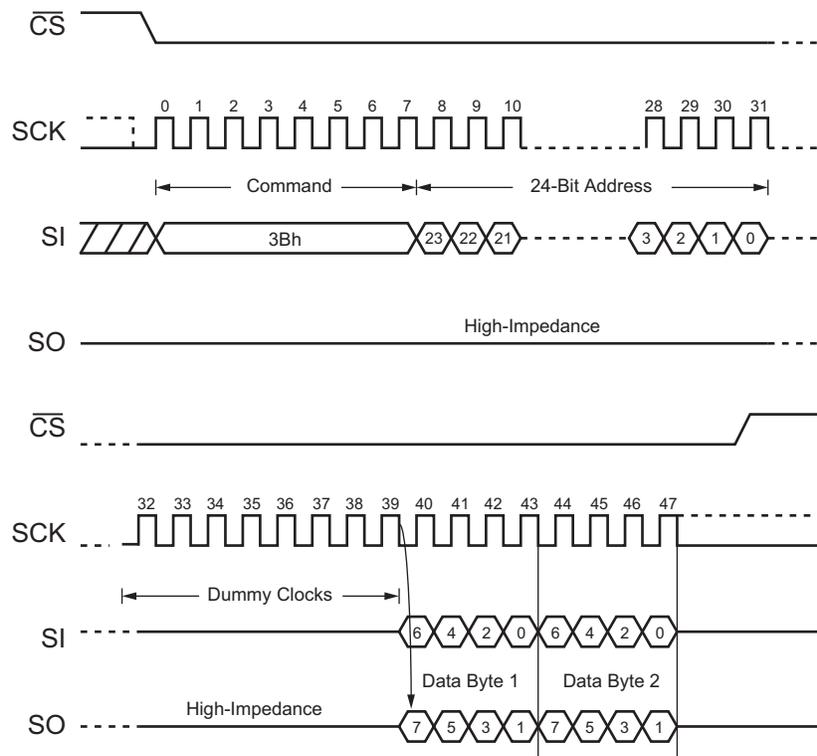


Figure 13: Fast Read Dual Output Command

2-Mbit, Ultra-Low Energy Serial Flash Memory

6.2.4 Fast Read Dual I/O (BBh)

The Dual-I/O Fast Read Array command is similar to the Dual-Output Read Array command and can be used to sequentially read a continuous stream of data from the device by providing the clock pin once the initial starting address with two bits of address on each clock and two bits of data on every clock cycle.

To perform the Dual-I/O Fast Read Array operation, the  $\overline{CS}$  pin must first be asserted; then, the opcode BBh must be clocked into the device. After the opcode has been clocked in, the three address bytes must be clocked in to specify the location of the first byte to read within the memory array. Following the three address bytes, a single mode byte also must be clocked into the device.

After the three address bytes and the mode byte have been clocked in, additional clock cycles output data on both the SO and SI pins. The data is always output with the MSB of a byte first, and the MSB is always output on the SO pin. During the first clock cycle, bit seven of the first data byte is output on the SO pin, while bit six of the same data byte is output on the SI pin. During the next clock cycle, bits five and four of the first data byte are output on the SO and SI pins, respectively. The sequence continues with each byte of data output after every four clock cycles. When the last byte (0FFFFFFh) of the memory array has been read, the device continues reading from the beginning of the array (000000h). No delays are incurred when wrapping around from the end of the array to the beginning of the array. Deasserting the  $\overline{CS}$  pin terminates the read operation and puts the SO and SI pins into a high-impedance state. The  $\overline{CS}$  pin can be deasserted at any time and does not require that a full byte of data be read.

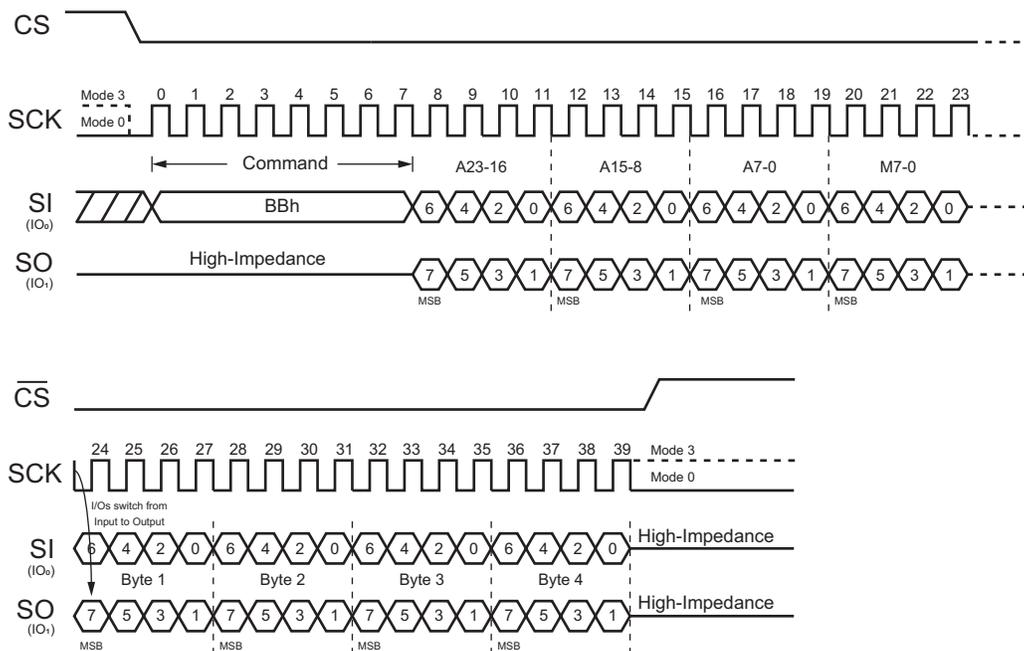


Figure 14: Fast Read Dual I/O Command (Initial command or previous M5-4#10)

Fast Read Dual I/O with “Continuous Read Mode”

The Fast Read Dual I/O command can further reduce command overhead through setting the Continuous Read Mode bits (M7-0) after the input Address bits (A23-0), as shown in Figure 7-5. The upper nibble of M7-4 controls the length of the next Fast Read Dual I/O command through the inclusion, or exclusion, of the first byte command code. The lower nibble bits of M3-0 are don't care (“x”). However, the I/O pins must be high-impedance prior to the falling edge of the first data out clock. If the “Continuous Read Mode” bits M5-4 = (1,0), the next Fast Read Dual I/O command (after CS is raised and then lowered) does not require the BBh command code. This reduces the command sequence by eight clocks and allows the Read address to be immediately entered after CS is asserted low. If the “Continuous Read Mode” bits M5-4 do not equal to (1,0), the next command (after CS is raised and then lowered) requires the first byte command code, thus returning to normal operation. A Continuous Read Mode Reset command can also be used to reset M7-0 before issuing normal commands.

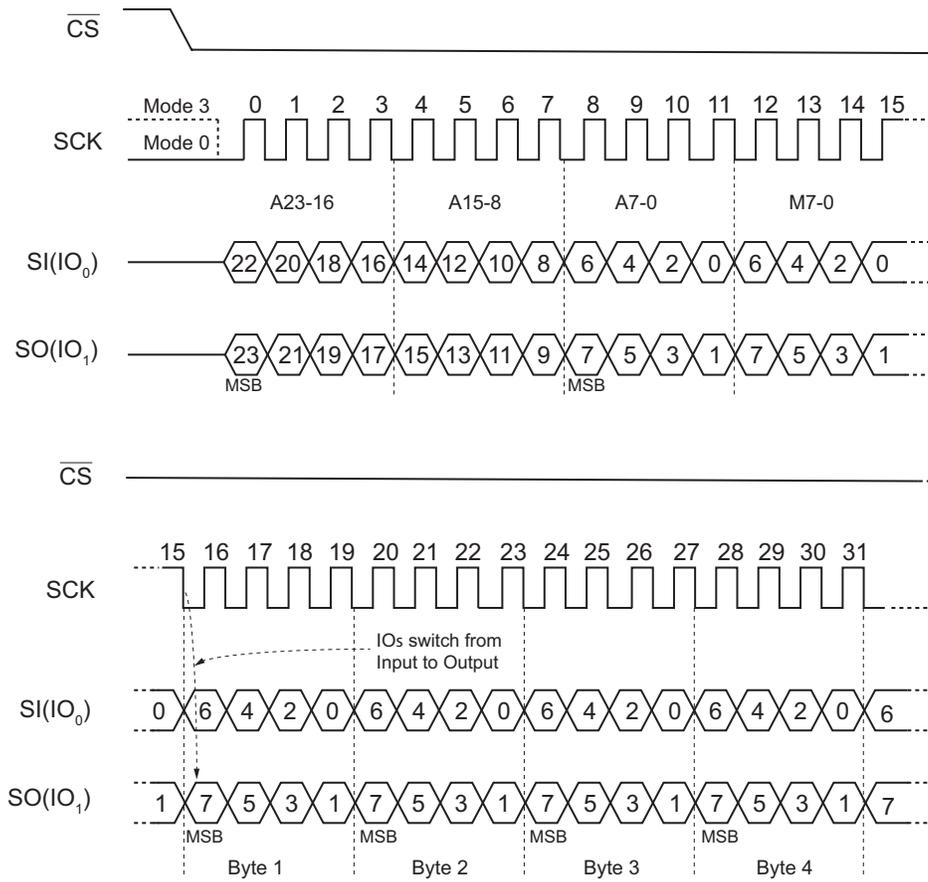


Figure 15: Fast Read Dual I/O Command (Previous command M5-4=10)

6.2.5 Fast Read Quad Output (6Bh)

The Quad-Output Fast Read Array command is followed by a three-byte address (A23 - A0) and one dummy byte, each bit being latched in during the rising edge of SCK; then, the memory contents are shifted out four bits per clock cycle from IO<sub>3</sub>, IO<sub>2</sub>, IO<sub>1</sub>, and IO<sub>0</sub>. The address automatically increments to the next higher address after each byte of data is shifted out.

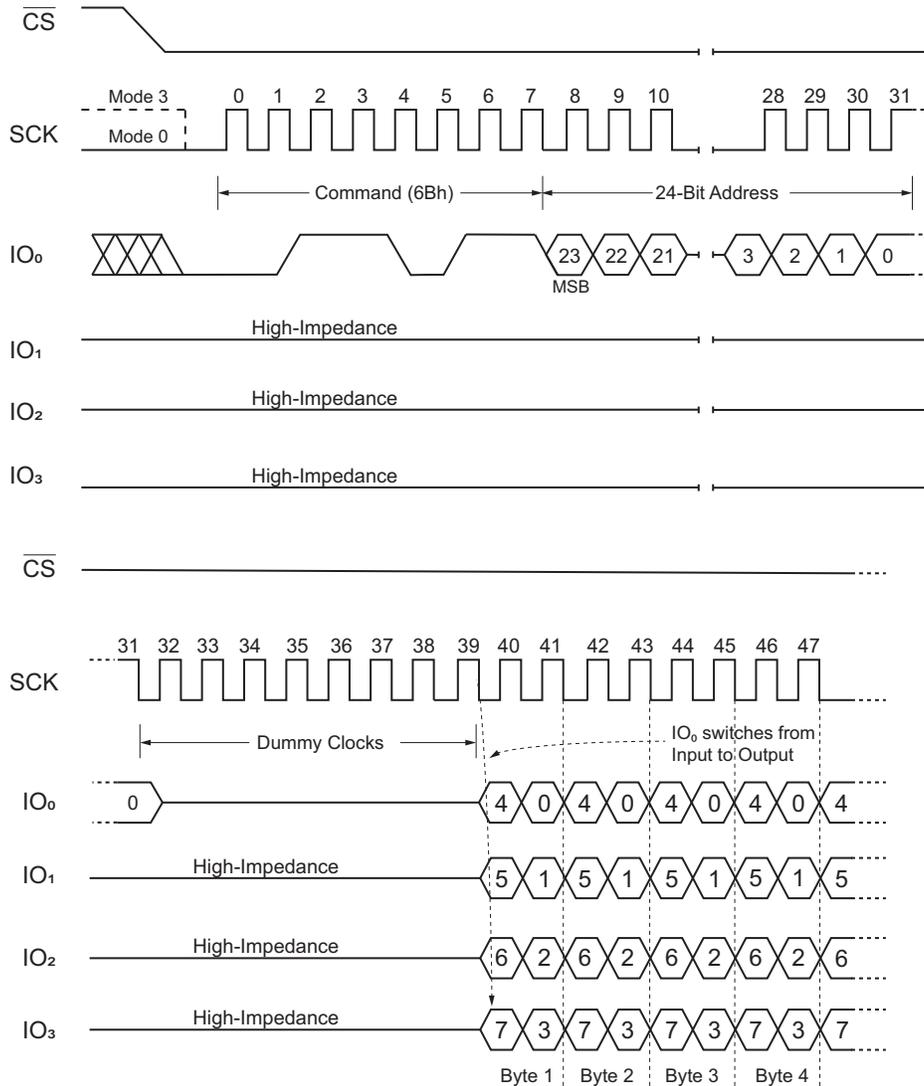


Figure 16: Fast Read Quad Output Command

2-Mbit, Ultra-Low Energy Serial Flash Memory

6.2.6 Fast Read Quad I/O (EBh)

The Quad-I/O Fast Read Array command is similar to the Quad-Output Fast Read Array command. It allows four bits of address to be clocked into the device on every clock cycle, rather than just one.

To perform the Quad-I/O Read Array operation, the  $\overline{CS}$  pin must first be asserted; then, the opcode EBh must be clocked into the device. After the opcode has been clocked in, the three address bytes must be clocked in to specify the location of the first byte to read within the memory array. Following the three address bytes, a single mode byte must also be clocked into the device.

After the three address bytes, the mode byte and two dummy bytes have been clocked in, additional clock cycles output data on the IO<sub>3:0</sub> pins. The data is output with the MSB of a byte first, and the MSB is output on the IO<sub>3</sub> pin. During the first clock cycle, bit 7 of the first data byte is output on the IO<sub>3</sub> pin while bits 6, 5, and 4 of the same data byte are output on the IO<sub>2</sub>, IO<sub>1</sub>, and IO<sub>0</sub> pins, respectively. During the next clock cycle, bits 3, 2, 1, and 0 of the first data byte are output on the IO<sub>3</sub>, IO<sub>2</sub>, IO<sub>1</sub>, and IO<sub>0</sub> pins, respectively. The sequence continues with each byte of data being output after every two clock cycles.

When the last byte (0FFFFFFh) of the memory array has been read, the device continues reading from the beginning of the array (000000h). No delays are incurred when wrapping around from the end of the array to the beginning of the array. Deasserting the  $\overline{CS}$  pin terminates the read operation and puts the IO<sub>3</sub>, IO<sub>2</sub>, IO<sub>1</sub>, and IO<sub>0</sub> pins into a high-impedance state. The  $\overline{CS}$  pin can be deasserted at any time and does not require a full byte of data to be read. The Quad Enable bit (QE) of the Status Register must be set to enable for the Quad-I/O Read Array command.

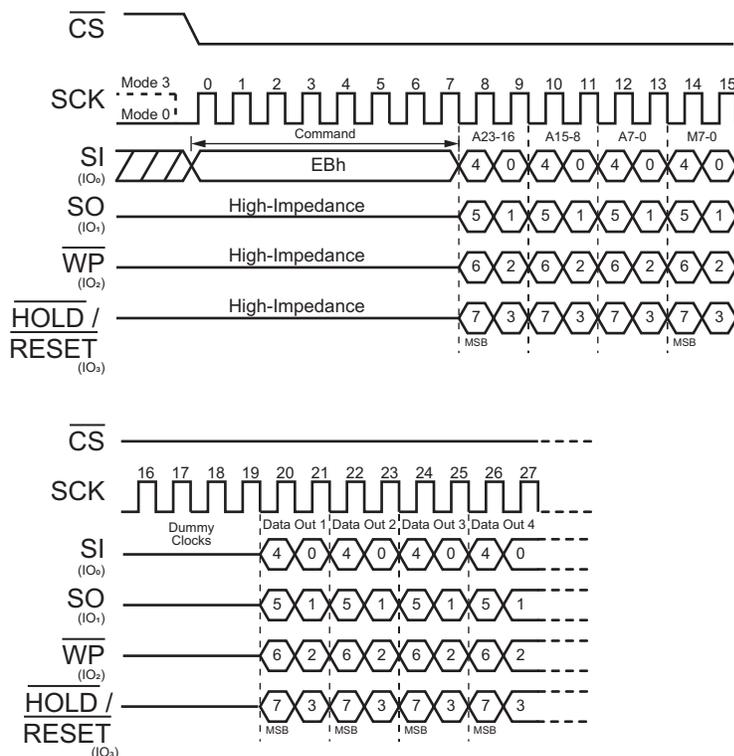


Figure 17: Fast Read Quad I/O Command (Initial command or previous M5-4#10)

Quad-I/O Fast Read Quad I/O with “Continuous Read Mode”

The Fast Read Quad I/O command can further reduce command overhead through setting the Continuous Read Mode bits (M7-0) after the input Address bits (A23-0), as shown in Figure 17. The upper nibble (M7-4) of the Continuous Read Mode bits controls the length of the next Fast Read Quad I/O command through the inclusion, or exclusion, of the first byte command code. The lower nibble bits (M3-0) of the Continuous Read Mode bits are don't care. However, the IO pins must be high-impedance before the falling edge of the first data out clock. If the Continuous Read Mode bits M5-4 = (1,0), the next Quad-I/O Read Array command (after CS is raised and then lowered) does not require the EBh command code, as shown in Figure 18. This reduces the command

2-Mbit, Ultra-Low Energy Serial Flash Memory

sequence by eight clocks and allows the Read address to be immediately entered after  $\overline{CS}$  is asserted low. If the Continuous Read Mode bits M5-4 do not equal to (1,0), the next command (after  $\overline{CS}$  is raised and then lowered) requires the first byte command code, thus returning to normal operation. A Continuous Read Mode Reset command can also be used to reset M7-0 before issuing normal commands.

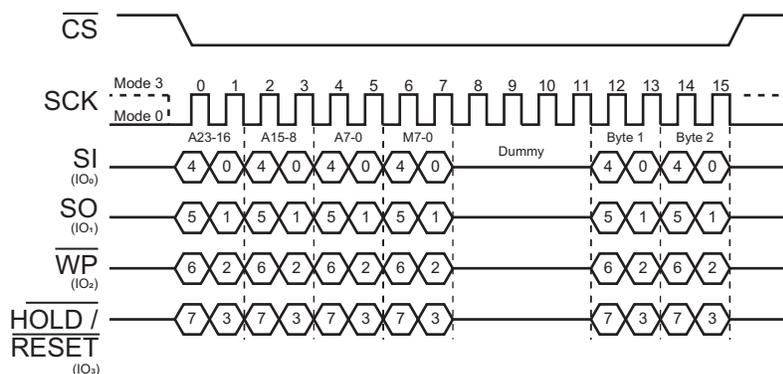


Figure 18: Fast Read Quad I/O Command (Previous command set M5-4=10)

2-Mbit, Ultra-Low Energy Serial Flash Memory

6.2.7 Set Burst with Wrap (77h)

The Set Burst with Wrap command is used in conjunction with the Quad I/O Fast Read and Quad I/O Word Fast Read command to access a fixed length (8-, 16-, 32-, or 64-byte) section within a 256-byte page in standard SPI mode (see Table 9 and Figure 19).

Table 9: Wrap Around Length Based on Wrap Bits

W6	W5	W4 = 0		W4 = 1 (default)	
		Wrap Around	Wrap Length	Wrap Around	Wrap Length
0	0	Yes	8-byte	No	N/A
0	1	Yes	16-byte	No	N/A
1	0	Yes	32-byte	No	N/A
1	1	Yes	64-byte	No	N/A

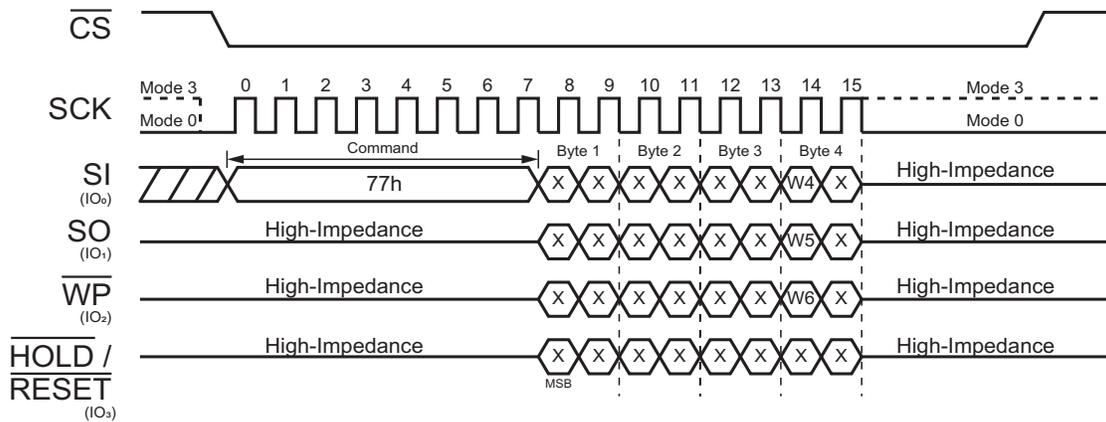


Figure 19: Set Burst with Wrap Command

The Set Burst with Wrap command sequence is:  $\overline{CS}$  goes low → Send Set Burst with Wrap command → Send 24 Dummy bits → Send 8 “Wrap bits” →  $\overline{CS}$  goes high.

If W6-4 is set by a Set Burst with Wrap command, all the following “Fast Read Quad I/O” and “Word Read Quad I/O” commands use the W6-4 setting to access the 8-, 16-, 32-, or 64-byte section within any page. To exit the “Wrap Around” function and return to normal read operation, issue another Set Burst with Wrap command to set W4=1. The default value of W4 at power-on is 1.

6.3 ID AND POWER COMMANDS

Three commands (9Fh/90h/ABh) are supported to access device identification that can indicate the manufacturer, device type, and capacity (density). The returned data bytes provide the information, as shown in Table 10.

Table 10: AT25EU0021A ID Definition Table

Command	Opcode	Mfg ID (Byte #1)	Device ID (Byte #2)	Device ID (Byte #3)
Read Manufacturing and Device ID	9Fh	1Fh	11h	01h
Read ID (Legacy Command)	90h	1Fh		11h
Read ID (Dual I/O)	92h	1Fh		11h
Read ID (Quad I/O)	94h	1Fh		11h
Resume from Deep Power-Down and Read Device ID	ABh			11h

2-Mbit, Ultra-Low Energy Serial Flash Memory

6.3.1 Release Power-down / Device ID (ABh)

The Release from Power-down / Device ID command is a multi-purpose command. It can be used to release the device from the power-down state, or obtain the devices electronic identification (ID) number.

To release the device from the power-down state, the command is issued by driving the  $\overline{CS}$  pin low, transferring the opcode ABh and driving  $\overline{CS}$  high, as shown in Figure 20. Release from power-down takes the time of  $t_{RES1}$  (see Section 7.6, AC Characteristics) before the device resumes normal operation and other commands are accepted. The CS pin must remain high during the  $t_{RES1}$  time.

When used only to obtain the Device ID while not in the power-down state, the command is initiated by driving the  $\overline{CS}$  pin low and transferring the opcode ABh, followed by three dummy bytes. The Device ID bits are then transferred out on the falling edge of SCK, with the most significant bit (MSB) first. The Device ID value for the AT25EU0021A is listed in Manufacturer and Device Identification table. The Device ID can be read continuously. The command is completed by driving  $\overline{CS}$  high.

When used to release the device from the power-down state and obtain the Device ID, the command is the same as previously described and shown in Figure 21, except that after  $\overline{CS}$  is driven high it must remain high for a time of  $t_{RES2}$  (see Section 7.6, AC Characteristics). After this time, the device resumes normal operation, and other commands are accepted. If the Release from Power-down / Device ID command is issued while an Erase, Program, or Write cycle is in process (when RDY/BSY = 1) the command is ignored and has no effect on the current cycle.

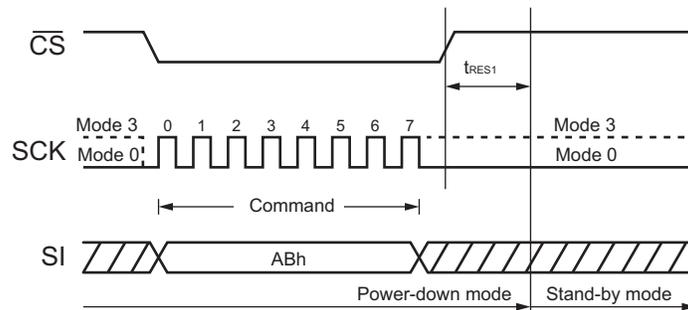


Figure 20: Release Power-Down Command

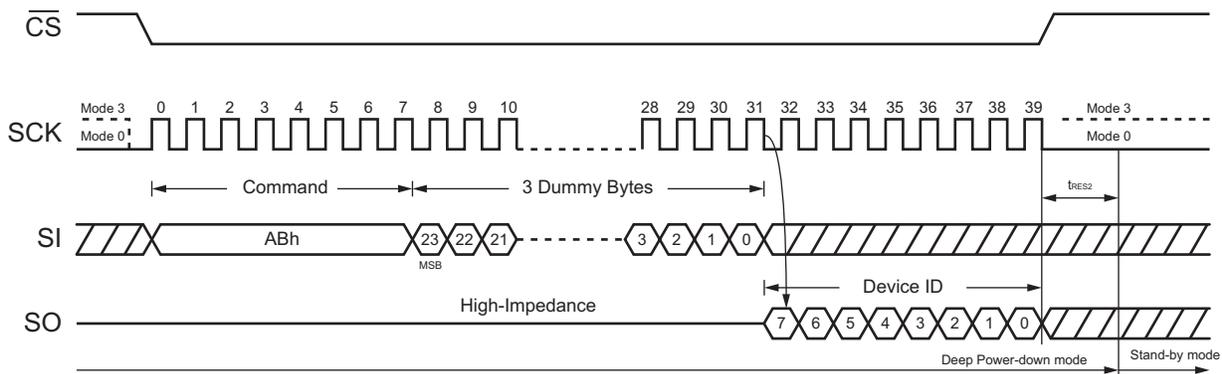


Figure 21: Release Power-Down / Device ID Command

6.3.2 Read Manufacturer / Device ID (90h)

The Read Manufacturer/Device ID command is an alternative to the Release from Power-down / Device ID command that provides both the JEDEC assigned manufacturer ID and the specific device ID.

The Read Manufacturer / Device ID command can operate at the highest possible frequency of  $f_C$  (see Section 7.6, AC Characteristics). The command is initiated by driving the  $\overline{CS}$  pin low and transferring the opcode 90h followed by a 24-bit address (A23-A0). After this, the Manufacturer ID for Dialog Semiconductor (1Fh) and the Device ID are transferred out on the falling edge of SCK, with most significant bit (MSB) first, as shown in Section 22, Read Manufacturer / Device ID Command. The Device ID values for the AT25EU0021A are listed in Manufacturer and Device Identification table. The address A23-A1 is an unrelated item and has no effect on the result of the command. If the A0 is initially set to 1, the Device ID is read first and then followed by the Manufacturer ID. If the A0 is initially set to 0 the Manufacturer ID is read first and then followed by the Device ID. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The command is completed by driving  $\overline{CS}$  high.

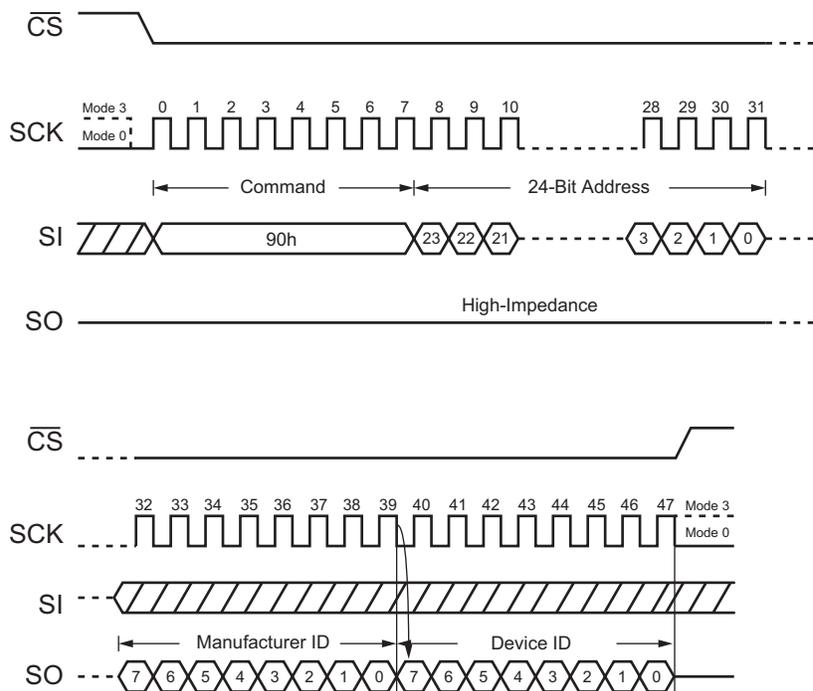


Figure 22: Read Manufacturer / Device ID Command

2-Mbit, Ultra-Low Energy Serial Flash Memory

6.3.3 Dual I/O Read Manufacture ID/ Device ID (92h)

The Dual I/O Read Manufacturer/Device ID instruction is an alternative to the Release from Power-Down/Device ID instruction that provides both the JEDEC-assigned Manufacturer ID and the specific Device ID by Dual I/O.

The instruction is initiated by driving the  $\overline{CS}$  pin low and shifting the instruction code 92h, followed by a 24-bit address (A23 - A0) of 000000h. If the 24-bit address is initially set to 000001h, the Device ID is read first.

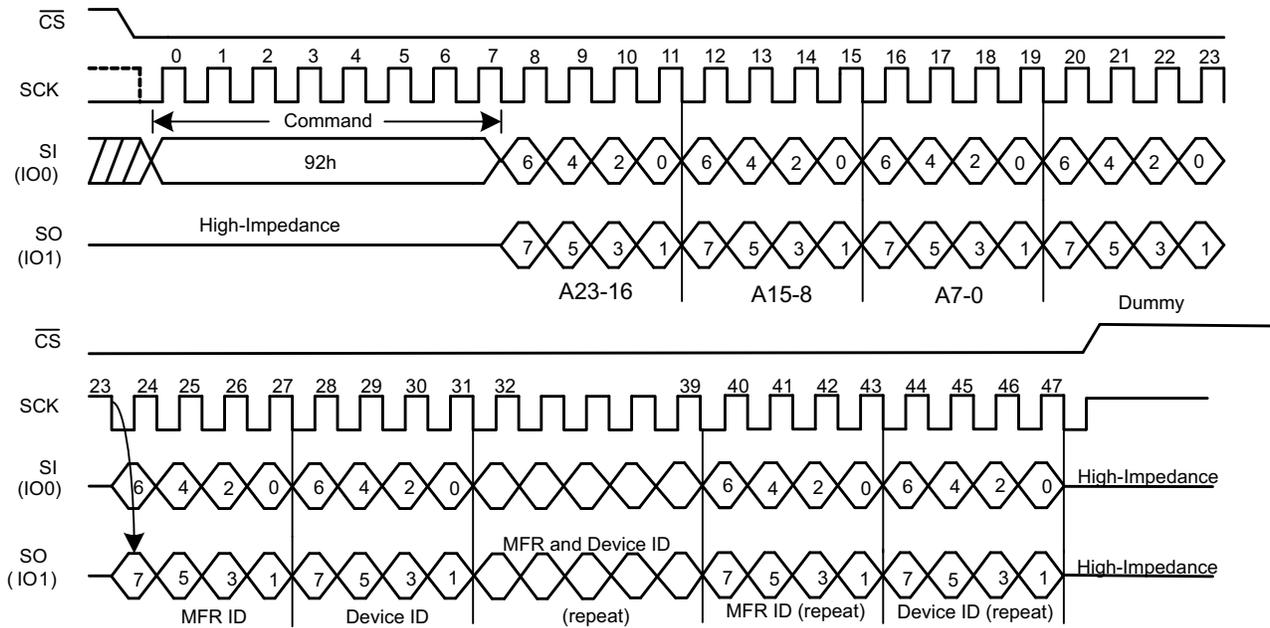


Figure 23: Dual I/O Read Manufacture ID/ Device ID Timing

2-Mbit, Ultra-Low Energy Serial Flash Memory

6.3.4 Quad I/O Read Manufacture ID / Device ID (94h)

The Quad I/O Read Manufacturer/Device ID instruction is an alternative to the Release from Power-Down/Device ID instruction that provides both the JEDEC assigned Manufacturer ID and the specific Device ID by quad I/O.

The instruction is initiated by driving the  $\overline{CS}$  pin low and shifting the instruction code 94h, followed by a 24-bit address (A23 - A0) of 000000h and four dummy clocks. If the 24-bit address is initially set to 000001h, the Device ID is read out first.

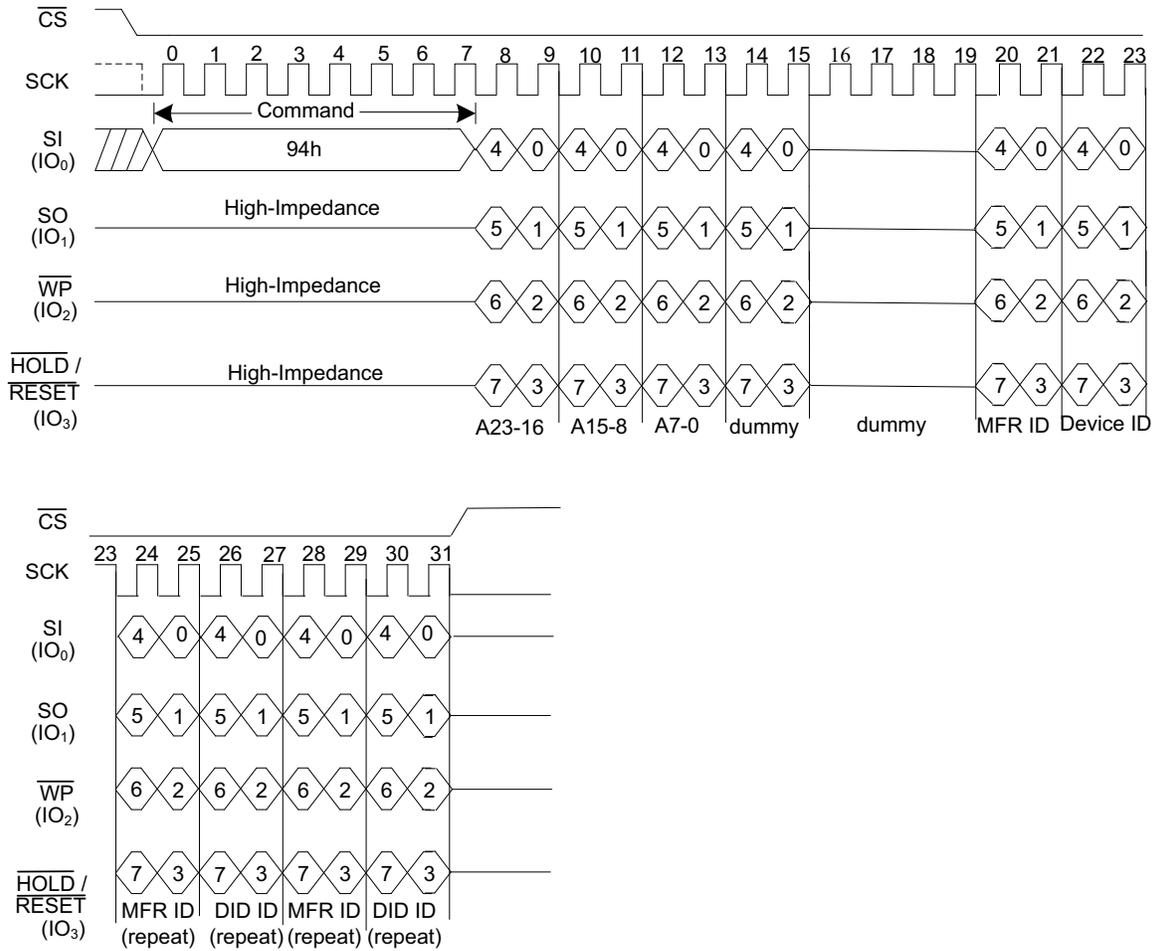


Figure 24: Quad I/O Read Manufacture ID / Device ID Sequence Diagram

2-Mbit, Ultra-Low Energy Serial Flash Memory

6.3.5 Read JEDEC ID (9Fh)

The Read JEDEC ID command can operate at the highest possible frequency of  $f_C$  (see Section 7.6, AC Characteristics). For compatibility reasons, the AT25EU0021A provides several commands to electronically determine the identity of the device. The Read JEDEC ID command is compatible with the JEDEC standard for SPI-compatible serial memories that was adopted in 2003. The command is initiated by driving the  $\overline{CS}$  pin low and transferring the opcode 9Fh. The JEDEC assigned Manufacturer ID byte for Dialog Semiconductor (1Fh) and two Device ID bytes are then transferred out on the falling edge of SCK, with the most significant bit (MSB) first (see Figure 25). For memory type and capacity values, see Table 10.

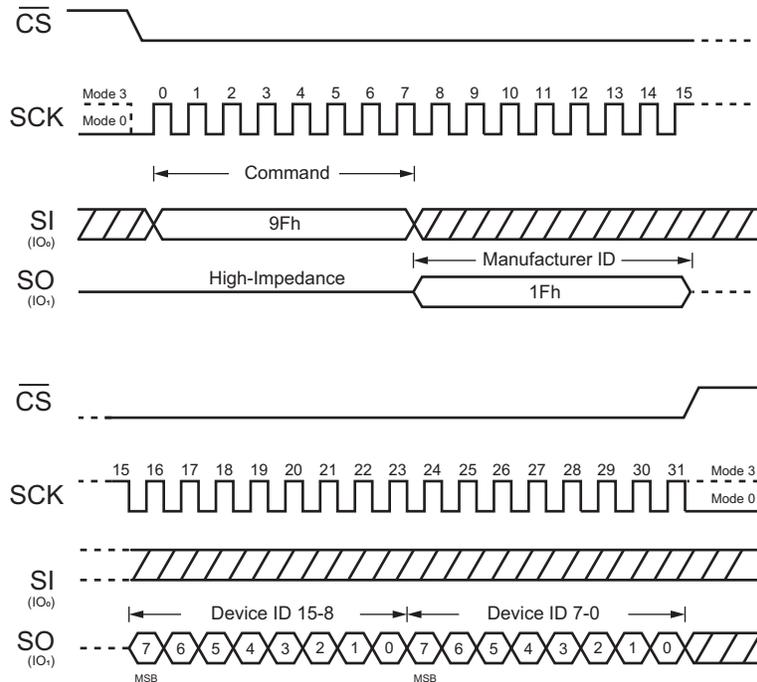


Figure 25: Read JEDEC ID Command

6.3.6 Read Unique ID Number (4Bh)

The Read Unique ID Number command can operate at the highest possible frequency of  $f_C$  (see Section 7.6, AC Characteristics). The Read Unique ID Number command accesses a factory-set, read-only, 128-bit number that is unique to each AT25EU-0021A device. The ID number can be used in conjunction with user software methods to help prevent copying or cloning of a system. The Read Unique ID command is initiated by driving the  $\overline{CS}$  pin low and transferring the opcode 4Bh, followed by four bytes of dummy clocks. After this, the 128-bit ID is transferred out on the falling edge of SCK, as shown in Figure 26.

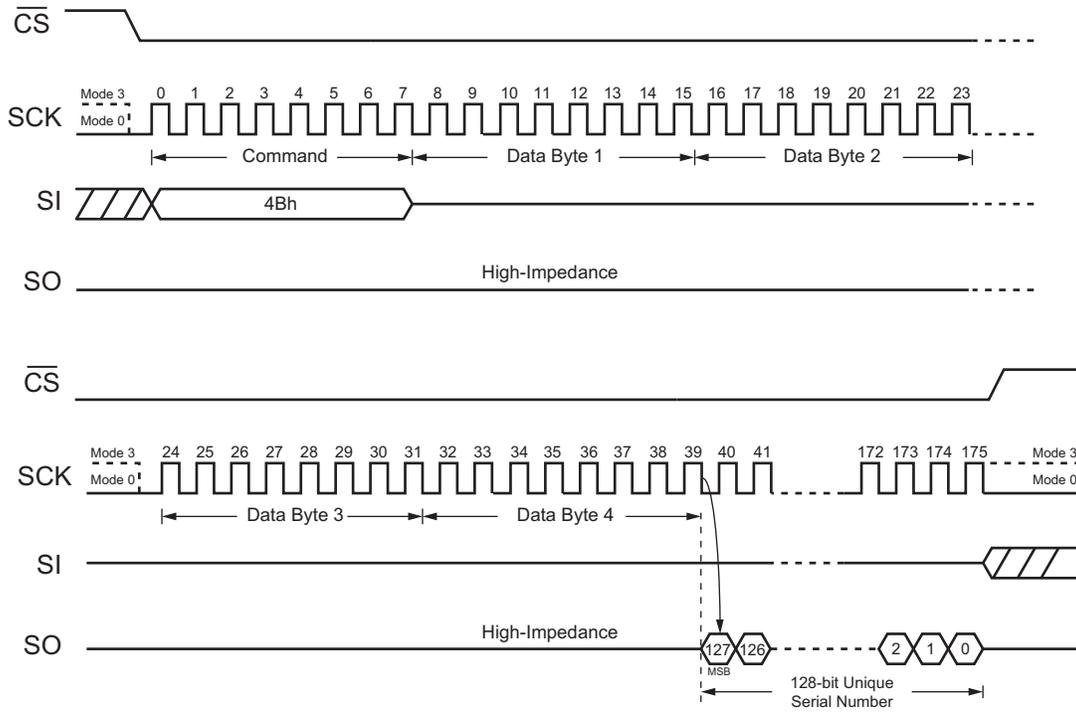


Figure 26: Read Unique ID Sequence Diagram

### 6.3.7 Deep Power-Down (B9h)

Although the standby current during normal operation is relatively low, it can be reduced further with the Power-down command. The lower power consumption makes the Power-down command especially useful for battery-powered applications (see ICC1 and ICC2 in [Section 7.4, DC Characteristics](#)). The command is initiated by driving the  $\overline{\text{CS}}$  pin low and transferring the opcode B9h, as shown in [Figure 27](#). The  $\overline{\text{CS}}$  pin must be driven high after the eighth bit has been latched. If this is not done, the Power-down command is not executed. After  $\overline{\text{CS}}$  is driven high, the power-down state is entered within the time of  $t_{\text{DP}}$  (see [Section 7.6, AC Characteristics](#)). While in the power-down state, only the Release Power-down / Device ID (ABh) command, which restores the device to normal operation, is recognized. All other commands are ignored. This includes the Read Status Register command, which is always available during normal operation. Ignoring all but one command makes the power-down state a useful condition for securing maximum write-protection. The device always powers-up in the normal operation with the standby current of ICC1

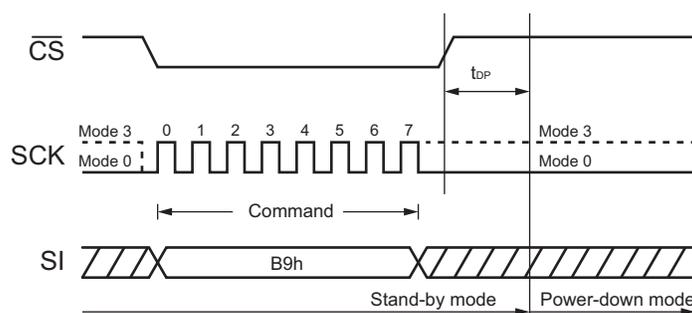


Figure 27: Deep Power-Down Command

6.4 PROGRAM / ERASE AND SECURITY COMMANDS

6.4.1 Page Program (02h)

The Page Program command allows from one to 256 bytes (a page) of data to be programmed at previously erased (FFh) memory locations. A Write Enable command must be executed before the device can accept the Page Program command (Status Register bit WEL= 1). The command is initiated by driving the CS pin low then transferring the opcode 02h, followed by a 24-bit address (A23-A0) and at least one data byte, onto the SI pin. The CS pin must be held low for the entire length of the command while data is being sent to the device. The Page Program command sequence is shown in Figure 28. If more than 256 bytes are sent to the device, previously latched data are discarded, and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page. CS must be driven high after the eighth bit of the last data byte has been latched in; otherwise, the Page Program command is not executed. As with the write and erase commands, the CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done, the Page Program command is not executed. After CS is driven high, the self-timed Page Program command commences for a time of  $t_{PP}$  (see Section 7.6, AC Characteristics). While the Page Program cycle is in progress, the Read Status Register command can be accessed for checking the status of the RDY/BSY bit. The RDY/BSY bit is a 1 during the Page Program cycle; it becomes a 0 when the cycle is finished and the device is ready to accept other commands. After the Page Program cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Page Program command is not executed if the addressed page is protected by the Block Protect (BP4, BP3, BP2, BP1, and BP0) bits.

**WARNING:** Programming a memory location that was not previously erased can result in corruption of the data and is not recommended. Data should be programmed only to erased locations.

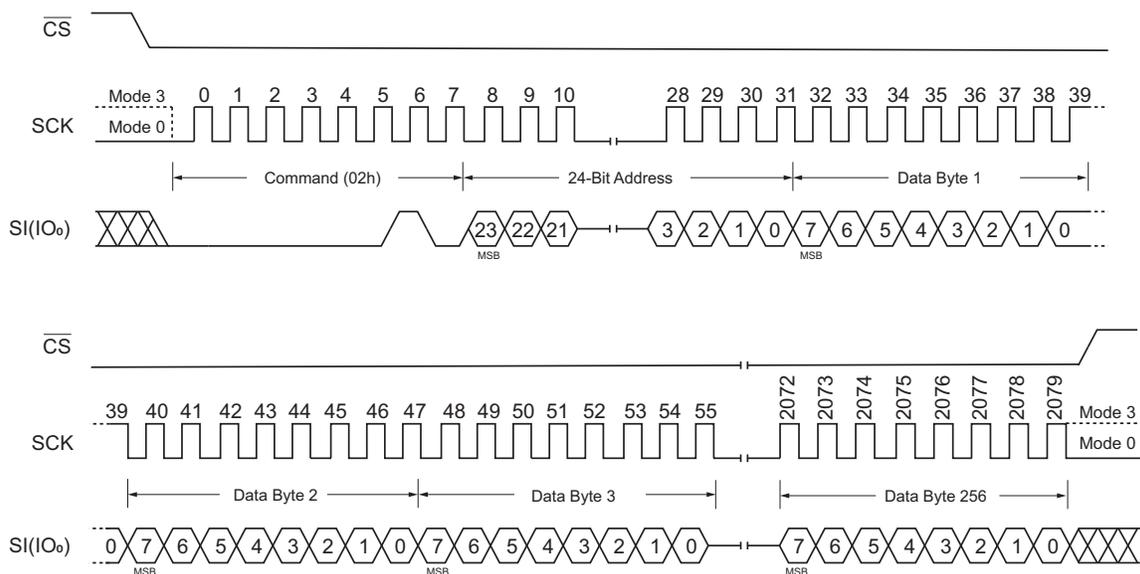


Figure 28: Page Program Command

2-Mbit, Ultra-Low Energy Serial Flash Memory

6.4.2 Dual Page Program (A2h)

This command allows up to 256 bytes of data to be programmed at previously erased (FFh) memory locations using the SI SO pins. The Dual Page Program can improve performance for PROM Programmer and applications that have slow clock speeds <5MHz. Systems with faster clock speed do not realize much benefit from this command since the inherent page program time is much longer than the time it takes to clock in the data.

A Write Enable command must be executed before the device can accept the Dual Page Program command (Status Register 1, WEL=1). The command is initiated by driving the CS pin low, then shifting the opcode A2h, followed by a 24-bit address (A23-A0) and at least one data byte, into the IO pins. The CS pin must be held low for the entire length of the command while data is being sent to the device. All other functions of Dual input Page Program are identical to standard Page Program.

**WARNING:** Programming a memory location that was not previously erased can result in corruption of the data and is not recommended. Data should be programmed only to erased locations.

The Dual Page Program instruction sequence is shown in Figure 29.

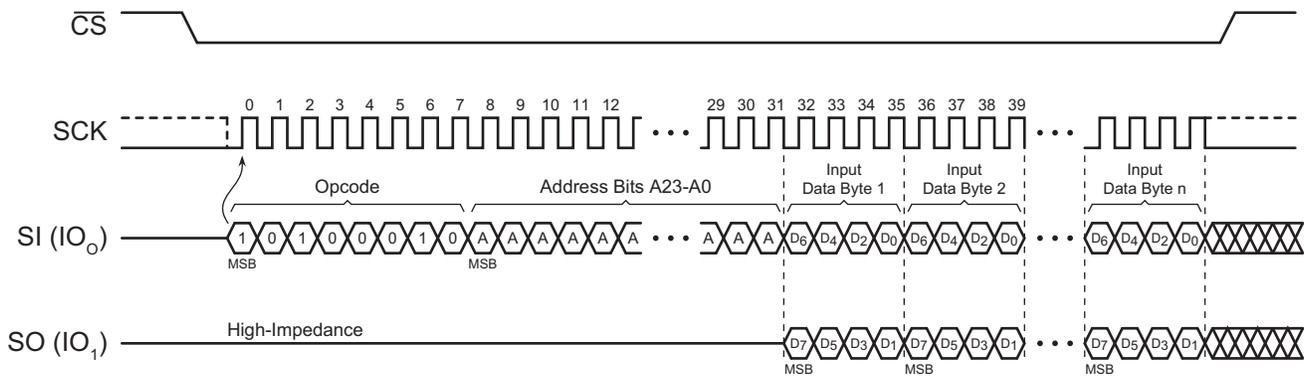


Figure 29: Dual Page Program Command

2-Mbit, Ultra-Low Energy Serial Flash Memory

6.4.3 Quad Page Program (32h)

The Quad Page Program command allows up to 256 bytes of data to be programmed at previously erased (FFh) memory locations using the SI, SO, WP, and HOLD pins. The Quad Page Program can improve performance for PROM Programmer and applications that have slow clock speeds <5 MHz. Systems with faster clock speed do not realize much benefit for the Quad Page Program command since the inherent page program time is much longer than the time it take to clock-in the data.

To use Quad Page Program, the Quad Enable (QE) bit in Status Register-2 must be set to 1. A Write Enable command must be executed before the device can accept the Quad Page Program command (Status Register-1, WEL=1). The command is initiated by driving the CS pin low, then shifting the opcode 32h, followed by a 24-bit address (A23-A0) and at least one data byte, into the IO pins. The CS pin must be held low for the entire length of the command while data is being sent to the device. All other functions of Quad Page Program are identical to standard Page Program.

**WARNING:** Programming a memory location that was not previously erased can result in corruption of the data and is not recommended. Data should be programmed only to erased locations.

The Quad Page Program command sequence is shown in Figure 30.

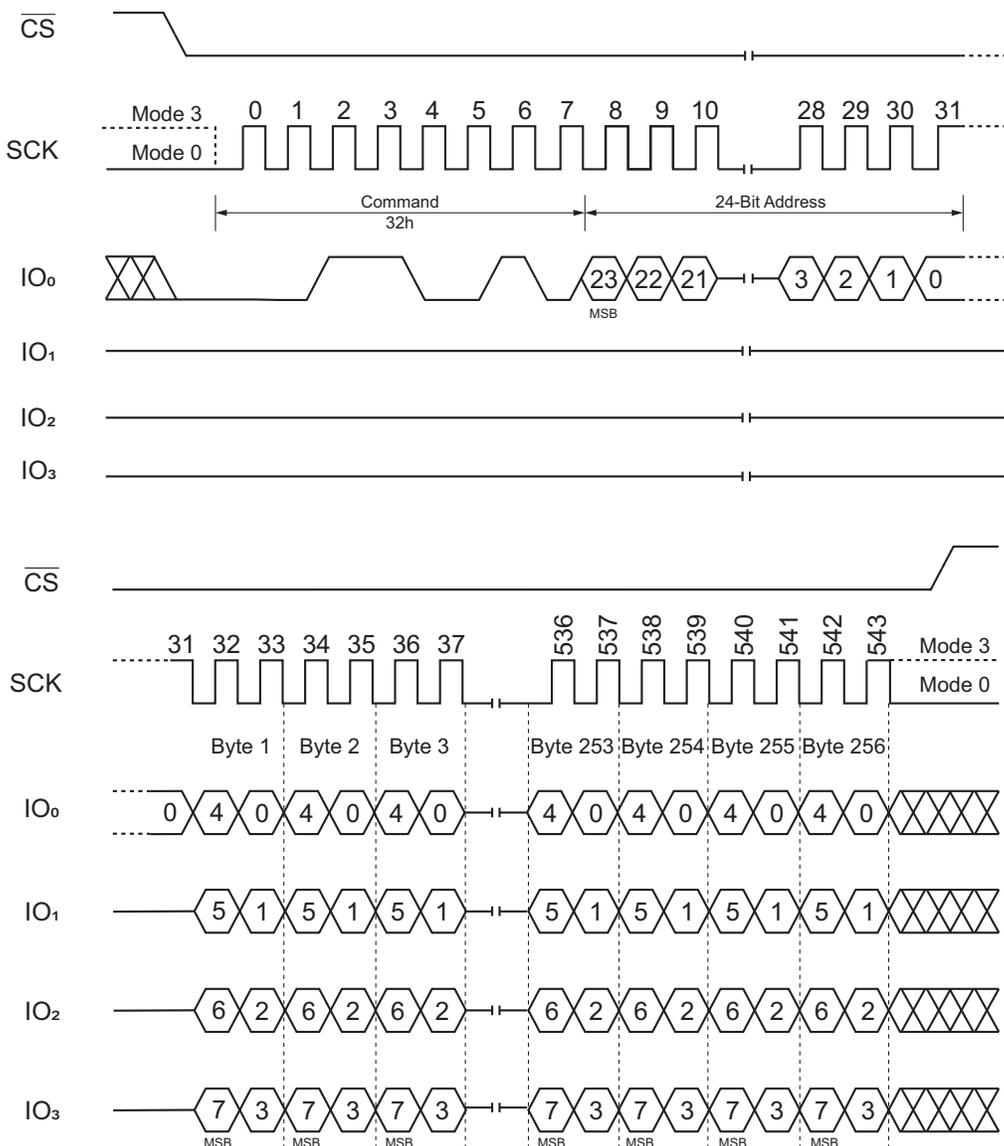


Figure 30: Quad Input Page Program Command

6.4.4 Page Erase (81h/DBh)

The Page Erase (PE) command erases the data of the chosen Page to be logical 1. A Write Enable (WREN) command must execute to set the Write Enable Latch (WEL) bit before sending the Page Erase (PE). To perform a Page Erase with the standard page size (256 bytes), clock the opcode 81h or DBh into the device, followed by three address bytes comprised of two page address bytes that specify the page in the main memory to be erased. The address A7-A0 is an unrelated item.

The sequence of issuing PE command is:  $\overline{CS}$  goes low → sending PE opcode → three-byte address on SI →  $\overline{CS}$  goes high.

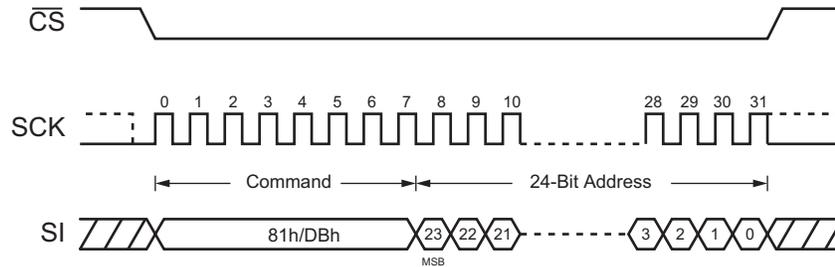


Figure 31: Page Erase Command

6.4.5 4 kB Block Erase (20h)

This command sets all memory within a specified block (4 kB) to the erased state of all 1s (FFh). A Write Enable command must be executed before the device can accept the 4 kB Block Erase command (Status Register bit WEL must equal 1). The command is initiated by driving the  $\overline{CS}$  pin low and transferring the opcode 20h, followed a 24-bit block address. The address A11-A0 is an unrelated item and has no effect on the result of the command. The 4 kB Block Erase command sequence is shown in Figure 32.

The  $\overline{CS}$  pin must be driven high after the eighth bit of the last byte has been latched. If this is not done, the 4 kB Block Erase command is not executed. After  $\overline{CS}$  is driven high, the self-timed 4 kB Block Erase command commences for a time of  $t_{SE}$  (see Section 7.6, AC Characteristics). While the Block Erase cycle is in progress, the Read Status command can still be accessed for checking the status of the RDY/BSY bit. The RDY/BSY bit is a 1 during the Block Erase cycle; it becomes a 0 when the cycle is finished and the device is ready to accept other commands. After the Block Erase cycle has finished, the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Block Erase command is not executed if the addressed page is protected by the Block Protect (BP4, BP3, BP2, BP1, and BP0) bits.

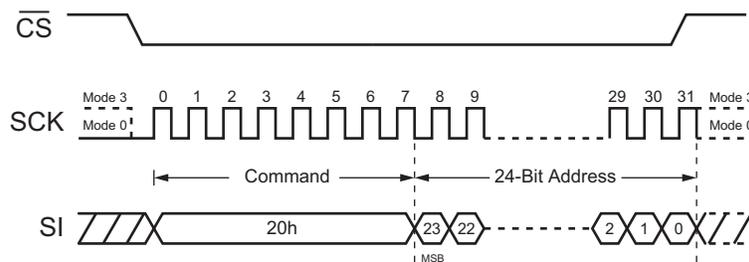


Figure 32: 4 kB Block Erase Command

## 2-Mbit, Ultra-Low Energy Serial Flash Memory

## 6.4.6 32 kB Block Erase (52h)

The 32 kB Block Erase command sets all memory within a specified block (32 kB) to the erased state of all 1s (FFh). A Write Enable command must be executed before the device can accept the 32 kB Block Erase command (Status Register bit WEL must equal 1). The command is initiated by driving the  $\overline{\text{CS}}$  pin low and transferring the opcode 52h followed a 24-bit block address (A23-A0). The address A14-A0 is an unrelated item and has no effect on the result of the command. The Block Erase command sequence is shown in Figure 33.

The  $\overline{\text{CS}}$  pin must be driven high after the eighth bit of the last byte has been latched. If this is not done, the 32 kB Block Erase command is not executed. After  $\overline{\text{CS}}$  is driven high, the self-timed 32 kB Block Erase command commences for a time duration of  $t_{\text{BE1}}$  (see Section 7.6, AC Characteristics). While the 32 kB Block Erase cycle is in progress, the Read Status Register command can still be accessed for checking the status of the RDY/BSY bit. The RDY/BSY bit is a 1 during the 32 kB Block Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other commands. After the 32 kB Block Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The 32 kB Block Erase command is not executed if the addressed page is protected by the Block Protect (BP4, BP3, BP2, BP1, and BP0) bits.

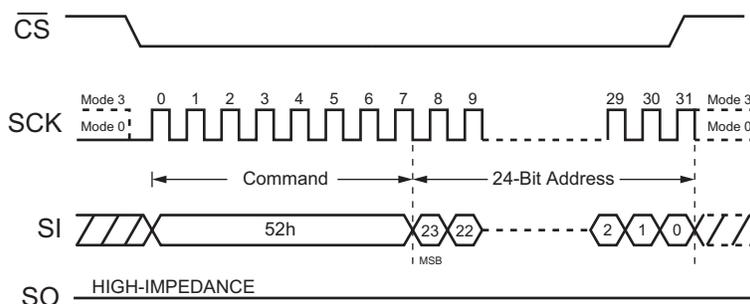


Figure 33: 32 kB Block Erase Command

## 2-Mbit, Ultra-Low Energy Serial Flash Memory

## 6.4.7 64 kB Block Erase (D8h)

The 64 kB Block Erase command sets all memory within a specified block (64K-bytes) to the erased state of all 1s (FFh). A Write Enable command must be executed before the device can accept the 64 kB Block Erase command (Status Register bit WEL must equal 1). The command is initiated by driving the  $\overline{\text{CS}}$  pin low and transferring the opcode D8h, followed a 24-bit block address (A23-A0). The address A15-A0 is an unrelated item and has no effect on the result of the command. The 64 kB Block Erase command sequence is shown in Figure 34.

The  $\overline{\text{CS}}$  pin must be driven high after the eighth bit of the last byte has been latched. If this is not done, the 64 kB Block Erase command is not executed. After  $\overline{\text{CS}}$  is driven high, the self-timed 64 kB Block Erase command commences for a time of  $t_{\text{BE2}}$  (see Section 7.6, AC Characteristics). While the 64 kB Block Erase cycle is in progress, the Read Status Register command can be accessed for checking the status of the RDY/BSY bit. The RDY/BSY bit is 1 during the 64 kB Block Erase cycle; it becomes a 0 when the cycle is finished and the device is ready to accept other commands. After the 64 kB Block Erase cycle has finished, the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The 64 kB Block Erase command is not executed if the addressed page is protected by the Block Protect (BP4, BP3, BP2, BP1, and BP0) bits.

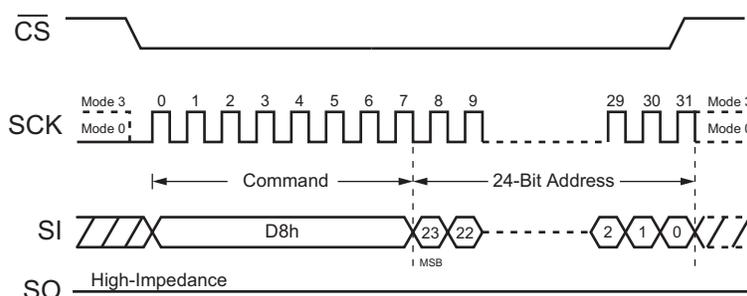


Figure 34: 64 kB Block Erase Command

## 2-Mbit, Ultra-Low Energy Serial Flash Memory

## 6.4.8 Chip Erase (C7h / 60h)

The Chip Erase command sets all memory within the device to the erased state of 1s (FFh). A Write Enable command must be executed before the device can accept the Chip Erase command (Status Register bit WEL must equal 1). The command is initiated by driving the  $\overline{\text{CS}}$  pin low and transferring the opcode C7h or 60h. The Chip Erase command sequence is shown in Figure 35.

The  $\overline{\text{CS}}$  pin must be driven high after the eighth bit has been latched. If this is not done, the Chip Erase command is not executed. After  $\overline{\text{CS}}$  is driven high, the self-timed Chip Erase command commences for a time of  $t_{\text{CE}}$  (see Section 7.6, AC Characteristics). While the Chip Erase cycle is in progress, the Read Status Register command can still be accessed to check the status of the RDY/BSY bit. The RDY/BSY bit = 1 during the Chip Erase cycle; it becomes a 0 when finished and the device is ready to accept other commands. After the Chip Erase cycle has finished, the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Chip Erase command is not executed if any memory region is protected by the Block Protect (BP4, BP3, BP2, BP1, and BP0) bits.

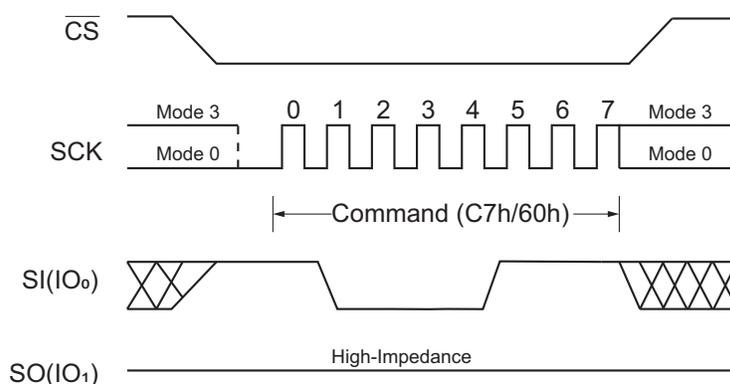


Figure 35: Chip Erase Command

## 6.4.9 Program/Erase Suspend (75h)

The Program/Erase Suspend command 75h allows the system to interrupt a Page Program or a Page/4K/32K/64K Block Erase operation and then read data from any other block. After the program or erase operation has entered the suspended state, the memory array can be read except for the page being programmed or the page/block being erased. And after the erase operation has entered the suspended state, the memory array can be programmed (except for the page/block being erased. Write status register operation cannot be suspended. The Erase/Program security registers operation cannot be suspended. The Program/Erase Suspend command sequence is shown in Figure 36.

Table 11: Readable Area of Memory While a Program or Erase Operation is Suspended

Suspended Operation	Readable Region Of Memory Array
Page Program	All but the Page being programmed.
Page Erase	All but the Page being Erased.
Block Erase(4 kB)	All but the 4 kB Block being Erased.
Block Erase(32 kB)	All but the 32 kB Block being Erased.
Block Erase(64 kB)	All but the 64 kB Block being Erased.

When the Serial NOR Flash receives the Suspend command, there is a latency of  $t_{\text{PSL}}$  or  $t_{\text{ESL}}$  before the Write Enable Latch (WEL) bit clears to 0 and the SUS sets to 1. After the latency, the device is ready to accept one of the commands listed in Table 8 (for example: FAST READ). See the Section 7.6, AC Characteristics for  $t_{\text{PSL}}$  and  $t_{\text{ESL}}$  timings. Table 13 lists the commands for which the  $t_{\text{PSL}}$  and  $t_{\text{ESL}}$  latencies do not apply. For example, 05h, 48h, 66h, and 99h can be issued at any time after the Suspend command. Status Register bit 15 (SUS) can be read to check the suspend status. The SUS sets to 1 when a program or erase command is suspended. The SUS clears to 0 when the program or erase command is resumed.

Table 12: Acceptable Commands During Program/Erase Suspend After  $t_{PSL}/t_{ESL}$  -

Command Name	Opcode	Suspend Type	
		Program	Erase
Read Data	03h	*	*
Fast Read	0Bh	*	*
Dual Output Fast Read	3Bh	*	*
Dual I/O Fast Read	BBh	*	*
Quad Output Fast Read	6Bh		
Quad I/O Fast Read	EBh		
Read SFDP	5Ah	*	*
Read JEDEC ID	9Fh	*	*
Mftr./Device ID	90h	*	*
Read Security Registers	48h	*	*
Set Burst with Wrap	77h	*	*
Write Enable	06h		*
Write Disable	04h	*	*
Program/Erase Resume	7Ah	*	*
Page Program	02h		*
Dual Page Program	A2h		*
Quad Page Program	32h		*
Release Power-Down/Device ID	ABh	*	*

Table 13: Acceptable Commands During Suspend ( $t_{PSL}/t_{ESL}$  Not Required)

Command Name	Opcode	Suspend Type	
		Program	Erase
Read Status Register-1	05H	*	*
Read Status Register-2	35H	*	*
Active Status Interrupt	25H	*	*
Enable Reset	66H	*	*
Reset Device	99H	*	*

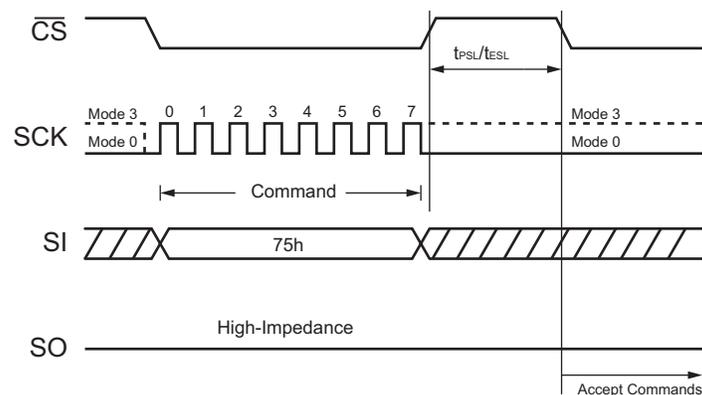


Figure 36: Program/Erase Suspend Command

6.4.10 Program/Erase Resume (7Ah)

The Program/Erase Resume command 7Ah must be written to resume the Program or Page/Block Erase operation after the Program/Erase Suspend. The Program/Erase Resume command 7Ah is accepted by the device only if the SUS bit in the Status Register is 1 and the RDY/BSY bit is 0. After the command is issued, the SUS bit is cleared from 1 to 0, the RDY/BSY bit is set from 0 to 1 within 200 ns, and the Page, or 4/32/64 kB block completes the program/erase operation. If the SUS bit is 0 or the RDY/BSY bit is 1, the Program/Erase Resume command 7Ah is ignored. The Program/Erase Resume command sequence is shown in Figure 37.

Program/Erase Resume command is ignored if the previous Program/Erase Suspend operation was interrupted by an unexpected power-off. It is required that a subsequent Program/Erase Suspend command not to be issued within a minimum of time of  $t_{SUS}$  following a previous Resume command.

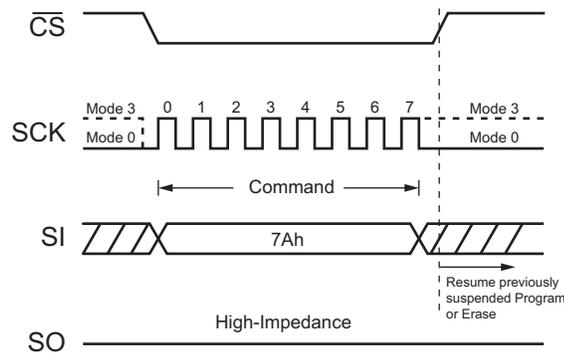


Figure 37: Program/Erase Resume Command

2-Mbit, Ultra-Low Energy Serial Flash Memory

6.4.11 Erase Security Registers (44h)

The AT25EU0021A offers three 512-byte Security Registers that can be erased and programmed individually. These registers can be used by the system manufacturers to store security and other important information separately from the main memory array.

The Erase Security Register command is similar to the 4 kB Block Erase command. A Write Enable command must be executed before the device can accept the Erase Security Register command (Status Register bit WEL must be 1). The command is initiated by driving the CS pin low and transferring the opcode 44h, followed by a 24-bit address (A23-A0).

Table 14: Erase Security Coding

Address	A23-16	A15-12	A11-9	A8-0
Security Register #1	00h	0 0 0 1	0 0 0	Don't Care
Security Register #2	00h	0 0 1 0	0 0 0	Don't Care
Security Register #3	00h	0 0 1 1	0 0 0	Don't Care

The Erase Security Register command sequence is shown in Figure 38. The  $\overline{CS}$  pin must be driven high after the eighth bit of the last byte has been latched. If this is not done, the command is not executed. After  $\overline{CS}$  is driven high, the self-timed Erase Security Register operation commences for a time of  $t_{SE}$  (see Section 7.6, AC Characteristics). While the Erase Security Register cycle is in progress, the Read Status Register command can be accessed for checking the status of the RDY/BSY bit. The RDY/BSY bit is a 1 during the erase cycle; it becomes a 0 when the cycle is finished and the device is ready to accept other commands. After the Erase Security Register cycle has finished, the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Security Register Lock Bits (LB3-1) in the Status Register-2 can be used to OTP protect the security registers. Once a lock bit is set to 1, the corresponding security register (LB3-1 corresponds to S13-11) is permanently locked, and the Erase Security Register command to that register is ignored (see Section 5 for details).

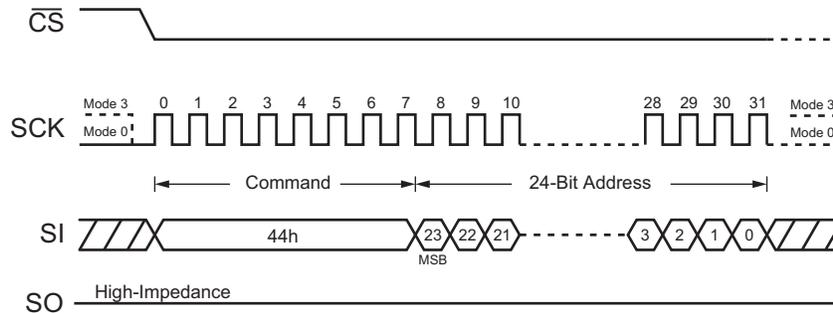


Figure 38: Erase Security Register Command

6.4.12 Program Security Registers (42h)

The Program Security Register command is similar to the Page Program command. It allows from one to 512 bytes of security register data to be programmed by two times (one time program 256 bytes) at previously erased (FFh) memory locations. A Write Enable command must be executed before the device can accept the Program Security Register command (Status Register bit WEL= 1). The command is initiated by driving the  $\overline{CS}$  pin low, then transferring the opcode 42h, followed by a 24-bit address (A23-A0) and at least one data byte, onto the SI pin. The  $\overline{CS}$  pin must be held low for the entire length of the command while data is being sent to the device.

Table 15: Program Security Register Coding

Address	A23-16	A15-12	A11-9	A8-0
Security Register #1	00h	0 0 0 1	0 0 0	Byte Address
Security Register #2	00h	0 0 1 0	0 0 0	Byte Address
Security Register #3	00h	0 0 1 1	0 0 0	Byte Address

The Program Security Register command sequence is shown in Figure 39. The Security Register Lock Bits (LB3-1) in the Status Register-2 can be used to OTP protect the security registers. Once a lock bit is set to 1, the corresponding security register is permanently locked, and the Program Security Register command to that register is ignored.

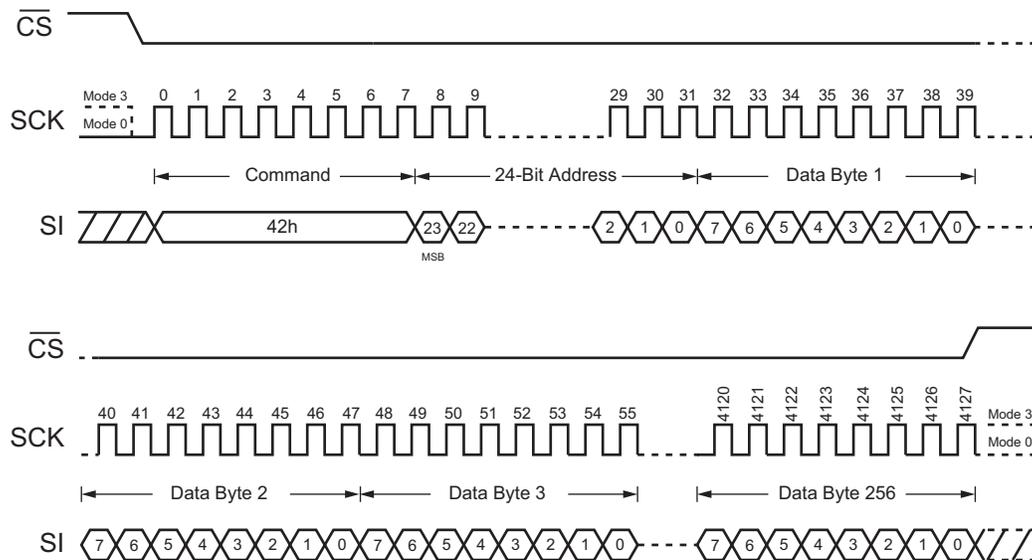


Figure 39: Program Security Register Command

6.4.13 Read Security Registers (48h)

The Read Security Register command is similar to the Fast Read command; it allows one or more data bytes to be sequentially read from one of the three security registers. The command is initiated by driving the CS pin low and then transferring the opcode 48h followed by a 24-bit address (A23-A0) and eight dummy clocks into the SI pin. The code and address bits are latched on the rising edge of the SCK pin. After the address is received, the data byte of the addressed memory location is transferred out on the SO pin at the falling edge of SCK, with the most significant bit (MSB) first. The byte address is automatically incremented to the next byte address after each byte of data is transferred out. Once the byte address reaches the last byte of the register (byte address FFh), it resets to address 00h, the first byte of the register, and continue to increment. The command is completed by driving CS high. The Read Security Register command sequence is shown in Figure 40. If a Read Security Register command is issued while an Erase, Program, or Write cycle is in progress (RDY/BSY=1), the command is ignored and does not have any effect on the current cycle. The Read Security Register command allows a clock frequency up to the maximum of  $f_C$  (see Section 7.6, AC Characteristics).

Table 16: Read Security Register Coding

Address	A23-16	A15-12	A11-9	A8-0
Security Register #1	00h	0 0 0 1	0 0 0	Byte Address
Security Register #2	00h	0 0 1 0	0 0 0	Byte Address
Security Register #3	00h	0 0 1 1	0 0 0	Byte Address

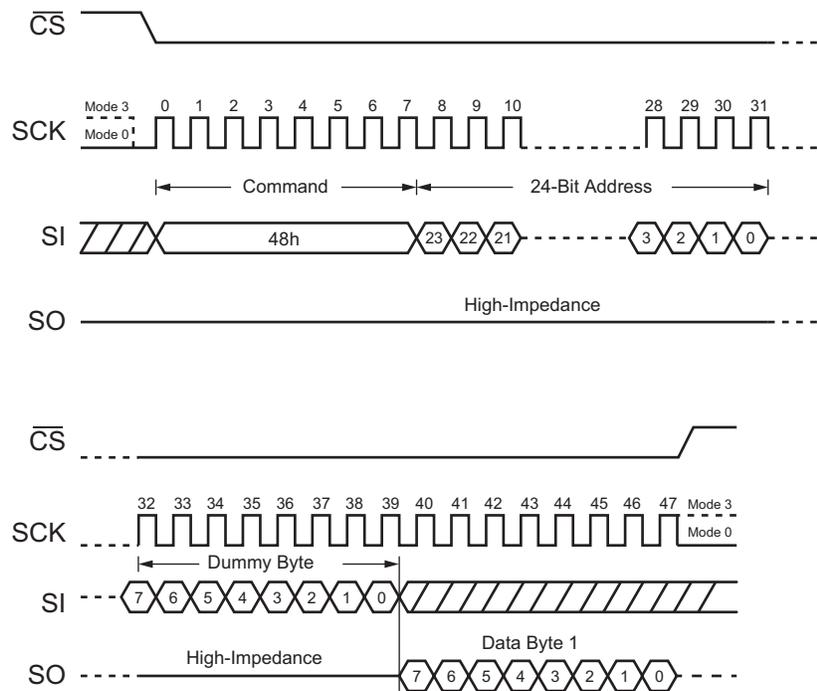


Figure 40: Read Security Command

6.4.14 Enable Reset (66h) and Reset Device (99h)

The AT25EU0021A provides a software Reset command. Once the Reset command is accepted, any on-going internal operations are terminated, and the device returns to its default power-on state; it then also loses all the current volatile settings, such as Volatile Status Register bits, Write Enable Latch (WEL) status, Program/Erase Suspend status, Continuous Read Mode bit setting (M7-M0), Wrap Bit setting (W6-W4). To avoid accidental reset, both commands must be issued in sequence. Any commands other than Reset (99h) after the Enable Reset (66h) command disables the Reset Enable state, and a new sequence of Enable Reset (66h) and Reset (99h) is needed to reset the device. Once the Reset command is accepted by the device, the device takes  $t_{RST}$  to reset. During this period, no command is accepted. Data corruption can happen if there is an on-going or suspended internal Erase or Program operation when the Reset command sequence is accepted by the device. Check the RDY/BSY bit and the SUS bit in the Status Register before issuing the Reset command sequence.

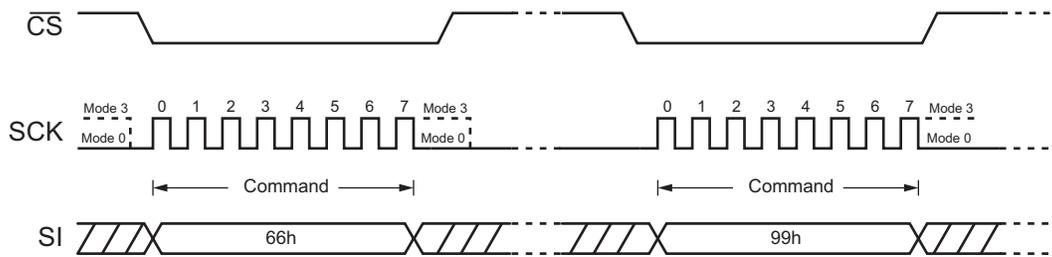


Figure 41: Enable Reset and Reset Command Sequence

6.4.15 Read Serial Flash Discoverable Parameter (5Ah)

The Serial Flash Discoverable Parameter (SFDP) standard provides a consistent method of describing the functional and feature capabilities of serial flash devices in a standard set of internal parameter tables. These parameter tables can be interrogated by host system software to enable adjustments needed to accommodate divergent features from multiple vendors. The concept is similar to the one found in the Introduction of JEDEC Standard JESD68 on CFI. SFDP is based on JEDEC Standard JESD216B. The SFDP is a special order. Contact Dialog Semiconductor.

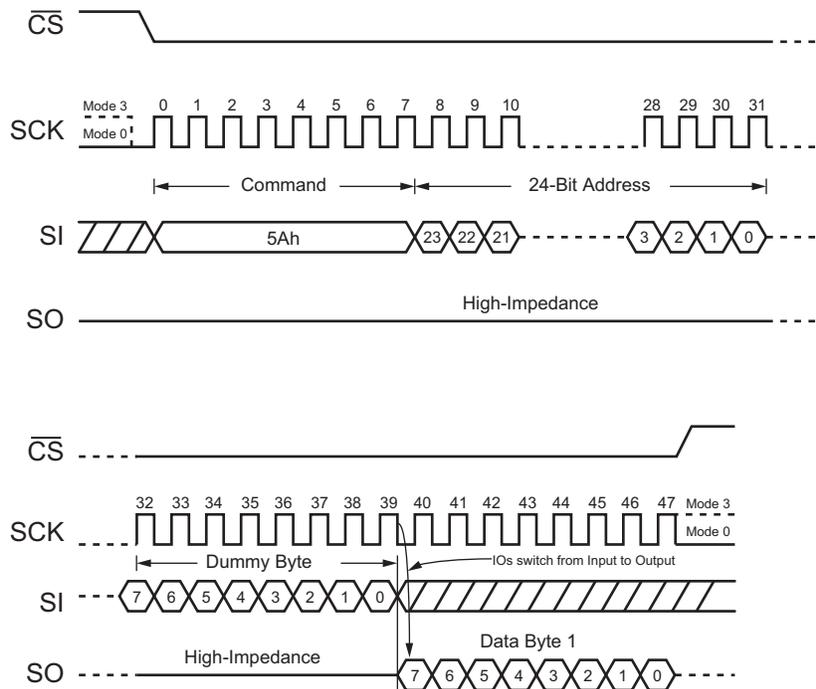


Figure 42: Read Serial Flash Discoverable Parameter Command

## 7 Electrical Characteristics

### 7.1 ABSOLUTE MAXIMUM RATINGS

This device has been designed and tested for the specified operation ranges. Proper operation outside of these levels is not guaranteed. Exposure to absolute maximum ratings can affect device reliability. Exposure beyond absolute maximum ratings can cause permanent damage.

**Table 17: Absolute Maximum Ratings**

Parameter	Symbol	Conditions	Range	Unit
Supply Voltage	$V_{CC}$		-0.6 to $V_{CC}+0.6$	V
Voltage Applied to Any Pin	$V_{IO}$	Relative to Ground	-0.6 to $V_{CC}+0.6$	V
Transient Voltage on any Pin	$V_{IOT}$	<20 ns Transient Relative to Ground	-1.0 V to $V_{CC}+1.0$ V	V
Storage Temperature	$T_{STG}$		-65 to +150	°C
Lead Temperature	$T_{LEAD}$		See Note 2	°C
Electrostatic Discharge Voltage	$V_{ESD}$	Human Body Model(3)	-2000 to +2000	V

**Notes:**

- This device has been designed and tested for the specified operation ranges. Proper operation outside of these levels is not guaranteed. Exposure to absolute maximum ratings can affect device reliability. Exposure beyond absolute maximum ratings can cause permanent damage.
- Compliant with JEDEC Standard J-STD-20C for small-body Sn-Pb or Pb-free (Green) assembly and the European directive on restrictions on hazardous substances (RoHS) 2002/95/EU.
- JEDEC Std JESD22-A114A (C1 = 100 pF, R1 = 1500  $\Omega$ , R2 = 500  $\Omega$ ).

### 7.2 OPERATING RANGES

**Table 18: Operating Ranges**

Parameter	Symbol	Conditions	Min	Max	Unit
Supply Voltage	VCC	$f_C = 85$ MHz, $F_R = 33$ MHz	1.65	3.6	V
Operating Temperature	TA	Industrial	-40	85	°C

7.3 POWER-UP / POWER-DOWN TIMING AND REQUIREMENTS

The parameters in the following table are characterized only.

Table 19: Timing Requirements for Power-Up/Down

Parameter	Symbol	Min	Max	Unit
VCC (min) to CS Low	$t_{VSL}$	300		$\mu s$
Write Inhibit Threshold Voltage	$V_{WI}$	1.0	1.4	V

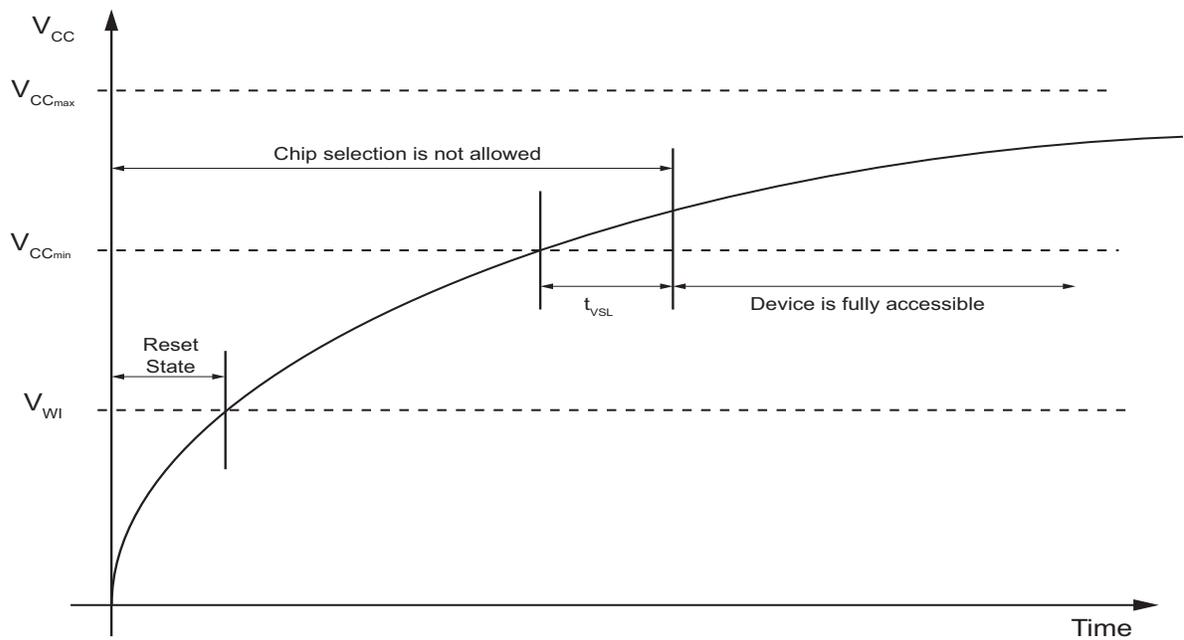


Figure 43: Power-Up Timing and Voltage Levels

## 2-Mbit, Ultra-Low Energy Serial Flash Memory

## 7.4 DC CHARACTERISTICS

Table 20: DC Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Capacitance <sup>1</sup>	C <sub>IN</sub>	V <sub>IN</sub> = 0 V 1			6	pF
Output Capacitance <sup>1</sup>	C <sub>OUT</sub>	V <sub>OUT</sub> = 0 V 1			8	pF
Input Leakage	I <sub>LI</sub>	All inputs at CMOS level			±2	μA
Output Leakage	I <sub>LO</sub>	All inputs at CMOS level			±2	μA
Standby Current	ICC1	CS = VCC, V <sub>IN</sub> = GND or VCC		10	14.5	μA
Power-Down Current	ICC2	CS = VCC, V <sub>IN</sub> = GND or VCC		0.1	1.8	μA
Normal Read Current (03h)	ICC3	F = 1 MHz; I <sub>OUT</sub> = 0 mA		0.8	1.3	mA
		F = 33 MHz; I <sub>OUT</sub> = 0 mA		1.0	2.0	mA
Read Current (0Bh)	ICC4	F = 50 MHz; I <sub>OUT</sub> = 0 mA		1.1	2.3	mA
		F = 85 MHz; I <sub>OUT</sub> = 0 mA		1.5	3.0	mA
Program Current	ICC5	CS = VCC RDY/BSY = 1		1.5	3.0	mA
Erase Current	ICC6	CS = VCC RDY/BSY = 1		1.5	3.0	mA
Input Low Voltage	V <sub>IL</sub>				VCC x 0.2	V
Input High Voltage	V <sub>IH</sub>		VCC x 0.8			V
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 100 μA			0.2	V
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -100 μA	VCC - 0.2			V

1. Tested on sample basis and specified through design and characterization data. TA = 25° C, VCC = 1.8 V.

## 7.5 AC MEASUREMENT CONDITIONS

Table 21: AC Measurement Conditions

Parameter	Symbol	Min	Max	Unit
Input Capacitance	C <sub>IN</sub>		6	pF
Output Capacitance	C <sub>OUT</sub>		6	pF
Load Capacitance	C <sub>L</sub>		30	pF
Input Rise and Fall Times	T <sub>R</sub> , T <sub>F</sub>		5	ns
Input Pulse Voltages	V <sub>IN</sub>	0.2 VCC - 0.8 VCC		V
Input Timing Reference Voltages	IN	0.5 VCC - 0.5 VCC		V
Output Timing Reference Voltages	OUT	0.5 VCC - 0.5 VCC		V

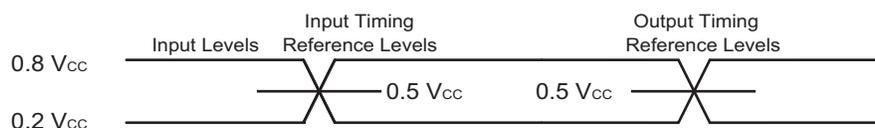


Figure 44: AC Measurement I/O Waveform

## 2-Mbit, Ultra-Low Energy Serial Flash Memory

## 7.6 AC CHARACTERISTICS

Table 22: AC Electrical Characteristics

Parameter	Symbol	ALT	Min	Typ	Max	Unit
Maximum clock frequency for all opcodes except 03h, 6Bh, and EBh	$f_C$	$f_{C1}$			85	MHz
Maximum Clock Frequency for opcodes 6Bh and EBh					70	MHz
Maximum Clock Frequency for 03h	$f_R$				33	MHz
Clock High, Low Time	$t_{CLH}, t_{CLL}$ <sup>1</sup>		5.5			ns
Clock Rise Time peak to peak	$t_{CLCH}$ <sup>2</sup>		0.1			V/ns
Clock Fall Time peak to peak	$t_{CHCL}$ <sup>2</sup>		0.1			V/ns
CS Active Setup Time relative to CLK	$t_{SLCH}$	$t_{CSS}$	5			ns
CS Not Active Hold Time relative to CLK	$t_{CHSL}$		5			ns
Data In Setup Time	$t_{DVCH}$	$t_{DSU}$	2			ns
Data In Hold Time	$t_{CHDX}$	$t_{DH}$	3			ns
Output Disable Time	$t_{SHQZ}$ <sup>2</sup>	$t_{DIS}$			6	ns
CS Active Hold Time relative to CLK	$t_{CHSH}$	$t_{CSS}$	5			ns
CS Not Active Setup Time relative to CLK	$t_{SHCH}$		5			ns
Clock Low to Output Valid	$t_{CLQV1}$	$t_{V1}$			7	ns
CS Deselect Time from read to next Read	$t_{SHSL}$	$t_{CSH}$	15			ns
CS Deselect Time from Write, Erase, Program to Read Status Register			30			ns
Clock Low to Output Valid loading 30pF	$t_{CLQV}$	$t_V$			7.5	ns
Clock Low to Output Valid loading 15pF					6.5	ns
Output Hold Time	$t_{CLQX}$	$t_{HO}$	0			ns
HOLD Active Setup Time relative to CLK	$t_{HLCH}$ <sup>2</sup>		5			ns
HOLD Active Hold Time relative to CLK	$t_{CHHH}$ <sup>2</sup>		5			ns
HOLD Not Active Setup Time relative to CLK	$t_{HHCH}$ <sup>2</sup>		5			ns
HOLD Not Active Hold Time relative to CLK	$t_{CHHL}$ <sup>2</sup>		5			ns
HOLD to Output Low-Z	$t_{HHQX}$ <sup>2</sup>	$t_{LZ}$			6	ns
HOLD to Output High-Z	$t_{HLQZ}$ <sup>2</sup>	$t_{HZ}$			6	ns
Write Protect Setup Time Before CS Low	$t_{WHSL}$ <sup>3</sup>		20			ns
Write Protect Hold Time After CS High	$t_{SHWL}$ <sup>3</sup>		100			ns
CS High to Deep Power-down Mode	$t_{DP}$ <sup>2</sup>				3	$\mu$ s
CS High to Standby Mode without ID Read	$t_{RES1}$ <sup>2</sup>				8	$\mu$ s
CS High to Standby Mode with ID Read	$t_{RES2}$ <sup>2</sup>				8	$\mu$ s
CS High to next command after Reset	$t_{RST}$ <sup>2</sup>		300			$\mu$ s
Write Status Register Cycle Time	$t_W$			6.5	12	ms
Byte Program Time	$t_{BP1}$			2	3	ms
Erase Suspend Latency	$t_{ESL}$				20	$\mu$ s
Program Suspend Latency	$t_{PSL}$				20	$\mu$ s
Latency between Program Resume and next Suspend	$t_{PRS}$		20			$\mu$ s
Latency between Erase Resume and next Suspend	$t_{ERS}$		20			$\mu$ s
Page Program Time	$t_{PP}$			2	3	ms
Page Erase Time	$t_{PE}$			8	12	ms
Block Erase Time (4 kB)	$t_{BLKE-4kB}$			8	12	ms

Table 22: AC Electrical Characteristics (Continued)

Parameter	Symbol	ALT	Min	Typ	Max	Unit
Block Erase Time (32 kB)	$t_{BLKE-32kB}$			8	12	ms
Block Erase Time (64 kB)	$t_{BLKE-64kB}$			8	12	ms
Chip Erase Time	$t_{CE}$			8	12	ms

1. Clock high + clock low must be less than, or equal to, 1/fC.
2. Value guaranteed by design and/or characterization; not 100% tested in production.
3. Only applicable as a constraint for a write Status Register command when SRP[1:0] = (0,1).

7.7 SERIAL OUTPUT TIMING

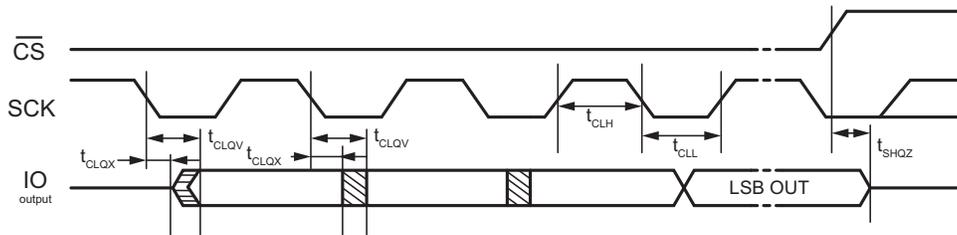


Figure 45: Serial Output Timing

7.8 SERIAL INPUT TIMING

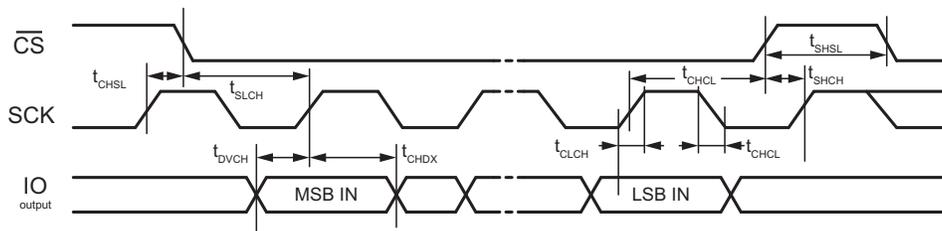


Figure 46: Serial Input Timing

7.9 HOLD TIMING

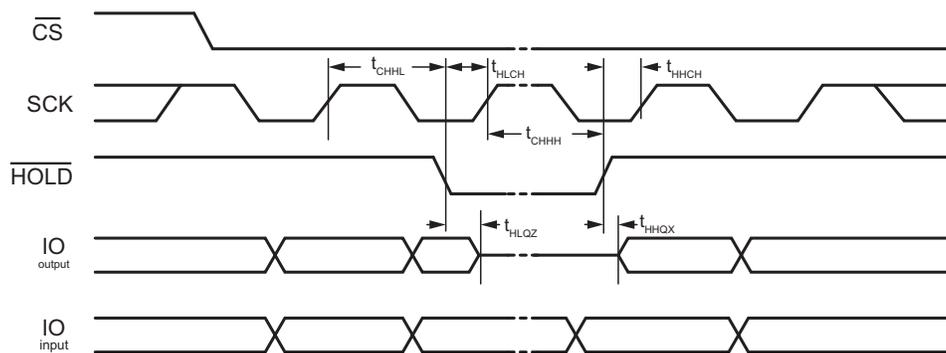


Figure 47: HOLD Timing

7.10  $\overline{WP}$  TIMING

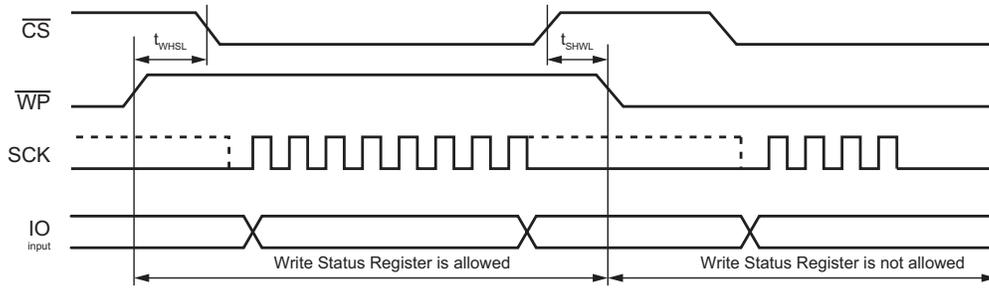
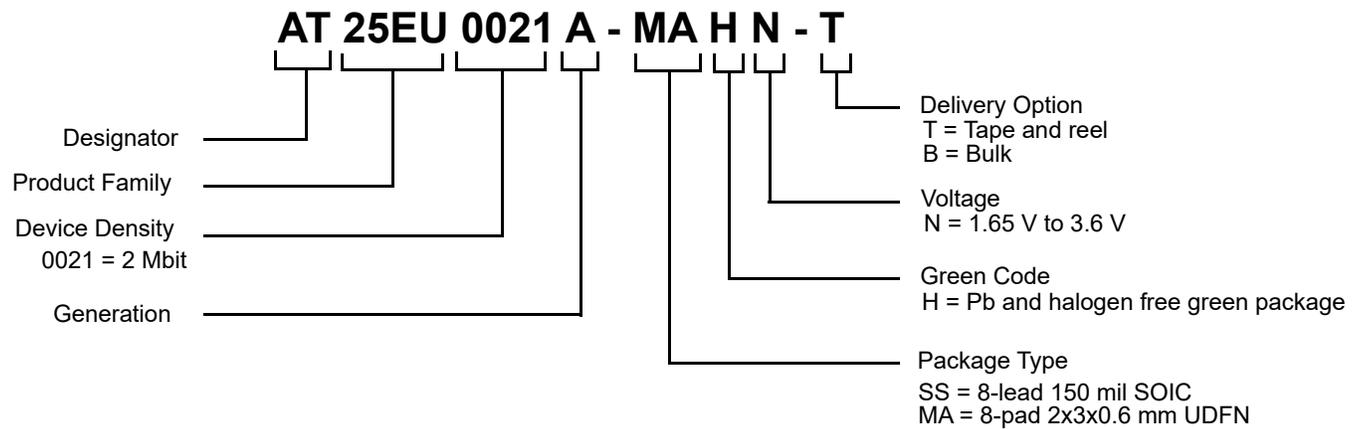


Figure 48:  $\overline{WP}$  Timing

## 8 Ordering Information



**Table 23: Ordering Codes**

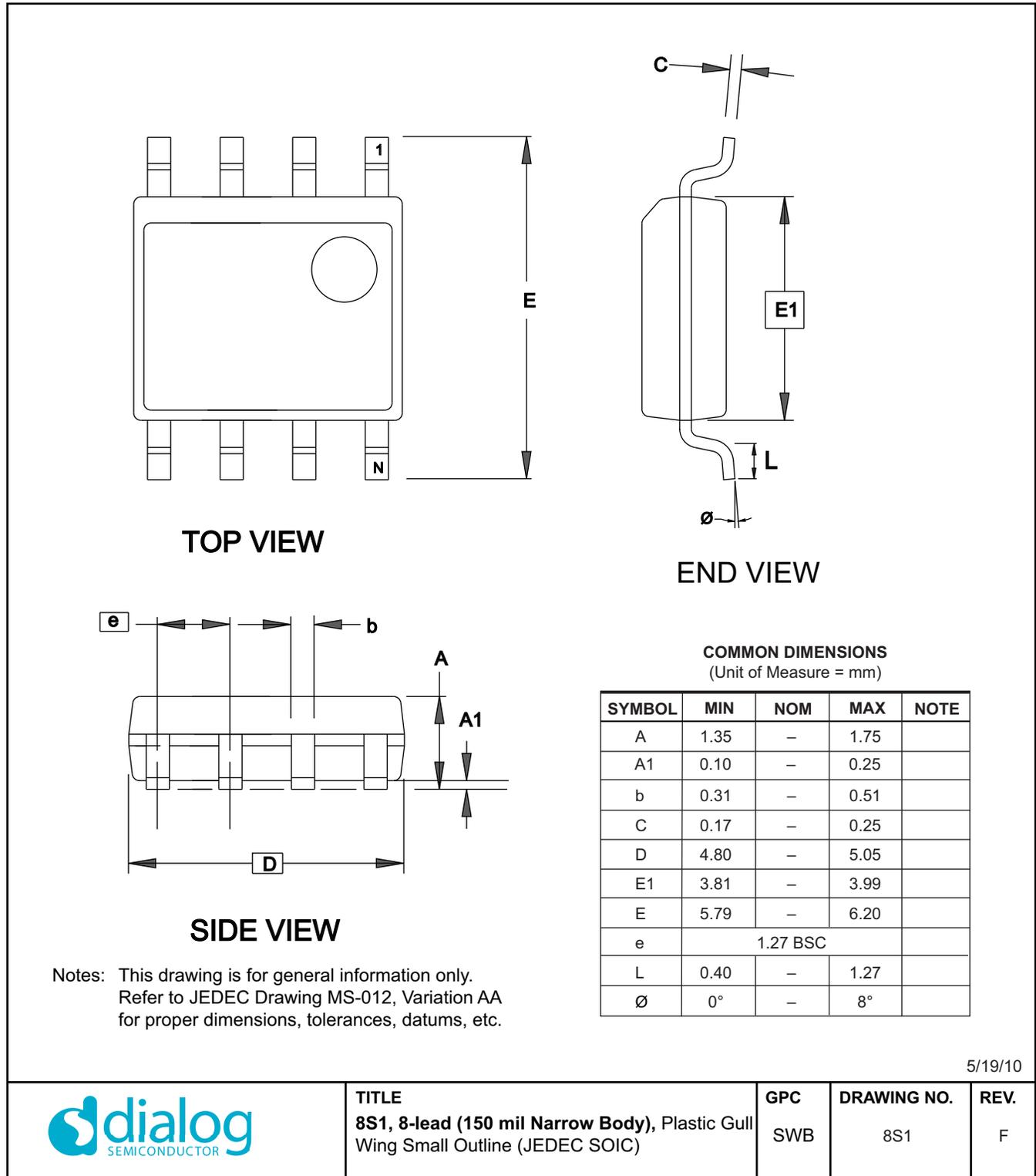
Ordering Code	Package	Lead Finish	Operating Voltage	Delivery Option
AT25EU0021A-SSHN-T	8-lead SOIC (150 mil)	Pb and Halogen Free	1.65 V - 3.6 V	Tape and Reel
AT25EU0021A-SSHN-B				Bulk
AT25EU0021A-MAHN-T	8-pad 2x3x0.6 mm UDFN			Tape and Reel

**Table 24: Package Types**

Designation	Description
8S1	8-lead, 150 mil Narrow, Plastic Gull Wing Small Outline Package (JEDEC SOIC)
8MA3	8-pad, 2x3x0.6 mm, Thermally Enhanced Plastic Ultra Thin Dual Flat No Lead Package (UDFN)

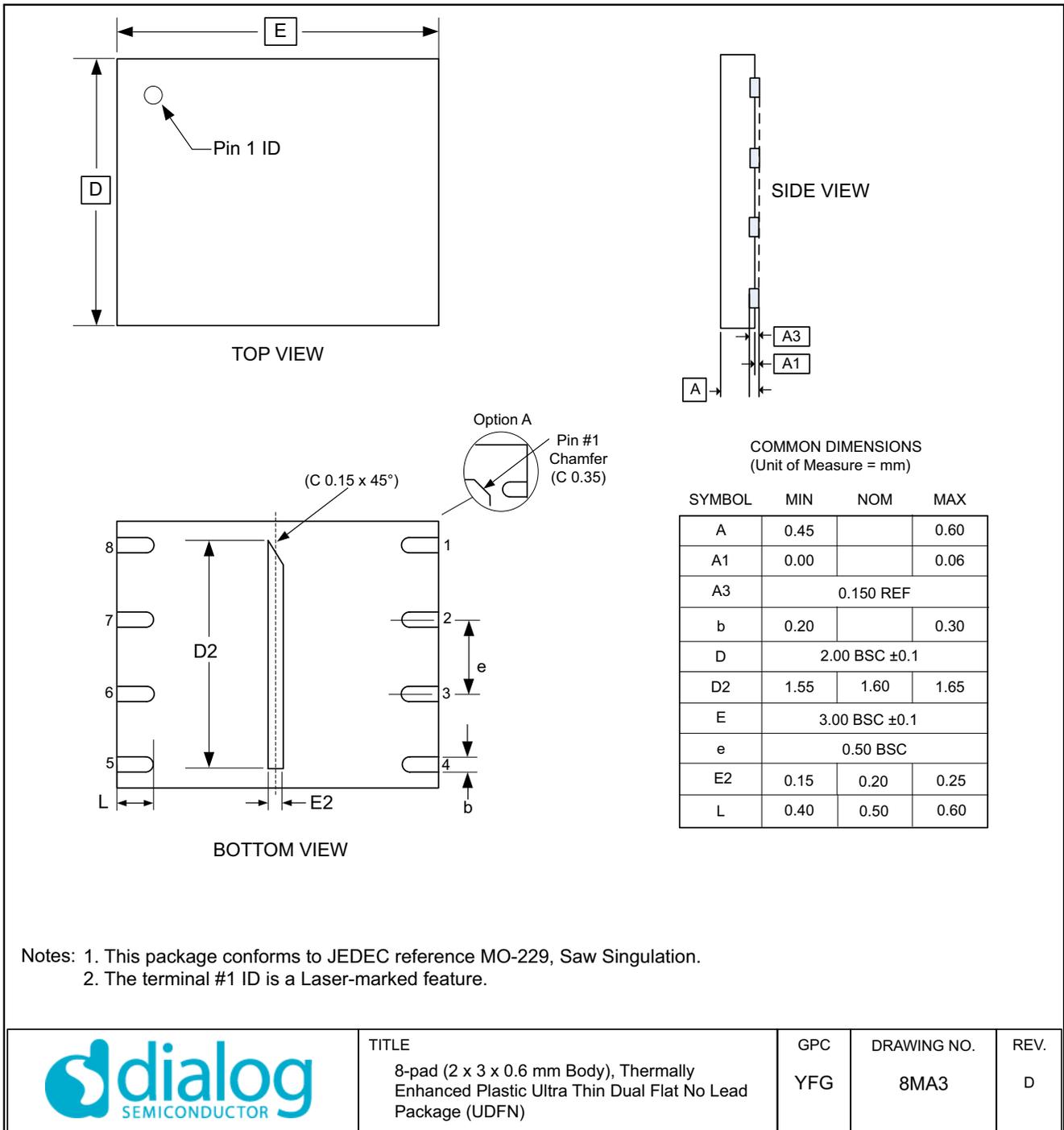
## 9 Packaging Information

### 9.1 EIGHT-PIN SOIC 150-MIL



2-Mbit, Ultra-Low Energy Serial Flash Memory

9.2 EIGHT-PAD 2 X 3 X 0.6 MM UDFN



## Revision History

Revision	Date	Description
A	02-2021	Initial release.
B	04-2021	<p>Added descriptions for following commands: 3Bh, BBh, 6Bh, EBh, and 77h.</p> <p>Changed active read current from 1 mA to 1.2 mA.</p> <p>Changed data retention from 10 to 20 years.</p> <p>Changed UDFN size from 6x5 to 2x3.</p> <p>Changed WIP bit name to RDY/BSY bit.</p> <p>Combined the Status Register information (section 5) into three tables.</p> <p>Added description of commands 92h and 94h.</p> <p>Corrected or expanded entries to Tables 10, 19, and 23.</p> <p>Made additions to Figure 1.</p> <p>Corrected units in Section 4.1.1.</p>
C	07-2021	<p>Removed "Advanced" and inserted "Preliminary."</p> <p>Added Sections 4.1 and 4.2.</p> <p>Corrected the definition of the QE bit in Table 3.</p> <p>Added information for opcodes A2h and 32h in Table 8.</p> <p>Added descriptions for opcodes A2h and 32h in Sections 6.4.2 and 6.4.3, respectively.</p> <p>Completed the command names in Table 12.</p> <p>Updated values in Tables 19 and 20, as well as Section 8.6.</p>
D	11-2021	<p>Updated package drawing for 2x3 UDFN (Section 9.2)</p> <p>Updated the values in Section 7.4 (DC Electrical Characteristics).</p> <p>Updated the values in Section 7.6 (AC Characteristics).</p> <p>Added feature supports to the SPI list for dual and quad operations.</p> <p>Removed "Preliminary" designation from datasheet.</p> <p>Added a warning to Sections 6.4.1, 6.4.2, and 6.4.3.</p>

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