Product Change Notification / SYST-23QFBP679

Date:

24-Feb-2022

Product Category:

8-bit Microcontrollers

PCN Type:

Document Change

Notification Subject:

ERRATA - AVR32DA28/32/48 Silicon Errata and Data Sheet Clarification Document Revision

Affected CPNs:

SYST-23QFBP679_Affected_CPN_02242022.pdf
SYST-23QFBP679_Affected_CPN_02242022.csv

Notification Text:

SYST-23QFBP679

Microchip has released a new Product Documents for the AVR32DA28/32/48 Silicon Errata and Data Sheet Clarification of devices. If you are using one of these devices please read the document located at AVR32DA28/32/48 Silicon Errata and Data Sheet Clarification.

Notification Status: Final

Description of Change:
1) Added data sheet clarifications:
   - 3.1. Features
   - 3.2. FUSE - Configuration and User Fuses
   - 3.5. Electrical Characteristics - Peripheral Power Consumption
   - 3.6. Electrical Characteristics - Memory Programming Specifications
   - 3.7. Electrical Characteristics - VREF
   - 3.8. Electrical Characteristics - DAC
   - 3.9. Electrical Characteristics - ADC
2) Updated data sheet clarifications:
   - 3.3. RSTCTRL - Reset Controller
   - 3.4. TWI - Two-Wire Interface

Impacts to Data Sheet: None

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 24 Feb 2022

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Attachments:

AVR32DA28/32/48 Silicon Errata and Data Sheet Clarification

Please contact your local Microchip sales office with questions or concerns regarding this notification.

Terms and Conditions:

If you wish to receive Microchip PCNs via email please register for our PCN email service at our PCN home page select register then fill in the required fields. You will find instructions about registering for Microchips PCN email service in the PCN FAQ section.

If you wish to change your PCN profile, including opt out, please go to the PCN home page select login and sign into your myMicrochip account. Select a profile option from the left navigation bar and make the applicable selections.

Affected Catalog Part Numbers (CPN)

AVR32DA28-E/SO
AVR32DA28-E/SP
AVR32DA28-E/SS
AVR32DA28-I/SO
AVR32DA28-I/SP
AVR32DA28-I/SS
AVR32DA28-I/SSVAO
AVR32DA28T-E/SO
AVR32DA28T-E/SS
AVR32DA28T-I/SO
AVR32DA28T-I/SS
AVR32DA28T-I/SSVAO
AVR32DA32-E/PT
AVR32DA32-E/PTVAO
AVR32DA32-E/RXB
AVR32DA32-E/RXBVAO
AVR32DA32-I/PT
AVR32DA32-I/RXB
AVR32DA32T-E/PT
AVR32DA32T-E/RXB
AVR32DA32T-E/RXBVAO
AVR32DA32T-I/PT
AVR32DA32T-I/RXB
AVR32DA48-E/6LX
AVR32DA48-E/6LXVAO
AVR32DA48-E/PT
AVR32DA48-E/PTVAO
AVR32DA48-I/6LX
AVR32DA48-I/PT
AVR32DA48T-E/6LX
AVR32DA48T-E/6LXV01
AVR32DA48T-E/6LXVAO
AVR32DA48T-E/PT
AVR32DA48T-E/PTVAO
AVR32DA48T-I/6LX
AVR32DA48T-I/PT

AVR32DA28/32/48

AVR32DA Silicon Errata and Data Sheet Clarification

The AVR32DA28/32/48 devices you have received conform functionally to the current device data sheet (www.microchip.com/DS40002228), except for the anomalies described in this document. The errata described in this document will likely be addressed in future revisions of the AVR32DA28/32/48 devices.

Notes:

- This document summarizes all the silicon errata issues from all the silicon revisions, previous as well as current
- Refer to the Device/Revision ID section in the current device data sheet (www.microchip.com/DS40002228) for more detailed information on Device Identification and Revision IDs for your specific device, or contact your local Microchip sales office for assistance

Table of Contents

1. Silicon Issue Summary

Legend

- **-** Erratum is not applicable.
- **X** Erratum is applicable.

Peripheral	Short Description	Valid for Silicon Revision	
		Rev. A3(1)	Rev. A4
Device	2.2.1. Some Reserved Fuse Bits Are '1'	X	-
	2.2.2. CRC Check During Reset Initialization Is not Functional	X	X
CCL	2.3.1. The LINK Input Source Selection for LUT3 Is not Functional on 28- and 32-Pin Devices	X	X
CLKCTRL	2.4.1. PLL Status not Working as Expected	X	X
DAC	2.5.1. DAC Output Buffer Lifetime Drift	X	X
NVMCTRL	2.6.1. Flash Multi-Page Erase Can Erase Write Protected Section	X	X
PORT	2.7.1. Digital Input on Pin Automatically Disabled When Pin Selected for Analog Input	X	X
RSTCTRL	2.8.1. BOD Registers not Reset When UPDI Is Enabled	X	X
TCA	2.9.1. Restart Will Reset Counter Direction in NORMAL and FRQ Mode	X	X
TCB	2.10.1. CCMP and CNT Registers Operate as 16-Bit Registers in 8-Bit PWM Mode	X	X
TCD	2.11.1. Asynchronous Input Events not Working When TCD Counter Prescaler Is Used	X	X
	2.11.2. CMPAEN Controls All WOx for Alternative Pin Functions	X	X
	2.11.3. Halting TCD and Wait for SW Restart Does Not Work if Compare Value A is 0 or Dual Slope Mode is Used	X	X
TWI	2.12.1. The Output Pin Override Does not Function as Expected	X	X
	2.12.2. Flush Non-Functional	X	X
USART	2.13.1. Open-Drain Mode Does not Work When TXD Is Configured as Output	X	X
	2.13.2. Start-of-Frame Detection Can Unintentionally Be Triggered in Active Mode	X	X
ZCD	2.14.1. All ZCD Output Selection Bits Are Tied to the ZCD0 Bit	X	X

Note:

1. This revision is the initial release of the silicon.

2. Silicon Errata Issues

2.1 Errata Details

-	Erratum is not applicable.
X	Erratum is applicable.

2.2 Device

2.2.1 Some Reserved Fuse Bits Are '1'

For material with date code 2033 (manufactured in the year 2020, week 33) or older, the default fuse values are not compliant with the data sheet. The fuse values will read out as listed below:

- BODCFG = `0x10`
- OSCCFG = `0x78` (The device will use the OSCHF clock source)
- SYSCFG0 = `0xF2`
- SYSCFG1 = `0xF8`

Work Around
None.

Affected Silicon Revisions

Rev. A3	Rev. A4
X	-

2.2.2 CRC Check During Reset Initialization Is not Functional

For material with date code 2136 (manufactured in the year 2021, week 36) or older, the CRCSRC bit field in the SYSCFG0 fuse is ignored during Reset initialization. A CRC check will not be performed during Reset initialization. CRCSCAN is only available from the software.

Work Around
None.

Affected Silicon Revisions

Rev. A3	Rev. A4
X	X

2.3 CCL - Configurable Custom Logic

2.3.1 The LINK Input Source Selection for LUT3 Is not Functional on 28- and 32-Pin Devices

The LINK option (INSELn in LUT3CTRLB or LUT3CTRLC is '`0x2`') does not work; the output from LUT0 will not get connected as an input to LUT3. This occurs only on 28-pin and 32-pin devices.

Work Around
Connect LUT0 output to LUT3 input using the Event System.

Affected Silicon Revisions

Rev. A3	Rev. A4
X	X

2.4 CLKCTRL - Clock Controller

2.4.1 PLL Status not Working as Expected

The PLL Status (PLLS) bit in the Main Clock Status (MCLKSTATUS) register will never be set to '1' if the Run Standby (RUNSTDBY) bit in PLL Control A (PLLCTRLA) register is set to '1' and no peripherals are requesting the PLL oscillator.

Work Around

None.

Affected Silicon Revisions

Rev. A3	Rev. A4
X	X

2.5 DAC - Digital-to-Analog Converter

2.5.1 DAC Output Buffer Lifetime Drift

The offset of the DAC output buffer can drift over lifetime if the device is powered with the DAC output buffer disabled.

Work Around

Keep the DAC output buffer enabled (OUTEN in DACn.CTRLA is '1') continuously or compensate by measuring the DAC output voltage offset with the ADC and adjust the DAC data register value (DATA[9:0] in DACn.DATA) accordingly.

Affected Silicon Revisions

Rev. A3	Rev. A4
X	X

2.6 NVMCTRL - Nonvolatile Memory Controller

2.6.1 Flash Multi-Page Erase Can Erase Write Protected Section

When using Flash Multi-Page Erase mode, only the first page in the selected address range is verified to be within a section that is not write-protected. If the address range includes any write-protected Application Data pages, it will erase them.

Work Around

None.

Affected Silicon Revisions

Rev. A3	Rev. A4
X	X

2.7 PORT - I/O Configuration

2.7.1 Digital Input on Pin Automatically Disabled When Pin Selected for Analog Input

If an input pin is selected to be analog input, the digital input function for those pins is automatically disabled.

Work Around
None

Affected Silicon Revisions

Rev. A3	Rev. A4
X	X

2.8 RSTCTRL - Reset Controller

2.8.1 BOD Registers not Reset When UPDI Is Enabled

If the UPDI is enabled, the VLMCTRL, INTCTRL, and INTFLAGS registers in BOD will not be reset by other reset sources than POR.

Work Around
None

Affected Silicon Revisions

Rev. A3	Rev. A4
X	X

2.9 TCA - 16-Bit Timer/Counter Type A

2.9.1 Restart Will Reset Counter Direction in NORMAL and FRQ Mode

When the TCA is configured to a NORMAL or FRQ mode (WGMODE in TCAn.CTRLB is '0x0' or '0x1'), a RESTART command or Restart event will reset the count direction to default. The default is counting upwards.

Work Around
None.

Affected Silicon Revisions

Rev. A3	Rev. A4
X	X

2.10 TCB - 16-Bit Timer/Counter Type B

2.10.1 CCMP and CNT Registers Operate as 16-Bit Registers in 8-Bit PWM Mode

When the TCB is operating in 8-bit PWM mode (CNTMODE in TCBn.CTRLB is '0x7'), the low and high bytes for the CNT and CCMP registers operate as 16-bit registers for read and write. They cannot be read or written independently.

Work Around
Use 16-bit register access. Refer to the data sheet for further information.

Affected Silicon Revisions

Rev. A3	Rev. A4
X	X

2.11 TCD - 12-Bit Timer/Counter Type D

2.11.1 Asynchronous Input Events not Working When TCD Counter Prescaler Is Used

When configuring TCD to use asynchronous input events (CFG in TCDn.EVCTRLx is '0x2') and the TCD Counter Prescaler (CNTPRES in TCDn.CTRLA) is different from '0x0', events can be missed.

Work Around
Use the TCD Synchronization Prescaler (SYNCPRES in TCDn.CTRLA) instead of the TCD Counter Prescaler. Alternatively, use synchronous input events (CFG in TCDn.EVCTRLx is not '0x2') if the input events are longer than one CLK_TCD_CNT cycle.

Affected Silicon Revisions

Rev. A3	Rev. A4
X	X

2.11.2 CMPAEN Controls All WOx for Alternative Pin Functions

When TCD alternative pins are enabled (TCD0 in PORTMUX.TCDROUTEA is not '0x0'), all waveform outputs (WOx) are controlled by Compare A Enable (CMPAEN in TCDn.FAULTCTRL).

Work Around
None.

Affected Silicon Revisions

Rev. A3	Rev. A4
X	X

2.11.3 Halting TCD and Wait for SW Restart Does Not Work if Compare Value A is 0 or Dual Slope Mode is Used

Halting TCD and wait for software restart (INPUTMODE in TCDn.INPUTCTRLA is '0x7') does not work if compare value A is 0 (CMPASET in TCDn.CMPASET is '0x0') or Dual Slope mode is used (WGMODE in TCDn.CTRLB is '0x3').

Work Around
Configure the compare value A (CMPASET in TCDn.CMPASET) to be different from 0 and do not use Dual Slope mode (WGMODE in TCDn.CTRLB is not '0x3').

Affected Silicon Revisions

Rev. A3	Rev. A4
X	X

2.12 TWI - Two-Wire Interface

2.12.1 The Output Pin Override Does not Function as Expected

When TWI is enabled, it overrides the output pin driver, but not the output value. The output on the line will always be high when the value in the PORTx.OUT register is '1' for the pins corresponding to the SDA or SCL.

Work Around
Ensure that the values in the PORTx.OUT register corresponding to the SCL and SDA pins are '0' before enabling the TWI.

Affected Silicon Revisions

Rev. A3	Rev. A4
X	X

2.12.2 Flush Non-Functional

Issuing a Flush by writing to the FLUSH bit in TWIn.MCTRLB can cause the TWI Host to be stuck in Unknown bus state (see BUSSTATE in TWIn.MSTATUS).

Work Around
Disable and re-enable the Host using the ENABLE bit in TWIn.MCTRLA. A normal operation does not require the use of FLUSH.

Affected Silicon Revisions

Rev. A3	Rev. A4
X	X

2.13 USART - Universal Synchronous and Asynchronous Receiver and Transmitter

2.13.1 Open-Drain Mode Does not Work When TXD Is Configured as Output

When configured as an output, the USART TXD pin can drive the pin high regardless of whether the Open-Drain mode is enabled or not.

Work Around
Configure the TXD pin as an input by writing the corresponding bit in PORTx.DIR to '0' when using Open-Drain mode.

Affected Silicon Revisions

Rev. A3	Rev. A4
X	X

2.13.2 Start-of-Frame Detection Can Unintentionally Be Triggered in Active Mode

The Start-of-Frame Detection feature enables the USART to wake up from Standby sleep mode upon data reception. The Start-of-Frame Detector can unintentionally be triggered when the Start-of-Frame Detection Enable (SFDEN) bit in the USART Control B (USARTn.CTRLB) register is set, and the device is in Active mode. If the Receive Data (RXDATA) registers are read while receiving new data, the Receive Complete Interrupt Flag (RXCIF) in the USARTn.STATUS register is cleared. This triggers the Start-of-Frame Detector and falsely detects the following falling edge as a start bit. When the Start-of-Frame Detector detects a start condition, the frame reception is restarted, resulting in corrupt received data. Note that the USART Receive Start Interrupt Flag (RXSIF) always is '0' when in Active mode. No interrupt will be triggered.

Work Around

Disable Start-of-Frame Detection by writing '0' to the Start-of-Frame Detection Enable (SFDEN) bit in the USART Control B (USARTn.CTRLB) register when the device is in Active mode. Re-enable it by writing the bit to '1' before transitioning to Standby sleep mode. This work around depends on a protocol preventing a new incoming frame when re-enabling Start-of-Frame Detection. Re-enabling Start-of-Frame Detection, while a new frame is already incoming, will result in corrupted received data.

Affected Silicon Revisions

Rev. A3	Rev. A4
X	X

2.14 ZCD - Zero-Cross Detector

2.14.1 All ZCD Output Selection Bits Are Tied to the ZCD0 Bit

The Zero Cross Detector n Output (ZCDn) bits in the Pin Position (PORTMUX.ZCDROUTEA) register are tied to ZCD0. Any write to ZCD0 will be reflected in the ZCD1 and ZCD2 as well. Writing to ZCD1 and/or ZCD2 has no effect.

Work Around

Use the Event System or CCL to make the output of ZCD1 or ZCD2 available on a pin.

Affected Silicon Revisions

Rev. A3	Rev. A4
X	X

3. Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (www.microchip.com/DS40002228).

Note: Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

3.1 Features

A clarification has been made to change the Flash endurance specification in the *Memories* bullet point in the *Features* list.

- Memories
  - 128 KB in-system self-programmable Flash memory
  - 512B EEPROM
  - 16 KB SRAM
  - 32B of user row in nonvolatile memory that can keep data during chip-erase and be programmed while the device is locked
  - Write/erase endurance
    - Flash: **1,000** cycles
    - EEPROM: 100,000 cycles
  - Data retention: 40 years at 55°C

3.2 FUSE - Configuration and User Fuses

A clarification of the EEPROM Save During Chip Erase (EESAVE) fuse description in the System Configuration 0 (SYSCFG0) fuse has been made.

Bit 0 - EESAVE EEPROM Save During Chip Erase

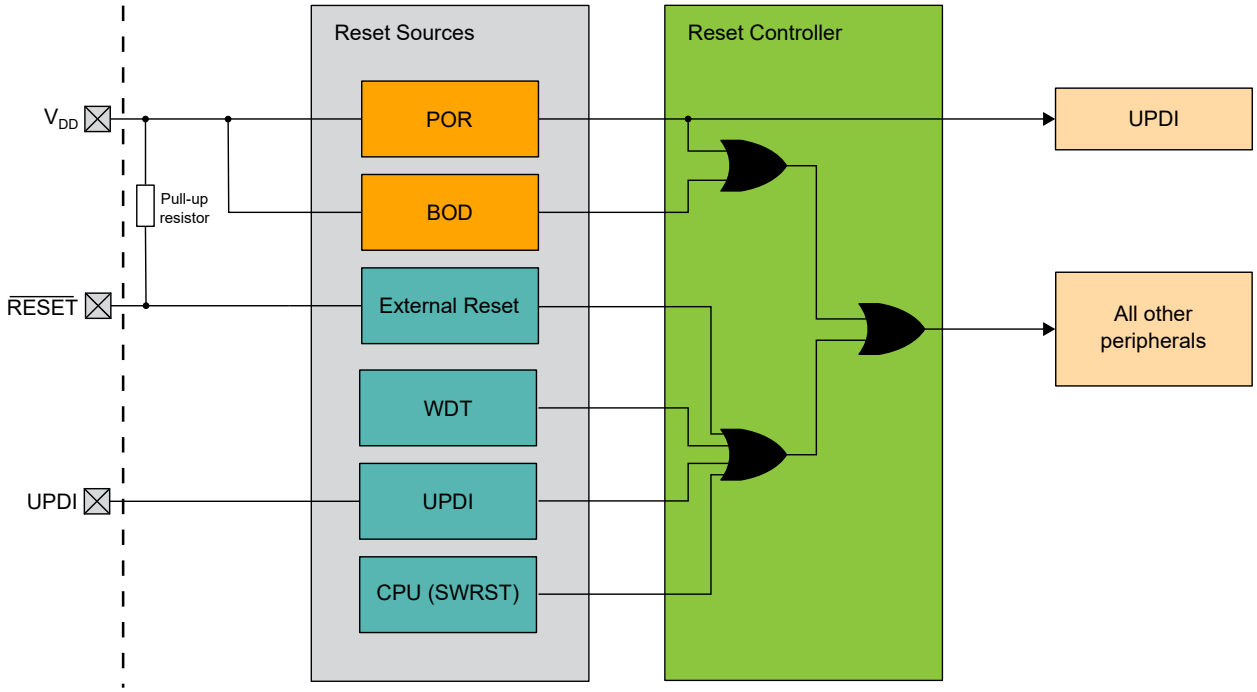
This bit controls if the EEPROM will be erased or not during a chip erase.

Value	Name	Description
0	DISABLE	EEPROM erased during chip erase
1	ENABLE	EEPROM not erased during chip erase **regardless of whether the device is locked or not**

3.3 RSTCTRL - Reset Controller

A clarification has been made to add the missing block diagram figure.

Figure 3-1. Reset System Overview



3.4 TWI - Two-Wire Interface

A clarification of the clock stretching in the SDA Setup Time (SDASETUP) bit description in the TWI Control A (CTRLA) register has been made.

Bit 4 - SDASETUP SDA Setup Time

This bit is used in TWI Client mode **with clock stretching** to select the clock hold time and ensure the minimum setup time on the SDA out signal.

Value	Name	Description
0	4CYC	SDA setup time is four clock cycles
1	8CYC	SDA setup time is eight clock cycles

3.5 Electrical Characteristics - Peripheral Power Consumption

To update the ADC power consumption (I_{DD_ADC}) in the *Peripheral Power Consumption* table, a clarification has been made.

Table 37-6. Peripheral Power Consumption(1)

Operating Conditions:
- V_{DD} = 3.0V
- T_A = 25°C
- OSCHF at 4 MHz used as clock source
- Device in Standby sleep mode

Symbol	Description	Min.	Typ. †	Max. 85°C	Max. 125°C	Unit	Conditions
I_{DD_WDT}	Watchdog Timer (WDT)	—	600	900	1500	nA	32.768 kHz internal oscillator
I_{DD_VREF}	Voltage Reference (VREF)	—	175	300	320	µA	ADC0REF enabled, V_{REF} = 2.048V
		—	71	90	92	µA	ACREF enabled, V_{REF} = 2.048V
		—	40	60	62	µA	DACREF enabled, V_{REF} = 2.048V
I_{DD_BOD}	Brown-out Detector (BOD)	—	17	25	27	µA	Brown-out Detect (BOD) continuous
		—	1.6	10	12	µA	Brown-out Detect (BOD) sampling @128 Hz, including I_{DD_OSC32K}
		—	0.95	10	12	µA	Brown-out Detect (BOD) sampling @32 Hz, including I_{DD_OSC32K}
I_{DD_TCA}	16-bit Timer/Counter Type A (TCA)	—	6	—	—	µA	CLK_PER = OSCHF/4 = 1 MHz
I_{DD_TCB}	16-bit Timer/Counter Type B (TCB)	—	3.6	—	—	µA	
I_{DD_TCD}	12-bit Timer/Counter Type D (TCD)	—	4.6	—	—	µA	
I_{DD_RTC}	Real-Time Counter (RTC)	—	0.7	18	25.5	µA	RTC running at 1.024 kHz from OSC32K
			3.9	20	26	µA	RTC running at 1.024 kHz from XOSC32K, XOSC32KCTRLA.LPMODE = 0
			2.1	18	25	µA	RTC running at 1.024 kHz from XOSC32K, XOSC32KCTRLA.LPMODE = 1
I_{DD_OSC32K}	32.768 kHz Internal Oscillator (OSC32K)	—	600	900	1500	nA	
$I_{DD\_XOSC32K}$	32.768 kHz Crystal Oscillator (XOSC32K)	—	2	—	—	µA	XOSC32KCTRLA.LPMODE = 0
		—	1.2	—	—	µA	XOSC32KCTRLA.LPMODE = 1
I_{DD_OSCHF}	Internal High Frequency Oscillator (OSCHF)	—	185	—	—	µA	OSCHF at 4 MHz

.....continued							
Operating Conditions: • V_{DD} = 3.0V • T_A = 25°C • OSCHF at 4 MHz used as clock source • Device in Standby sleep mode							
Symbol	**Description**	**Min.**	**Typ. †**	**Max. 85°C**	**Max. 125°C**	**Unit**	**Conditions**
I_{DD_ADC}	Analog-to-Digital Converter (ADC)	—	300	600	650	nA	ADC - Nonconverting
		—	1.1	1.4	1.5	**mA**	ADC @60 ksps(2)
		—	1.1	1.5	1.6	**mA**	ADC @120 ksps(2)
I_{DD_AC}	Analog Comparator (AC)	—	70	105	110	µA	CTRLA.POWER = 0x0
		—	17	30	32	µA	CTRLA.POWER = 0x1
		—	12	20	22	µA	CTRLA.POWER = 0x2
I_{DD_DAC}	Digital-to-Analog Converter (DAC)	—	120	140	160	µA	DAC + DACOUT, V_{DACREF} = V_{DD}/2
		—	8	13	34	µA	DAC, V_{DACREF} = V_{DD}/2
I_{DD_UART}	Universal Synchronous and Asynchronous Receiver and Transmitter (USART)	—	8.2	—	—	µA	USART Enabled @9600 Baud
I_{DD_SPI}	Serial Peripheral Interface (SPI)	—	4	—	—	µA	SPI Host @100 kHz
I_{DD_TWI}	Two-Wire Interface (TWI)	—	8	—	—	µA	TWI Host @100 kHz
		—	6	—	—	µA	TWI Client @100 kHz
$I_{DD\_NVM\_ERASE}$	Flash Programming Erase	—	6.8	—	—	mA	
$I_{DD\_NVM\_WRITE}$	Flash Programming Write	—	9.2	—	—	mA	

† Data in the “Typ.” column is at T_A = 25°C and V_{DD} = 3.0V unless otherwise specified. These parameters are for design guidance only and are not tested.

Notes:

1. Current consumption of the module only. To calculate the total internal power consumption of the microcontroller, add the power consumption values of all the peripherals and the clock sources used to the base power consumption given in the *Power Consumption* section.
2. Average power consumption with ADC active in Free Running mode.

3.6 Electrical Characteristics - Memory Programming Specifications

A clarification has been made to change the Flash memory cell endurance specification in the *Memory Programming Specifications* table.

Table 37-8. Memory Programming Specifications

Symbol	Description	Min.	Typ. †	Max.	Unit	Conditions
Data EEPROM Memory Specifications						
E_D*	Data EEPROM byte endurance	100k	—	—	Erase/Write cycles	-40°C ≤ T_A ≤ +85°C
t_{D_RET}	Characteristic retention	—	40	—	Year	Provided no other violated specifications
V_{D_RW}	V_{DD} for Read or Erase/Write operation	V_{DDMIN}	—	V_{DDMAX}	V	
N_{D_REF}*	Total Erase/Write cycles before refresh	1M	4M	—	Erase/Write cycles	-40°C ≤ T_A ≤ +85°C
t_{D_CE}	Byte/Multibyte/Full EEPROM Erase time	—	10	10.5	ms	
t_{D_WRE}	Byte Write time	—	70	75	µs	
t_{D_BEW}	Byte Erase and Write time	—	10.07	—	ms	
Program Flash Memory Specifications						
E_P*	**Flash memory cell endurance**	**1k**	—	—	Erase/Write cycles	
t_{P_RET}	Characteristic retention	—	40	—	Year	
V_{P_RD}	V_{DD} for Read operation	V_{DDMIN}	—	V_{DDMAX}	V	
V_{P_REW}	V_{DD} for Erase/Write operation	V_{DD}(1)	—	V_{DDMAX}	V	
t_{P_CE}	Chip Erase time	—	11	11.6	ms	
t_{P_PE}	Page Erase time	—	10	10.5	ms	
t_{P_WRD}	Byte/Word Write time	—	70	75	µs	

† Data in the “Typ.” column is at T_A = 25°C and V_{DD} = 3.0V unless otherwise specified. These parameters are for design guidance only and are not tested.

* These parameters are characterized but not tested in production.

Note:

1. During Chip Erase, the Brown-out Detector (BOD) configured with BODLEVEL0 is forced ON. The erase attempt will fail if the supply voltage V_{DD} is below V_{BOD} for BODLEVEL0.

3.7 Electrical Characteristics - VREF

A clarification has been made to change the maximum accuracy of VREF in the *V_{REF} Specifications* table.

Table 37-17. V_{REF} Specifications

Symbol	Description	Min.	Typ. †	Max.	Unit	Conditions
V_{VREF_1V024}(1)	Internal Voltage Reference 1.024V	-4	—	**4**	%	V_{DD} ≥ 2.5V, -40°C ≤ TA ≤ +85°C
V_{VREF_2V048}(1)	Internal Voltage Reference 2.048V	-4	—	**4**	%	V_{DD} ≥ 2.5V, -40°C ≤ TA ≤ +85°C
V_{VREF_4V096}(1)	Internal Voltage Reference 4.096V	-4	—	**4**	%	V_{DD} ≥ 4.55V, -40°C ≤ TA ≤ +85°C
V_{VREF_2V500}(1)	Internal Voltage Reference 2.5V	-4	—	**4**	%	V_{DD} ≥ 2.7V, -40°C ≤ TA ≤ +85°C

.....continued						
Symbol	**Description**	**Min.**	**Typ. †**	**Max.**	**Unit**	**Conditions**
V_{VREFA}	VREFA input pin voltage	1.8	—	V_{DD}	V	V_{DD} < 2.7V
		1.024	—	V_{DD}	V	V_{DD} ≥ 2.7V
t_{INTREF} *	Delay for changing voltage reference	—	2	—	µs	
t_{VREF_ST} *	VREF Start-up Time	—	10	—	µs	CLKCTRL.MCLKCTRLA = 0x00 or 0x03
		—	200	—	µs	CLKCTRL.MCLKCTRLA = 0x01 or 0x02

† Data in the "Typ." column is at T_A = 25°C and V_{DD} = 3.0V unless otherwise specified. These parameters are for design guidance only and are not tested.

***** These parameters are characterized but not tested in production.

Note:

1. The symbol V_{VREF_xVxxx} refers to the respective values of the REFSEL bit fields in the VREF.ADC0REF, VREF.DAC0REF and VREF.ACREF registers.

3.8 Electrical Characteristics - DAC

A clarification has been made to update the conditions in the *DAC Electrical Specifications* table.

Table 37-22. DAC Electrical Specifications

Operating Conditions: • V_{DD} = 3.0V • T_A = 25ºC						
Symbol	**Description**	**Min.**	**Typ. †**	**Max.**	**Unit**	**Conditions**
V_{DD}	Supply voltage	1.8	—	5.5	V	
V_{OUT}	Output voltage range	GND	—	V_{DD}	V	
V_{LSB}	Resolution	—	10	—	Bit	
V_{ACC}	Absolute accuracy	—	1	—	LSb	**0x023 ≤ DAC.DATA < 0x3DC**
t_{ST}	Settling Time(1)	—	7	—	µs	V_{DACREF} = V_{DD} = 3.0V, 50 pF Load
		—	10	—	µs	V_{DACREF} = V_{DD} = 5.5V, 50 pF Load
INL	Integral nonlinearity	-2.3	1	2.3	LSb	**0x023 ≤ DAC.DATA < 0x3DC**
DNL	Differential nonlinearity	-0.2	0.2	0.7	LSb	**0x023 ≤ DAC.DATA < 0x3DC**
E_{OFF}	Offset error	1.7	2.8	5	LSb	**0x023 ≤ DAC.DATA < 0x3DC**
E_{GAIN}	Gain error	-3.3	-1.1	0.7	LSb	**0x023 ≤ DAC.DATA < 0x3DC**

† Data in the "Typ." column is at T_A = 25°C and V_{DD} = 3.0V unless otherwise specified. These parameters are for design guidance only and are not tested.

Note:

1. Settling time measured while DAC.DATA[9:0] transitions from '0x000' to '0x3FF'.

3.9 Electrical Characteristics - ADC

A clarification has been made for ADC Specifications in the *ADC Accuracy Specifications* table.

Table 37-23. ADC Accuracy Specifications

Operating Conditions: • V_{DD} = 3.0V • T_A = 25ºC						
Symbol	**Description**	**Min.**	**Typ. †**	**Max.**	**Unit**	**Conditions**
N_R	Resolution	—	—	12	bit	
E_{INL}	Integral nonlinearity error	-1	0.1	1	LSb	**V_{DD} = V_{REF} = 3.0V**
E_{DNL}	Differential nonlinearity error(1)	-1	0.1	1	LSb	**V_{DD} = V_{REF} = 3.0V**
E_{OFF}	Offset error	1.3	3	5	LSb	**V_{DD} = V_{REF} = 3.0V**
E_{GAIN}	Gain error	-5	1.5	5	LSb	**V_{DD} = V_{REF} = 3.0V**
E_{ABS}	Absolute error	—	—	—	LSb	**V_{DD} = V_{REF} = 3.0V**
V_{ADCREF}	ADC reference voltage	**1.8**	—	V_{DD}	V	
V_{AIN}	Full-scale range	GND	—	V_{ADCREF}	V	
Z_{AIN}	Recommended impedance of analog voltage source	—	**1**	—	kΩ	
R_{VREFA}	ADC voltage reference ladder impedance(2)	—	50	—	kΩ	

† Data in the “Typ.” column is at T_A = 25°C and V_{DD} = 3.0V unless otherwise specified. These parameters are for design guidance only and are not tested.

Notes:

1. The ADC conversion result never decreases with an increase in the input and has no missing codes.
2. This is the impedance seen by the VREFA pin when the external reference is selected.

4. Document Revision History

Note: The document revision is independent of the silicon revision.

4.1 Revision History

Doc. Rev.	Date	Comments
D	02/2022	• Added data sheet clarifications: – 3.1. Features – 3.2. FUSE - Configuration and User Fuses – 3.5. Electrical Characteristics - Peripheral Power Consumption – 3.6. Electrical Characteristics - Memory Programming Specifications – 3.7. Electrical Characteristics - VREF – 3.8. Electrical Characteristics - DAC – 3.9. Electrical Characteristics - ADC • Updated data sheet clarifications: – 3.3. RSTCTRL - Reset Controller – 3.4. TWI - Two-Wire Interface
C	10/2021	• Updated errata: – Device: *Some Reserved Fuse Bits Are '1'* – Device: *CRC Check During Reset Initialization Is Not Functional* – USART: *Start-of-Frame Detection Can Unintentionally Be Enabled in Active Mode When RXCIF Is '0'* • Added errata: – CLKCTRL: *PLL Status Not Working as Expected* – DAC: *DAC Output Buffer Lifetime Drift* – NVMCTRL: *Flash Multi-Page Erase Can Erase Write Protected Section* – TCD: *Halting TCD and Wait for SW Restart Does Not Work if Compare Value A Is 0 or Dual Slope Mode Is Used* – TWI: *Flush Nonfunctional*
B	11/2020	• Add new device revision (A4) • Added errata: – Device: *Some Reserved Fuse Bits Are '1'* – Device: *CRC Check During Reset Initialization Is Not Functional* – CCL: *The LINK Input Source Selection for LUT3 Is Not Functional on 28- and 32-Pin Device* – RSTCTRL: *BOD Registers Not Reset When UPDI Is Enabled* – TCA: *Restart Will Reset Counter Direction in NORMAL and FRQ Mode* – TCB: *CCMP and CNT Registers Operate as 16-Bit Registers in 8-Bit PWM Mode* – TCD: *Asynchronous Input Events Not Working When TCD Counter Prescaler Is Used* – USART: *Start-of-Frame Detection Can Unintentionally Be Enabled in Active Mode When RXCIF Is '0'*
A	06/2020	Initial document release

The Microchip Website

Microchip provides online support via our website at www.microchip.com/. This website is used to make files and information easily available to customers. Some of the content available includes:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQs), technical support requests, online discussion groups, Microchip design partner program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

Product Change Notification Service

Microchip's product change notification service helps keep customers current on Microchip products. Subscribers will receive email notification whenever there are changes, updates, revisions or errata related to a specified product family or development tool of interest.

To register, go to www.microchip.com/pcn and follow the registration instructions.

Customer Support

Users of Microchip products can receive assistance through several channels:

- Distributor or Representative
- Local Sales Office
- Embedded Solutions Engineer (ESE)
- Technical Support

Customers should contact their distributor, representative or ESE for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in this document.

Technical support is available through the website at: www.microchip.com/support

Microchip Devices Code Protection Feature

Note the following details of the code protection feature on Microchip products:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner, within operating specifications, and under normal conditions.
- Microchip values and aggressively protects its intellectual property rights. Attempts to breach the code protection features of Microchip product is strictly prohibited and may violate the Digital Millennium Copyright Act.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not mean that we are guaranteeing the product is "unbreakable". Code protection is constantly evolving. Microchip is committed to continuously improving the code protection features of our products.

Legal Notice

This publication and the information herein may be used only with Microchip products, including to design, test, and integrate Microchip products with your application. Use of this information in any other manner violates these terms. Information regarding device applications is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. Contact your local Microchip sales office for additional support or, obtain additional support at www.microchip.com/en-us/support/design-help/client-support-services.

Trademarks

ISBN: 978-1-5224-9701-1

Quality Management System

For information regarding Microchip's Quality Management Systems, please visit www.microchip.com/quality.

Worldwide Sales and Service

AMERICAS	ASIA/PACIFIC	ASIA/PACIFIC	EUROPE
Corporate Office 2355 West Chandler Blvd. Chandler, AZ 85224-6199 Tel: 480-792-7200 Fax: 480-792-7277 Technical Support: www.microchip.com/support Web Address: www.microchip.com **Atlanta** Duluth, GA Tel: 678-957-9614 Fax: 678-957-1455 **Austin, TX** Tel: 512-257-3370 **Boston** Westborough, MA Tel: 774-760-0087 Fax: 774-760-0088 **Chicago** Itasca, IL Tel: 630-285-0071 Fax: 630-285-0075 **Dallas** Addison, TX Tel: 972-818-7423 Fax: 972-818-2924 **Detroit** Novi, MI Tel: 248-848-4000 **Houston, TX** Tel: 281-894-5983 **Indianapolis** Noblesville, IN Tel: 317-773-8323 Fax: 317-773-5453 Tel: 317-536-2380 **Los Angeles** Mission Viejo, CA Tel: 949-462-9523 Fax: 949-462-9608 Tel: 951-273-7800 **Raleigh, NC** Tel: 919-844-7510 **New York, NY** Tel: 631-435-6000 **San Jose, CA** Tel: 408-735-9110 Tel: 408-436-4270 **Canada - Toronto** Tel: 905-695-1980 Fax: 905-695-2078	**Australia - Sydney** Tel: 61-2-9868-6733 **China - Beijing** Tel: 86-10-8569-7000 **China - Chengdu** Tel: 86-28-8665-5511 **China - Chongqing** Tel: 86-23-8980-9588 **China - Dongguan** Tel: 86-769-8702-9880 **China - Guangzhou** Tel: 86-20-8755-8029 **China - Hangzhou** Tel: 86-571-8792-8115 **China - Hong Kong SAR** Tel: 852-2943-5100 **China - Nanjing** Tel: 86-25-8473-2460 **China - Qingdao** Tel: 86-532-8502-7355 **China - Shanghai** Tel: 86-21-3326-8000 **China - Shenyang** Tel: 86-24-2334-2829 **China - Shenzhen** Tel: 86-755-8864-2200 **China - Suzhou** Tel: 86-186-6233-1526 **China - Wuhan** Tel: 86-27-5980-5300 **China - Xian** Tel: 86-29-8833-7252 **China - Xiamen** Tel: 86-592-2388138 **China - Zhuhai** Tel: 86-756-3210040	**India - Bangalore** Tel: 91-80-3090-4444 **India - New Delhi** Tel: 91-11-4160-8631 **India - Pune** Tel: 91-20-4121-0141 **Japan - Osaka** Tel: 81-6-6152-7160 **Japan - Tokyo** Tel: 81-3-6880- 3770 **Korea - Daegu** Tel: 82-53-744-4301 **Korea - Seoul** Tel: 82-2-554-7200 **Malaysia - Kuala Lumpur** Tel: 60-3-7651-7906 **Malaysia - Penang** Tel: 60-4-227-8870 **Philippines - Manila** Tel: 63-2-634-9065 **Singapore** Tel: 65-6334-8870 **Taiwan - Hsin Chu** Tel: 886-3-577-8366 **Taiwan - Kaohsiung** Tel: 886-7-213-7830 **Taiwan - Taipei** Tel: 886-2-2508-8600 **Thailand - Bangkok** Tel: 66-2-694-1351 **Vietnam - Ho Chi Minh** Tel: 84-28-5448-2100	**Austria - Wels** Tel: 43-7242-2244-39 Fax: 43-7242-2244-393 **Denmark - Copenhagen** Tel: 45-4485-5910 Fax: 45-4485-2829 **Finland - Espoo** Tel: 358-9-4520-820 **France - Paris** Tel: 33-1-69-53-63-20 Fax: 33-1-69-30-90-79 **Germany - Garching** Tel: 49-8931-9700 **Germany - Haan** Tel: 49-2129-3766400 **Germany - Heilbronn** Tel: 49-7131-72400 **Germany - Karlsruhe** Tel: 49-721-625370 **Germany - Munich** Tel: 49-89-627-144-0 Fax: 49-89-627-144-44 **Germany - Rosenheim** Tel: 49-8031-354-560 **Israel - Ra'anana** Tel: 972-9-744-7705 **Italy - Milan** Tel: 39-0331-742611 Fax: 39-0331-466781 **Italy - Padova** Tel: 39-049-7625286 **Netherlands - Drunen** Tel: 31-416-690399 Fax: 31-416-690340 **Norway - Trondheim** Tel: 47-72884388 **Poland - Warsaw** Tel: 48-22-3325737 **Romania - Bucharest** Tel: 40-21-407-87-50 **Spain - Madrid** Tel: 34-91-708-08-90 Fax: 34-91-708-08-91 **Sweden - Gothenberg** Tel: 46-31-704-60-40 **Sweden - Stockholm** Tel: 46-8-5090-4654 **UK - Wokingham** Tel: 44-118-921-5800 Fax: 44-118-921-5820