Product Change Notification / SYST-10ZGXL795

Date:

11-Mar-2022

Product Category:

8-bit Microcontrollers

PCN Type:

Document Change

Notification Subject:

ERRATA - AVR128DA28/32/48/64 Silicon Errata and Data Sheet Clarification

Affected CPNs:

SYST-10ZGXL795_Affected_CPN_03112022.pdf
SYST-10ZGXL795_Affected_CPN_03112022.csv

Notification Text:

SYST-10ZGXL795

Microchip has released a new Product Documents for the AVR128DA28/32/48/64 Silicon Errata and Data Sheet Clarification of devices. If you are using one of these devices please read the document located at AVR128DA28/32/48/64 Silicon Errata and Data Sheet Clarification.

Notification Status: Final

Description of Change:
• Added data sheet clarifications:
  – 3.1. Features
  – 3.2. FUSE - Configuration and User Fuses
  – 3.5. Electrical Characteristics - Peripheral Power Consumption
  – 3.6. Electrical Characteristics - Memory Programming Specifications
  – 3.7. Electrical Characteristics - VREF
  – 3.8. Electrical Characteristics - DAC
  – 3.9. Electrical Characteristics - ADC
• Updated data sheet clarifications:
  – 3.3. RSTCTRL - Reset Controller
  – 3.4. TWI - Two-Wire Interface
Impacts to Data Sheet: None

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 11 Mar 2022

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachments:

AVR128DA28/32/48/64 Silicon Errata and Data Sheet Clarification

Please contact your local Microchip sales office with questions or concerns regarding this notification.

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Affected Catalog Part Numbers (CPN)

AVR128DA28-E/SO
AVR128DA28-E/SP
AVR128DA28-E/SS
AVR128DA28-E/SSVAO
AVR128DA28-I/SO
AVR128DA28-I/SP
AVR128DA28-I/SS
AVR128DA28T-E/SO
AVR128DA28T-E/SS
AVR128DA28T-E/SSVAO
AVR128DA28T-I/SO
AVR128DA28T-I/SS
AVR128DA32-E/PT
AVR128DA32-E/PTVAO
AVR128DA32-E/RXB
AVR128DA32-E/RXBVAO
AVR128DA32-I/PT
AVR128DA32-I/RXB
AVR128DA32T-E/PT
AVR128DA32T-E/PTVAO
AVR128DA32T-E/RXB
AVR128DA32T-E/RXBVAO
AVR128DA32T-I/PT
AVR128DA32T-I/RXB
AVR128DA48-E/6LX
AVR128DA48-E/6LXVAO
AVR128DA48-E/PT
AVR128DA48-E/PTVAO
AVR128DA48-I/6LX
AVR128DA48-I/PT
AVR128DA48T-E/6LX
AVR128DA48T-E/6LXVAO
AVR128DA48T-E/PT
AVR128DA48T-E/PTVAO
AVR128DA48T-I/6LX
AVR128DA48T-I/PT
AVR128DA64-E/MR
AVR128DA64-E/MRVAO
AVR128DA64-E/PT
AVR128DA64-I/MR
AVR128DA64-I/PT
AVR128DA64T-E/MR
AVR128DA64T-E/MRVAO
AVR128DA64T-E/PT
AVR128DA64T-E/PTV01
AVR128DA64T-E/PTVAO

AVR128DA64T-I/MR
AVR128DA64T-I/PT

AVR128DA28/32/48/64

AVR128DA Silicon Errata and Data Sheet Clarification

The AVR128DA28/32/48/64 devices you have received conform functionally to the current device data sheet (www.microchip.com/DS40002183), except for the anomalies described in this document. The errata described in this document will likely be addressed in future revisions of the AVR128DA28/32/48/64 devices.

Notes:

- This document summarizes all the silicon errata issues from all the silicon revisions, previous as well as current
- Refer to the Device/Revision ID section in the current device data sheet (www.microchip.com/DS40002183) for more detailed information on Device Identification and Revision IDs for your specific device, or contact your local Microchip sales office for assistance

Table of Contents

1. Silicon Issue Summary

Legend

- **-** Erratum is not applicable.
- **X** Erratum is applicable.

Peripheral	Short Description	Valid for Silicon Revision		
		Rev. A6(1)	Rev. A7	Rev. A8
Device	2.2.1. Some Reserved Fuse Bits Are '1'	X	X	X
	2.2.2. CRC Check During Reset Initialization Is not Functional	X	X	X
CCL	2.3.1. The LINK Input Source Selection for LUT3 Is not Functional on 28- and 32-Pin Devices	X	X	X
CLKCTRL	2.4.1. PLL Status not Working as Expected	X	X	X
DAC	2.5.1. DAC Output Buffer Lifetime Drift	X	X	X
EVSYS	2.6.1. Port Pins PB[7:6] and PE[7:4] Are not Connected to the Event System	X	X	X
NVMCTRL	2.7.1. Flash Mapping Into Data Space not Working Properly	X	X	X
	2.7.2. Flash Multi-Page Erase Can Erase Write Protected Section	X	X	X
PORT	2.8.1. Digital Input on Pin Automatically Disabled When Pin Selected for Analog Input	X	X	X
RSTCTRL	2.9.1. BOD Registers not Reset When UPDI Is Enabled	X	X	X
SPI	2.10.1. SSD Bit Must Be Set When SPIROUTE Value = NONE	X	X	X
TCA	2.11.1. TCA1 Pinout Alternative 2 and 3 not Functional	X	X	X
	2.11.2. Restart Will Reset Counter Direction in NORMAL and FRQ Mode	X	X	X
TCB	2.12.1. CCMP and CNT Registers Operate as 16-Bit Registers in 8-Bit PWM Mode	X	X	X
TCD	2.13.1. Asynchronous Input Events not Working When TCD Counter Prescaler Is Used	X	X	X
	2.13.2. CMPAEN Controls All WOx for Alternative Pin Functions	X	X	X
	2.13.3. Halting TCD and Wait for SW Restart Does Not Work if Compare Value A is 0 or Dual Slope Mode is Used	X	X	X
TWI	2.14.1. The Output Pin Override Does not Function as Expected	X	X	X
	2.14.2. The 50 ns and 300 ns SDA Hold Time Selection Bits Are Swapped	X	X	X
	2.14.3. Flush Non-Functional	X	X	X
USART	2.15.1. Open-Drain Mode Does not Work When TXD Is Configured as Output	X	X	X
	2.15.2. Start-of-Frame Detection Can Unintentionally Be Triggered in Active Mode	X	X	X
ZCD	2.16.1. All ZCD Output Selection Bits Are Tied to the ZCD0 Bit	X	X	X

Note:

1. This revision is the initial release of the silicon.

2. Silicon Errata Issues

2.1 Errata Details

-	Erratum is not applicable.
X	Erratum is applicable.

2.2 Device

2.2.1 Some Reserved Fuse Bits Are '1'

For material with date code 2033 (manufactured in the year 2020, week 33) or older, the default fuse values are not compliant with the data sheet. The fuse values will read out as listed below:

- BODCFG = `0x10`
- OSCCFG = `0x78` (The device will use the OSCHF clock source)
- SYSCFG0 = `0xF2`
- SYSCFG1 = `0xF8`

Work Around
None.

Affected Silicon Revisions

Rev. A6	Rev. A7	Rev. A8
X	X	X

2.2.2 CRC Check During Reset Initialization Is not Functional

For material with date code 2136 (manufactured in the year 2021, week 36) or older, the CRCSRC bit field in the SYSCFG0 fuse is ignored during Reset initialization. A CRC check will not be performed during Reset initialization. CRCSCAN is only available from the software.

Work Around
None.

Affected Silicon Revisions

Rev. A6	Rev. A7	Rev. A8
X	X	X

2.3 CCL - Configurable Custom Logic

2.3.1 The LINK Input Source Selection for LUT3 Is not Functional on 28- and 32-Pin Devices

The LINK option (INSELn in LUT3CTRLB or LUT3CTRLC is '`0x2`') does not work; the output from LUT0 will not get connected as an input to LUT3. This occurs only on 28-pin and 32-pin devices.

Work Around
Connect LUT0 output to LUT3 input using the Event System.

Affected Silicon Revisions

Rev. A6	Rev. A7	Rev. A8
X	X	X

2.4 CLKCTRL - Clock Controller

2.4.1 PLL Status not Working as Expected

The PLL Status (PLLS) bit in the Main Clock Status (MCLKSTATUS) register will never be set to '1' if the Run Standby (RUNSTDBY) bit in PLL Control A (PLLCTRLA) register is set to '1' and no peripherals are requesting the PLL oscillator.

Work Around
None.

Affected Silicon Revisions

Rev. A6	Rev. A7	Rev. A8
X	X	X

2.5 DAC - Digital-to-Analog Converter

2.5.1 DAC Output Buffer Lifetime Drift

The offset of the DAC output buffer can drift over lifetime if the device is powered with the DAC output buffer disabled.

Work Around
Keep the DAC output buffer enabled (OUTEN in DACn.CTRLA is '1') continuously or compensate by measuring the DAC output voltage offset with the ADC and adjust the DAC data register value (DATA[9:0] in DACn.DATA) accordingly.

Affected Silicon Revisions

Rev. A6	Rev. A7	Rev. A8
X	X	X

2.6 EVSYS - Event System

2.6.1 Port Pins PB[7:6] and PE[7:4] Are not Connected to the Event System

Port pins PB[7:6] and PE[7:4] are not connected to the Event System. This is true for both input and output signals into the Event System on these pins.

Work Around
None.

Affected Silicon Revisions

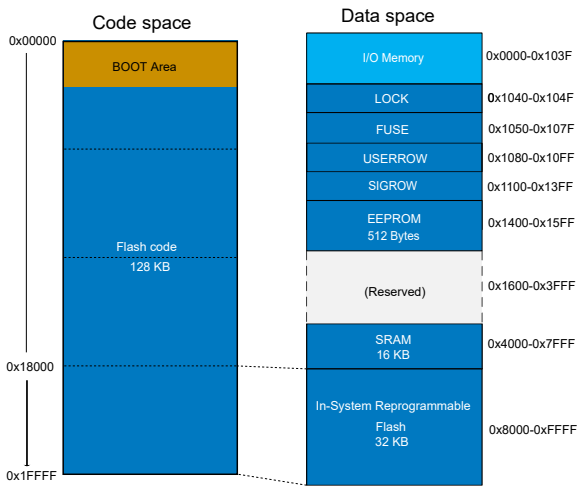
Rev. A6	Rev. A7	Rev. A8

X	X	X

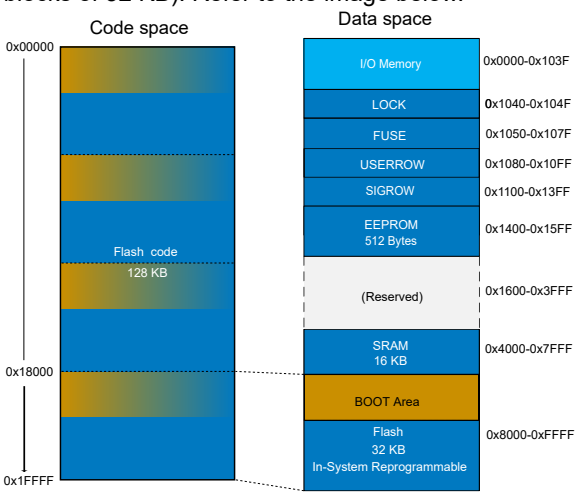
2.7 NVMCTRL - Nonvolatile Memory Controller

2.7.1 Flash Mapping Into Data Space not Working Properly

The inter-section Flash protection mechanism does not take into account the FLMAP bit field when checking if the address is in BOOT, APPCODE or APPDATA areas. It uses for comparison only the address offset between Flash start address in data space (0x8000) and the accessed address. This will cause the mirroring of the BOOT area in each Flash section selected by FLMAP (in blocks of 32 KB). Refer to the image below.



BOOT area for devices without issue



BOOT area for devices with issue

For read operations, the FLMAP bits work as documented when the Boot Read Protect (BOOTRP) bit is not enabled. For write operations, the inter-section Flash protection works properly only when FLMAP is set to `'0x00'`.

Work Around

Use only store program memory `(SPM)` instructions to write and load program memory `(LPM)` instructions to read Flash memory.

Affected Silicon Revisions

Rev. A6	Rev. A7	Rev. A8
X	X	X

2.7.2 Flash Multi-Page Erase Can Erase Write Protected Section

When using Flash Multi-Page Erase mode, only the first page in the selected address range is verified to be within a section that is not write-protected. If the address range includes any write-protected Application Data pages, it will erase them.

Work Around

None.

Affected Silicon Revisions

Rev. A6	Rev. A7	Rev. A8
X	X	X

2.8 PORT - I/O Configuration

2.8.1 Digital Input on Pin Automatically Disabled When Pin Selected for Analog Input

If an input pin is selected to be analog input, the digital input function for those pins is automatically disabled.

Work Around
None

Affected Silicon Revisions

Rev. A6	Rev. A7	Rev. A8
X	X	X

2.9 RSTCTRL - Reset Controller

2.9.1 BOD Registers not Reset When UPDI Is Enabled

If the UPDI is enabled, the VLMCTRL, INTCTRL, and INTFLAGS registers in BOD will not be reset by other reset sources than POR.

Work Around
None

Affected Silicon Revisions

Rev. A6	Rev. A7	Rev. A8
X	X	X

2.10 SPI - Serial Peripheral Interface

2.10.1 SSD Bit Must Be Set When SPIROUTE Value = NONE

When operating either SPIn module, when the PORTMUX.SPIROUTE selection is NONE, the $\overline{SS}$ pin must be disabled (CTRLB.SSD = 1) to maintain Host mode operation.

Work Around
None

Affected Silicon Revisions

Rev. A6	Rev. A7	Rev. A8
X	X	X

2.11 TCA - 16-Bit Timer/Counter Type A

2.11.1 TCA1 Pinout Alternative 2 and 3 not Functional

It is not possible to configure TCA1 in PORTMUX.TCAROUTEA to use pinout alternatives 2 and 3.

Work Around
Use TCA1 pinout alternative 0 or 1.

Affected Silicon Revisions

Rev. A6	Rev. A7	Rev. A8
X	X	X

2.11.2 Restart Will Reset Counter Direction in NORMAL and FRQ Mode

When the TCA is configured to a NORMAL or FRQ mode (WGMODE in TCAn.CTRLB is '0x0' or '0x1'), a RESTART command or Restart event will reset the count direction to default. The default is counting upwards.

Work Around
None.

Affected Silicon Revisions

Rev. A6	Rev. A7	Rev. A8
X	X	X

2.12 TCB - 16-Bit Timer/Counter Type B

2.12.1 CCMP and CNT Registers Operate as 16-Bit Registers in 8-Bit PWM Mode

When the TCB is operating in 8-bit PWM mode (CNTMODE in TCBn.CTRLB is '0x7'), the low and high bytes for the CNT and CCMP registers operate as 16-bit registers for read and write. They cannot be read or written independently.

Work Around
Use 16-bit register access. Refer to the data sheet for further information.

Affected Silicon Revisions

Rev. A6	Rev. A7	Rev. A8
X	X	X

2.13 TCD - 12-Bit Timer/Counter Type D

2.13.1 Asynchronous Input Events not Working When TCD Counter Prescaler Is Used

When configuring TCD to use asynchronous input events (CFG in TCDn.EVCTRLx is '0x2') and the TCD Counter Prescaler (CNTPRES in TCDn.CTRLA) is different from '0x0', events can be missed.

Work Around
Use the TCD Synchronization Prescaler (SYNCPRES in TCDn.CTRLA) instead of the TCD Counter Prescaler. Alternatively, use synchronous input events (CFG in TCDn.EVCTRLx is not '0x2') if the input events are longer than one CLK_TCD_CNT cycle.

Affected Silicon Revisions

Rev. A6	Rev. A7	Rev. A8

X	X	X

2.13.2 CMPAEN Controls All WOx for Alternative Pin Functions

When TCD alternative pins are enabled (TCD0 in PORTMUX.TCDROUTEA is not '0x0'), all waveform outputs (WOx) are controlled by Compare A Enable (CMPAEN in TCDn.FAULTCTRL).

Work Around
None.

Affected Silicon Revisions

Rev. A6	Rev. A7	Rev. A8
X	X	X

2.13.3 Halting TCD and Wait for SW Restart Does Not Work if Compare Value A is 0 or Dual Slope Mode is Used

Halting TCD and wait for software restart (INPUTMODE in TCDn.INPUTCTRLA is '0x7') does not work if compare value A is 0 (CMPASET in TCDn.CMPASET is '0x0') or Dual Slope mode is used (WGMODE in TCDn.CTRLB is '0x3').

Work Around
Configure the compare value A (CMPASET in TCDn.CMPASET) to be different from 0 and do not use Dual Slope mode (WGMODE in TCDn.CTRLB is not '0x3').

Affected Silicon Revisions

Rev. A6	Rev. A7	Rev. A8
X	X	X

2.14 TWI - Two-Wire Interface

2.14.1 The Output Pin Override Does not Function as Expected

When TWI is enabled, it overrides the output pin driver, but not the output value. The output on the line will always be high when the value in the PORTx.OUT register is '1' for the pins corresponding to the SDA or SCL.

Work Around
Ensure that the values in the PORTx.OUT register corresponding to the SCL and SDA pins are '0' before enabling the TWI.

Affected Silicon Revisions

Rev. A6	Rev. A7	Rev. A8
X	X	X

2.14.2 The 50 ns and 300 ns SDA Hold Time Selection Bits Are Swapped

The bits corresponding to the SDA Hold Time (SDAHOLD) bit field in the TWIn.CTRLA register are swapped.

Work Around
Use the 50 ns bit field selection for the 300 ns hold time and vice versa.

Affected Silicon Revisions

Rev. A6	Rev. A7	Rev. A8
X	X	X

2.14.3 Flush Non-Functional

Issuing a Flush by writing to the FLUSH bit in TWIn.MCTRLB can cause the TWI Host to be stuck in Unknown bus state (see BUSSTATE in TWIn.MSTATUS).

Work Around

Disable and re-enable the Host using the ENABLE bit in TWIn.MCTRLA. A normal operation does not require the use of FLUSH.

Affected Silicon Revisions

Rev. A6	Rev. A7	Rev. A8
X	X	X

2.15 USART - Universal Synchronous and Asynchronous Receiver and Transmitter

2.15.1 Open-Drain Mode Does not Work When TXD Is Configured as Output

When configured as an output, the USART TXD pin can drive the pin high regardless of whether the Open-Drain mode is enabled or not.

Work Around

Configure the TXD pin as an input by writing the corresponding bit in PORTx.DIR to '0' when using Open-Drain mode.

Affected Silicon Revisions

Rev. A6	Rev. A7	Rev. A8
X	X	X

2.15.2 Start-of-Frame Detection Can Unintentionally Be Triggered in Active Mode

The Start-of-Frame Detection feature enables the USART to wake up from Standby sleep mode upon data reception. The Start-of-Frame Detector can unintentionally be triggered when the Start-of-Frame Detection Enable (SFDEN) bit in the USART Control B (USARTn.CTRLB) register is set, and the device is in Active mode. If the Receive Data (RXDATA) registers are read while receiving new data, the Receive Complete Interrupt Flag (RXCIF) in the USARTn.STATUS register is cleared. This triggers the Start-of-Frame Detector and falsely detects the following falling edge as a start bit. When the Start-of-Frame Detector detects a start condition, the frame reception is restarted, resulting in corrupt received data. Note that the USART Receive Start Interrupt Flag (RXSIF) always is '0' when in Active mode. No interrupt will be triggered.

Work Around

Disable Start-of-Frame Detection by writing '0' to the Start-of-Frame Detection Enable (SFDEN) bit in the USART Control B (USARTn.CTRLB) register when the device is in Active mode. Re-enable it by writing the bit to '1' before transitioning to Standby sleep mode. This work around depends on a protocol preventing a new incoming frame when re-enabling Start-of-Frame Detection. Re-enabling Start-of-Frame Detection, while a new frame is already incoming, will result in corrupted received data.

Affected Silicon Revisions

Rev. A6	Rev. A7	Rev. A8
X	X	X

2.16 ZCD - Zero-Cross Detector

2.16.1 All ZCD Output Selection Bits Are Tied to the ZCD0 Bit

The Zero Cross Detector n Output (ZCDn) bits in the Pin Position (PORTMUX.ZCDROUTEA) register are tied to ZCD0. Any write to ZCD0 will be reflected in the ZCD1 and ZCD2 as well. Writing to ZCD1 and/or ZCD2 has no effect.

Work Around

Use the Event System or CCL to make the output of ZCD1 or ZCD2 available on a pin.

Affected Silicon Revisions

Rev. A6	Rev. A7	Rev. A8
X	X	X

3. Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (www.microchip.com/DS40002183).

Note: Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

3.1 Features

A clarification has been made to change the Flash endurance specification in the *Memories* bullet point in the *Features* list.

- Memories
  - 128 KB in-system self-programmable Flash memory
  - 512B EEPROM
  - 16 KB SRAM
  - 32B of user row in nonvolatile memory that can keep data during chip-erase and be programmed while the device is locked
  - Write/erase endurance
    - Flash: **1,000** cycles
    - EEPROM: 100,000 cycles
  - Data retention: 40 years at 55°C

3.2 FUSE - Configuration and User Fuses

A clarification of the EEPROM Save During Chip Erase (EESAVE) fuse description in the System Configuration 0 (SYSCFG0) fuse has been made.

Bit 0 - EESAVE EEPROM Save During Chip Erase

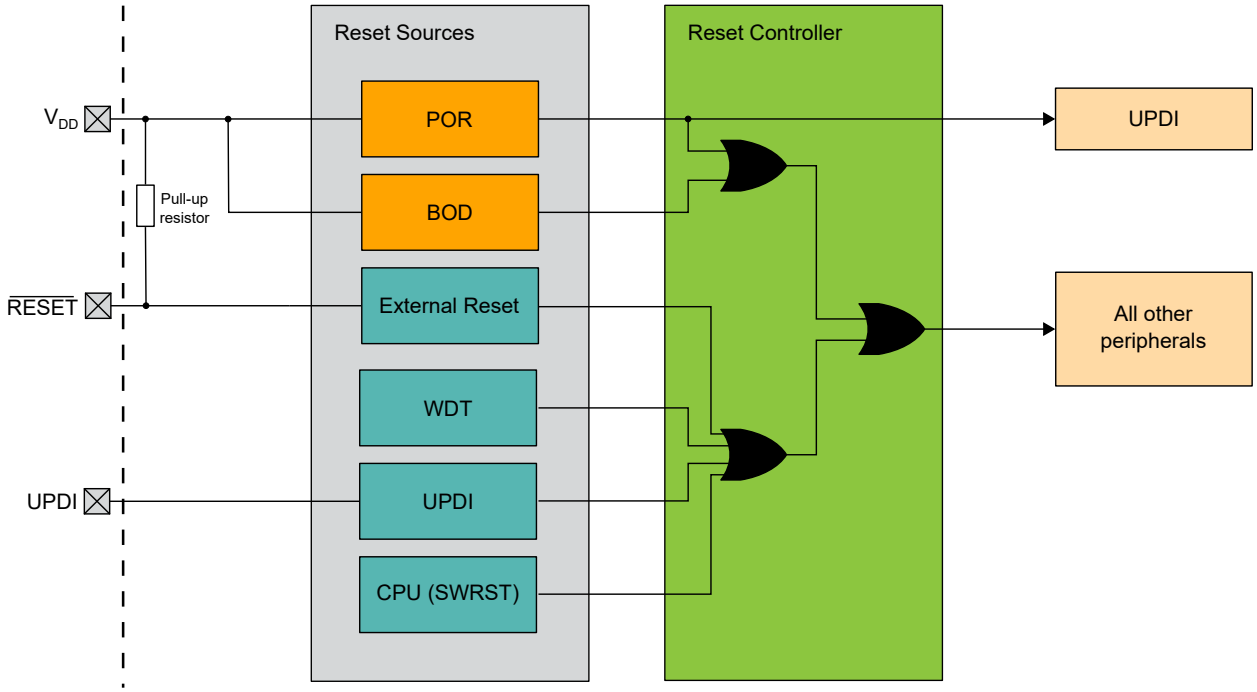
This bit controls if the EEPROM will be erased or not during a chip erase.

Value	Name	Description
0	DISABLE	EEPROM erased during chip erase
1	ENABLE	EEPROM is not erased during chip erase **regardless of whether the device is locked or not**

3.3 RSTCTRL - Reset Controller

A clarification has been made to add the missing block diagram figure.

Figure 3-1. Reset System Overview



3.4 TWI - Two-Wire Interface

A clarification of the clock stretching in the SDA Setup Time (SDASETUP) bit description in the TWI Control A (CTRLA) register has been made.

Bit 4 - SDASETUP SDA Setup Time

This bit is used in TWI Client mode **with clock stretching** to select the clock hold time and ensure the minimum setup time on the SDA out signal.

Value	Name	Description
0	4CYC	SDA setup time is four clock cycles
1	8CYC	SDA setup time is eight clock cycles

3.5 Electrical Characteristics - Peripheral Power Consumption

To update the ADC power consumption (I_{DD_ADC}) in the *Peripheral Power Consumption* table, a clarification has been made.

Table 37-6. Peripheral Power Consumption(1)

Operating Conditions:
- V_{DD} = 3.0V
- T_A = 25°C
- OSCHF at 4 MHz used as clock source
- Device in Standby sleep mode

Symbol	Description	Min.	Typ. †	Max. 85°C	Max. 125°C	Unit	Conditions
I_{DD_WDT}	Watchdog Timer (WDT)	—	600	900	1500	nA	32.768 kHz internal oscillator
I_{DD_VREF}	Voltage Reference (VREF)	—	175	300	320	µA	ADC0REF enabled, V_{REF} = 2.048V
		—	71	90	92	µA	ACREF enabled, V_{REF} = 2.048V
		—	40	60	62	µA	DACREF enabled, V_{REF} = 2.048V
I_{DD_BOD}	Brown-out Detector (BOD)	—	17	25	27	µA	Brown-out Detect (BOD) continuous
		—	1.6	10	12	µA	Brown-out Detect (BOD) sampling @128 Hz, including I_{DD_OSC32K}
		—	0.95	10	12	µA	Brown-out Detect (BOD) sampling @32 Hz, including I_{DD_OSC32K}
I_{DD_TCA}	16-bit Timer/Counter Type A (TCA)	—	6	—	—	µA	CLK_PER = OSCHF/4 = 1 MHz
I_{DD_TCB}	16-bit Timer/Counter Type B (TCB)	—	3.6	—	—	µA	
I_{DD_TCD}	12-bit Timer/Counter Type D (TCD)	—	4.6	—	—	µA	
I_{DD_RTC}	Real-Time Counter (RTC)	—	0.7	18	25.5	µA	RTC running at 1.024 kHz from OSC32K
			3.9	20	26	µA	RTC running at 1.024 kHz from XOSC32K, XOSC32KCTRLA.LPMODE = 0
			2.1	18	25	µA	RTC running at 1.024 kHz from XOSC32K, XOSC32KCTRLA.LPMODE = 1
I_{DD_OSC32K}	32.768 kHz Internal Oscillator (OSC32K)	—	600	900	1500	nA	
$I_{DD\_XOSC32K}$	32.768 kHz Crystal Oscillator (XOSC32K)	—	2	—	—	µA	XOSC32KCTRLA.LPMODE = 0
		—	1.2	—	—	µA	XOSC32KCTRLA.LPMODE = 1
I_{DD_OSCHF}	Internal High Frequency Oscillator (OSCHF)	—	185	—	—	µA	OSCHF at 4 MHz

.....continued

Operating Conditions:
- V_{DD} = 3.0V
- T_A = 25°C
- OSCHF at 4 MHz used as clock source
- Device in Standby sleep mode

Symbol	Description	Min.	Typ. †	Max. 85°C	Max. 125°C	Unit	Conditions
I_{DD_ADC}	Analog-to-Digital Converter (ADC)	—	300	600	650	nA	ADC - Nonconverting
		—	1.1	1.4	1.5	**mA**	ADC @60 ksps(2)
		—	1.1	1.5	1.6	**mA**	ADC @120 ksps(2)
I_{DD_AC}	Analog Comparator (AC)	—	70	105	110	µA	CTRLA.POWER = 0x0
		—	17	30	32	µA	CTRLA.POWER = 0x1
		—	12	20	22	µA	CTRLA.POWER = 0x2
I_{DD_DAC}	Digital-to-Analog Converter (DAC)	—	120	140	160	µA	DAC + DACOUT, V_{DACREF} = V_{DD}/2
		—	8	13	34	µA	DAC, V_{DACREF} = V_{DD}/2
I_{DD_UART}	Universal Synchronous and Asynchronous Receiver and Transmitter (USART)	—	8.2	—	—	µA	USART Enabled @9600 Baud
I_{DD_SPI}	Serial Peripheral Interface (SPI)	—	4	—	—	µA	SPI Host @100 kHz
I_{DD_TWI}	Two-Wire Interface (TWI)	—	8	—	—	µA	TWI Host @100 kHz
		—	6	—	—	µA	TWI Client @100 kHz
$I_{DD\_NVM\_ERASE}$	Flash Programming Erase	—	6.8	—	—	mA	
$I_{DD\_NVM\_WRITE}$	Flash Programming Write	—	9.2	—	—	mA	

† Data in the "Typ." column is at T_A = 25°C and V_{DD} = 3.0V unless otherwise specified. These parameters are for design guidance only and are not tested.

Notes:
1. Current consumption of the module only. To calculate the total internal power consumption of the microcontroller, add the power consumption values of all the peripherals and the clock sources used to the base power consumption given in the *Power Consumption* section.
2. Average power consumption with ADC active in Free Running mode.

3.6 Electrical Characteristics - Memory Programming Specifications

A clarification has been made to change the Flash memory cell endurance specification in the *Memory Programming Specifications* table.

Table 37-8. Memory Programming Specifications

Symbol	Description	Min.	Typ. †	Max.	Unit	Conditions
Data EEPROM Memory Specifications						
E_D*	Data EEPROM byte endurance	100k	—	—	Erase/Write cycles	-40°C ≤ T_A ≤ +85°C
t_{D_RET}	Characteristic retention	—	40	—	Year	Provided no other violated specifications
V_{D_RW}	V_{DD} for Read or Erase/Write operation	V_{DDMIN}	—	V_{DDMAX}	V	
N_{D_REF}*	Total Erase/Write cycles before refresh	1M	4M	—	Erase/Write cycles	-40°C ≤ T_A ≤ +85°C
t_{D_CE}	Byte/Multibyte/Full EEPROM Erase time	—	10	10.5	ms	
t_{D_WRE}	Byte Write time	—	70	75	µs	
t_{D_BEW}	Byte Erase and Write time	—	10.07	—	ms	
Program Flash Memory Specifications						
E_P*	**Flash memory cell endurance**	**1k**	—	—	Erase/Write cycles	
t_{P_RET}	Characteristic retention	—	40	—	Year	
V_{P_RD}	V_{DD} for Read operation	V_{DDMIN}	—	V_{DDMAX}	V	
V_{P_REW}	V_{DD} for Erase/Write operation	V_{DD}(1)	—	V_{DDMAX}	V	
t_{P_CE}	Chip Erase time	—	11	11.6	ms	
t_{P_PE}	Page Erase time	—	10	10.5	ms	
t_{P_WRD}	Byte/Word Write time	—	70	75	µs	

† Data in the "Typ." column is at T_A = 25°C and V_{DD} = 3.0V unless otherwise specified. These parameters are for design guidance only and are not tested.

* These parameters are characterized but not tested in production.

Note:

1. During Chip Erase, the Brown-out Detector (BOD) configured with BODLEVEL0 is forced ON. The erase attempt will fail if the supply voltage V_{DD} is below V_{BOD} for BODLEVEL0.

3.7 Electrical Characteristics - VREF

A clarification has been made to change the maximum accuracy of VREF in the *V_{REF} Specifications* table.

Table 37-17. V_{REF} Specifications

Symbol	Description	Min.	Typ. †	Max.	Unit	Conditions
V_{VREF_1V024}(1)	Internal voltage reference 1.024V	-4	—	**4**	%	V_{DD} ≥ 2.5V, -40°C ≤ TA ≤ +85°C
V_{VREF_2V048}(1)	Internal voltage reference 2.048V	-4	—	**4**	%	V_{DD} ≥ 2.5V, -40°C ≤ TA ≤ +85°C
V_{VREF_4V096}(1)	Internal voltage reference 4.096V	-4	—	**4**	%	V_{DD} ≥ 4.55V, -40°C ≤ TA ≤ +85°C
V_{VREF_2V500}(1)	Internal voltage reference 2.5V	-4	—	**4**	%	V_{DD} ≥ 2.7V, -40°C ≤ TA ≤ +85°C

.....continued						
Symbol	**Description**	**Min.**	**Typ. †**	**Max.**	**Unit**	**Conditions**
V_{VREFA}	VREFA input pin voltage	1.8	—	V_{DD}	V	V_{DD} < 2.7V
		1.024	—	V_{DD}	V	V_{DD} ≥ 2.7V
t_{INTREF} *	Delay for changing voltage reference	—	2	—	µs	
t_{VREF_ST} *	VREF start-up time	—	10	—	µs	CLKCTRL.MCLKCTRLA = 0x00 or 0x03
		—	200	—	µs	CLKCTRL.MCLKCTRLA = 0x01 or 0x02

† Data in the "Typ." column is at T_A = 25°C and V_{DD} = 3.0V unless otherwise specified. These parameters are for design guidance only and are not tested.

***** These parameters are characterized but not tested in production.

Note:

1. The symbol V_{VREF_xVxxx} refers to the respective values of the REFSEL bit fields in the VREF.ADC0REF, VREF.DAC0REF and VREF.ACREF registers.

3.8 Electrical Characteristics - DAC

A clarification has been made to update the conditions in the *DAC Electrical Specifications* table.

Table 37-22. DAC Electrical Specifications

Operating Conditions: • V_{DD} = 3.0V • T_A = 25ºC						
Symbol	**Description**	**Min.**	**Typ. †**	**Max.**	**Unit**	**Conditions**
V_{DD}	Supply voltage	1.8	—	5.5	V	
V_{OUT}	Output voltage range	GND	—	V_{DD}	V	
V_{LSB}	Resolution	—	10	—	Bit	
V_{ACC}	Absolute accuracy	—	1	—	LSb	**0x023 ≤ DAC.DATA < 0x3DC**
t_{ST}	Settling Time(1)	—	7	—	µs	V_{DACREF} = V_{DD} = 3.0V, 50 pF Load
		—	10	—	µs	V_{DACREF} = V_{DD} = 5.5V, 50 pF Load
INL	Integral nonlinearity	-2.3	1	2.3	LSb	**0x023 ≤ DAC.DATA < 0x3DC**
DNL	Differential nonlinearity	-0.2	0.2	0.7	LSb	**0x023 ≤ DAC.DATA < 0x3DC**
E_{OFF}	Offset error	1.7	2.8	5	LSb	**0x023 ≤ DAC.DATA < 0x3DC**
E_{GAIN}	Gain error	-3.3	-1.1	0.7	LSb	**0x023 ≤ DAC.DATA < 0x3DC**

† Data in the "Typ." column is at T_A = 25°C and V_{DD} = 3.0V unless otherwise specified. These parameters are for design guidance only and are not tested.

Note:

1. Settling time measured while DAC.DATA[9:0] transitions from '0x000' to '0x3FF'.

3.9 Electrical Characteristics - ADC

A clarification has been made for ADC Specifications in the *ADC Accuracy Specifications* table.

Table 37-23. ADC Accuracy Specifications

Operating Conditions: • V_{DD} = 3.0V • T_A = 25ºC						
Symbol	**Description**	**Min.**	**Typ. †**	**Max.**	**Unit**	**Conditions**
N_R	Resolution	—	—	12	bit	
E_{INL}	Integral nonlinearity error	**-1.5**	0.1	**1.5**	LSb	**V_{DD} = V_{REF} = 3.0V**
E_{DNL}	Differential nonlinearity error(1)	-1	0.1	1	LSb	**V_{DD} = V_{REF} = 3.0V**
E_{OFF}	Offset error	**-5**	3	5	LSb	**V_{DD} = V_{REF} = 3.0V**
E_{GAIN}	Gain error	-5	1.5	5	LSb	**V_{DD} = V_{REF} = 3.0V**
E_{ABS}	Absolute error	—	—	—	LSb	**V_{DD} = V_{REF} = 3.0V**
V_{ADCREF}	ADC reference voltage	**1.8**	—	V_{DD}	V	
V_{AIN}	Full-scale range	GND	—	V_{ADCREF}	V	
Z_{AIN}	Recommended impedance of analog voltage source	—	**1**	—	kΩ	
R_{VREFA}	ADC voltage reference ladder impedance(2)	—	50	—	kΩ	

† Data in the “Typ.” column is at T_A = 25°C and V_{DD} = 3.0V unless otherwise specified. These parameters are for design guidance only and are not tested.

Notes:

1. The ADC conversion result never decreases with an increase in the input and has no missing codes.
2. This is the impedance seen by the VREFA pin when the external reference is selected.

4. Document Revision History

Note: The document revision is independent of the silicon revision.

4.1 Revision History

Doc. Rev.	Date	Comments
D	02/2022	• Added data sheet clarifications: – 3.1. Features – 3.2. FUSE - Configuration and User Fuses – 3.5. Electrical Characteristics - Peripheral Power Consumption – 3.6. Electrical Characteristics - Memory Programming Specifications – 3.7. Electrical Characteristics - VREF – 3.8. Electrical Characteristics - DAC – 3.9. Electrical Characteristics - ADC • Updated data sheet clarifications: – 3.3. RSTCTRL - Reset Controller – 3.4. TWI - Two-Wire Interface
C	10/2021	• Updated errata: – Device: *Some Reserved Fuse Bits Are '1'* – Device: *CRC Check During Reset Initialization Is Not Functional* – USART: *Start-of-Frame Detection Can Unintentionally Be Enabled in Active Mode When RXCIF Is '0'* • Added errata: – CLKCTRL: *PLL Status Not Working as Expected* – DAC: *DAC Output Buffer Lifetime Drift* – TCD: *Halting TCD and Wait for SW Restart Does Not Work if Compare Value A Is 0 or Dual Slope Mode Is Used* – TWI: *Flush Nonfunctional* – Electrical Characteristics: *Endurance of PFM Cell lower is than specified*
B	11/2020	• Add new device revision (A8) • Added errata: – Device: *Some Reserved Fuse Bits Are '1'* – Device: *CRC Check During Reset Initialization Is Not Functional* – CCL: *The LINK Input Source Selection for LUT3 Is Not Functional on 28- and 32-Pin Device* – RSTCTRL: *BOD Registers Not Reset When UPDI Is Enabled* – TCA: *Restart Will Reset Counter Direction in NORMAL and FRQ Mode* – TCB: *CCMP and CNT Registers Operate as 16-Bit Registers in 8-Bit PWM Mode* – TCD: *Asynchronous Input Events Not Working When TCD Counter Prescaler Is Used* – TCD: *CMPAEN Controls All WOx for Alternative Pin Functions* – USART: *Start-of-Frame Detection Can Unintentionally Be Enabled in Active Mode When RXCIF Is '0'* – ZCD: *All ZCD Output Selection Bits Are Tied to the ZCD0 Bit*
A	04/2020	Initial document release

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