Datasheet

DS000686

AS5116

On-Axis Magnetic Position Sensor with Analog Sine-Cosine Outputs

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Content Guide

1 General Description

The AS5116 is a contactless magnetic position sensor for accurate angular measurement over a full mechanical turn of 360°.

Based on the Hall sensor technology, this device has a robust architecture that measures the orthogonal component of the flux density (Bz), over a full-turn rotation. To measure the angle, only a simple two-pole magnet rotating over the center of the package is required. The magnet can be placed above or below the device.

The absolute angle measurement provides an instant indication of the magnet's angular position. The angle information is provided by means of buffered differential sine and cosine voltages. The AS5116 operates at a supply voltage of 5 V or 3.3 V.

1.1 Key Benefits & Features

The benefits and features of AS5116, On-Axis Magnetic Position Sensor with Analog Sine-Cosine Outputs, are listed below:

Figure 1:
Added Value of Using AS5116

Benefits	Features
Highest reliability and durability	Contactless angle measurement
Accurate angle measurement	Low output noise
Low system costs – no shielding required	Low inherent INL
Enabler for safety critical applications	Magnetic stray field immunity overachieves ISO 11452-8
High precision analog output	Developed according to ISO26262
Small form factor	Fully differential buffered sine and cosine output signals
Fully automotive qualified	AEC – Q100, Grade 0

1.2 Applications

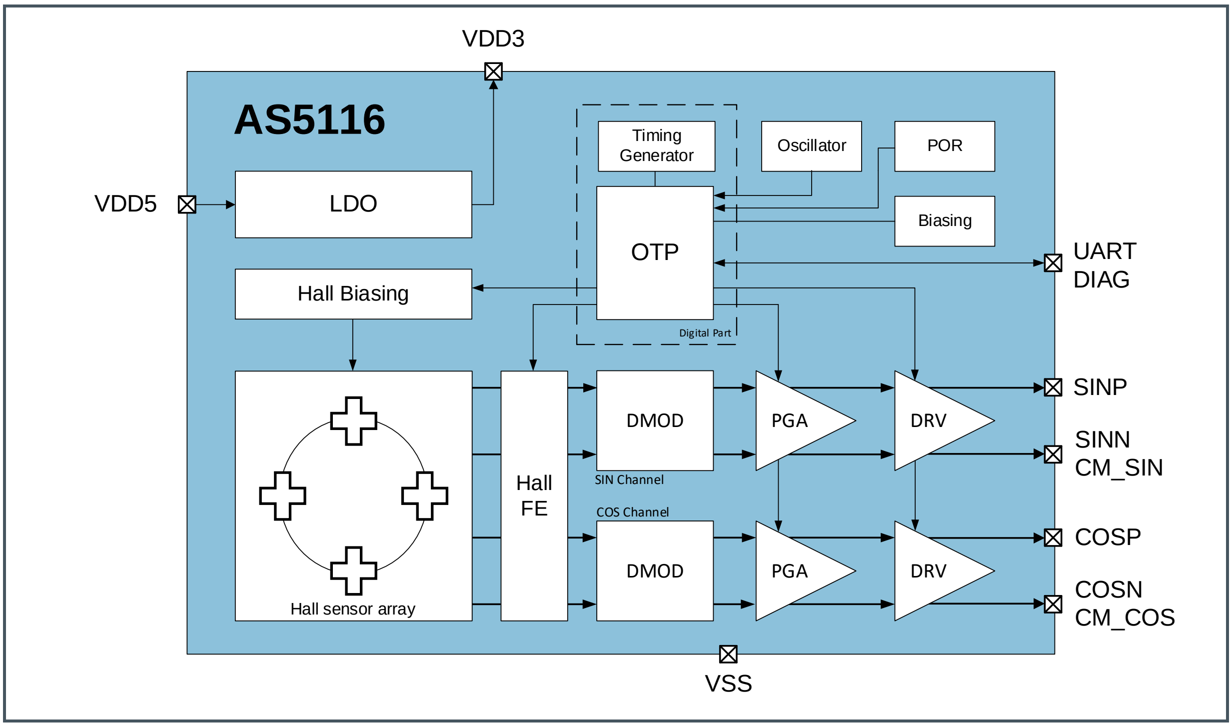
- Rotor angle sensing of electric commutated motors
- Electric power steering systems
- Electric pumps
- Actuators in transmission systems

- Starter/Generator systems
- Other 360° angle measurement solutions

1.3 Block Diagram

Figure 2 shows the block diagram of the AS5116 sensor.

Figure 2:
Functional Blocks of AS5116



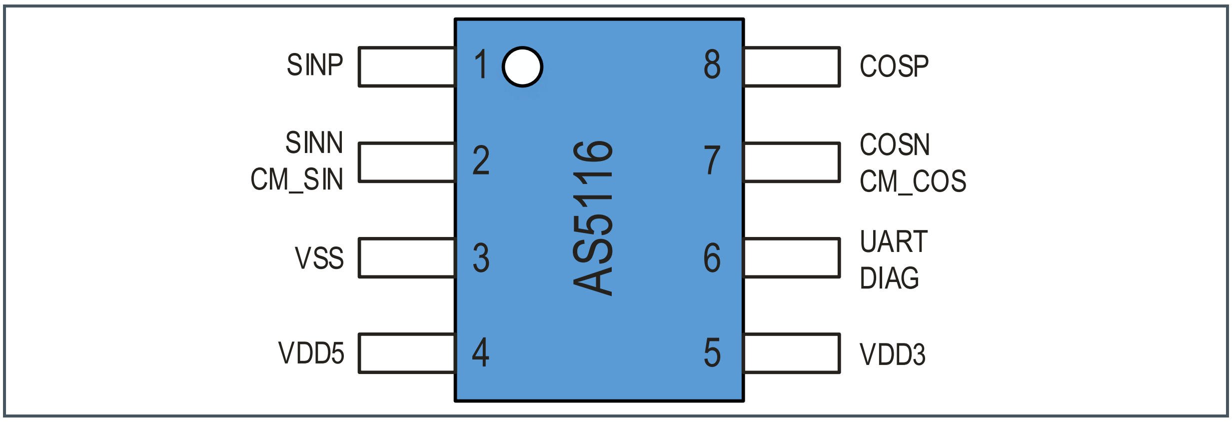
2 Ordering Information

Ordering Code	Package	Marking	Delivery Form	Delivery Quantity
AS5116-HSOT	SOIC8	AS5116	13” Tape & Reel	2500 pcs/reel
AS5116-HSOM	SOIC8	AS5116	7” Tape & Reel	500 pcs/reel
AS5116A-HSOT	SOIC8	AS5116A	13” Tape & Reel	2500 pcs/reel
AS5116A-HSOM	SOIC8	AS5116A	7” Tape & Reel	500 pcs/reel
AS5116B-HSOT	SOIC8	AS5116B	13” Tape & Reel	2500 pcs/reel
AS5116B-HSOM	SOIC8	AS5116B	7” Tape & Reel	500 pcs/reel

3 Pin Assignment

3.1 Pin Diagram AS5116

Figure 3:
Pin Diagram of AS5116 in SOIC8 Package



3.2 Pin Description AS5116

Figure 4:
Pin Description of AS5116 in SOIC8 Package

Pin Number	Pin Name	Pin Type	Description
1	SINP	Analog Out	Buffered sine channel, positive output
2	SINN CM_SIN	Analog Out	Buffered sine cannel, inverted output (default). Common mode level for sine channel (optional).
3	VSS	Supply	Common ground
4	VDD5	Supply	Supply voltage
5	VDD3	Analog Out	On chip low-dropout regulator output voltage. Requires an external 1 µF decoupling capacitor
6	UART DIAG	Digital I/O Digital Out	Communication Pin for OTP programming (default). Diagnostic output for on-chip diagnostic functions. This pin always has to be tied to VDD5 with the pull up resistor R_{pu}.
7	COSN CM_COS	Analog Out	Buffered cosine channel, inverted output (default). Common mode level for cosine channel (optional).
8	COSP	Analog Out	Buffered cosine channel, positive output

4 Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under “Operating Conditions” is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 5:
Absolute Maximum Ratings of AS5116

Symbol	Parameter	Min	Max	Unit	Comments
Electrical Parameters					
VDD5	DC Voltage at VDD5 pin	-0.3	7	V	
VREG	DC Voltage at VDD3 pin	-0.3	5	V	
VSS	DC Voltage at VSS pin	-0.3	0.3	V	
V_{IN}	Input Pin Voltage to Ground	-0.3	VDD5 + 0.3	V	
I_{SCR}	Input Current (latch-up immunity)	± 100		mA	AEC-Q100-004
Continuous Power Dissipation					
P_T	Total Power Dissipation		150	mW	
Electrostatic Discharge					
ESD_{HBM}	Electrostatic Discharge HBM	± 2000		V	AEC-Q100-002
ESD_{CDM}	Electrostatic Discharge CDM	± 500		V	AEC-Q100-011
Temperature Ranges and Storage Conditions					
T_A	Operating Ambient Temperature	-40	150	°C	
T_J	Operating Junction Temperature		165	°C	
T_{A_PROG}	Ambient Temperature during OTP Programming	0	45	°C	
T_{STRG}	Storage Temperature Range	- 55	150	°C	
T_{BODY}	Package Body Temperature		260	°C	IPC/JEDEC J-STD-020 (1)
RH_{NC}	Relative Humidity (non-condensing)	5	85	%	
MSL	Moisture Sensitivity Level	3			Represents a maximum floor lifetime of 168 h
Temperature Soldering					
T_{PEAK}	Peak Temperature		260	°C	IPC/JEDEC J-STD-020
t_{WELL}	Well Time above 217 °C	30	45	s	

(1) The reflow peak soldering temperature (body temperature) is specified according to IPC/JEDEC J-STD-020 “Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices.” The lead finish for Pb-free leaded packages is “Matte Tin” (100 % Sn)

5 Electrical Characteristics

All limits are guaranteed over the operating temperature range (-40°C to 150°C) and lifetime, unless otherwise noticed. The parameters with Min and Max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

Figure 6:
Electrical Characteristics of AS5116

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Operating Conditions						
VDD5	Positive Supply Voltage	5.0 V operation mode	4.5	5.0	5.5	V
VDD3	Positive Supply Voltage in 3V3 Mode	3.3 V operation mode, LDO shorted	3.0	3.3	3.6	V
VDDBURN	Positive Supply Voltage	Supply voltage required for programming in 3V3 operation	3.3		3.5	V
VREG	Regulated Voltage	Voltage at Vreg if sensor is in 5 V operation mode	3.2	3.4	3.6	V
VSS	Negative Supply Voltage		0		0	V
IDD	Supply Current	Depends on gain setting			17	mA
T_{POWER_ON}	Power Up Time				10	ms
Input Parameter						
BIN	Limit for Target Bz Peak Field	At the Hall element position inside the sensor	10		100	mT
VMAX	Maximum Rotation Speed		-30000		30000	RPM
Output Parameter						
VOUT	Analog Output Voltage Amplitude Limits		GND + 0.25		VDD – 0.5	V
VCM1	Output Common Mode Level	Default level	1.275	1.375	1.475	V
VCM2	Output Common Mode Level		1.975	2.125	2.275	V
IOUT	Analog Output Load Current		-1		1	mA
CLOAD	Analog Output Capacitive Load				10	nF
Digital IO Parameter - DIAG						
V_IH	High Level Input Voltage	UART mode enabled (default)	0.7 * VDD5			V
V_IL	Low Level Input Voltage	UART mode enabled (default)			0.3 * VDD5	V
V_OH	High Level Output Voltage		VDD5 - 0.5			V
V_OL	Low Level Output Voltage				VSS + 0.4	V
C_L	Capacitive Load				50	pF
I_OUT_5V	Output Current 5V Operation				4	mA

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_OUT_3V	Output Current 3V3 Operation				2	mA
External Components						
R_{pu}	Pull up resistor in Figure 28 and Figure 29		10		100	kΩ
C_{out}	Output capacitors C1, C2, C3 and C4 in Figure 28 and Figure 29		0.5		10	nF

Figure 7:
Key Performance Parameters

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
INL_error (1)	Based on Sensor Internal Imperfections	-40 °C to 150 °C		0.5	1	degree
INL_error + Magnet (1)	Non-Linearity @ Displacement of Magnet and Temperature -40 °C to 150 °C	Assuming N35H Magnet (D=8 mm, H=3 mm) 500 µm displacement in x and y. Package to magnet gap 1700 µm		0.6	1.2	degree
SINCOS_ORT_error (2)	Orthogonality Error. Defines deviation of ideal phase shift of 90° between SIN and COS output signals	Based on maximum INL_error.	-2		2	degree
SINCOS_GAIN_error (2)	Gain Mismatch between SIN and COS channel	Based on maximum INL_error	-3.5		3.5	%
NOISE5V	Maximum RMS Noise. Depending on Gain Configuration (see Figure 10).	VDD = 5 V (5 V operation)			2.47	mVrms
NOISE3V3	Maximum RMS Noise. Depending on Gain Configuration (see Figure 10).	VDD = 3.3 V (3V3 operation)			2.61	mVrms
TD	Propagation Delay		12	16	20	µs
M	Magnetic Sensitivity Differential Output Mode		8		60	mV/mT
GV	Gain Variation at 25 °C	Variation of selected absolute GAIN (Part to Part Variation)	-16		16	%
GV_Temp_AS5116 (3)	Gain Variation Over Temperature	-40°C to 150 °C (Gain drift of one single sensor)	-0.105	-0.05	0	%/°C
GV_Temp_AS5116A (4)	Gain Variation Over Temperature	-40 °C to 150 °C (Gain drift of one single sensor)	-0.075	-0.03	0	%/°C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
GV_Temp_AS5116B (5)	Gain Variation Over Temperature	-40 °C to 150 °C (Gain drift of one single sensor)	-0.075	-0.03	0	%/°C
HR	Hall Radius	Radius of circular Hall array		1.1		mm

(1) Valid for Differential Output Mode. Assuming a minimum $Vout_{P2P}$ voltage of 3000 mV. Differential consideration of output signals required.

(2) Worst case linearity error is limited and guaranteed by INL_max parameter.

(3) Parameter guaranteed by design. Worst case figure, valid for Gain_Code 24.

(4) Parameter guaranteed by design. Worst case figure, valid for Gain_Code 12.

6 Functional Description

The Hall-based magnetic position sensor, uses an array of planar sensors that convert the magnetic field component Bz perpendicular to the surface of the chip into a voltage. The signals coming from the Hall sensors are amplified, filtered and buffered before the information is available as sine and cosine voltages on the output. Gain respectively sensitivity of the complete signal path, can be defined by programming the Gain_Code in CONFIG2 register. The sensor is as well programmable to provide a full differential or single ended signal on the output.

Settings are in system programmable through an UART single wire interface. For achieving a high ASIL in the application, the sensor is fully supporting the ISO26262 implementation process (Detailed information on request).

6.1 IC Power Management

The AS5116 can be either powered from a 5.0 V supply using the on-chip low-dropout regulator (LDO) or from a 3.3 V voltage supply. The LDO (low-dropout) regulator is not intended to power any other loads, and it needs a 1 µF capacitor to ground located close for decoupling as shown Figure 8.

In 3V3 operation, VDD and VREG tied together.

Figure 8:
Pin Configuration in 5 V Operation Mode

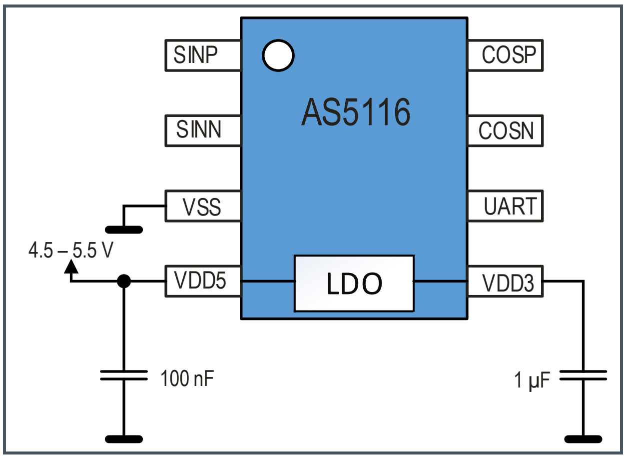
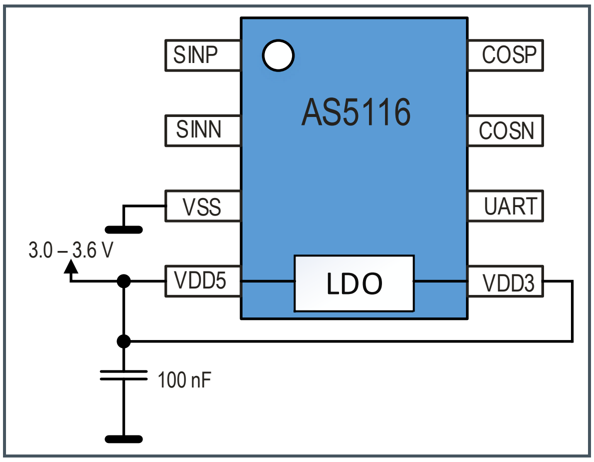


Figure 9:
Pin Configuration in 3V3 Operation Mode



6.2 Gain Configuration

The amplitudes of the output voltages are directly proportional to the Bz field of the magnet above the sensor. The user can select the appropriate Gain Setting out of 25 possible steps.

Figure 10:
Gain Table(1)

Gain_Code CONFIG2 Register 0x17 <1:5>	GAIN [mV/mT] 5V Operation Mode	Maximum RMS-Noise [mV] 5V Operation Mode	GAIN [mV/mT] 3V3 Operation Mode	Maximum RMS-Noise [mV] 3V3 Operation Mode
0	8	0.51	8	0.51
1	10	0.51	10	0.68
2	12	0.51	12	0.72
3	13.5	0.68	13	1.53
4	16	0.68	16	0.96
5	18	0.72	18	1.08
6	20	0.96	19.5	1.14
7	22.5	1.08	21.5	1.35
8	24	0.96	23	1.35
9	26.5	1.25	26	1.53
10	26.5	1.65	26.5	1.65
11	29	1.35	28.5	1.65
12	31.5	1.25	30	1.74
13	32.5	2.02	32.5	2.02
14	35	1.35	35	2.02
15	35.5	1.65	35.5	2.20
16	39	1.53	38	2.20
17	40	2.47	40	2.47
18	42.5	1.65	42.5	2.47
19	45	1.74	45	2.61
20	47.5	2.20	45	2.61
21	52	2.02	45	2.61
22	53.5	2.47	45	2.61
23	57	2.20	45	2.61
24	60	2.32	45	2.61

(1) Gain table representing typical values, maximum Part-to-Part gain variation GV is separately specified.

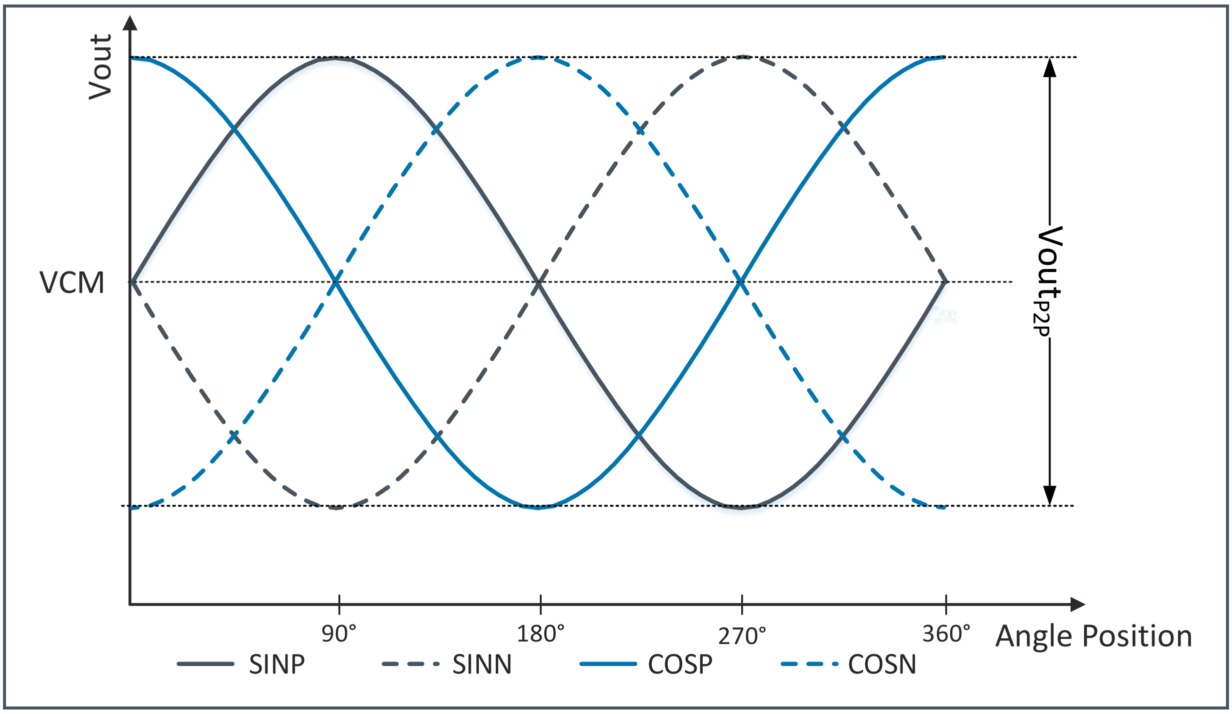
6.3 Behavior of Sensor Outputs

Following graphs show the behavior at different output settings over one mechanical 360° rotation.

6.3.1 Differential Output Mode (Default Setting)

Positive SINP and COSP signals in combination with inverted SINN and COSN are provided via the output pins of the sensor. High immunity against common cause errors, evoked by the environment of the sensor, is given due to the differential signal transmission. Fully differential signal inputs are required to digitize the analog outputs. VCM is defined via OTP programming.

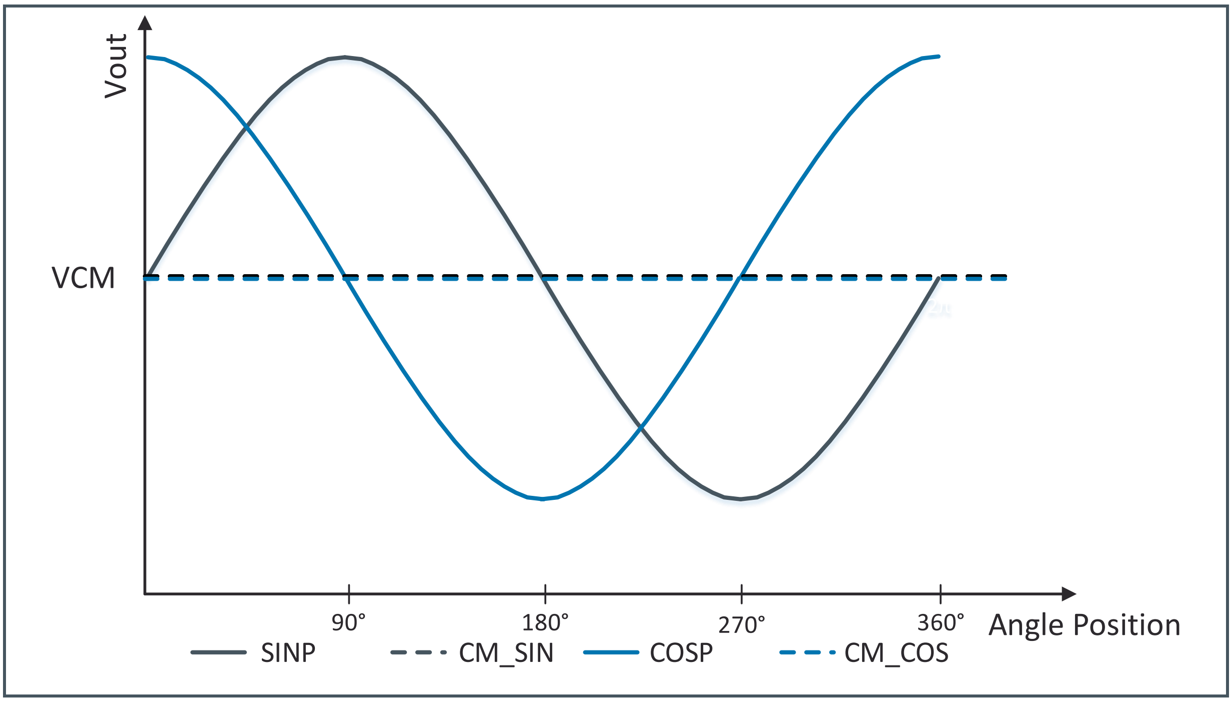
Figure 11:
Differential Output Behavior



6.3.2 Single-Ended Output Mode

Positive SINP and COSP signals in combination with the configured VCM level on CM_SIN and CM_COS are provided via the output pins of the sensor. To achieve best accuracy performance, fully differential signal inputs are recommended to digitize the analog outputs. As an alternative, single-ended measurement of all output signals with associated data processing (SINP - CM_SIN, COSP - CM_COS) is as well possible.

Figure 12:
Single-Ended Output Behavior

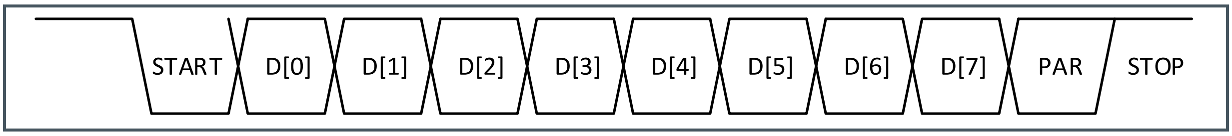


7 Digital Interface – UART

The AS5116 is equipped with an UART interface, which allows reading and writing the registers as well as permanently programming the non-volatile memory (OTP). By default (Diag_EN = 0) the AS5116 is in the so-called Communication Mode and the UART is connected to pin 6. In this mode, it is possible to configure the register settings.

The UART interface allows reading and writing two consecutive addresses. The standard UART sequence consists of four frames. Each frame begins with a start bit (START), which is followed by 8 data bits (D[0:7]), one parity bit (PAR), and a stop bit (STOP), as shown in Figure 13.

Figure 13:
UART Frame



The PAR bit is and Even Parity, calculated over the data bits (D[0:7]). Each frame is transferred LSB first.

Figure 14:
Standard UART Sequence

Frame Number	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
1	0x55							
2	R/W	ADDRESS						
3	DATA1							
4	DATA2							

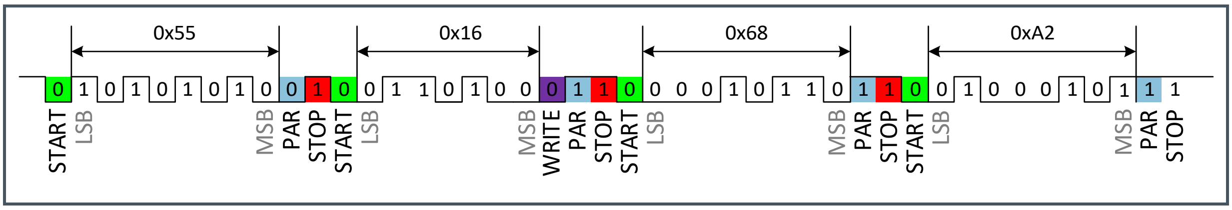
The first frame is the synchronization frame and consists of D[0:7] = 0x55 followed by the parity bit (PAR = 0) and the stop bit. This frame synchronizes the baud rate between the AS5116 and the UART Master. The UART baud rate have to stay in a range of 1.1 – 70 kbit/s.

The second frame contains the read/write command (Write: D[7] = 0; Read: D[7] = 1) and the address of the register (ADDRESS: D[0:6]).

The content of the third and fourth frames (DATA1 and DATA2) will be written to or read from the location specified by ADDRESS and ADDRESS+1.

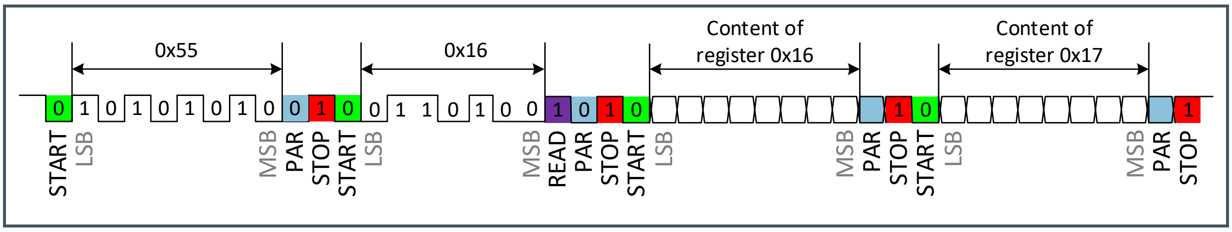
Figure 15 and Figure 16 show examples of Read and Write UART frame.

Figure 15:
UART – Write Example



In this UART – Write example the UART Master writes to CONFIG1 register 0x16 – 0x68 and to CONFIG2 register 0x17 – 0xA2.

Figure 16:
UART – Read Example



In this UART – Read example the UART Master reads from CONFIG1 register 0x16 and CONFIG2 register 0x17.

7.1 Register Description

The table below shows all accessible digital registers implemented in the AS5116 sensor.

Figure 17:
Register Overview

Address	Name	Function	Default	Description
0x01	UART_ERROR	R	0x00	Indication of framing and parity errors
0x03	P2RAM_CONTROL	R/W	0x00	P2RAM handling
0x16	CONFIG1	R/W/P	0x00	Configuration of output setting
0x17	CONFIG2	R/W/P	0x00	Configuration of gain and diagnostic mode
0x18	CUST_CHIP_ID1	R/W/P	0x00	Spare bits for custom chip ID
0x19	CUST_CHIP_ID2	R/W/P	0x00	Spare bits for custom chip ID
0x1A	CUST_CHIP_ID3	R/W/P	0x00	Spare bits for custom chip ID
0x1B	ECC	R/W/P	0x00	Configuration of ECC function
0x50	ECC_CHECKSUM	R	0x00	Calculated ECC checksum based on actual register settings
0x51	ECC_STATUS	R	0x00	Indicates actual ECC status if ECC function is enabled

7.1.1 UART_ERROR Register – 0x01

In the UART_ERROR Register problems during UART communication are indicated. Error bits are sticky and clear on read.

UART_SYNC Bit indicates a problem with the synchronization frame. This is usually the case if the Baudrate was not defined correctly. Baudrate window is defined from 1.1 kbit/s to 70 kbit/s.

UART_PARITY bit indicates a parity error during a UART-Write command. UART_FRAME bit indicates an error, if after synchronization the UART line stays low for more than twice the usual expected time (too long frame).

Figure 18:
UART_ERROR Register – 0x01

Bit Position	Bit Name	Default	Description
0	UART_SYNC	0	UART synchronization error
1	UART_PARITY	0	UART parity error
2	UART_FRAME	0	UART frame too long error

7.1.2 P2RAM_CONTROL Register – 0x03

The P2RAM_CONTROL Register handles all processes in combination with the OTP memory.

Description of OTP related commands and definition of the programming flow chart is given in section Configuration and Programming.

Figure 19:
P2RAM_CONTROL Register

Bit Position	Bit Name	Default	Description
0:1	State	0	P2RAM state
2	LOAD	0	Load latch from fuse array
3	BURN	0	Burn command to permanently store setting within OTP memory
6	GLOAD		Enabled guard band mode to check burn quality

7.1.3 CONFIG1 Register – 0x16

In CONFIG1 Register includes several possible configurations of the sensor outputs, like common mode level and pin configuration

Figure 20:
CONFIG1 Register

Bit Position	Bit Name	Default	Description
0:2	n.a.	0	Not applicable
3	VCM_Level	0	Output common mode level (0: VCM = 1.375 V, 1: VCM =2.125 V)
4	n.a.	0	Not applicable
5	CM_COS	0	Defines the output function of pin 7 (0: COSN, 1: CM_COS)
6	CM_SIN	0	Defines the output function of pin 2 (0: SINN, 1: CM_SIN)
7	INVERT_CH	0	Inverts the sign of the output channels

7.1.4 CONFIG2 Register – 0x17

CONFIG 2 Register includes the sensitivity settings and a bit to enable the diagnostic mode.

Figure 21:
CONFIG2 Register

Bit Position	Bit Name	Default	Description
0	Diag_EN	0	Enables diagnostic mode when the bit is set to "1"
1:5	Gain_Code	0	Defines the sensitivity of the sensor
6:7	n.a.	0	Not applicable

7.1.5 CUST_CHIP_ID1 Register – 0x18

Figure 22:
CUST_CHIP_ID1

Bit Position	Bit Name	Default	Description
0:7	CUST_CHIP_ID1	0	Spare bits for customized tracking information

7.1.6 CUST_CHIP_ID2 Register – 0x19

Figure 23:
CUST_CHIP_ID2

Bit Position	Bit Name	Default	Description
0:7	CUST_CHIP_ID2	0	Spare bits for customized tracking information

7.1.7 CUST_CHIP_ID3 Register – 0x1A

Figure 24:
CUST_CHIP_ID3

Bit Position	Bit Name	Default	Description
0:7	CUST_CHIP_ID3	0	Spare bits for customized tracking information

7.1.8 ECC Register – 0x1B

Within ECC (Error-Correction Code) register, the ECC function is configured and enabled.

Figure 25:
ECC Register

Bit Position	Bit Name	Default	Description
0:6	ECC_Chsum	0	ECC checksum programmed by user
7	ECC_EN	0	Enables ECC function

Figure 26:
ECC CHECKSUM

Bit Position	Bit Name	Default	Description
0:6	ECC_Chsum_calc	0	Internal calculated ECC checksum

Figure 27:
ECC STATUS

Bit Position	Bit Name	Default	Description
0	ECC_EN_after_check	0	ECC_EN after error correction
1:2	ECC_Error	0	ECC Error code: 0: P2RAM bytes in customer area are correct (or ECC_EN = 0) 1: Single bit error in P2RAM. P2RAM output corrected by ECC function 2: Two or more bits are defect in P2RAM block. No correction possible - major system error

8 Functional Safety

AS5116 is fully supporting the ISO26262 and enables applications to fulfill Automotive Safety Integrity Levels up to ASIL C.

8.1 Safety Manual

The safety manual, available upon request, contains all the necessary information for the system integrator, to integrate AS5116 in a safety related item.

AS5116 is supporting the ISO26262 as Safety Element out of Context (SEooC).

The safety manual includes the following information:

- Product development lifecycle
- Description of the technical safety concept on system level
- Detailed information of Assumption of Use of the element with respect to its intended use, which includes
  - System Safe State information
  - Fault Tolerant Time Interval
  - Coverage information

As part of the Safety Manual, the Verification and Safety Analysis Report includes following information:

- HW architectural metric results (Single Point Fault Metric)
- Description of verifications based on the ISO26262
- Detailed FMEDA

9 Application Information

Several wiring options and configurations of AS5116 are possible. The most likely used options are shown in the following section.

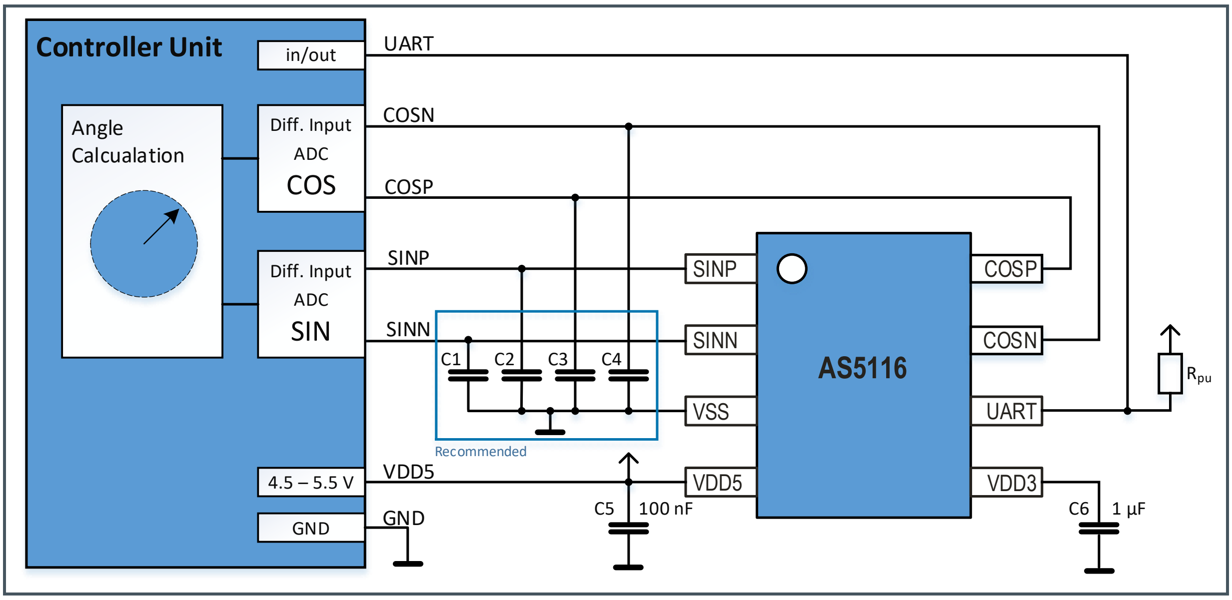
9.1 Differential Mode

By default, the configuration of the sensor is in differential output mode. Positive SINP and COSP signals, as well as the inverted SINN and COSN signals are provided.

This is the recommended output configuration, due to the best common mode rejection. Fully differential inputs are required on controller side. To improve the angle accuracy, a one-time end of line calibration of offset and gain error is recommended before calculating the angle position.

9.1.1 Minimum Wiring Diagram

Figure 28:
AS5116 Minimum Wiring Diagram, Differential Output Mode



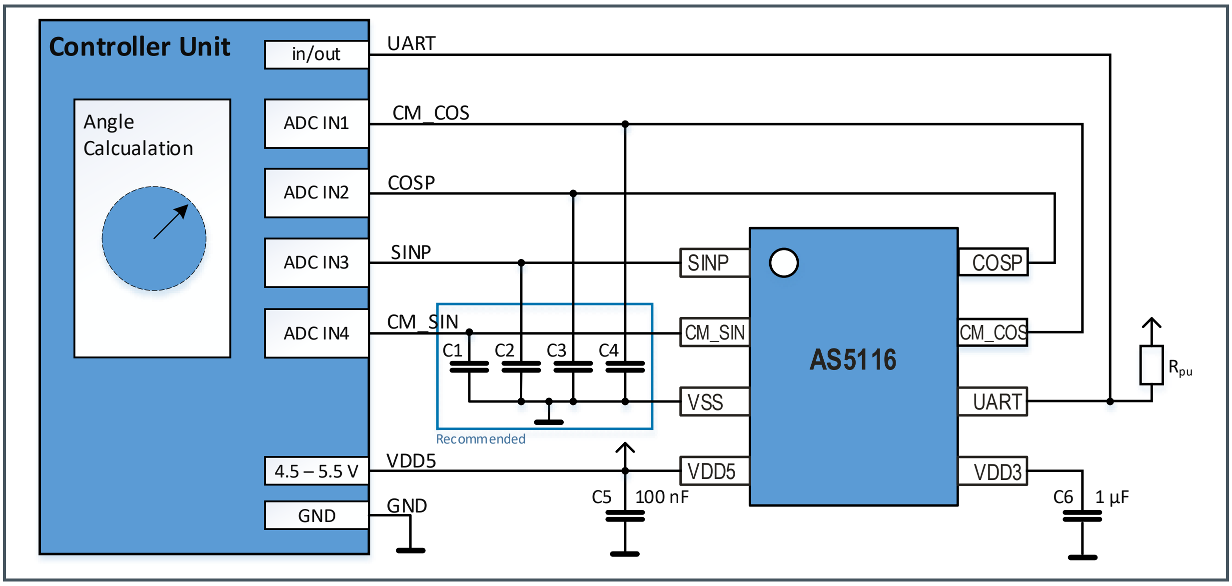
(1) C1=C2=C3=C3=C4=Cout
(2) Parameters for Cout and Rpu are described in chapter “Electrical Characteristics”

9.2 Single Ended Mode

In single-ended configuration, all voltage measurements are reverenced to VSS level. For safety reasons, it is recommended to check as well the levels of CM_SIN and CM_COS with separate analog inputs. The measured common mode voltages should be used to calculate the differential sine/cosine values. Otherwise, the signal common mode level has to be determined in the controller based on one sine/cosine period. To improve the angle accuracy, a one-time end of line calibration of offset and gain error is recommended before calculating the angle position.

9.2.1 Minimum Wiring Diagram

Figure 29:
AS5116 Minimum Wiring Diagram, Single Ended Output Mode



(1) C1=C2=C3=C3=C4=Cout
(2) Parameters for Cout and Rpu are described in chapter “Electrical Characteristics”

9.2.2 Output Amplitude Calculation

The output amplitude of sine and cosine signals are directly proportional to the selected GAIN setting and the Bz-Field of the available target magnet. Following equations explain how the calculation is done based on a typical example. Using that approach, a very convenient estimation of the output amplitudes is possible.

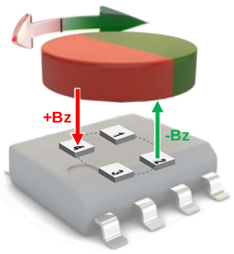
Equation 1: Vout Peak to Peak – Single Ended Input

$$Vout_{SE\_P2P} = 2 \cdot Bz_{max} \cdot GAIN$$

Equation 2: Vout Peak to Peak – Differential Input

$$Vout_{DIF\_P2P} = 4 \cdot Bz_{max} \cdot GAIN$$

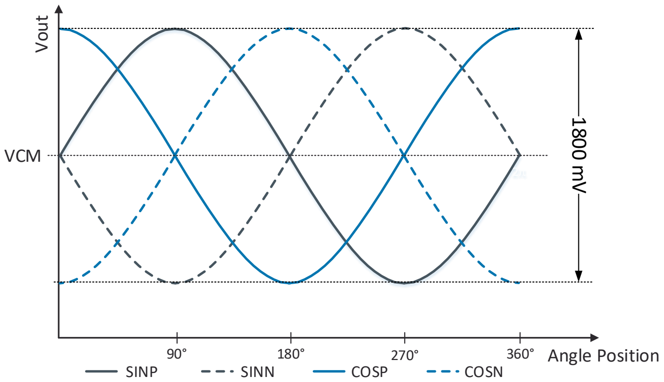
Output Amplitude Calculation – Example



Assumptions: Gain Setting = 30 mV/mT, Bz_{max} = 30 mT

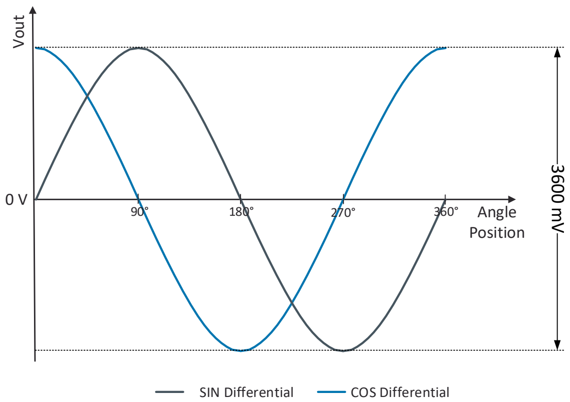
Equation 3:

$$\mathrm{Vout}_{\mathrm{SE\_P2P}} = 2 \cdot 30 \cdot 30 = 1800\ \mathrm{mV}$$



Equation 4:

$$Vout_{DIF\_P2P} = 4 \cdot 30 \cdot 30 = 3600\ mV$$



9.2.3 Diagnostic Mode

In default configuration, the sensor is in communication mode. Pin 6 acts as single wire UART interface connection and can be used to configure all relevant customer setting.

During the programming process, it is possible to enable the diagnostic function by programming the “Diag_EN” bit in the CONFIG2 Register – 0x17. In that case, pin 6 is acting as diagnostic output after the next power on reset of the sensor.

The diagnostic function checks if the status of the OTP register is still valid and correct. It is directly linked to the ECC_error status 1 and 2 (ECC_STATUS Register – 0x51).

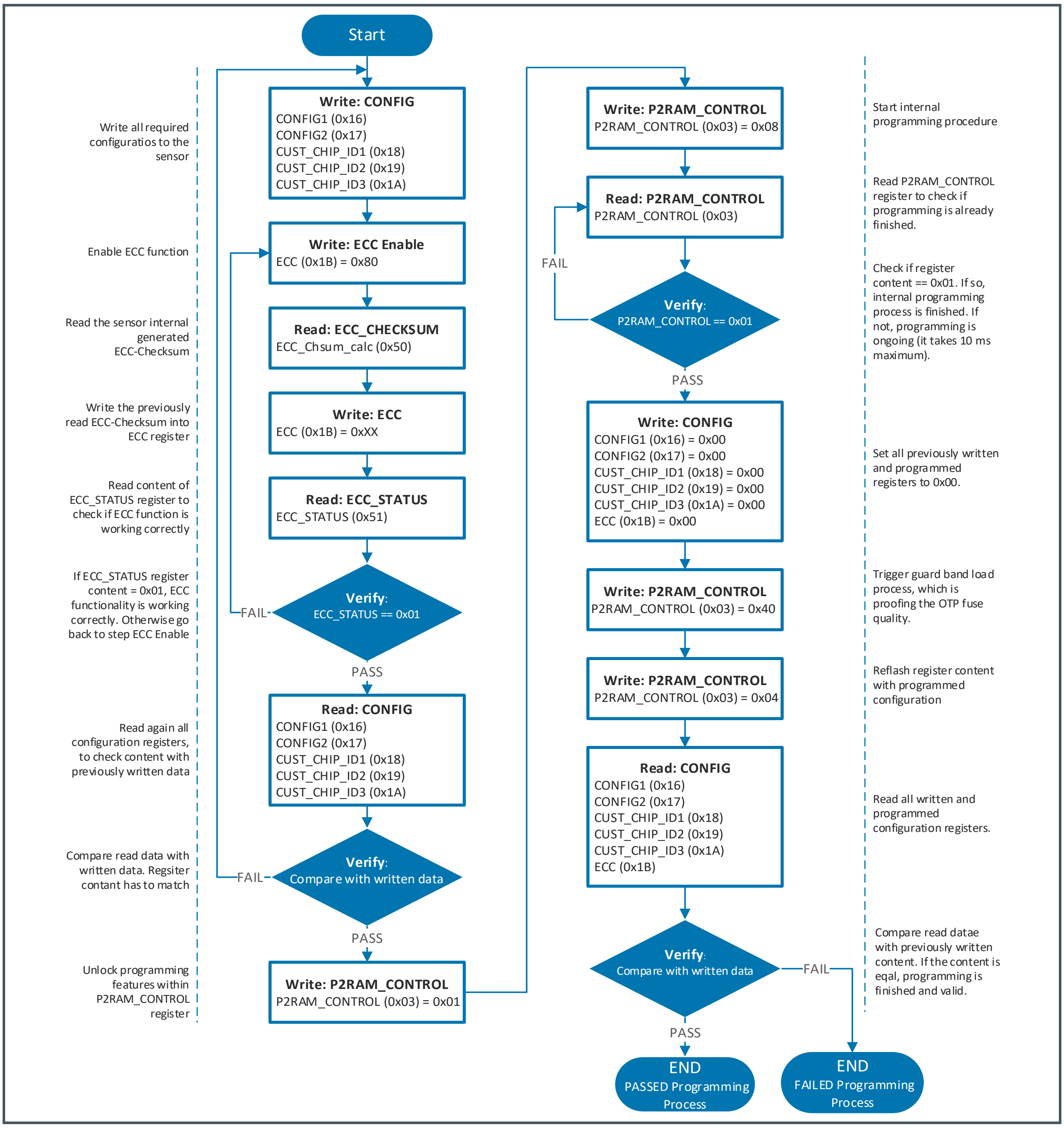
Figure 30:
DIAG Output State Definition

State of DIAG Pin 6	Output Level	Description
0	GND	OTP status ok
1	VDD	OTP error One or more bits flipped in OTP section. As result unexpected behavior of the sensor could occur.

10 Configuration and Programming

The non-volatile memory is used to permanently program the configuration. To program the nonvolatile memory, the UART interface is used. The programming could be performed either in 5 V or in 3V3 operation mode operation. Tighter limits of the supply voltage in 3V3 operation has to be considered (VDDBURN).

Figure 31:
AS5116 Programming Flow



11 Preconfigured Versions

Beside the fully flexible AS5116 version, further preconfigured variants with fixed CONFIG Register settings are available. By using an already programmed AS5116, no further OTP configuration of the sensor is possible.

11.1 AS5116A

AS5116A is configured in Single-Ended mode. SINN and COSN outputs represent the common mode voltage. A fixed gain configuration of 31.5 mV/mT is chosen (Gain_Code 12). OTP Diagnostic and internal ECC check are enabled and show the actual status on UART/DIAG pin.

Figure 32:
AS5116A – Register Settings

Gain_Code CONFIG2 <1:5>	DIAG_EN CONFIG2 <0>	VCM_Level CONFIG1 <3>	CM_COS, CM_SIN CONFIG1 <5:6>	INVERT_CH CONFIG1 <7>
12 – 31.5 mV/mT	Enabled	2.125 V	Enabled	Disabled

Figure 33:
AS5116A – Output Behavior

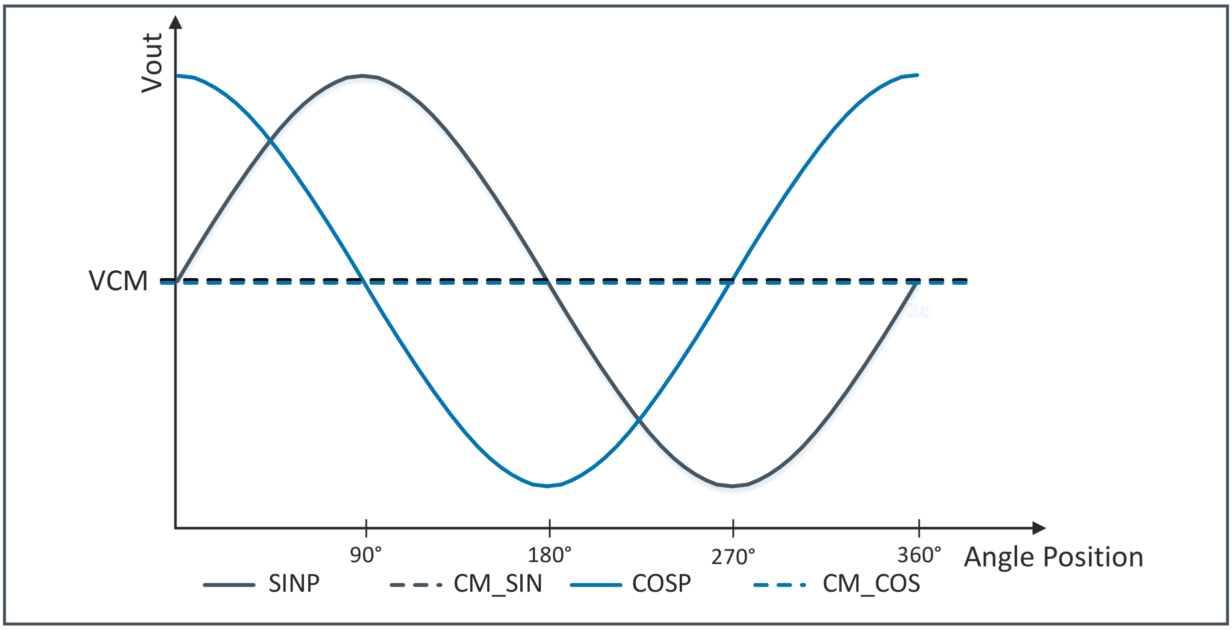
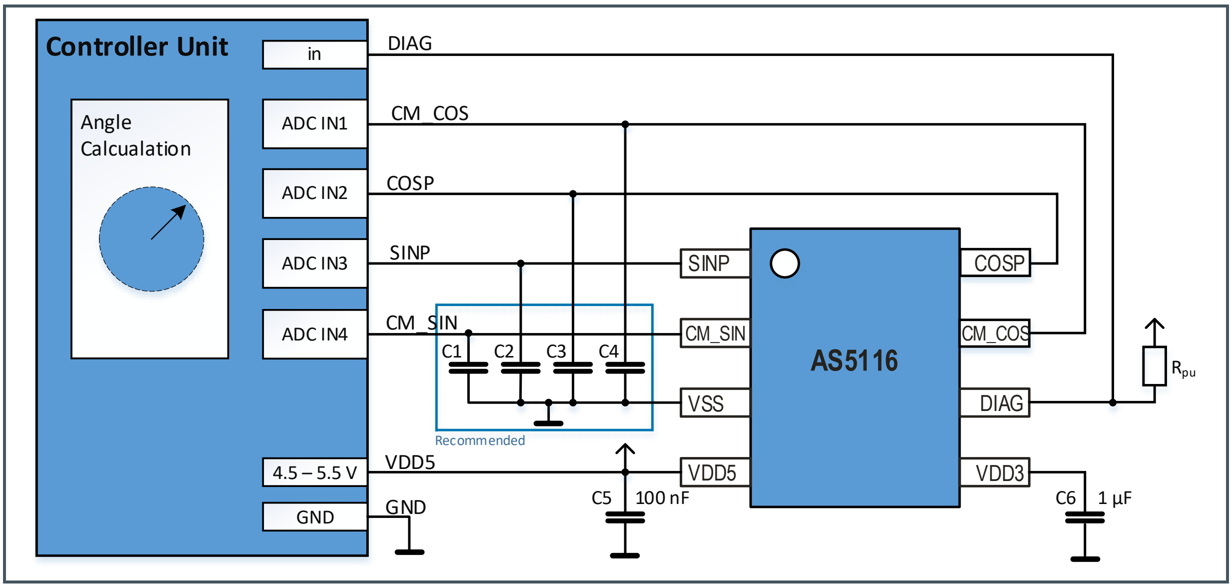


Figure 34:
AS5116A – Wiring Diagram, Single Ended Output Mode



(1) C1=C2=C3=C3=C4=Cout
(2) Parameters for Cout and Rpu are described in chapter “Electrical Characteristics”

11.2 AS5116B

AS5116B is configured in Differential mode. A fixed gain configuration of 31.5 mV/mT is chosen (Gain_Code 12). OTP Diagnostic and internal ECC check are enabled and show the actual status on UART/DIAG pin.

Figure 35:
AS5116B – Register Settings

Gain_Code CONFIG2 <1:5>	DIAG_EN CONFIG2 <0>	VCM_Level CONFIG1 <3>	CM_COS, CM_SIN CONFIG1 <5:6>	INVERT_CH CONFIG1 <7>
12 – 31.5 mV/mT	Enabled	2.125 V	Disabled	Disabled

Figure 36:
AS5116B – Output Behavior

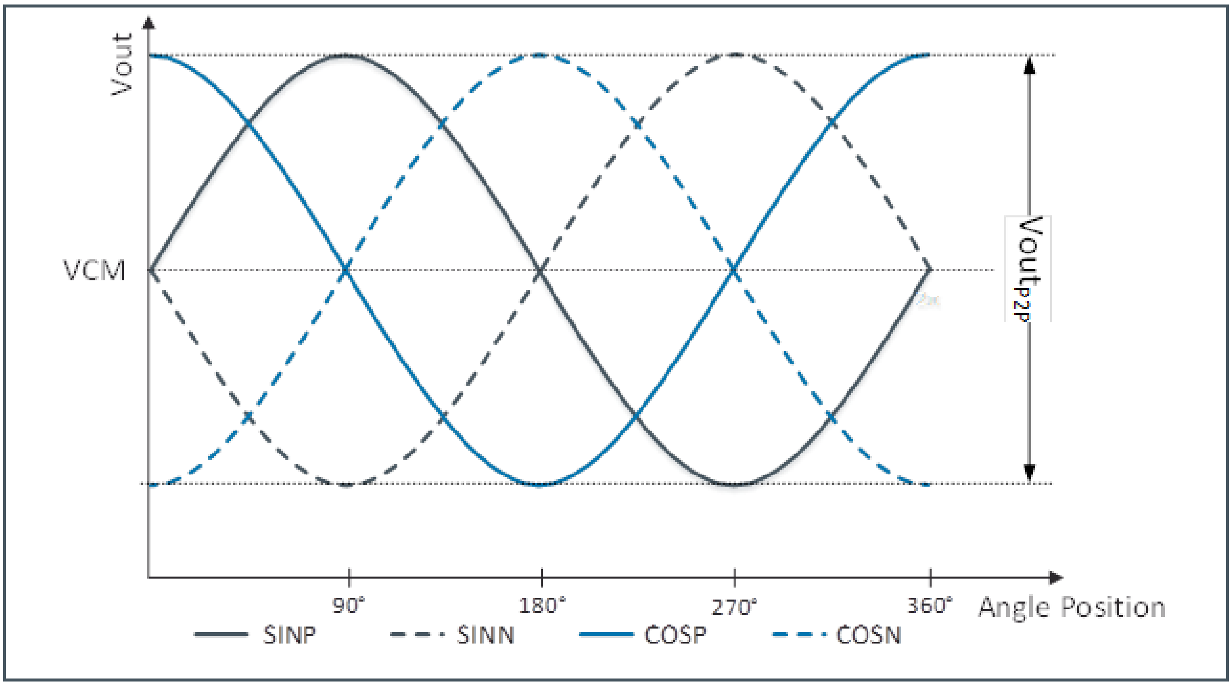
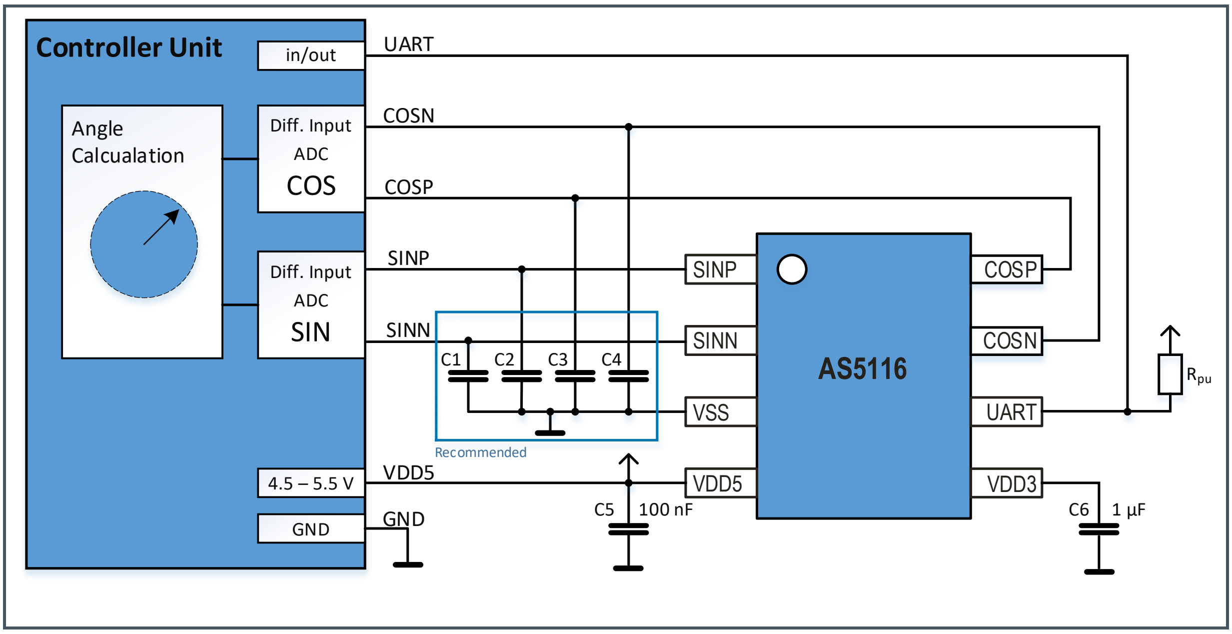


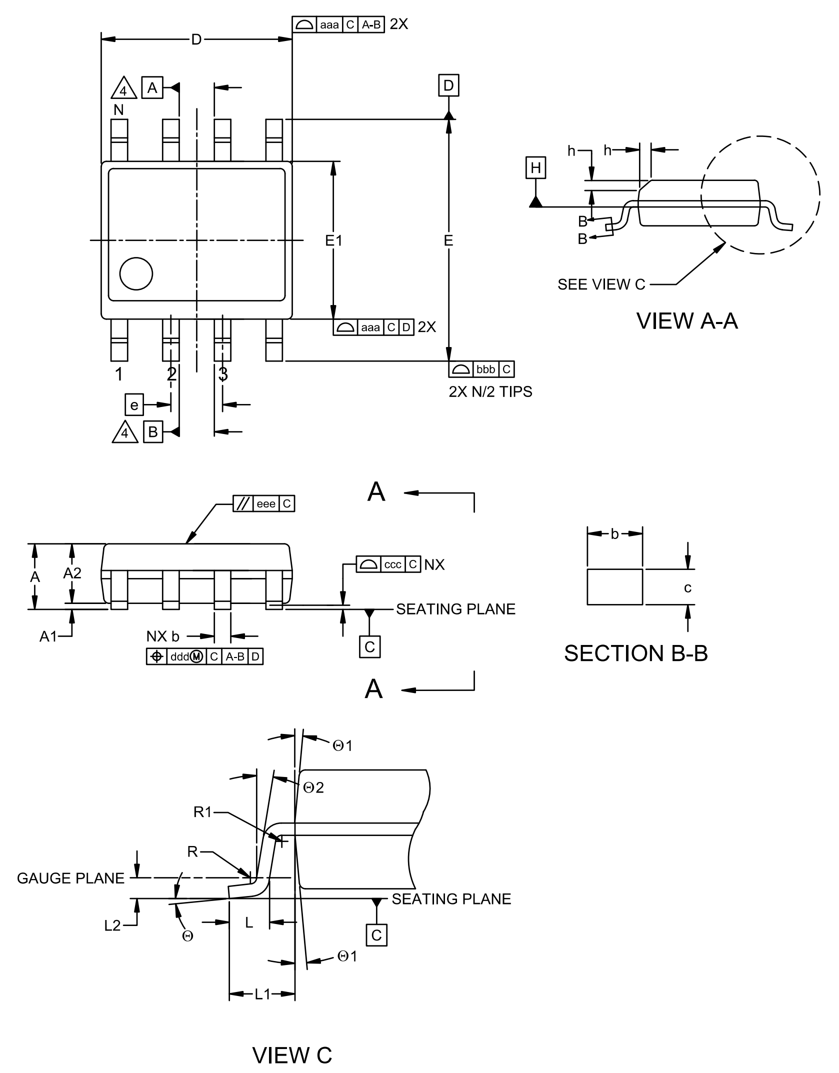
Figure 37:
AS5116B – Wiring Diagram, Differential Output Mode



(1) C1=C2=C3=C3=C4=Cout
(2) Parameters for Cout and Rpu are described in chapter "Electrical Characteristics"

12 Package Drawings & Markings

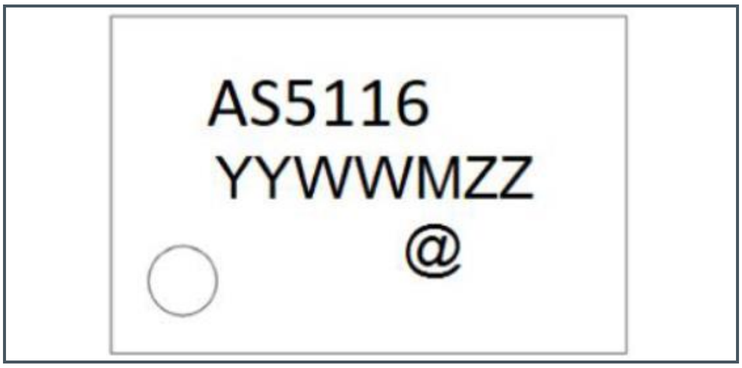
Figure 38:
SOIC8 Package Outline Drawing



Ref.	Min	Nom	Max
A	-	-	1.75
A1	0.10	-	0.25
A2	1.25	-	-
b	0.31	-	0.51
c	0.17	-	0.25
D	4.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
L	0.40	-	1.27
L1	1.04 REF		
L2	0.25 BSC		
R	0.07	-	-
R1	0.07	-	-
h	0.25	-	0.50
Θ	0°	-	8°
Θ2	5°	-	15°
Θ3	0°	-	-
aaa	-	0.10	-
bbb	-	0.20	-
ccc	-	0.10	-
ddd	-	0.25	-
eee	-	0.10	-
fff	-	0.15	-
ggg	-	0.15	-
N	8		

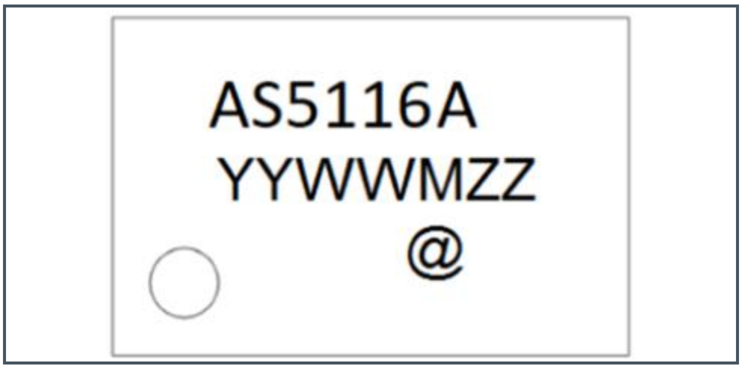
(1) All dimensions are in millimeters (angles in degrees).
(2) Dimensioning and tolerances conform to ASME Y14.5M-1994.
(3) N is the total number of terminals.
(4) Datum A&B to be determined by datum H.
(5) This package contains no lead (Pb).
(6) This drawing is subject to change without notice.

Figure 39:
SOIC8 Package Marking/Code for AS5116



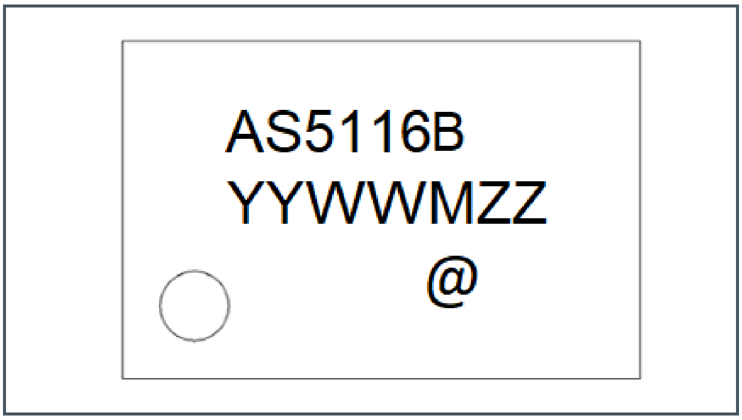
YY	Manufacturing Year
WW	Manufacturing Week
M	Assembly Plant Identifier
ZZ	Assembly Traceability Code
@	Sublot Identifier

Figure 40:
SOIC8 Package Marking/Code for AS5116A



YY	Manufacturing Year
WW	Manufacturing Week
M	Assembly Plant Identifier
ZZ	Assembly Traceability Code
@	Sublot Identifier

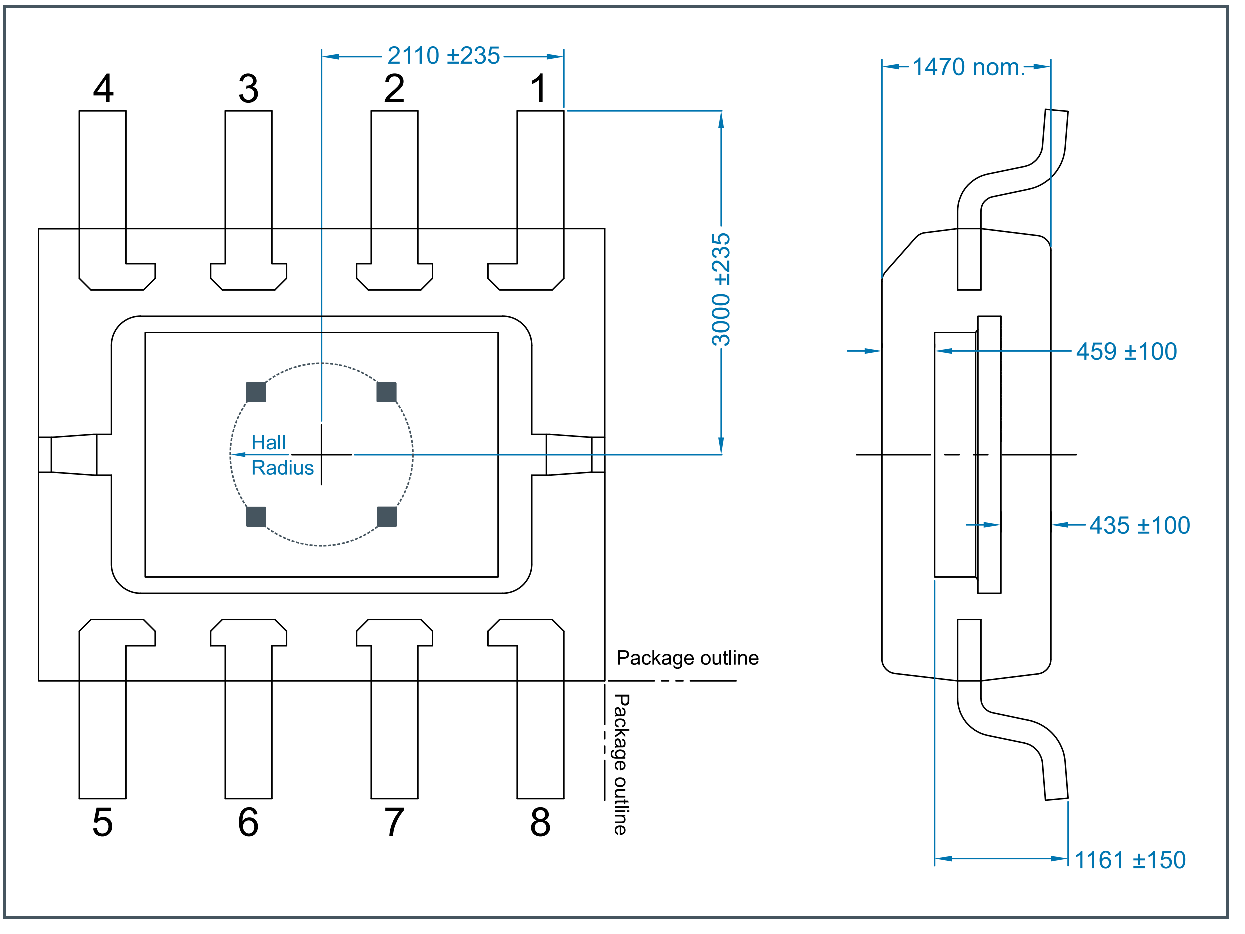
Figure 41:
SOIC8 Package Marking/Code for AS5116B



YY	Manufacturing Year
WW	Manufacturing Week
M	Assembly Plant Identifier
ZZ	Assembly Traceability Code
@	Sublot Identifier

13 Mechanical Data

Figure 42:
SOIC8 Die Placement and Hall Array Position



(1) All dimensions in micrometers
(2) The Hall array center is located in the center of the IC package. Hall array radius is 1.1 mm.
(3) Die thickness is 356 µm nominal
(4) Adhesive thickness 20 ± 10 µm
(5) Leadframe downset 200 ± 25 µm
(6) Leadframe thickness 200 ± 8 µm

14 Revision Information

Changes from previous version to current revision v4-00	Page
Updated Ordering information	2
Added Chapter 11.2 AS5116B	28
Added Figure 41	31

- Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
- Correction of typographical errors is not explicitly mentioned.

15 Legal Information

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ams Green (RoHS compliant and no Sb/Br/Cl): ams Green defines that in addition to RoHS compliance, our products are free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material) and do not contain Chlorine (Cl not exceed 0.1% by weight in homogeneous material).

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