PCI-5142 Specifications

2022-07-06

Contents

PCI-5142 Specifications

Definitions

Warranted specifications describe the performance of a model under stated operating conditions and are covered by the model warranty. Warranted specifications account for measurement uncertainties, temperature drift, and aging. Warranted specifications are ensured by design or verified during production and calibration.

Characteristics describe values that are relevant to the use of the model under stated operating conditions but are not covered by the model warranty.

- **Typical** specifications describe the performance met by a majority of models.
- **Nominal** specifications describe an attribute that is based on design, conformance testing, or supplemental testing.
- **Measured** specifications describe the measured performance of a representative model.

Specifications are **Typical** unless otherwise noted.

Conditions

Specifications are valid under the following conditions unless otherwise noted.

- All filter settings
- All impedance selections
- Sample clock set to 100 MS/s

Vertical

Analog Input (Channel 0 and Channel 1)

Number of channels	Two (simultaneously sampled)
Connector	BNC

Impedance and Coupling

Input impedance (software-selectable)	50 Ω ± 2.0% 1 MΩ ± 0.75% in parallel with a nominal capacitance of 27 pF ± 2 pF
Input coupling (software-selectable)	AC[1] DC GND

Voltage Levels

Range (V_{pk-pk})	Vertical Offset Range	
	50 Ω	1 MΩ
0.2 V	±0.1 V	
0.4 V	±0.2 V	
1 V	±0.5 V	
2 V	±1 V	
4 V	±2 V	
10 V	—	±5 V

Range (V_{pk-pk})	Vertical Offset Range	
	50 Ω	1 MΩ
20 V	—	—

Table 1. Full Scale (FS) Input Range and Programmable Vertical Offset

Maximum input overload	
50 Ω	7 V RMS with |Peaks| ≤10 V
1 MΩ	|Peaks| ≤42 V

Accuracy

Resolution	14 bits

Range (V_{pk-pk})	50 Ω	1 MΩ
0.2 V and 0.4 V	±(0.65% of input + 2.0 mV)	
1 V	±(0.65% of input + 2.0 mV)	
2 V	±(0.65% of input + 2.2 mV)	
4 V	±(0.65% of input + 8.0 mV)	
10 V	±(0.65% of input + 10.0 mV)	
20 V	—	±(0.65% of input + 15.0 mV)

Table 2. DC Accuracy (Programmable Vertical Offset = 0 V)[2], Warranted

Programmable vertical offset accuracy[2]	±0.5% of offset setting

Range (V_{pk-pk})	50 Ω	1 MΩ
0.2 V, 0.4 V, 1 V, and 2 V	±(0.057% of Input + 0.006% of FS + 100 µV) per °C	
4 V, 10 V	±(0.057% of Input + 0.006% of FS + 900 µV) per °C	
20 V	—	±(0.057% of Input + 0.006% of FS + 900 µV) per °C

Table 3. DC Drift, Nominal

AC amplitude accuracy[2]	
50 Ω	±0.06 dB (±0.7%) at 50 kHz
1 MΩ	±0.09 dB (±1.0%) at 50 kHz

Crosstalk[3]	≤-100 dB at 10 MHz

Bandwidth and Transient Response

Bandwidth (±3 dB, filters off)[4]	
0.2 V_{pk-pk} input range	80 MHz up to 40 °C, warranted[5]
All other input ranges	100 MHz, warranted

Rise/fall time	
0.2 V_{pk-pk} input range	4.2 ns
All other input ranges	3.5 ns

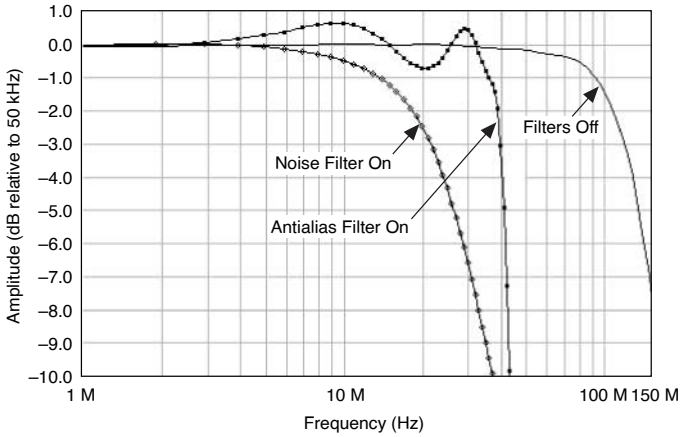
Bandwidth limit filters[6]	
Noise filter	20 MHz
	2-pole Bessel filter
Anti-alias Filter	40 MHz (-6 dB)
	35 MHz (±3 dB), warranted
	6-pole Chebyshev filter

AC coupling cutoff (-3 dB)	12 Hz [7]

Filter Settings	Input Range (V_{pk-pk})	50 Ω and 1 MΩ
Filters off	0.2 V	±0.4 dB (DC to 20 MHz) ±1 dB (20 MHz to 40 MHz)
	All other input ranges	±0.4 dB (DC to 20 MHz) ±1 dB (20 MHz to 50 MHz)
Anti-alias filter on	All input ranges	±1.2 dB (DC to 16 MHz) ±1.6 dB (16 MHz to 32 MHz)

Table 4. Passband Flatness[4]

Figure 1. PCI-5142 Frequency Response, Measured



Spectral Characteristics

Input Range (V_{pk-pk})	50 Ω	1 MΩ
0.2 V	75 dBc	70 dBc
0.4 V	75 dBc	70 dBc
1 V	75 dBc	70 dBc

Input Range (V_{pk-pk})	50 Ω	1 MΩ
2 V	75 dBc	70 dBc
4 V	65 dBc	70 dBc
10 V	65 dBc	60 dBc
20 V	—	60 dBc

Table 5. Spurious-Free Dynamic Range (SFDR) with Harmonics[8]

Input Range (V_{pk-pk})	50 Ω	1 MΩ
0.2 V	-75 dBc	-68 dBc
0.4 V	-75 dBc	-68 dBc
1 V	-75 dBc	-68 dBc
2 V	-73 dBc	-68 dBc
4 V	-63 dBc	-68 dBc
10 V	-63 dBc	-58 dBc
20 V	—	-58 dBc

Table 6. Total Harmonic Distortion (THD)[9]

Intermodulation distortion[10]	-75 dBc

Input Range (V_{pk-pk})	50 Ω		1 MΩ	
	Filters Off	Anti-alias Filter On	Filters Off	Anti-alias Filter On
0.2 V	60 dB	60 dB	56 dB	60 dB
0.4 V	62 dB	62 dB	61 dB	62 dB
1 V	62 dB	62 dB	62 dB	62 dB
2 V	62 dB	62 dB	62 dB	62 dB
4 V	—	—	61 dB	62 dB

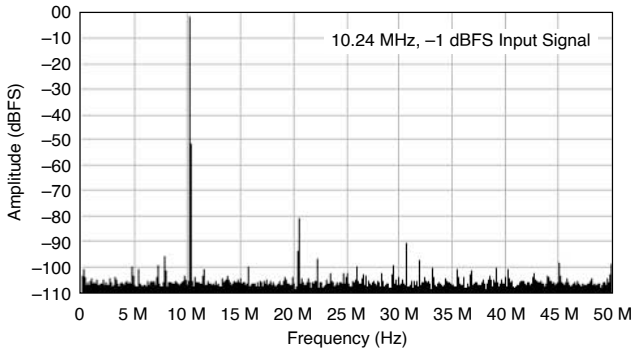
Table 7. Signal-to-Noise Ratio (SNR)[11]

Input Range (V_{pk-pk})	50 Ω		1 MΩ	
	Filters Off	Anti-alias Filter On	Filters Off	Anti-alias Filter On
0.2 V	60 dB	60 dB	56 dB	59 dB
0.4 V	62 dB	62 dB	60 dB	61 dB

Input Range (V_{pk-pk})	50 Ω		1 MΩ	
	Filters Off	Anti-alias Filter On	Filters Off	Anti-alias Filter On
1 V	62 dB	62 dB	61 dB	61 dB
2 V	62 dB	62 dB	61 dB	61 dB
4 V	—	—	60 dB	61 dB

Table 8. Signal to Noise and Distortion (SINAD)[12]

Figure 2. PCI-5142 Dynamic Performance, 50 Ω, 1 V Input Range, Measured



Input Range (V_{pk-pk})	50 Ω (V RMS)	1 MΩ (V RMS)
0.2 V	56 µV (0.028% of FS)	72 µV (0.036% of FS)
0.4 V	92 µV (0.023% of FS)	92 µV (0.023% of FS)
1 V	230 µV (0.023% of FS)	230 µV (0.023% of FS)
2 V	460 µV (0.023% of FS)	460 µV (0.023% of FS)
4 V	920 µV (0.023% of FS)	920 µV (0.023% of FS)
10 V	2.3 mV (0.023% of FS)	2.3 mV (0.023% of FS)
20 V	—	4.6 mV (0.023% of FS)

Table 9. RMS Noise (Noise Filter On)[13]

Input Range (V_{pk-pk})	50 Ω (V RMS)	1 MΩ (V RMS)
0.2 V	82 µV (0.041% of FS)	96 µV (0.048% of FS)
0.4 V	100 µV (0.025% of FS)	120 µV (0.030% of FS)
1 V	250 µV (0.025% of FS)	300 µV (0.030% of FS)
2 V	500 µV (0.025% of FS)	600 µV (0.030% of FS)
4 V	1 mV (0.025% of FS)	1.2 mV (0.030% of FS)
10 V	2.5 mV (0.025% of FS)	3 mV (0.030% of FS)

Input Range (V_{pk-pk})	50 Ω (V RMS)	1 MΩ (V RMS)
20 V	—	6 mV (0.030% of FS)

Table 10. RMS Noise (Anti-alias Filter On)[13]

Input Range (V_{pk-pk})	50 Ω (V RMS)	1 MΩ (V RMS)
0.2 V	90 µV (0.045% of FS)	110 µV (0.055% of FS)
0.4 V	100 µV (0.025% of FS)	160 µV (0.040% of FS)
1 V	250 µV (0.025% of FS)	300 µV (0.030% of FS)
2 V	500 µV (0.025% of FS)	600 µV (0.030% of FS)
4 V	1 mV (0.025% of FS)	1.6 mV (0.040% of FS)
10 V	2.5 mV (0.025% of FS)	3 mV (0.030% of FS)
20 V	—	6 mV (0.030% of FS)

Table 11. RMS Noise (Filters Off)[13]

Figure 3. PCI-5142 Spectral Noise Density on 0.2 V Input Range, Full Bandwidth, 50 Ω Input Impedance, Nominal

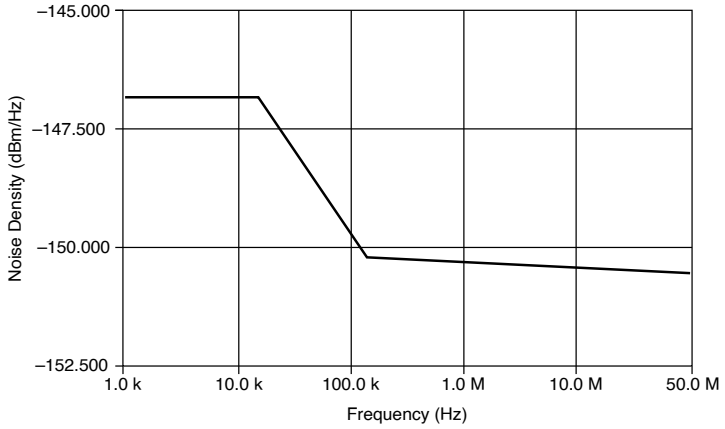
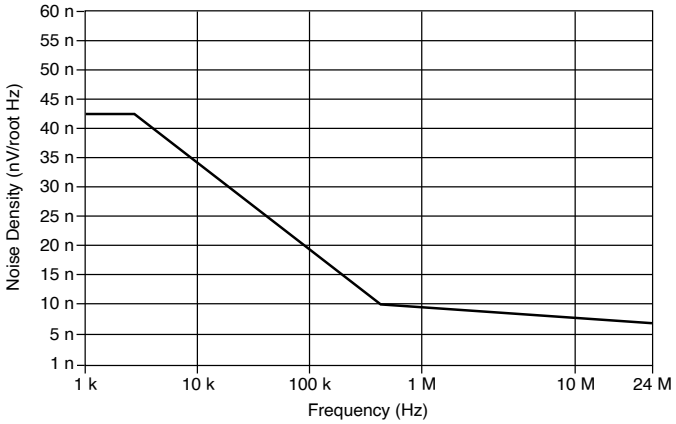


Figure 4. PCI-5142 Spectral Noise Density on 0.2 V Input Range, Noise Filter Enabled, 1 MΩ Input Impedance, Nominal



Horizontal

Sample Clock

Sources	
Internal	Onboard clock (internal VCXO)[14]
External	CLK IN (front panel SMB connector)

Onboard Clock (Internal VCXO)

Sample rate range	
Real-time sampling (single shot)	1.526 kS/s to 100 MS/s[15]
Random interleaved sampling (RIS)	200 MS/s to 2 GS/s in multiples of 100 MS/s

Phase noise density[16]	
100 Hz input frequency	<-100 dBc/Hz

1 kHz input frequency	<-120 dBc/Hz
10 kHz input frequency	<-130 dBc/Hz
Sample clock jitter[17]	≤1 ps RMS (100 Hz to 100 kHz) ≤2 ps RMS (100 Hz to 1 MHz)
Timebase frequency	100 MHz
Timebase accuracy	
Not phase-locked to Reference clock	±25 ppm, warranted
Phase-locked to Reference clock	Equal to the Reference clock accuracy
Sample clock delay range	±1 Sample clock period
Sample clock delay resolution	≤10 ps

Related information

- For more information about the Sample clock and decimation, refer to the NI High-Speed Digitizers Help, available online at ni.com/manuals.

External Sample Clock

Source	CLK IN (front panel SMB connector)
Frequency range[18]	
CLK IN	30 MHz to 105 MHz
Duty cycle tolerance	45% to 55%

Related information

- For more information about the Sample clock and decimation, refer to the NI High-Speed Digitizers Help, available online at ni.com/manuals.

Sample Clock Exporting

Destination	Maximum Frequency
CLK OUT (front panel SMB connector)	105 MHz
PXI_Trig <0..6> (backplane connector)[19]	20 MHz
PFI <0..1> (front panel 9-pin mini-circular DIN connector)[19]	25 MHz
RTSI <0..6>[19]	20 MHz

Table 12. Exported Sample Clock Destinations

Phase-Locked Loop (PLL) Reference Clock

Sources	RTSI 7 CLK IN (front panel SMB connector)
Frequency range	5 MHz to 20 MHz in 1 MHz increments[20]
Duty cycle tolerance	45% to 55%
Exported Reference clock destinations	CLK OUT (front panel SMB connector) PFI <0..1> (front panel 9-pin mini-circular DIN connector) RTSI <0..7>

CLK IN (Sample Clock and Reference Clock Input, Front Panel Connector)

Input voltage range	
Sine wave (V_{pk-pk})	0.65 V to 2.8 V (0 dBm to 13 dBm)
Square wave (V_{pk-pk})	0.2 V to 2.8 V
Maximum input overload[21]	7 V RMS with |Peaks| ≤10 V
Impedance	50 Ω
Coupling	AC

CLK OUT (Sample Clock and Reference Clock Output, Front Panel Connector)

Output impedance	50 Ω
Logic type	3.3 V CMOS
Maximum drive current	±48 mA

Trigger

Reference (Stop) Trigger

Trigger types	Edge Window

	Hysteresis Video Digital Immediate Software
Trigger sources	CH 0 CH 1 TRIG PXI_Trig <0..6> PFI <0..1> PXI Star Trigger Software RTSI <0..6>

Note Refer to the following sections and the **NI High-Speed Digitizers Help** for more information about what sources are available for each trigger type.

Time-to-Digital Conversion Circuit (TDC)	Onboard Clock	External Clock
On	100 ps	—
Off	10 ns	External clock period

Table 13. Time Resolution

TDC	Rearm Time
On	10 µs
Off	2 µs

Table 14. Minimum Rearm Time[22]

TDC	Onboard Clock	External Clock
On	10 µs to 171.79 s	—
Off	2 µs to 171.79 s	200 × **External Clock Period** to (2^{32} - 1) × **External Clock Period**

Table 15. Holdoff

Analog Trigger

Trigger types	Edge Window Hysteresis
Sources	CH 0 (front panel BNC connector) CH 1 (front panel BNC connector) TRIG (front panel BNC connector)
Trigger level range CH 0, CH 1 TRIG (external trigger)	 100% of FS ±5 V
Trigger level resolution	10 bits (1 in 1,024)
Edge trigger sensitivity, warranted	

CH 0, CH 1	2.5% of FS up to 50 MHz Increases to 5% of FS at 100 MHz
TRIG (external trigger, V_{pk-pk})	0.25 V up to 100 MHz Increases to 1 V at 200 MHz

Level accuracy

CH 0, CH 1	±3.5% of FS up to 10 MHz
TRIG (external trigger)	±0.35 V (±3.5% of FS) up to 10 MHz

Jitter	≤80 ps RMS [23]

Trigger filters

Low-frequency (LF) reject	50 kHz
High-frequency (HF) reject	50 kHz

Digital Trigger

Trigger type	Digital
Sources	RTSI <0..6> PFI <0..1> (front panel 9-pinmini-circular DIN connector)

Video Trigger

Trigger type	Video
Sources	CH 0 (front panel BNC connector) CH 1 (front panel BNC connector) TRIG (front panel BNC connector)
Video trigger types	Specific Line Any Line Specific Field
Standard	Negative sync of NTSC, PAL, or SECAM signal

External Trigger

Connector	TRIG (front panel BNC connector)
Impedance	1 MΩ in parallel with 22 pF
Coupling	AC, DC
AC coupling cutoff (-3 dB)	12 Hz
Input voltage range	±5 V
Maximum input overload	|Peaks| ≤42 V

PFI 0 and PFI 1 (Programmable Function Interface)

Connector	AUX I/O (9-pin mini-circular DIN)
Direction	Bidirectional

As an Input (Trigger)

Destinations	Start trigger (acquisition arm) Reference (stop) trigger Arm Reference trigger Advance trigger
Input impedance	150 kΩ, nominal
V_{IH}	2.0 V
V_{IL}	0.8 V
Maximum input overload	-0.5 V to 5.5 V
Maximum frequency	25 MHz

As an Output (Event)

Sources	Ready for Start Start trigger (acquisition arm) Ready for Reference Reference (stop) trigger

	End of Record
	Ready for Advance
	Advance trigger
	Done (end of acquisition)
	Probe Compensation[24]
Output impedance	50 Ω
Logic type	3.3 V CMOS
Maximum drive current	±24 mA
Maximum frequency	25 MHz

Waveform Specifications

Onboard memory size	
64 MB per channel option	32 MS per channel[25]
256 MB per channel option	128 MS per channel[25]
Minimum record length	1 sample
Number of pretrigger samples	Zero up to full record length[26]
Number of posttrigger samples	Zero up to full record length[26]
Maximum number of records in onboard memory	

64 MB/channel	100,000[27]
256 MB/channel	100,000[27]

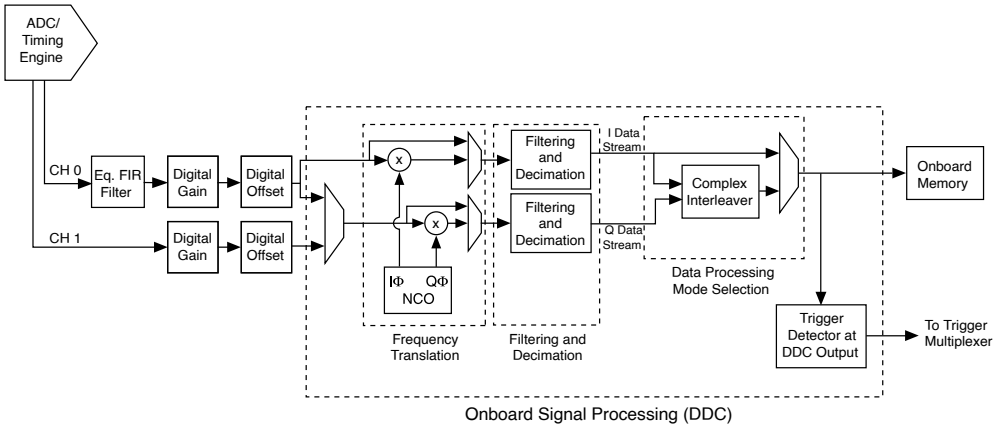
Allocated onboard memory per record	
Real data processing mode	(**Record Length** × 2 bytes/S) + 200 bytes, rounded up to next multiple of either 128 bytes or 512 bytes, whichever is greater
Complex data processing mode	(**Record Length** × 4 bytes/S) + 200 bytes, rounded up to next multiple of either 128 bytes or 512 bytes, whichever is greater

Related information

- For more information about the Sample clock and decimation, refer to the NI High-Speed Digitizers Help, available online at ni.com/manuals.

Onboard Signal Processing (OSP)

Figure 5. PCI-5142 Onboard Signal Processing Block Diagram



Note To use onboard signal processing (OSP) on the PCI-5142, the DDC Enabled property/attribute must be set to TRUE.

The following four OSP operations are available:

- Send one IF signal to CH 0 and perform quadrature downconversion on the signal (complex data is returned).
- Send I and Q baseband signals to CH 0 and CH 1 and perform alias-protected decimation (complex data is returned).
- Send a signal to CH 0 and perform alias-protected decimation (real data is returned).
- Send a signal to CH 0 and perform real downconversion on the signal (real data is returned).

Number of digital downconverters (DDCs)	1
Data processing modes[28]	Real (I path only) Complex (IQ)
OSP decimation range[29]	1, 2, 4, 6, 8, 10 12 to 4,096 (multiples of 4) 4,096 to 8,192 (multiples of 8) 8,192 to 16,384 (multiples of 16)
Sample rate range[30] Internal Sample clock timebase	6.1 kS/s to 100 MS/s (real or complex)
External Sample clock timebase	Sample clock timebase/OSP decimation
Real flat bandwidth	0.4 × **Sample Rate**
Complex flat bandwidth[31]	0.8 × **Sample Rate**

Digital Gain and Offset

Digital gain and offset resolution	18 bits
Digital gain range	-1.5 to +1.5 |Values| < 1 attenuate user data
Digital offset range	(-0.4 × **Vertical Range**) to (+0.4 × **Vertical Range**)[32]
Output	(**ADC Data** × **Digital Gain**) + **Digital Offset**.[33]

Numerically-Controlled Oscillator (NCO)

Frequency range[34]	
Internal Sample clock timebase	0 Hz to 50 MHz
External Sample clock timebase	0 Hz to (0.5 × **Sample Clock Timebase**)
Frequency resolution	
Internal Sample clock timebase	355 nHz
External Sample clock timebase	**Sample Clock Timebase** / 2^{48}
I and Q phase resolution	0.0055 °
Tuning time	1 ms

Digital Performance

Maximum NCO spur	<-100 dBFS
Decimating filter passband ripple	<0.1 dB [35]
Decimating filter out-of-band suppression	>80 dB [36]

IF Demodulation Performance

Modulation Configuration[37]	Measurement Type	Value
GSM Physical Layer[38]	Modulation Error Ratio (MER)	62 dB
	Error Vector Magnitude (EVM)	<0.2% RMS
W-CDMA Physical Layer[39]	MER	52 dB
	EVM	<0.4% RMS
DVB Physical Layer[40]	MER	48 dB
	EVM	<0.4% RMS
20 MSymbols/s, 64 QAM[41]	MER	39 dB
	EVM	<0.8% RMS
26.09 MSymbols/s, 64 QAM[42]	MER	36 dB
	EVM	<1.0% RMS
34.78 MSymbols/s, 64 QAM[43]	MER	32 dB
	EVM	<1.6% RMS

Table 16. IF Demodulation Performance

IQ Baseband Demodulation Performance

Modulation Configuration[44]	Measurement Type	Value
GSM physical layer[45]	Modulation Error Ratio (MER)	41 dB
	Error Vector Magnitude (EVM)	<0.8% RMS
W-CDMA Physical Layer[46]	MER	41 dB
	EVM	<0.9% RMS

Modulation Configuration[44]	Measurement Type	Value
DVB Physical Layer[47]	MER	40 dB
	EVM	<0.9% RMS
20 MSymbols/s, 64 QAM[48]	MER	33 dB
	EVM	<1.4% RMS

Table 17. IQ Baseband Demodulation Performance

Waveform Acquisition Times

Conditions	64 MB	256 MB
Sample rate = 100 MS/s, OSP disabled	0.336 s	1.34 s
Sample rate = 1 MS/s, real mode, OSP enabled	33.6 s	2 min 14 s
Sample rate = 100 kS/s, real mode, OSP enabled	5 min 36 s	22 min 22 s

Table 18. Maximum Acquisition Time[49]

Figure 6. Decimation Filter Frequency Response (Real Mode), 10 MS/s Sample Rate, Measured

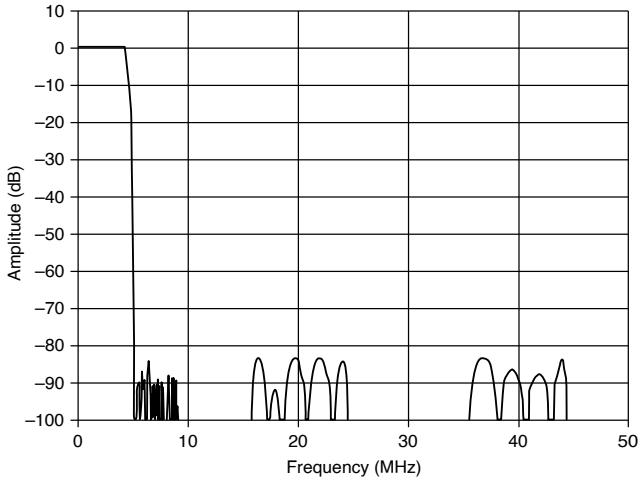


Figure 7. GSM Physical Layer, Measured[50]

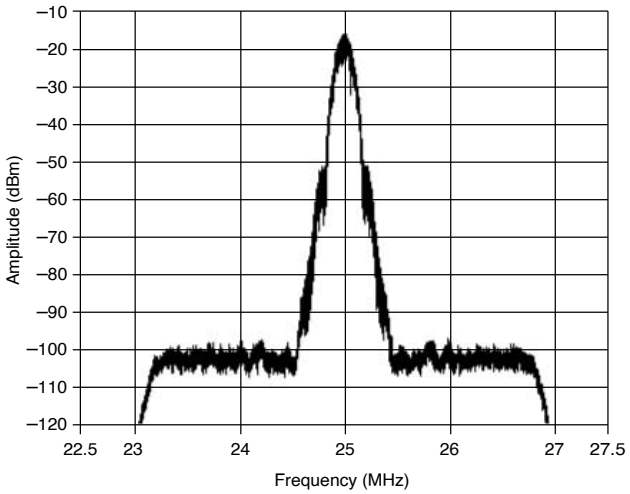


Figure 8. W-CDMA Physical Layer, Measured[51]

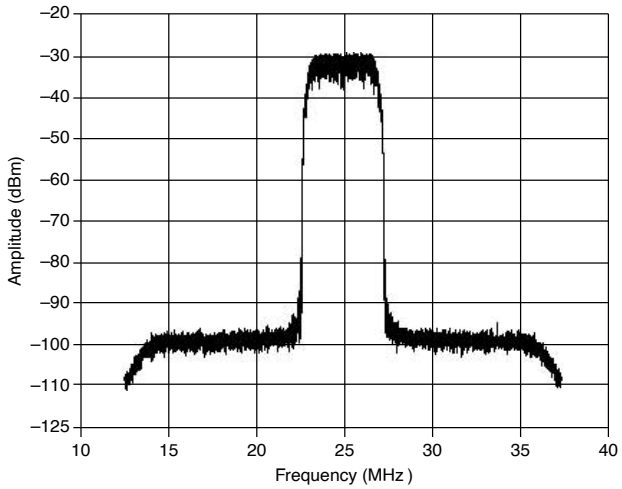


Figure 9. DVB Physical Layer, Measured[52]

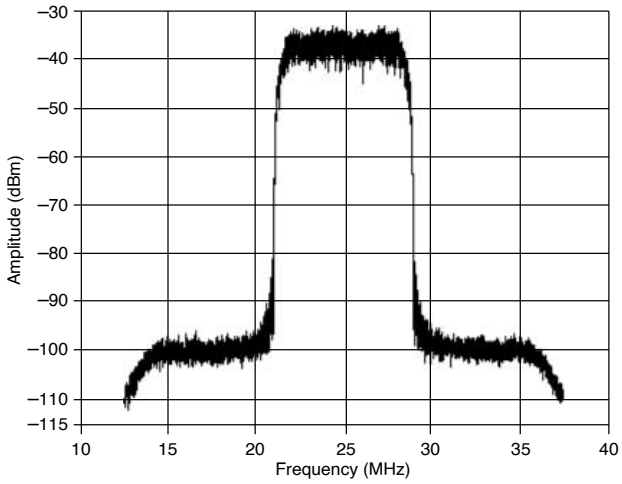
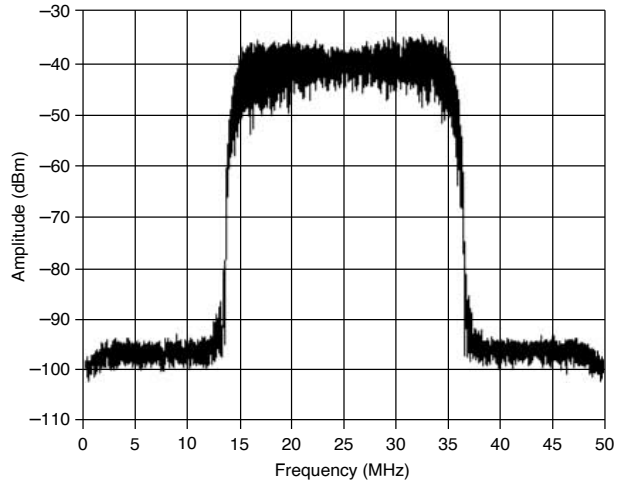


Figure 10. 20 MSymbols/s 64 QAM, Measured[53]



Calibration

External Calibration

External calibration calibrates the VCXO and the voltage reference. All calibration constants are stored in nonvolatile memory.

Self-Calibration

Self-calibration is done on software command. The calibration corrects for gain, offset, frequency response, triggering, and timing adjustment errors for all input ranges.

Calibration Specifications

Interval for external calibration	2 years
Warm-up time[54]	15 minutes

Software

Driver Software

Driver support for this device was first available in NI-SCOPE3.0.

NI-SCOPE is an IVI-compliant driver that allows you to configure, control, and calibrate the PCI-5142. NI-SCOPE provides application programming interfaces for many development environments.

Application Software

NI-SCOPE provides programming interfaces, documentation, and examples for the following application development environments:

- LabVIEW
- LabWindows™/CVI™
- Measurement Studio
- Microsoft Visual C/C++
- .NET (C# and VB.NET)

Interactive Soft Front Panel and Configuration

When you install NI-SCOPE on a 64-bit system, you can monitor, control, and record measurements from the PCI-5142 using InstrumentStudio.

InstrumentStudio is a software-based front panel application that allows you to perform interactive measurements on several different device types in a single program.

Note InstrumentStudio is supported only on 64-bit systems. If you are using a 32-bit system, use the NI-SCOPE–specific soft front panel instead of InstrumentStudio.

Interactive control of the PCI-5142 was first available via InstrumentStudio in NI-SCOPE18.1 and via the NI-SCOPE SFP in NI-SCOPE2.4. InstrumentStudio and the NI-SCOPE SFP are included on the NI-SCOPE media.

NI Measurement & Automation Explorer (MAX) also provides interactive configuration and test tools for the PCI-5142. MAX is included on the driver media.

Synchronization

Synchronization with the NI-TClk API [55]

NI-TClk is an API that enables system synchronization of supported PXI modules in one or more PXI chassis, which you can use with the PCI-5142 and NI-SCOPE.

NI-TClk uses a shared Reference Clock and triggers to align the Sample Clocks of PXI modules and synchronize the distribution and reception of triggers. These signals are routed through the PXI chassis backplane without external cable connections between PXI modules in the same chassis.

Module-to-module skew, between PCI-5142 modules using NI-TClk [56]
NI-TClk synchronization without manual adjustment [57]

Skew, Peak-to-Peak [58]	500 ps
NI-TClk synchronization with manual adjustment [57]	
Skew after manual adjustment	≤5 ps
Sample Clock delay/adjustment resolution	≤5 ps

Power

Current draw	
+3.3 V DC	3.4 A
+5 V DC	2.7 A
+12 V DC	110 mA
-12 V DC	0 A
Total power	26.1 W

Physical

Dimensions	35.5 cm × 2.0 cm × 11.3 cm (14.0 in × 0.8 in × 4.4 in)
Weight	470 g (16.6 oz)

Environment

Maximum altitude	2,000 m (at 25 °C ambient temperature)
Pollution Degree	2

Indoor use only.

Operating Environment

Ambient temperature range	0 °C to 45 °C (Tested in accordance with IEC 60068-2-1 and IEC 60068-2-2.)
Relative humidity range	10% to 90%, noncondensing (Tested in accordance with IEC 60068-2-56.)

Storage Environment

Ambient temperature range	-40 °C to 71 °C (Tested in accordance with IEC 60068-2-1 and IEC 60068-2-2.)
Relative humidity range	5% to 95%, noncondensing (Tested in accordance with IEC 60068-2-56.)

Compliance and Certifications

Safety Compliance Standards

This product is designed to meet the requirements of the following electrical equipment safety standards for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 61010-1, CSA C22.2 No. 61010-1

Note For safety certifications, refer to the product label or the Product Certifications and Declarations section.

Electromagnetic Compatibility

This product meets the requirements of the following EMC standards for electrical equipment for measurement, control, and laboratory use:

- EN 61326-1 (IEC 61326-1): Class A emissions; Basic immunity
- EN 55011 (CISPR 11): Group 1, Class A emissions
- EN 55022 (CISPR 22): Class A emissions
- EN 55024 (CISPR 24): Immunity
- AS/NZS CISPR 11: Group 1, Class A emissions
- AS/NZS CISPR 22: Class A emissions
- FCC 47 CFR Part 15B: Class A emissions
- ICES-001: Class A emissions

Note In the United States (per FCC 47 CFR), Class A equipment is intended for use in commercial, light-industrial, and heavy-industrial locations. In Europe, Canada, Australia, and New Zealand (per CISPR 11), Class A equipment is intended for use only in heavy-industrial locations.

Note Group 1 equipment (per CISPR 11) is any industrial, scientific, or medical equipment that does not intentionally generate radio frequency energy for the treatment of material or inspection/analysis purposes.

Note For EMC declarations, certifications, and additional information, refer to the Product Certifications and Declarations section.

CE Compliance CE

This product meets the essential requirements of applicable European Directives, as follows:

- 2014/35/EU; Low-Voltage Directive (safety)
- 2014/30/EU; Electromagnetic Compatibility Directive (EMC)
- 2011/65/EU; Restriction of Hazardous Substances (RoHS)

Product Certifications and Declarations

Refer to the product Declaration of Conformity (DoC) for additional regulatory compliance information. To obtain product certifications and the DoC for NI products, visit ni.com/product-certifications, search by model number, and click the appropriate link.

Environmental Management

NI is committed to designing and manufacturing products in an environmentally responsible manner. NI recognizes that eliminating certain hazardous substances from our products is beneficial to the environment and to NI customers.

For additional environmental information, refer to the **Engineering a Healthy Planet** web page at ni.com/environment. This page contains the environmental regulations and directives with which NI complies, as well as other environmental information not included in this document.

EU and UK Customers

- Waste Electrical and Electronic Equipment (WEEE)—At the end of the product life cycle, all NI products must be disposed of according to local laws and regulations. For more information about how to recycle NI products in your region, visit ni.com/environment/weee.

电子信息产品污染控制管理办法（中国 RoHS）

- 中国 RoHS— NI 符合中国电子信息产品中限制使用某些有害物质指令(RoHS)。关于 NI 中国 RoHS 合规性信息，请登录 ni.com/environment/rohs_china。(For information about China RoHS compliance, go to ni.com/environment/rohs_china.)

[1] AC coupling available on 1 MΩ input only.

[2] Within ±5 °C of self-calibration temperature.

[3] CH 0 to/from CH 1, and external trigger to CH 0 or CH 1.

[4] Referenced to 50 kHz

[5] 78 MHz above 40 °C.

[6] Only one filter can be enabled at any given time. The anti-alias filter is enabled by default.

[7] AC coupling available on 1 MΩ input impedance only.

[8] 10 MHz, -1 dBFS input signal. Includes the 2nd through the 5th harmonics. Measured from 5 kHz to 50 MHz.

[9] 10 MHz, -1 dBFS input signal. Includes the 2nd through the 5th harmonics.

[10] 0.2 V to 2.0 V input ranges with 50 Ω input impedance. Two tones at 10.2 MHz and 11.2 MHz. Each tone is -7 dBFS.

[11] 10 MHz, -1 dBFS input signal. Excludes harmonics. Measured from DC to 50 MHz.

[12] 10 MHz, -1 dBFS input signal. Includes harmonics. Measured from DC to 50 MHz.

[13] 50 Ω terminator connected to input.

[14] Internal Sample clock is locked to the Reference clock or derived from the onboard VCXO.

[15] In normal operation mode (non-OSP mode), divide by **n** decimation is used for all rates less than 100 MS/s. Non-OSP decimation does not protect the acquired data from undersampling aliasing. Non-OSP decimation and OSP decimation are mutually exclusive.

[16] 10 MHz input signal.

[17] Includes the effects of the converter aperture uncertainty and the clock circuitry jitter. Excludes trigger jitter.

[18] In normal operation mode (non-OSP mode), divide by **n** decimation is available, where 1 ≤ **n** ≤ 65,535. Non-OSP decimation does not protect the acquired data from undersampling aliasing. Non-OSP decimation and OSP decimation are mutually exclusive.

[19] Decimated Sample clock only.

[20] 10 MHz default. The PLL Reference clock frequency must be accurate to ±50 ppm.

[21] Overvoltage and reverse polarity protected.

[22] Holdoff set to 0. Onboard Sample clock at maximum rate.

[23] Within ±5 °C of self-calibration temperature.

[24] 1 kHz, 50% duty cycle square wave. PFI 1 front panel connector only.

[25] Assumes 2-byte samples. In Complex data processing mode (only available when using onboard signal processing), each sample is 4 bytes, so this number is halved.

[26] Single-record mode and multiple-record mode.

[27] It is possible to exceed these numbers if you fetch records while acquiring data.

[28] Complex mode is used for both IQ baseband decimation and quadrature downconversion.

[29] OSP decimation protects acquired data from high-frequency aliasing within the ADC Nyquist zone, whereas non-OSP decimation does not. Non-OSP decimation and OSP decimation are mutually exclusive.

[30] For sample rates less than 6.1 kS/s, use an external Sample clock or perform additional software decimation.

[31] For example, complex bandwidth is 40 MHz with a complex sample rate of 50 MS/s.

[32] Applied after digital gain.

[33] (-0.5 × **Vertical Range**) ≤ **Output** ≤ (+0.5 × **Vertical Range**)

[34] Undersampling can be used for carrier frequencies >50 MHz.

[35] Passband is from 0 to (0.4 × **IQ Rate**).

[36] Stopband suppression from (0.6 × **IQ Rate**).

[37] 1 V vertical range, 50 Ω input impedance, no analog filter, 25 MHz carrier. Demodulation, including resampling (sample rate conversion) and pulse shaping, was done with the NI Modulation Toolkit in the host PC/ controller.

[38] 1.25 MS/s sample rate, MSK modulation, 270.833 kSymbols/s, Gaussian, BT = 0.3.

[39] 6.25 MS/s sample rate, QPSK modulation, 3.84 MSymbols/s, root raised cosine, alpha = 0.22.

[40] 10 MS/s sample rate, 32 QAM modulation, 6.92 MSymbols/s, root raised cosine, alpha = 0.15.

[41] 50 MS/s sample rate, 64 QAM modulation, 20 MSymbols/s, root raised cosine, alpha = 0.15.

[42] 50 MS/s sample rate, 64 QAM modulation, 26.09 MSymbols/s, root raised cosine, alpha = 0.15, 30 MHz bandwidth.

[43] 50 MS/s sample rate, 64 QAM modulation, 34.78 MSymbols/s, root raised cosine, alpha = 0.15, 40 MHz bandwidth.

[44] 1 V input range, 50 Ω input impedance, no analog filter. Demodulation, including resampling (sample rate conversion) and pulse shaping, done with the NI Modulation Toolkit on the host PC/controller. This is a measurement of system performance. The IQ Baseband generation was implemented with two TClk-synchronized NI PXI-5421 arbitrary waveform generators.

[45] 1.25 MS/s sample rate, MSK modulation, 270.833 kSymbols/s, Gaussian, BT = 0.3

[46] 6.25 MS/s sample rate, QPSK modulation, 3.84 MSymbols/s, root raised cosine, alpha = 0.22

[47] 10 MS/s sample rate, 32 QAM modulation, 6.92 MSymbols/s, root raised cosine, alpha = 0.15

[48] 50 MS/s sample rate, 64 QAM modulation, 20 MSymbols/s, root raised cosine, alpha = 0.15

[49] For complex (IQ) mode, the acquisition time is halved.

[50] 1 V input range, 50 Ω input impedance, no analog filter, 25 MHz carrier, 4.17 MS/s sample rate, MSK modulation, 270.833 kSymbols/s, Gaussian, BT = 0.3.

[51] 1 V input range, 50 Ω input impedance, no analog filter, 25 MHz carrier, 25 MS/s sample rate, QPSK modulation, 3.84 MSymbols/s, root raised cosine, alpha = 0.22.

[52] 1 V input range, 50 Ω input impedance, no analog filter, 25 MHz carrier, 25 MS/s sample rate, 32 QAM modulation, 6.92 MSymbols/s, root raised cosine, alpha = 0.15.

[53] 1 V input range, 50 Ω input impedance, no analog filter, 25 MHz carrier, 50 MS/s sample rate, 64 QAM modulation, 20 MSymbols/s, root raised cosine, alpha = 0.15.

[54] Warm-up time begins after the NI-SCOPE driver is loaded.

[55] NI-TClk installs with NI-SCOPE.

[56] Although you can use NI-TClk to synchronize non-identical modules, these specifications apply only to synchronizing identical modules. Specifications are valid under the following conditions:

- All modules installed in the same chassis.
- All filters are disabled.
- NI-TClk used to align the sample clocks of each module.
- All parameters set to identical values for each module.
- Self-calibration completed.
- Ambient temperature within ±1 °C of self-calibration.

For other configurations, including multi-chassis systems, contact NI Technical Support at **ni.com/support**.

[57] Manual adjustment is the process of minimizing synchronization jitter and skew by adjusting Trigger Clock (TClk) signals using the instrument driver.

[58] Caused by clock and analog delay differences. Tested with a PXIe-1082 chassis with maximum slot to slot skew of 100 ps. Valid within ±1 °C of self-calibration.