NI-5752/5752B Safety, Environmental, and Regulatory Information

2022-07-11

Contents

NI 5752/5752B Specifications

This document lists specifications for the NI 5752/5752B adapter module. Pair these specifications with the specifications listed in your FlexRIO FPGA module specifications document or your Controller for FlexRIO specifications document.

Caution The protection provided by the NI 5752/5752B can be impaired if it is used in a manner not described in this document.

Caution To avoid permanent damage to the NI 5752/5752B, disconnect all signals connected to the NI 5752/5752B before powering down the module, and only connect signals after the module has been powered on by the FlexRIO FPGA module or the Controller for FlexRIO.

Note These specifications are characteristic at 25 °C unless otherwise noted.

Maximum and **minimum** specifications are warranted not to exceed these values within certain operating conditions and include the effects of temperature and uncertainty unless otherwise noted.

Characteristic specifications are unwarranted values that are representative of an average unit operating at room temperature

Typical specifications are unwarranted values that are representative of a majority (90%) of units within certain operating conditions and include the effects of temperature and uncertainty unless otherwise noted.

Note Using the NI 5752/5752B in a manner not described in this document may impair the protection that the NI 5752/5752B provides.

Specifications are subject to change without notice. For the most recent device specifications, visit ni.com/manuals.

FlexRIO Documentation

Document	Location	Description
Getting started guide for your FlexRIO FPGA module or controller for FlexRIO	Available from the Start menu and at ni.com/manuals.	Contains installation instructions for your FlexRIO system.
Specifications document for your FlexRIO FPGA module or controller for FlexRIO	Available from the Start menu and at ni.com/manuals.	Contains specifications for your FlexRIO FPGA module or controller for FlexRIO.
Getting started guide for your adapter module	Available from the Start menu and at ni.com/manuals.	Contains signal information, examples, and CLIP details for your adapter module.
Specifications document for your adapter module	Available from the Start menu and at ni.com/manuals.	Contains specifications for your adapter module.
LabVIEW FPGA Module Help	Embedded in **LabVIEW Help** and at ni.com/manuals.	Contains information about the basic functionality of the LabVIEW FPGA Module.
Real-Time Module Help	Embedded in **LabVIEW Help** and at ni.com/manuals.	Contains information about real-time programming concepts, step-by-step instructions for using LabVIEW with the Real-Time Module, reference information about Real-Time Module VIs and functions, and information about LabVIEW features on real-time operating systems.
FlexRIO Help	Available from the Start menu and at ni.com/manuals.	Contains information about the FPGA module front panel connectors and I/O, controller for FlexRIO front panel connectors and I/O, programming instructions, and adapter module component-level IP (CLIP).
LabVIEW Examples	Available in NI Example Finder. In LabVIEW, click Help > Find Examples > Hardware Input and Output > FlexRIO.	Contains examples of how to run FPGA VIs and Host VIs on your device.

Document	Location	Description
IPNet	Located at ni.com/ipnet.	Contains LabVIEW FPGA functions and intellectual property to share.
FlexRIO product page	Located at ni.com/flexrio.	Contains product information and data sheets for FlexRIO devices.

Table 1. FlexRIO Documentation Locations and Descriptions

Absolute Maximum Ratings

Caution Stresses beyond those listed in this section may cause permanent damage to the adapter module. Avoid swapping the analog and digital cables because doing so will short the digital output terminals to ground.

(AI+, AI-)	±2.1 V
External clock input	-0.5 V to 3.5 V
Digital input	-0.5 V to 3.5 V
Digital output current	2 mA

Analog Input (AI 0 to AI 31)

General Characteristics

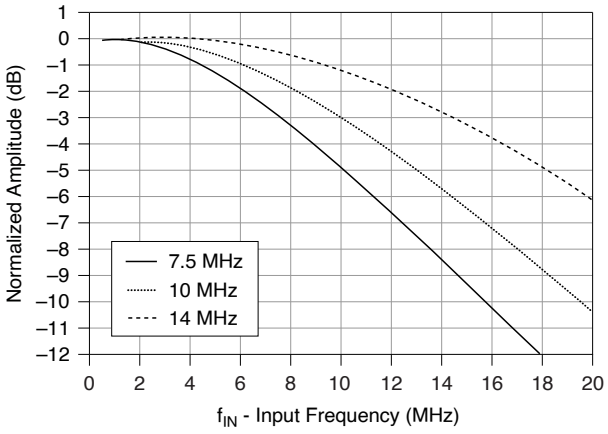
Type of connector	2 VHDCI (dual stack)
Number of channels	32, differential, simultaneously sampled (single-ended can be achieved by setting the VGA gain to 6 dB)
Max input voltage swing	

Differential	2 V_{pk-pk}
Single-ended	1 V_{pk-pk}
Gain range	-5 dB to 31 dB
Gain resolution	0.125 dB
Common mode range	±1 VDC
Input impedance	100 Ω (AI+, AI-)
Coupling	AC-coupled
ADC manufacturer part number	AFE5801 monolithic analog front end, including a variable gain amplifier and a 12-bit differential pipelined A/D converter

Specific Characteristics

Anti-aliasing filter (-3 dB)	7.5 MHz, 10 MHz, and 14 MHz

Figure 1. Anti-aliasing Filter Frequency Response -0 dB Reference at 800 kHz Amplitude



Gain error	
-5 dB to 28 dB	±1.2 dB
>28 dB	±1.8 dB
AC coupling cutoff	16 kHz[1]
Crosstalk	<-75 dB at 1 MHz[2]
Signal-to-noise ratio (SNR)	66 dBc[3]
Spurious-free dynamic range (SFDR)	65 dBc [4]
Total harmonic distortion (THD)	64 dBc[5]
Average noise density	7.4 nV/√Hz[6]

Figure 2. Characteristic Dynamic Performance, Spectrum-64,000 Samples, Coarse Gain 6 dB, 2 MHz, -1 dBFS Differential-Ended Input Signal

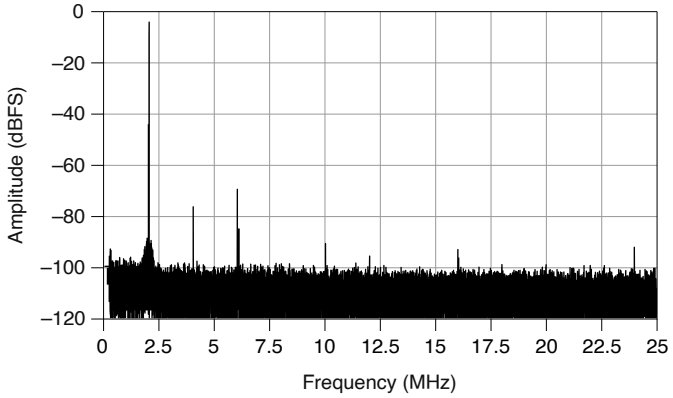


Figure 3. Characteristic Dynamic Performance, Spectrum-64,000 Samples, Coarse Gain 12 dB, 2 MHz, -1 dBFS Differential-Ended Input Signal

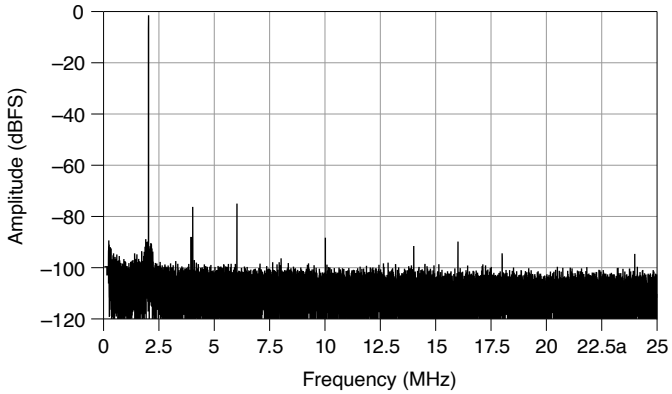


Figure 4. Characteristic Dynamic Performance, Spectrum-64,000 Samples, Coarse Gain 30 dB, 2 MHz, -1 dBFS Differential-Ended Input Signal

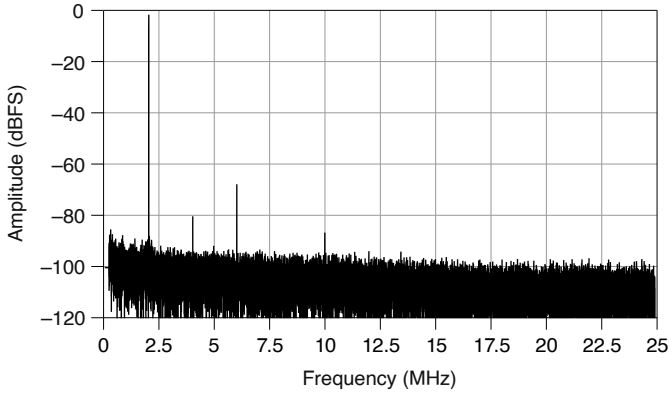


Figure 5. Characteristic Dynamic Performance, Spectrum-64,000 Samples, Coarse Gain 6 dB, 2 MHz, -6 dBFS Single-Ended Input Signal

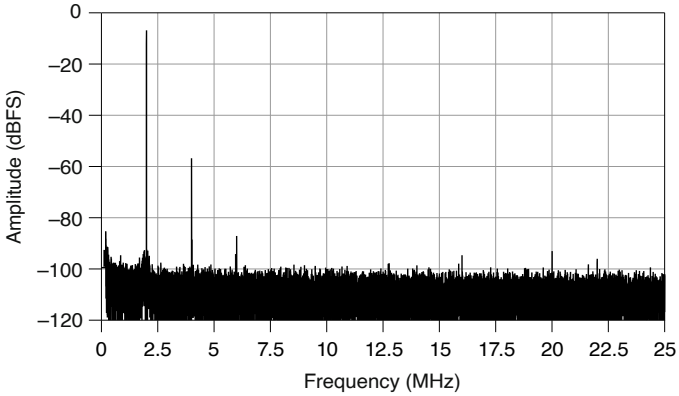
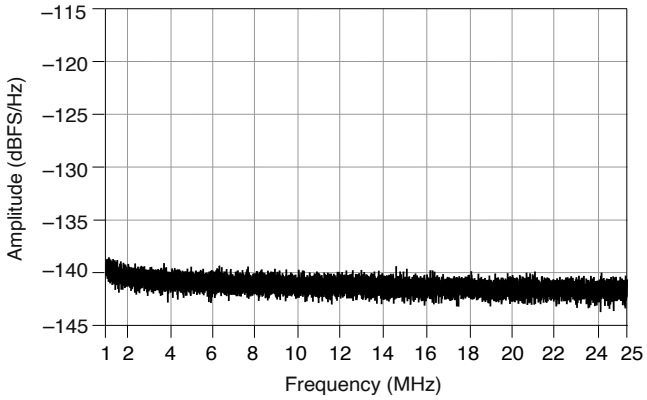


Figure 6. Characteristic Noise Density, Spectrum-64,000 Samples, Coarse Gain 0 dB



Sample Clock

Sample Clock sources	50 MHz onboard clock, Sync Clock (PXIe_DSTARA)[7],[8], or CLK IN[9] (front panel SMB)
Sample Clock frequency range	25 MHz to 50 MHz[10]

CLK IN

Connector	SMB
Logic level	3.3 V CMOS
Minimum high-level input voltage (V_{IH})	2.2 V
Maximum low-level input voltage (V_{IL})	0.6 V
Input impedance	> 50 kΩ
Input coupling	DC

Duty cycle	45% to 55%

Digital Inputs

Number of channels	2
Connector	VHDCI
Minimum high-level input voltage (V_{IH} (min))	2.0 V
Maximum low-level input voltage (V_{IL} (max))	0.8 V

Digital Outputs

Number of channels	16
Connector	VHDCI
Minimum high-level output voltage (V_{OH} (min))	2.4 V
Maximum low-level output voltage (V_{OL} (max))	0.55 V
Maximum output current	1 mA
Minimum pulse width	10 ns
Maximum toggle frequency	1 MHz, all outputs toggling

Caution Avoid swapping the analog and digital cables because doing so will short the digital output terminals to ground and cause harmful currents to flow out from the module.

Power

Power requirements from the FPGA device	
+12 V	200 mA, 2.4 W max
+3.3 V	878 mA, 2.9 W max
Total power	5.3 W

Physical

Dimensions	12.9 × 2.0 × 12.1 cm (5.1 × 0.8 × 4.7 in.)
Weight	284 g (10 oz)
Front panel connectors	One SMB connector and three 68-pin VHDCI connectors

Environment

Maximum altitude	2,000 m (800 mbar) (at 25 °C ambient temperature)
Pollution Degree	2

Indoor use only.

Operating Environment

Ambient temperature range	0 °C to 55 °C (Tested in accordance with IEC 60068-2-1 and IEC 60068-2-2. Meets MIL-PRF-28800F Class 3 low temperature limit and MIL-PRF-28800F Class 2 high temperature limit.)
Relative humidity range	10% to 90%, noncondensing (Tested in accordance with IEC 60068-2-56.)

Storage Environment

Ambient temperature range	-20 °C to 71 °C (Tested in accordance with IEC 60068-2-1 and IEC 60068-2-2. Meets MIL-PRF-28800F Class 3 limits.)
Relative humidity range	5% to 95%, noncondensing (Tested in accordance with IEC 60068-2-56.)

Shock and Vibration

Operating shock	30 g peak, half-sine, 11 ms pulse (Tested in accordance with IEC 60068-2-27. Meets MIL-PRF-28800F Class 2 limits.)

Random vibration

Operating	5 Hz to 500 Hz, 0.3 g_{rms} (Tested in accordance with IEC 60068-2-64.)
Nonoperating	5 Hz to 500 Hz, 2.4 g_{rms} (Tested in accordance with IEC 60068-2-64. Test profile exceeds the requirements of MIL-PRF-28800F, Class 3.)

Compliance and Certifications

Safety

This product is designed to meet the requirements of the following electrical equipment safety standards for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 61010-1, CSA C22.2 No. 61010-1

Note For UL and other safety certifications, refer to the product label or the Online Product Certification section.

Electromagnetic Compatibility

This product meets the requirements of the following EMC standards for electrical equipment for measurement, control, and laboratory use:

- EN 61326-1 (IEC 61326-1): Class A emissions; Basic immunity
- EN 55011 (CISPR 11): Group 1, Class A emissions
- EN 55022 (CISPR 22): Class A emissions
- EN 55024 (CISPR 24): Immunity
- AS/NZS CISPR 11: Group 1, Class A emissions
- AS/NZS CISPR 22: Class A emissions
- FCC 47 CFR Part 15B: Class A emissions
- ICES-001: Class A emissions

Note In the United States (per FCC 47 CFR), Class A equipment is intended for use in commercial, light-industrial, and heavy-industrial locations. In Europe, Canada, Australia, and New Zealand (per CISPR 11), Class A equipment is intended for use only in heavy-industrial locations.

Note Group 1 equipment (per CISPR 11) is any industrial, scientific, or medical equipment that does not intentionally generate radio frequency energy for the treatment of material or inspection/analysis purposes.

Note For EMC declarations, certifications, and additional information, refer to the Online Product Certification section.

CE Compliance CE

This product meets the essential requirements of applicable European Directives, as follows:

- 2014/35/EU; Low-Voltage Directive (safety)
- 2014/30/EU; Electromagnetic Compatibility Directive (EMC)

Online Product Certification

Refer to the product Declaration of Conformity (DoC) for additional regulatory compliance information. To obtain product certifications and the DoC for this product, visit ni.com/certification, search by model number or product line, and click the appropriate link in the Certification column.

Environmental Management

NI is committed to designing and manufacturing products in an environmentally responsible manner. NI recognizes that eliminating certain hazardous substances from our products is beneficial to the environment and to NI customers.

For additional environmental information, refer to the **Minimize Our Environmental Impact** web page at ni.com/environment. This page contains the environmental regulations and directives with which NI complies, as well as other environmental information not included in this document.

Waste Electrical and Electronic Equipment (WEEE)

> **EU Customers** At the end of the product life cycle, all NI products must be disposed of according to local laws and regulations. For more information about how to recycle NI products in your region, visit ni.com/environment/weee.

电子信息产品污染控制管理办法（中国 RoHS）

> **中国客户** National Instruments 符合中国电子信息产品中限制使用某些有害物质指令(RoHS)。关于 National Instruments 中国 RoHS 合规性信息，请登录 ni.com/environment/rohs_china。(For information about China RoHS compliance, go to ni.com/environment/rohs_china.)

[1] 100 Ω source assumed, AFE5801 internal VGA DC coupling enabled

[2] Measured on one channel with the test signal applied to another channel, with the same range setting on both channels

[3] -1 dBFS differential input signal, 6 dB gain, f_{in} = 2 MHz

[4] -1 dBFS differential input signal, 17 dB gain, f_{in} = 2 MHz

[5] -1 dBFS differential input signal, 17 dB gain, f_{in} = 2 MHz

[6] Input referenced, 5 MHz, 31 dB gain, low-noise mode

[7] Sync Clock (PXIe_DSTARA) is only available on NI PXI Express FlexRIO FPGA modules, such as the NI PXIe-796xR. On PXI Express modules, Sync Clock is driven by the PXIe_DSTARA signal from the PXI/PXI Express backplane. For NI PXI modules, such as the NI PXI-795xR, and controllers for FlexRIO, such as the NI-793xR, Sync Clock (PXIe_DSTARA) is not available.

[8] If you change the frequency of Sync Clock (PXIe_DSTARA) or CLK IN (when used as the Sample Clock), you must assert ForceInit.

[9] If you change the frequency of Sync Clock (PXIe_DSTARA) or CLK IN (when used as the Sample Clock), you must assert ForceInit.

[10] If you change the frequency of Sync Clock (PXIe_DSTARA) or CLK IN (when used as the Sample Clock), you must assert ForceInit.