PCIe-1477 Features

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Contents

NI PCIe-14xx Purpose

The NI PCIe-1477 is an image acquisition device with a PCIe 2.0 x8 host interface. It has a user-configurable FPGA for highly customized image processing applications and supports many Lite, Base, Medium, Full, 72-bit, and 80-bit configuration Camera Link-compatible cameras at up to 85 MHz. Power over Camera Link (PoCL) is supported for simplified system connectivity. The user-configurable FPGA allows the user to customize triggering and control using a variety of auxiliary IO provided via a digital I/O connector, an I/O extension connector, and RTSI. This document describes the NI PCIe-1477 features and capabilities.

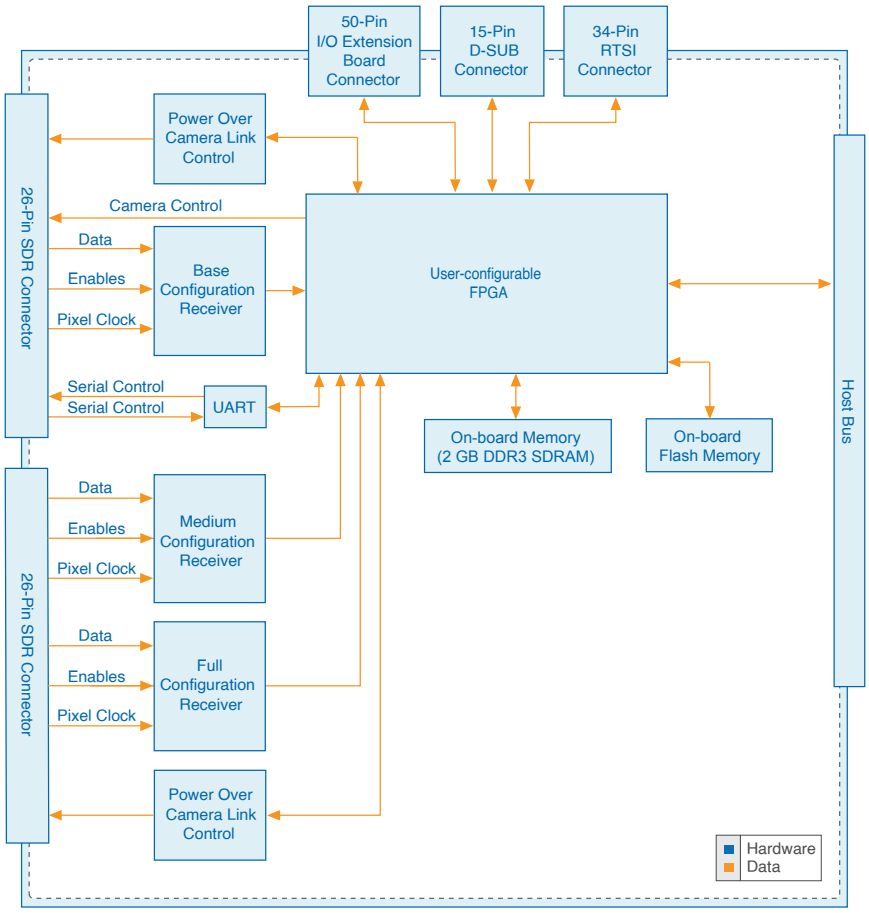
Hardware Overview

This chapter provides an overview of NI PCIe-1477 hardware functionality and explains the operations of the functional units on the device.

Functional Overview

The NI PCIe-1477 features a flexible, reconfigurable architecture for custom image acquisition and image processing applications with Camera Link cameras.

Figure 1. NI PCIe-1477 Block Diagram



Camera Link and the NI PCIe-1477

The NI PCIe-1477 supports Camera Link Lite, Base, Medium, Full, 72-bit, and 80-bit configurations.

The Camera Link specification includes up to 80 data bits, enable signals, and asynchronous serial transmission, as well as four digital camera control lines. The four camera control lines can be configured to generate precise timing signals for controlling exposure time, frame rates, and other digital camera acquisition control signals.

The Camera Link standard defines physical connections between image acquisition devices and cameras, and it allows for flexibility of image format and data transfer protocols. The camera manufacturer defines image parameters, such as image resolution and the number of bits per pixel, and camera control parameters, such as frame-on-demand and exposure control signals.

Medium, Full, 72-bit, and 80-bit configurations require using two Camera Link connectors. These configurations allow for more data throughput by offering multiple synchronized data channels between the camera and the NI PCIe-1477.

User-Configurable FPGA

The NI PCIe-1477 provides a user-configurable FPGA to allow users to write a fully customized image processing data path with LabVIEW FPGA. The user-configurable FPGA is particularly well suited to applications that require high-throughput and/or low-latency image processing. To reduce the development time, NI Vision Development Module provides many image processing functions that can be implemented with the NI PCIe-1477 user-configurable FPGA. Alternatively, users may write their own image processing functions for some specific or complex tasks using LabVIEW FPGA or low-level languages such as VHDL. Together with the image processing functions provided by NI Vision Development Module, the NI PCIe-1477 provides users the flexibility to implement complex and fully customized image processing algorithms with the user-configurable FPGA. The user-configurable FPGA also allows the user to customize triggering and control using a variety of auxiliary IO provided via a digital I/O connector, an I/O extension connector, and RTSI.

Notice During FPGA reconfiguration, a PCIe link loss period of ≤100 ms will occur.

On-board Flash Memory

The NI PCIe-1477 includes a flash memory on-board, allowing users to store their FPGA bitfile in the flash memory with NI MAX. The user FPGA bitfile will be loaded from the flash memory after a system power cycle. For more information on downloading a bitfile to NI FPGA target, visit ni.com/info and enter the Info Code autoloadbitfile.

On-board Memory

The NI PCIe-1477 includes 2,048 MB of DDR3 SDRAM on-board, supporting peak throughputs of up to 10.66 GB/s. This memory is directly accessible from the LabVIEW FPGA application and its use is entirely controlled by the user. The LabVIEW FPGA memory interface allows the physical DRAM to be partitioned into multiple memory items, allowing the DRAM to appear as multiple independent memories

and allowing it be employed for multiple uses simultaneously. For example, it can be used for multi-image processing algorithms, for data buffering, and/or as an image buffer for DMA transfers to the host computer memory.
Some host computer systems may not be able to keep up with peak data rates for brief periods of time due to system loading and other operations that may be occurring simultaneously. Buffering images before sending to the host computer significantly reduces the likelihood that an image will be dropped by the system.

Power over Camera Link (PoCL)

The NI PCIe-1477 supports Power over Camera Link with SafePower, in accordance with the Camera Link specification. This feature allows PoCL-capable cameras to be powered directly by the frame grabber, without the need for an additional power connection to the camera. Both Camera Link ports on the NI PCIe-1477 can supply power to the camera, allowing cameras to draw up to 4 W per port (8 W total). PoCL is only enabled when power is supplied via the 6-pin PCIe Auxiliary Power Connector.
PoCL on both connectors is enabled by default and can be controlled via an FPGA I/O Node.
The enabled PoCL circuitry on the frame grabber is fully compatible with both PoCL and non-PoCL cameras.
In order for the NI PCIe-1477 to power a camera, it must be used with a PoCL-compatible camera and PoCL-compatible Camera Link cables. No additional configuration is needed on the NI PCIe-1477 to switch between PoCL and non-PoCL cameras.

Serial Interface

The NI PCIe-1477 provides serial communication to and from the camera through two LVDS pairs in the Camera Link cable. All Camera Link serial communication uses one start bit, one stop bit, no parity, and no hardware handshaking.
The NI PCIe-1477 supports all baud rates specified by the Camera Link specification. Refer to the **NI PCIe-1477 Specifications** for a list of baud rates that the NI PCIe-1477 supports.
You can use the serial interface interactively with a manufacturer supplied camera control utility, or programmatically with LabVIEW.
Interactively:

- Manufacturer Supplied Camera Control Utility—Camera manufacturers who are compliant with the Camera Link 1.1 or later specification provide a camera control utility which sends the appropriate serial commands for configuring your camera through the device serial port.

Programmatically:

- Serial API—NI fully supports the recommended serial API described in the Camera Link Specification via clsernif.dll. This specification is available on the Automated Imaging Association (AIA) website at www.visiononline.org.
- LabVIEW—Use the serial interface programmatically, through example VIs that can be used for serial communication from the host context in LabVIEW. The serial example VIs for the NI PCIe-1477 can be found here: <LabVIEW Dir>\examples\Vision-RIO\PCIe-1477\Common\CL Serial NIFlexRIO.

Monitoring the Device Temperature

You can monitor the FPGA die temperature of the NI PCIe-1477 using an FPGA I/O Node. After adding an FPGA I/O Node to the block diagram, click the element section of the node, and select FPGA Temperature (C). The FPGA device may malfunction at temperatures over 95 °C. If the device measures greater than or equal to 95 °C, stop the FPGA application and consider moving the device to a more suitable environment.

Monitoring and Controlling the FPGA Fan

The FPGA fan is automatically turned on when FPGA reaches a certain temperature by default. You can monitor the FPGA Fan Speed of the NI PCIe-1477 using an FPGA I/O Node. After adding an FPGA I/O Node to the block diagram, click the element section of the node, and select FPGA Fan Speed (RPM). If there is error on the FPGA Fan, the FPGA Fan Error I/O Node will output 'True'. FPGA Fan control can be forced on by setting FPGA Fan Enable (Override) and FPGA Fan Override to 'True'.

Software Overview

Programming the NI PCIe-1477 requires the following application software and device driver. Install the software in the following order:

1. LabVIEW 2017 SP1 or later - Refer to the **LabVIEW Installation Guide** for installation instructions for LabVIEW and system requirements for the LabVIEW software. Refer to the **LabVIEW Upgrade Notes** for additional information about upgrading to the most recent version of LabVIEW.

   Note Documentation for LabVIEW is available by selecting Start » All Programs » National Instruments » LabVIEW » LabVIEW Manuals.

2. LabVIEW FPGA Module 2017 SP1 or later - Refer to the **LabVIEW FPGA Module Release and Upgrade Notes** for installation instructions and information about getting started with the LabVIEW FPGA Module.

   Note Documentation for the LabVIEW FPGA Module is available by selecting Start » All Programs » National Instruments » LabVIEW » LabVIEW Manuals.

3. NI-IMAQ I/O 18.5 or later - Refer to the **NI Vision Acquisition Software Release Notes** on the NI Vision Acquisition Software installation media for system requirements and installation instructions for the NI-IMAQ I/O driver.

   Note Documentation for the NI-IMAQ I/O driver software is available by selecting Start » All Programs » National Instruments » Vision » Documentation » NI-IMAQ I/O Documentation.

4. (Optional) NI Vision Development Module[1] - Refer to the **NI Vision Development Module Readme** on the NI Vision Development Module installation media for system requirements and installation instructions.

   Note Documentation for the NI Vision Development Module is available by selecting Start » All Programs » National Instruments » Vision » Documentation » Vision Documentation.

[1] VDM 17.5 or later for LabVIEW 2017 SP1 / VDM 18.0 or later for LabVIEW 2018

NI-IMAQ I/O Driver Software

The NI PCIe-1477 ships with NI Vision Acquisition Software, which includes the NI-IMAQ I/O driver software. The NI-IMAQ I/O driver software includes the kernel driver necessary for detecting and communicating with the NI PCIe-1477, the serial API that is used for configuring Camera Link cameras, and the support files necessary for creating and interacting with custom LabVIEW FPGA VIs.
The NI PCIe-1477 is an NI-RIO product and uses the NI-RIO API. See the installed examples (<LabVIEW Directory>\examples\Vision-RIO\PCIe-1477) for common acquisition templates. These examples can be used as a starting point for your application, and they can be modified to add custom image processing to accomplish your application-specific goals.

National Instruments Application Software

This section describes the National Instruments application software packages you can use to analyze and process the images you acquire with the NI PCIe-1477.

Vision Development Module

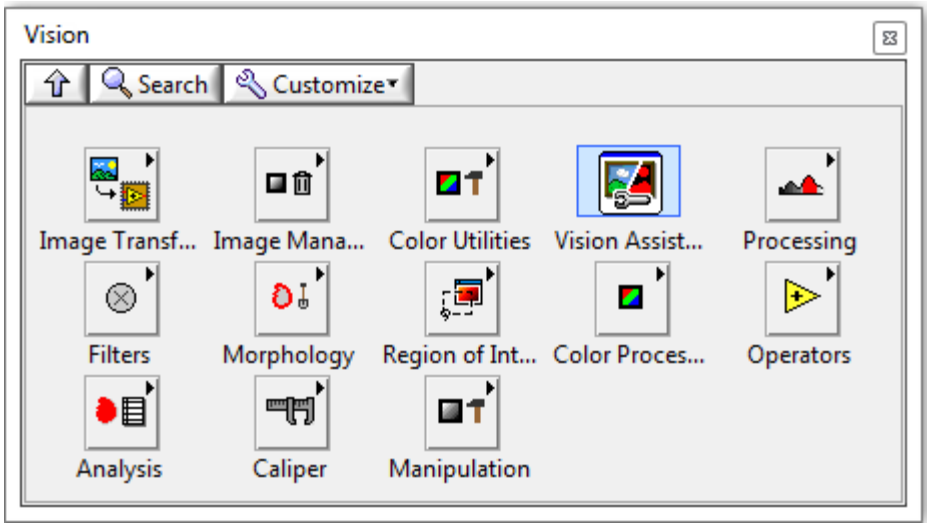
NI Vision Development Module (VDM), which consists of NI Vision and NI Vision Assistant, is an image acquisition, processing, and analysis library for common machine vision tasks, such as:

- Pattern matching
- Particle analysis
- Gauging
- Taking measurements
- Grayscale, color, and binary image display

You can use VDM functions individually or in combination. With VDM, you can acquire, display, and store images, as well as perform image analysis and processing.
Included with VDM, NI Vision Assistant is an interactive prototyping tool for machine vision and scientific imaging developers.
VDM, along with LabVIEW FPGA, lets developers achieve fully pipelined, low-latency, architecture-optimized vision IP on the FPGA. VDM with Vision Assistant helps in fast prototyping and code generation, FPGA resources estimation, automatic code

parallelization, and synchronization of parallel streams (for tasks such as latency balancing).
The NI PCIe-1477 provides a way for users to perform inline image processing. Users can have the acquisition logic and image processing logic running on the NI PCIe-1477. This ensures that there is no image transfer overhead between image acquisition logic and image processing logic. VDM includes more than fifty FPGA image processing functions as well as functions to transfer images efficiently between the FPGA and the host processor, as shown in the following figure.

Figure 2. Vision Palette for FPGA functions in Vision Development Module

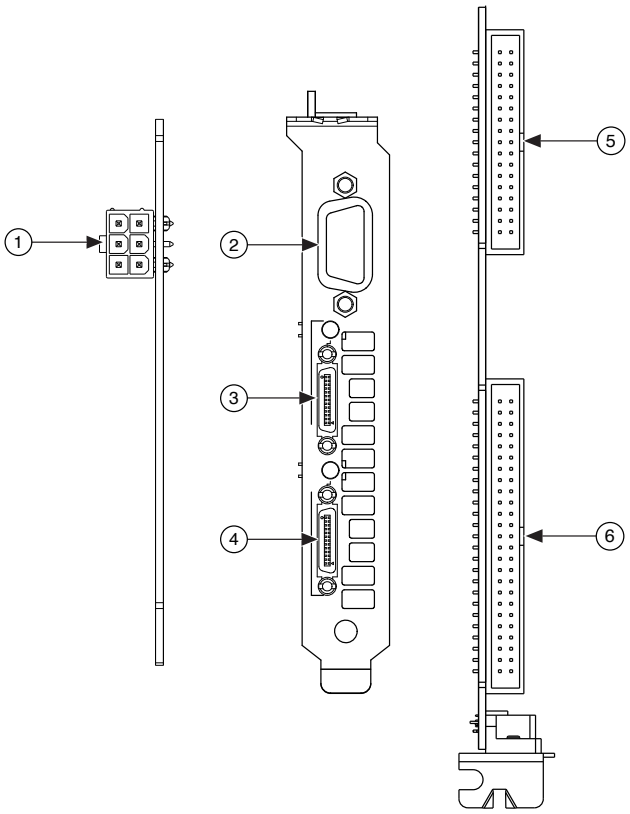


Running multiple image pipelines in parallel is a common requirement. Such scenarios dictate that at the time the pipelines merge into a single pipeline, the latency of the parallel pipelines must be balanced. VDM provides a synchronization buffer as part of its vision FPGA IP toolset which can help address this problem. If the latency differences between the pipelines are smaller, internal memory will be called, if not there would be a requirement of external memory.

Signal Connections

This section describes the connectors on the NI PCIe-1477. The following figure shows the connectors.

Figure 3. NI PCIe-1477 Connectors



1. 6-pin PCIe Auxiliary Power Connector
2. Digital I/O Connector
3. Base Camera Link Connector
4. Medium/Full Camera Link Connector
5. RTSI Connector
6. I/O Extension Connector

SDR Connectors

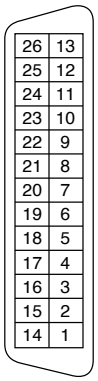
The Base and Medium/Full connectors are 26-pinSDR connectors that provide reliable high-frequency transfer rates between the camera and the NI PCIe-1477.

- For Lite and Base configuration cameras, connect one 26-pinSDRCamera Link cable to the Base port on the NI PCIe-1477.
- For Medium, Full, 72-bit, or 80-bit configuration cameras, connect one 26-pinSDRCamera Link cable to the Base port and one 26-pinSDR cable to the

Medium/Full port on the NI PCIe-1477. Ensure that the Base port cable is connected to the Base port on the camera and that the Medium/Full port cable is connected to the Medium/Full port on the camera.

The following figure shows the NI PCIe-1477 26-pin SDR connector.

Figure 4. 26-pin SDR Connector



The following tables list the pin descriptions for the Base connector and the Medium/Full connector.

Pin Number	Signal Name	Description
1	DGND/12 V	Digital Ground when connected to non-PoCL cameras and 12 V power supply when connected to PoCL cameras.
2	CC(4)-	LVDS, defined as camera inputs and device outputs, reserved for camera control. On some cameras, the camera controls allow the device to control exposure time and frame rate.
3	CC(3)+	LVDS, defined as camera inputs and device outputs, reserved for camera control. On some cameras, the camera controls allow the device to control exposure time and frame rate.
4	CC(2)-	LVDS, defined as camera inputs and device outputs, reserved for camera control. On some cameras, the camera controls allow the device to control exposure time and frame rate.
5	CC(1)+	LVDS, defined as camera inputs and device outputs, reserved for camera control. On some cameras, the camera controls allow the device to control exposure time and frame rate.
6	SerTFG+	Serial transmission to the NI PCIe-1477 from the camera.
7	SerTC-	Serial transmission to the camera from the NI PCIe-1477.
8	X(3)+	Base configuration data and enable signal from the camera to the NI PCIe-1477.

Pin Number	Signal Name	Description
9	XCLK+	Transmission clock on the Base configuration chip for Camera Link communication between the NI PCIe-1477 and the camera.
10	X(2)+	Base configuration data and enable signal from the camera to the NI PCIe-1477.
11	X(1)+	Base configuration data and enable signal from the camera to the NI PCIe-1477.
12	X(0)+	Base configuration data and enable signal from the camera to the NI PCIe-1477.
13	DGND	Digital ground
14	DGND	Digital ground
15	CC(4)+	LVDS, defined as camera inputs and device outputs, reserved for camera control. On some cameras, the camera controls allow the device to control exposure time and frame rate.
16	CC(3)-	LVDS, defined as camera inputs and device outputs, reserved for camera control. On some cameras, the camera controls allow the device to control exposure time and frame rate.
17	CC(2)+	LVDS, defined as camera inputs and device outputs, reserved for camera control. On some cameras, the camera controls allow the device to control exposure time and frame rate.
18	CC(1)-	LVDS, defined as camera inputs and device outputs, reserved for camera control. On some cameras, the camera controls allow the device to control exposure time and frame rate.
19	SerTFG-	Serial transmission to the NI PCIe-1477 from the camera.
20	SerTC+	Serial transmission to the camera from the NI PCIe-1477.
21	X(3)-	Base configuration data and enable signal from the camera to the NI PCIe-1477.
22	XCLK-	Transmission clock on the Base configuration chip for Camera Link communication between the NI PCIe-1477 and the camera.
23	X(2)-	Base configuration data and enable signal from the camera to the NI PCIe-1477.
24	X(1)-	Base configuration data and enable signal from the camera to the NI PCIe-1477.
25	X(0)-	Base configuration data and enable signal from the camera to the NI PCIe-1477.

Pin Number	Signal Name	Description
26	DGND/12 V	Digital Ground when connected to non-PoCL cameras and 12 V power supply when connected to PoCL cameras.

Table 1. NI PCIe-1477 Base Connector Signal Descriptions

Pin Number	Signal Name	Description
1	DGND/12 V	Digital Ground when connected to non-PoCL cameras and 12 V power supply when connected to PoCL cameras.
2	Z(3)+	Full configuration data and enable signal from the camera to the NI PCIe-1477.
3	ZCLK+	Transmission clock on the Full configuration chip for Camera Link communication between the NI PCIe-1477 and the camera.
4	Z(2)+	Full configuration data and enable signal from the camera to the NI PCIe-1477.
5	Z(1)+	Full configuration data and enable signal from the camera to the NI PCIe-1477.
6	Z(0)+	Full configuration data and enable signal from the camera to the NI PCIe-1477.
7	-	100 Ω differential termination with pin 20.
8	Y(3)+	Medium configuration data and enable signal from the camera to the NI PCIe-1477.
9	YCLK+	Transmission clock on the Medium configuration chip for Camera Link communication between the NI PCIe-1477 and the camera.
10	Y(2)+	Medium configuration data and enable signal from the camera to the NI PCIe-1477.
11	Y(1)+	Medium configuration data and enable signal from the camera to the NI PCIe-1477.
12	Y(0)+	Medium configuration data and enable signal from the camera to the NI PCIe-1477.
13	DGND	Digital ground
14	DGND	Digital ground
15	Z(3)-	Full configuration data and enable signal from the camera to the NI PCIe-1477.

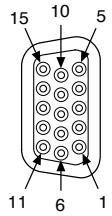
Pin Number	Signal Name	Description
16	ZCLK-	Transmission clock on the Full configuration chip for Camera Link communication between the NI PCIe-1477 and the camera.
17	Z(2)-	Full configuration data and enable signal from the camera to the NI PCIe-1477.
18	Z(1)-	Full configuration data and enable signal from the camera to the NI PCIe-1477.
19	Z(0)-	Full configuration data and enable signal from the camera to the NI PCIe-1477.
20	-	100 Ω differential termination with pin 7.
21	Y(3)-	Base configuration data and enable signal from the camera to the NI PCIe-1477.
22	YCLK-	Transmission clock on the Medium configuration chip for Camera Link communication between the NI PCIe-1477 and the camera.
23	Y(2)-	Base configuration data and enable signal from the camera to the NI PCIe-1477.
24	Y(1)-	Base configuration data and enable signal from the camera to the NI PCIe-1477.
25	Y(0)-	Base configuration data and enable signal from the camera to the NI PCIe-1477.
26	DGND/12 V	Digital Ground when connected to non-PoCL cameras and 12 V power supply when connected to PoCL cameras.

Table 2. NI PCIe-1477 Medium/Full Connector Signal Descriptions

D-SUB Connector

The 15-pin female high-density D-SUB connector connects to general purpose digital I/O, which includes six TTL I/O lines, two isolated inputs, and two bidirectional RS-422 ports, which can be used as a quadrature encoder input. The following table shows the connector assignments and descriptions.

Figure 5. 15-pin D-SUB Connector



Pin Number	Signal Name	Description
1	TTL I/O 0	TTL-compatible Digital I/O or external trigger
2	Iso Input 0+	24 V-compatible isolated current-sinking digital input
3	Diff 0+	Bidirectional RS-422 I/O (positive side), or quadrature encoder phase A+
4	Diff 1-	Bidirectional RS-422 I/O (negative side), or quadrature encoder phase B-
5	TTL I/O 4	TTL-compatible Digital I/O or external trigger
6	TTL I/O 1	TTL-compatible Digital I/O or external trigger
7	TTL I/O 2	TTL-compatible Digital I/O or external trigger
8	Iso Input 1+	24 V-compatible isolated current-sinking digital input
9	Diff 1+	Bidirectional RS-422 I/O (positive side), or quadrature encoder phase B+
10	TTL I/O 3	TTL-compatible Digital I/O or external trigger
11	Digital Ground	Digital Ground reference for quadrature encoder inputs and TTL I/O
12	Iso Input 0- Iso Input 1-	Common Ground reference for isolated digital inputs
13	Diff 0-	Bidirectional RS-422 I/O (negative side), or quadrature encoder phase A-
14	Digital Ground	Digital Ground reference for quadrature encoder inputs and TTL I/O
15	TTL I/O 5	TTL-compatible Digital I/O or external trigger

Table 6. NI PCIe-1477 15-pin D-SUB Connector Pin Descriptions

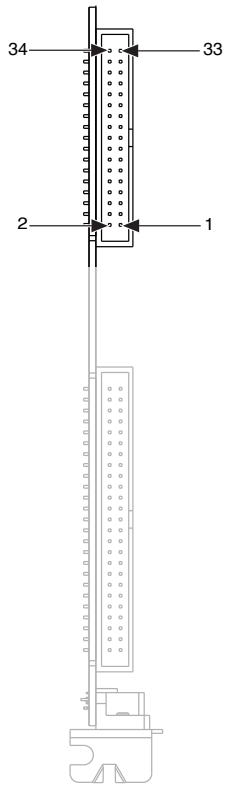
Tip Go to FPGA Digital I/O Node to Connector Pin Mapping for more information how each I/O node in the FPGA maps to the signals on the D-SUB connector.

RTSI Connector

The Real-Time System Integration (RTSI) connector allows connection to one or more NI DAQ devices. This allows I/O and trigger expansion beyond that normally available to the NI PCIe-1477. The RTSI bus should only be used with NI devices compatible with the RTSI bus.

Notice The RTSI connector is designed to work only with the NI products that have a RTSI connector. Each RTSI I/O is a bidirectional pin that is compatible with both 3.3 V (LVTTL/LVCMOS) and 5 V I/O (TTL/CMOS). No over-voltage protection, reverse voltage protection, or isolation is provided on this connector. Improper use of this connector will result in damage to the NI PCIe-1477. Use of a RTSI-compatible NI product is recommended.

Figure 6. RTSI Connector



Pin Number	Description
1 to 18	No connection

Pin Number	Description
19	Digital Ground
20	RTSI 0
21	Digital Ground
22	RTSI 1
23	Digital Ground
24	RTSI 2
25	Digital Ground
26	RTSI 3
27	Digital Ground
28	RTSI 4
29	Digital Ground
30	RTSI 5
31	Digital Ground
32	RTSI 6
33	Digital Ground
34	RTSI 7 / RTSI Clock

Table 6. NI PCIe-1477 RTSI Connector Pin Descriptions

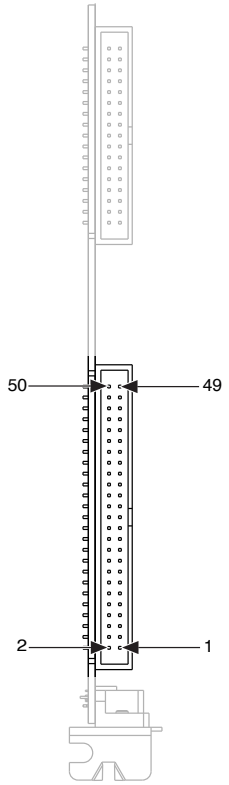
I/O Extension Connector

The I/O extension connector is designed to work only with the NI Camera Link I/O Extension Board, which is available in both PCIe and PCI form factors (NI part numbers 780869-01 and 779352-01). See the corresponding user manual for details and specifications for the external I/O of the extension board. The following table describes the pinout of the internal extension connector on the NI PCIe-1477, which controls the NI Camera Link I/O Extension Board.

Notice The I/O extension connector is designed to work only with the NI Camera Link I/O Extension Board. All the I/O on the extension connector is compatible only with 3.3 V (LVTTL/LVCMOS) I/O. No over-voltage protection, reverse voltage protection, or isolation is provided on this connector. Improper use of this connector will result in damage to the NI

PCIe-1477. Use of the NI Camera Link I/O Extension Board is recommended.

Figure 7. I/O Extension Connector



Pin Number	Signal Name	Direction	Description
1	Phase A	Input	Single-ended version of the extension board's quadrature encoder phase A input
2	Phase B	Input	Single-ended version of the extension board's quadrature encoder phase B input
3	Digital Ground	N/A	Ground reference for all I/O on extension connector
4	Iso In 2	Input	Non-isolated version of the extension board's isolated input
5	Iso Out 2 #	Output	Inverted, non-isolated version of the extension board's isolated output
6	Digital Ground	N/A	Ground reference for all I/O on extension connector
7	TTL In 1 #	Input	Inverted version of the extension board's TTL input
8	TTL In 2 #	Input	Inverted version of the extension board's TTL input

Pin Number	Signal Name	Direction	Description
9	Digital Ground	N/A	Ground reference for all I/O on extension connector
10	TTL In 3 #	Input	Inverted version of the extension board's TTL input
11	TTL In 4 #	Input	Inverted version of the extension board's TTL input
12	TTL In 5 #	Input	Inverted version of the extension board's TTL input
13	Digital Ground	N/A	Ground reference for all I/O on extension connector
14	TTL In 6 #	Input	Inverted version of the extension board's TTL input
15	TTL In 7 #	Input	Inverted version of the extension board's TTL input
16	TTL In 8 #	Input	Inverted version of the extension board's TTL input
17	Digital Ground	N/A	Ground reference for all I/O on extension connector
18	TTL Out 1	Output	Signal to be output to by the extension board's TTL output
19	TTL Out Enable 1	Output	Output enable (tristate disable) for the corresponding TTL
20	TTL Out 2	Output	Signal to be output to by the extension board's TTL output
21	Digital Ground	N/A	Ground reference for all I/O on extension connector
22	TTL Out Enable 2	Output	Output enable (tristate disable) for the corresponding TTL
23	TTL Out 3	Output	Signal to be output to by the extension board's TTL output
24	TTL Out Enable 3	Output	Output enable (tristate disable) for the corresponding TTL
25	Digital Ground	N/A	Ground reference for all I/O on extension connector
26	TTL Out 4	Output	Signal to be output to by the extension board's TTL output
27	TTL Out Enable 4	Output	Output enable (tristate disable) for the corresponding TTL
28	Digital Ground	N/A	Ground reference for all I/O on extension connector
29	TTL Out 5	Output	Signal to be output to by the extension board's TTL output
30	TTL Out Enable 5	Output	Output enable (tristate disable) for the corresponding TTL
31	TTL Out 6	Output	Signal to be output to by the extension board's TTL output

Pin Number	Signal Name	Direction	Description
32	Digital Ground	N/A	Ground reference for all I/O on extension connector
33	TTL Out Enable 6	Output	Output enable (tristate disable) for the corresponding TTL
34	TTL Out 7	Output	Signal to be output to by the extension board's TTL output
35	TTL Out Enable 7	Output	Output enable (tristate disable) for the corresponding TTL
36	Digital Ground	N/A	Ground reference for all I/O on extension connector
37	TTL Out 8	Output	Signal to be output to by the extension board's TTL output
38	TTL Out Enable 8	Output	Output enable (tristate disable) for the corresponding TTL
39	Digital Ground	N/A	Ground reference for all I/O on extension connector
40	Iso In 0	Input	Non-isolated version of the extension board's isolated input
41	Iso In 1	Input	Non-isolated version of the extension board's isolated input
42	Digital Ground	N/A	Ground reference for all I/O on extension connector
43	Iso Out 0 #	Output	Inverted, non-isolated version of the extension board's isolated output
44	Iso Out 1 #	Output	Inverted, non-isolated version of the extension board's isolated output
45	Board Present	Input	Indicates if the extension board is present
46	Reserved	N/A	Reserved
47	Digital Ground	N/A	Ground reference for all I/O on extension connector
48	Reserved	N/A	Reserved
49	Reserved	N/A	Reserved
50	Board Power Enable	Output	Signal to enable extension board power

Table 6. NI PCIe-1477 I/O Extension Connector Pin Descriptions

Tip Go to FPGA Digital I/O Node to Connector Pin Mapping for more information how each I/O node in the FPGA maps to the signals on the I/O Extension connector.

FPGA Digital I/O Node to Connector Pin Mapping

The following table shows how each FPGA I/O node in the FPGA maps to the signals on the NI PCIe-1477 D-SUB and I/O Extension Board D-SUB connectors.

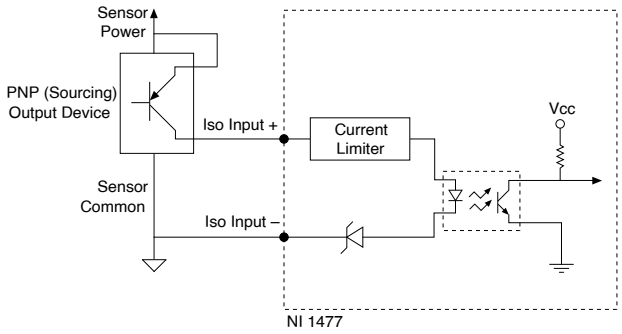
FPGA Digital I/O Node	Connector	Connector Signal Name
TTL 0	NI PCIe-1477 D-SUB	TTL I/O 0
TTL 1	NI PCIe-1477 D-SUB	TTL I/O 1
TTL 2	NI PCIe-1477 D-SUB	TTL I/O 2
TTL 3	NI PCIe-1477 D-SUB	TTL I/O 3
TTL 4	NI PCIe-1477 D-SUB	TTL I/O 4
TTL 5	NI PCIe-1477 D-SUB	TTL I/O 5
TTL 6	I/O Extension Board D-SUB	TTL I/O 1
TTL 7	I/O Extension Board D-SUB	TTL I/O 2
TTL 8	I/O Extension Board D-SUB	TTL I/O 3
TTL 9	I/O Extension Board D-SUB	TTL I/O 4
TTL 10	I/O Extension Board D-SUB	TTL I/O 5
TTL 11	I/O Extension Board D-SUB	TTL I/O 6
TTL 12	I/O Extension Board D-SUB	TTL I/O 7
TTL 13	I/O Extension Board D-SUB	TTL I/O 8
ISO In 0	NI PCIe-1477 D-SUB	Iso Input 0+, Iso Input 0-
ISO In 1	NI PCIe-1477 D-SUB	Iso Input 1+, Iso Input 1-
ISO In 2	I/O Extension Board D-SUB	Iso Input 0+, Iso Input 0-
ISO In 3	I/O Extension Board D-SUB	Iso Input 1+, Iso Input 1-
ISO In 4	I/O Extension Board D-SUB	Iso Input 2+, Iso Input 2-
ISO Out 0	I/O Extension Board D-SUB	Iso Output 0
ISO Out 1	I/O Extension Board D-SUB	Iso Output 1
ISO Out 2	I/O Extension Board D-SUB	Iso Output 2
QE Phase A (D-Sub)	NI PCIe-1477 D-SUB	Diff 0+, Diff 0-
QE Phase B (D-Sub)	NI PCIe-1477 D-SUB	Diff 1+, Diff 1-
QE Phase A (I/O Extension Board)	I/O Extension Board D-SUB	Phase A+, Phase A-
QE Phase B (I/O Extension Board)	I/O Extension Board D-SUB	Phase B+, Phase B-

Table 6. NI PCIe-1477 FPGA Digital I/O Node to Connector Pin Mapping

Connecting Signals

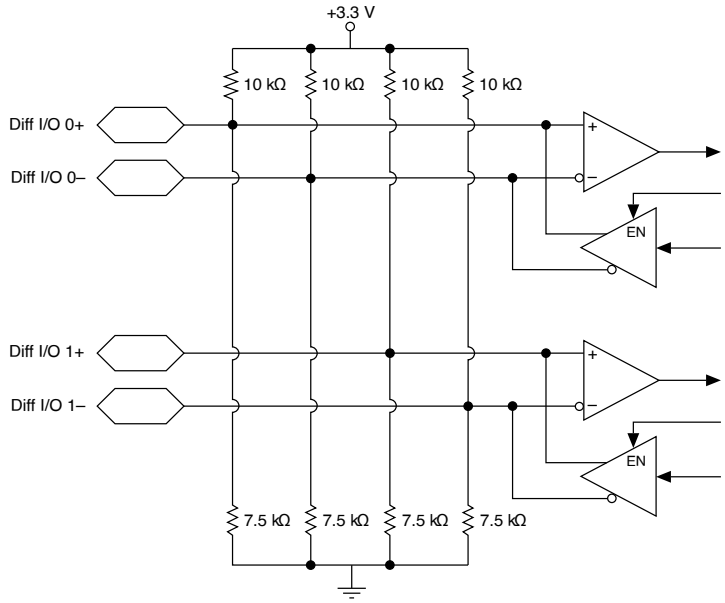
The following diagrams show how different signals are connected to the NI PCIe-1477. Use shielded cables for all applications. Unshielded cables are more susceptible to noise and can corrupt the signals.
The following figure shows how to connect an isolated input to a sourcing output device. Refer to the **NI PCIe-1477 Specifications** for information about switching thresholds and current requirements.

Figure 8. Connecting an Isolated Input to a Sourcing Output Device



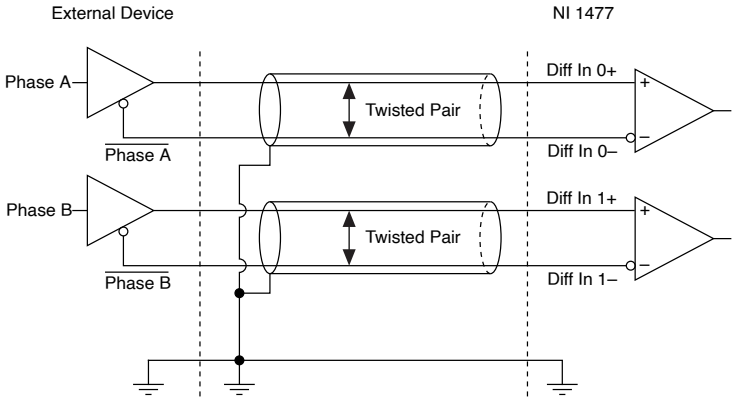
The following figure shows how the bidirectional differential I/O circuits are implemented internally on the NI PCIe-1477. The differential I/O circuit can output a differential (RS-422 compatible) signal. It can receive a differential (RS-422 compatible) or single-ended TTL signal. Differential signaling is recommended for improved reliability on these inputs.

Figure 9. NI PCIe-1477 Quadrature Encoder/RS-422 Input/Output Circuit



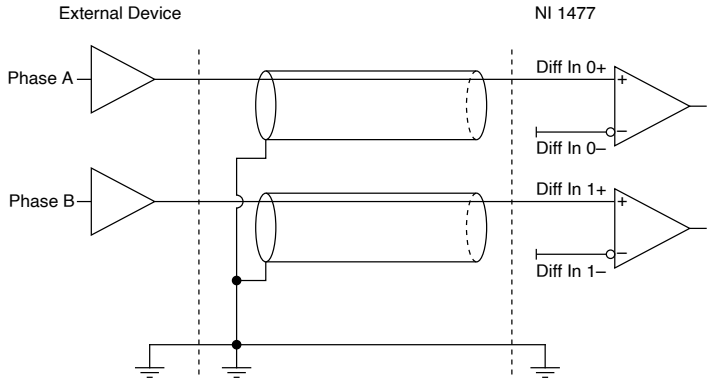
The following figure shows an example of connecting differential encoder line drivers.

Figure 10. Connecting Differential Line Drivers



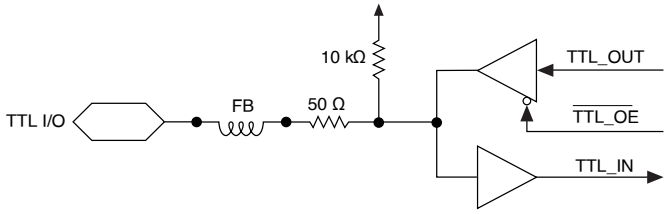
If single-ended TTL or encoder is used, the line should be connected to the positive connection. An example of connecting single-ended encoder drivers is shown as follows:

Figure 11. Connecting Single-Ended Line Drivers



The following figure shows how the TTL I/O circuit is implemented internally on the NI PCIe-1477.

Figure 12. NI PCIe-1477 TTL Input/Output Circuit



Cabling

Use a standard Camera Link cable to connect your camera to the 26-pin SDR connector on the NI PCIe-1477. Camera Link cables consist of two SDR-26 male plugs linked with a twin-axial shielded cable and are available in two shell configurations.
NI recommends that you use the following cables to connect your camera to the 26-pin SDR connectors on the NI PCIe-1477:

- SDR to SDR Camera Link, 5 m cable (part number 199746-05)
- MDR to SDR Camera Link, 5 m cable (part number 199745-05)
- 15-pin D-SUB Male to Female, 5 m cable (part number 147791-05)
- 15-pin D-SUB Male to Female, 2 m cable (part number 147791-02)
- 15-pin D-SUB to Pigtail, 5 m cable (part number 147792-05)

Note To ensure the quality of the high-speed signaling of the Camera Link interface, NI recommends that you purchase high-quality Camera Link

> cables that are rated for the expected pixel clock frequencies rather than build a custom cable.

Refer to the Camera Link Specification for more information about Camera Link cables. This specification is available on the Automated Imaging Association (AIA) website at www.visiononline.org.

NI Services

Visit ni.com/support to find support resources including documentation, downloads, and troubleshooting and application development self-help such as tutorials and examples.

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