PXIe-5186 Specifications





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PXIe-5186 Specifications.

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Definitions

Warranted specifications describe the performance of a model under stated operating conditions and are covered by the model warranty.

Characteristics describe values that are relevant to the use of the model under stated operating conditions but are not covered by the model warranty.

- **Typical** specifications describe the performance met by a majority of models.
- **Nominal** specifications describe an attribute that is based on design, conformance testing, or supplemental testing.

Conditions

Specifications are valid under the following conditions unless otherwise noted.

- For 50 Ω input channel, vertical range (Vpk-pk) set to 0.11, 0.2, 0.5, or 1
- For 50 Ω input channel, vertical range (Vpk-pk) set to 0.11, 0.2, 0.5, 1, 2, 5, or 10
- 1 MΩ input channel disconnected for 50 Ω input channel specifications, and 50 Ω input channel disconnected for 1 MΩ input channel specifications
- Sample clock set to 6.25 GS/s or 12.5 GS/s
- Onboard Sample clock locked to PXIe_CLK100 Reference clock
- 0 °C to 50 °C ambient temperature

Note Early versions of the PXIe-5186 only support 50Ω input impedance. Later versions support both 50Ω and 50Ω input impedance. To verify input impedances supported by your device, compare your device front panel with the diagrams at the end of this document. You can also check the device part number:

- PXIe-5186 module part numbers 193537x-0zL (where x is any letter and z is any number) only support 50 Ω input impedance.
- PXIe-5186 module part numbers 152961**x**-0**z**L (where **x** is any letter and **z** is any number) support both 50 Ω and 1 MΩ input impedance

Warranted specifications are valid under the following conditions unless otherwise noted.

- The PXIe-5186 is warmed up for 25 minutes at ambient temperature
- Self-calibration is completed after warm-up period or when switching from an external Sample and/or Reference clock to the Onboard clock
- Calibration cycle is maintained
- The PXI Express chassis fan speed is set to HIGH, the fan filters are clean if present, and the empty slots contain PXI chassis slot blockers and filler panels. For more information about cooling, refer to the Maintain Forced-Air Cooling Note to Users document available at ni.com/manuals.
- NI-SCOPE 3.9.6 or later instrument driver is used
- External calibration is performed at 23 °C ± 3 °C

Vertical

Analog Input (Channel 0 and Channel 1)

Number of channels	Two (simultaneously sampled)
Input type	Reference single-ended
Connectors	
СН 0, 50 Ω	SMA
CH 1, 50 Ω	SMA

CH 0, 1 MΩ	BNC
CH 1, 1 MΩ	BNC

Impedance and Coupling

Input impedance, typical				
50 Ω	$50 \Omega \pm 1.5\%$			
1 MΩ	$1\text{M}\Omega\pm1.0\%$ in parallel with a cha	aracteristic capacitance of 10 pF		
Input	Input coupling			
50 Ω	DC			
1 ΜΩ	AC, DC; software-selecta	able		
Voltage standing wave ratio (VSWR), characteristic ^[1]				
≥DC to	o ≤1 GHz	1.25:1		
>1 GHz	z to ≤5 GHz	1.8:1		

Figure 1. 50 Ω Input VSWR and Input Return Loss



Voltage Levels

Input	Input range (V _{pk-pk})	Vertical offset range (V)
50 Ω and 1 M Ω inputs	0.11 to 1 in >0.3 mV steps	±0.25
$1 \text{M}\Omega$ input only	>1 to 10 in >3 mV steps	±2.5

Table 1. Full Scale (FS) Input Range and Programmable Vertical Offset

Maximum input overload, characteristic ^[2]		
50 Ω	Peaks ≤1V	
1 ΜΩ	Peaks ≤42 V	

Accuracy

Resolution		8 bits
DC accurae	cy (programmable vertical offset = 0 Volts), war	ranted ^[3]
50 Ω	±(2% of input + 0.35% of FS + 0.7 n	nV)
1 ΜΩ	±(2% of input + 0.9% of FS + 1.3 m)	√)
Programmable vertical offset accuracy, warranted ^[3] ±1.2% of offset setting		
DC drift, cl	haracteristic ^[4]	
50 Ω	±(0.23% of input + 0.03% of FS) per °C	
1 ΜΩ	±(0.23% of input + 0.1% FS + 0.2 mV) per °C	
Programma	able vertical offset drift, characteristic ^[4]	±0.02% of offset setting per °C

AC amplitude accuracy, warranted ^[3]			
50 Ω	±0.35 dB at 50 kHz		
1 ΜΩ	±0.5 dB at 50 kHz		
AC amplitude drift, characterist	ic[4]	±0.014 dB per °C at 50 kHz	
Crosstalk (CH 0 to/from CH 1)	, characteristic ^[5]		
50 Ω			
≥DC to ≤1 GHz		–68 dB	
>1 GHz to ≤2.5 GHz		–60 dB	
>2.5 GHz to ≤5 GHz		–47 dB	
1 MΩ: ≥DC to ≤300 MHz		–62 dB	

Bandwidth and Transient Response

Bandwidth (-3 dB) ^[6]	
50 Ω, warranted	5 GHz, warranted
1 MΩ [7]	500 MHz, characteristic; 425 MHz, warranted
Rise/fall time, typical ^[8]	
50 Ω	105 ps
1 ΜΩ	750 ps

AC-coupling cutoff (-3 dB), typical ^[9]	10 Hz

Figure 1. NI 5186 Step Response, 50 Ω , -0.25 V Programmable Offset, 85 ps Rising Edge, Characteristic



Figure 3. PXIe-5186 Step Response, 1 M Ω , -0.25 V Programmable Offset, 500 ps Rising Edge, Characteristic





Figure 1. NI 5186 50Ω Frequency Response, Characteristic

Figure 5. PXIe-5186 1 M Ω Frequency Response, Characteristic



Spectral Characteristics

PXIe-5186 50 Ω Spectral Characteristics

PXIe-5186 1 M Ω Spectral Characteristics



1V pk-pk, 2 Vpk-pk, 5 Vpk-pk, or 10 Vpk-pk range 50 dBc >10 MHz 50 dBc >10 MHz to ≤300 MHz 41 dBc Total Harmonic Distortion (THD), characteristic ^[10] 0.11 V pk-pk, 0.2 Vpk-pk, or 0.5 Vpk-pk range -54 dBc >10 MHz -54 dBc >10 MHz to ≤300 MHz -44 dBc 1V pk-pk, 2 Vpk-pk, 5 Vpk-pk, or 10 Vpk-pk range -50 dBc >10 MHz to ≤300 MHz -40 dBc 10 MHz to ≤300 MHz -50 dBc >10 MHz to ≤300 MHz 5.9 300 MHz 5.9 300 MHz 5.9 300 MHz 6.3	>10 MHz to ≤300 MHz	45 dBc
≤10 MHz to ≤300 MHz 41 dBc 10 MHz to ≤300 MHz 41 dBc Total Harmonic Distortion (THD), characteristic ^[10] 0.11 V pk-pk, 0.2 Vpk-pk, or 0.5 Vpk-pk range ≤10 MHz to ≤300 MHz -54 dBc >10 MHz to ≤300 MHz -44 dBc 1V pk-pk, 2 Vpk-pk, 5 Vpk-pk, or 10 Vpk-pk range ≤10 MHz to ≤300 MHz -40 dBc ENOB, characteristic ^[11] 0.11 V pk-pk range 10 MHz 5.9 300 MHz 5.9	1 V _{pk-pk} , 2 V _{pk-pk} , 5 V _{pk-pk} , or 10 V _{pk-p}	_k range
>10 MHz to ≤300 MHz 41 dBc Total Harmonic Distortion (THD), characteristic ^[10] 0.11 V pk-pk, 0.2 Vpk-pk, or 0.5 Vpk-pk range ≤10 MHz 5300 MHz -54 dBc >10 MHz to ≤300 MHz -44 dBc 1 V pk-pk, 2 Vpk-pk, 5 Vpk-pk, or 10 Vpk-pk range ≤10 MHz to ≤300 MHz -40 dBc ENOB, characteristic ^[11] 0.11 V pk-pk range 10 MHz 5.9 300 MHz 5.9	≤10 MHz	50 dBc
Total Harmonic Distortion (THD), characteristic ^[10] 0.11 V pk-pk, 0.2 Vpk-pk, or 0.5 Vpk-pk range -54 dBc >10 MHz -54 dBc >10 MHz to ≤300 MHz -44 dBc 1V pk-pk, 2 Vpk-pk, 5 Vpk-pk, or 10 Vpk-pk range -50 dBc >10 MHz to ≤300 MHz -50 dBc >10 MHz to ≤300 MHz -40 dBc ≥10 MHz to ≤300 MHz -40 dBc ≥10 MHz to ≤300 MHz -50 dBc >10 MHz to ≤300 MHz 5.9 10 MHz 5.9 300 MHz 5.9 300 MHz 5.9 0.2 V pk-pk, 0.5 Vpk-pk, 1 Vpk-pk, 2 Vpk-pk, 5 Vpk-pk, or 10 Vpk-pk range 10 MHz 6.3	>10 MHz to ≤300 MHz	41 dBc
0.11 V pk-pk, 0.2 Vpk-pk, or 0.5 Vpk-pk range -54 dBc >10 MHz to ≤300 MHz -44 dBc 1 V pk-pk, 2 Vpk-pk, 5 Vpk-pk, or 10 Vpk-pk range -50 dBc >10 MHz to ≤300 MHz -50 dBc >10 MHz to ≤300 MHz -40 dBc >10 MHz to ≤300 MHz -40 dBc >10 MHz to ≤300 MHz -50 dBc 0.11 V pk-pk range -40 dBc 10 MHz 5.9 300 MHz 5.9 300 MHz 5.9 0.2 V pk-pk, 0.5 Vpk-pk, 1 Vpk-pk, 2 Vpk-pk, 5 Vpk-pk, or 10 Vpk-pk range 10 MHz 6.3	Total Harmonic Distortion (THD), char	acteristic ^[10]
≤10 MHz 10 ≤300 MHz 2000 HHz	0.11 V _{pk-pk} , 0.2 V _{pk-pk} , or 0.5 V _{pk-pk} ra	ange
>10 MHz to ≤300 MHz 1 V pk-pk, 2 V pk-pk, 5 V pk-pk, or 10 V pk-pk range ≤10 MHz 10 ≤300 MHz -50 dBc >10 MHz to ≤300 MHz -40 dBc ENOB, characteristic[11] 0.11 V pk-pk range 10 MHz 5.9 300 MHz 5.9	≤10 MHz	-54 dBc
1 V pk-pk, 2 Vpk-pk, 5 Vpk-pk, or 10 Vpk-pk range -50 dBc ≤10 MHz -50 dBc >10 MHz to ≤300 MHz -40 dBc ENOB, characteristic[11] 0.11 V pk-pk range 10 MHz 5.9 300 MHz 5.9 300 MHz 5.9 0.2 V pk-pk, 0.5 Vpk-pk, 1 Vpk-pk, 2 Vpk-pk, 5 Vpk-pk, or 10 Vpk-pk range 10 MHz 6.3	>10 MHz to ≤300 MHz	-44 dBc
≤10 MHz -50 dBc >10 MHz to ≤300 MHz -40 dBc ENOB, characteristic[11] 0.11 V pk-pk range 10 MHz 5.9 300 MHz 5.9 0.2 V pk-pk, 0.5 Vpk-pk, 1 Vpk-pk, 2 Vpk-pk, or 10 Vpk-pk range 10 MHz 6.3	1 V _{pk-pk} , 2 V _{pk-pk} , 5 V _{pk-pk} , or 10 V _{pk-p}	_k range
 >10 MHz to ≤300 MHz -40 dBc ENOB, characteristic^[11] 0.11 V pk-pk range 10 MHz 5.9 300 MHz 0.2 V pk-pk, 0.5 V pk-pk, 2 V pk-pk, 5 V pk-pk, or 10 V pk-pk range 10 MHz 6.3 	≤10 MHz	-50 dBc
ENOB, characteristic [11] 0.11 V pk-pk range 5.9 10 MHz 5.9 300 MHz 5.9 0.2 V pk-pk, 0.5 V pk-pk, 1 V pk-pk, 2 V pk-pk, 5 V pk-pk, or 10 V pk-pk range 10 MHz 6.3	>10 MHz to ≤300 MHz	-40 dBc
0.11 V _{pk-pk} range 10 MHz 5.9 300 MHz 5.9 0.2 V _{pk-pk} , 0.5 V _{pk-pk} , 1 V _{pk-pk} , 2 V _{pk-pk} , or 10 V _{pk-pk} range 10 MHz 6.3	ENOB, characteristic ^[11]	
10 MHz 5.9 300 MHz 5.9 О.2 V _{pk-pk} , 0.5 V _{pk-pk} , 2 V _{pk-pk} , 5 V _{pk-pk} , or 10 V _{pk-pk} range 10 MHz 6.3	0.11 V _{pk-pk} range	
300 MHz 5.9 0.2 V _{pk-pk}, 0.5 V_{pk-pk}, 1 V_{pk-pk}, 2 V_{pk-pk}, or 10 V_{pk-pk} range 10 MHz 6.3	10 MHz	5.9
0.2 V _{pk-pk} , 0.5 V _{pk-pk} , 1 V _{pk-pk} , 2 V _{pk-pk} , 5 V _{pk-pk} , or 10 V _{pk-pk} range 10 MHz 6.3	300 MHz	5.9
10 MHz 6.3	0.2 V _{pk-pk} , 0.5 V _{pk-pk} , 1 V _{pk-pk} , 2 V _{pk-p}	_k , 5 V _{pk-pk} , or 10 V _{pk-pk} range
	10 MHz	6.3

0.2 V _{pk-pk} , 0.5 V _{pk-pk} , 1 V _{pk-pk} , 2 V _{pk-pk} , 5 V _{pk-pk} , or 10 V _{pk-pk} range			

Noise

0.35% of FS		
0.5% of FS		
Average noise density, typical ^[14]		
-137 dBFS/Hz		
-134 dBFS/Hz		
	0.35% of FS 0.5% of FS bical^[14] -137 dBFS/Hz -134 dBFS/Hz	

Skew

Channel-to-channel skew, characteristic	
50 Ω to 50 Ω	< 10 ps
1 M\Omega to 1 MΩ	< 45 ps
50 Ω to 1 MΩ	< 1.5 ns

Horizontal

Sample Clock

Sources	
Internal	Onboard clock (internal VCO)[15]
External	Front panel SMA connector

Onboard Clock (Internal VCO)

Real-time sample rate range		
One channel enabled	190.740 kS/s to 12.5 GS/	/s[16]
Two channels enabled	190.740 kS/s to 6.25 GS/s ^[16]	
Random Interleaved Sampling (RIS) range		Up to 250 GS/s ^[17]

Figure 6. PXIe-5186 Phase Noise (Plotted without Spurs) at 1 GHz, 3 dBm Input Signal, Locked to 100 MHz PXI Express Backplane (Characteristic)



Sample clock jitter, characteristic ^[18]	500 fs rms (12 kHz to 10 MHz)
Timebase frequency	3.125 GHz
Timebase accuracy ^[19]	Accuracy equal to the backplane or user-provided Reference clock

External Sample Clock

Sources	CLK IN (front panel SMA connector)
Frequency range ^[20]	1.6 GHz to 3.125 GHz
Duty cycle tolerance, typical	45% to 55%

Phase-Locked Loop (PLL) Reference Clock

Sources		
Internal	PXIe_CLK100 (backplane connector)	
External	REF CLK (front panel SMB connector)	
Frequency ^[21]		10 MHz or 100 MHz
Duty cycle tolera	nce, characteristic	45% to 55%

CLK IN (Sample Clock Input, Front Panel Connector)

Input voltage range, characteristic	Sine wave: 0.45 V _{pk-pk} to 1.78 V _{pk-pk} (–3 dBm to 9 dBm)
Maximum input overload, characteristic	3 V _{rms} , Peaks ≤ 4.25 V
Impedance, nominal	50 Ω
Coupling	AC

REF CLK (Reference Clock In, Front Panel Connector)

Input voltage range, characteristic	Sine wave: -2 dBm to 16 dBm
Maximum input overload, typical	1.6 V _{rms} , Peaks ≤ 10 V (1 ms peak)
Impedance, nominal	50 Ω
Coupling	AC

Frequency ^[22]	10 MHz or 100 MHz

Trigger

Supported trigger	Reference (stop) trigger	
Trigger types	Edge, Digital, Immediate, and Software	
Trigger sources	CH 0, CH 1, TRIG, PXI_Trig <06>, and Software	
Time resolution		
Onboard Clock		
TDC (Time to Digital Conversion Circuit) on3 ps		3 ps
TDC off		2.56 ns
External clock, TDC off	External clock period × 8	
Rearm time ^[23]		
TDC on	10 µs	
TDC off	2 μs	
Holdoff	Rearm time to 10.99 s	
Trigger delay	From 0 to 1,450,000 seconds (15 days)	

Analog Trigger (Edge Trigger Type)

Sources	CH 0, CH 1, or TRIG
Trigger level range	
CH 0, CH 1	100% of FS
TRIG (external trigger)	±5 V
Voltage resolution	
CH 0, CH 1	8 bits (1 in 256)
TRIG (external trigger), characteristic	10 bits (1 in 1,024)
Edge trigger sensitivity	
CH 0, CH 1, typical	3% of FS at ≤1 GHz
TRIG (external trigger), characteristic	2% of FS at ≤100 MHz
Trigger level accuracy	
CH 0, CH 1, typical	±5% of FS at ≤100 MHz ^[24]
TRIG (external trigger), characteristic	±5% at ≤100 MHz ^[25]
Trigger jitter	
CH 0, CH 1, typical	≤16 ps rms
TRIG (external trigger), characteristic	≤16 ps rms

Digital Trigger (Digital Trigger Type)

Sources	PXIe_TRIG <06> (backplane connector)

TRIG (External Trigger, Front Panel Connector)

Connector	SMA
Impedance, nominal	50 Ω
Coupling	DC
Input voltage range, nominal	±5 V
Maximum input overload, characteristic	Peaks ≤ 6 V

TClk Specifications

You can use the National Instruments TClk synchronization method and the NI-TClk driver to align the Sample clocks on any number of SMC-based modules in a chassis. Specifications are valid for any number of NI 5185 or NI 5186 modules installed in one PXI Express chassis, with all parameters set to identical values for each SMC-based module. For more information about TClk synchronization, refer to the **NI-TClk Synchronization Help**, which is located within the **NI High-Speed Digitizers Help**. For other configurations, including multichassis systems, contact NI Technical Support at <u>ni.com/support</u>.

Note You can only use NI-TClk to synchronize NI 5185 or NI 5186 devices to other NI 5185 or NI 5186 devices. These specifications apply only to synchronizing identical modules without using an external Sample clock.

Intermodule SMC synchronization using NI-TClk for identical modules, characteristic

Skew ^[26]	500 ps
Skew after manual adjustment	160 ps
Sample clock delay/adjustment resolution	80 ps
Triggers that can be TClk synchronized ^[27]	Reference trigger

Waveform Specifications

Onboard memory sizes ^[28]	32 MB or 1 GB	
Minimum record length, characteristic	1 sample	
Number of pretrigger samples, characteristic ^[29]	Zero up to full record length	
Number of posttrigger samples, characteristic ^[29]	Zero up to full record length	
Maximum number of records in onboard memory, characteristic		
16 MB per channel	4,096 [30]	
512 MB per channel	100,000[30]	
Allocated onboard memory per record, characteristic	[(Record length × 1 byte/sample) + 1,500], rounded up to: 4 KB, 8 KB, 16 KB, 32 KB, 64 KB, or an integer multiple of 128 KB	

Memory Sanitization

For information about memory sanitization, refer to the **NI PXIe-5185/5186 Letter of Volatility**, which is available for download from <u>ni.com/manuals</u>.

Calibration

Power-up calibration	Automatically performed by the device at power-on to calibrate the gain, offset, and phase of the ADCs on the device. Typically takes 5 to 10 minutes to complete.
Self-calibration	Self-calibration is done on software command. The calibration corrects for gain, offset, triggering, and timing errors for all input ranges, excluding the External Trigger input channel (TRIG). Refer to the NI High-Speed Digitizers Help for information about when to self-calibrate the device.
External calibration	The external calibration calibrates the onboard references used in self- calibration, the input overload levels, and the external trigger levels. All calibration constants are stored in nonvolatile memory.
Interval for external calibration	1 year
Warm-up time	25 minutes

Power

+3.3 VDC	5.1 A
+12 VDC	6.1 A
+5 V _{aux}	12 mA

Total power	90 W

Software

Driver Software

This device is supported in NI-SCOPE 3.9.6 or later. NI-SCOPE is an IVI-compliant driver that allows you to configure, control, and calibrate the PXIe-5186 . NI-SCOPE provides application programming interfaces for many development environments.

Application Software

NI-SCOPE provides programming interfaces, documentation, and examples for the following application development environments:

- LabVIEW
- LabWindows[™]/CVI[™]
- Measurement Studio
- Microsoft Visual C/C++
- Microsoft Visual Basic

Interactive Soft Front Panel and Configuration

The NI-SCOPE Soft Front Panel version 3.9.6 or later supports interactive control of the PXIe-5186 . The NI-SCOPE Soft Front Panel is included on the NI-SCOPE DVD.

National Instruments Measurement & Automation Explorer (MAX) also provides interactive configuration and test tools for the PXIe-5186 . MAX is included on the NI-SCOPE DVD.

Physical

Dimensions and Weight

Dimensions	3U, 3 slot, PXI Express Module, 21.6 × 6.2 × 13.0 cm (8.5 × 2.4 × 5.1 in.)
Weight	•
50 Ω	1,208 g (42.61 oz.)
1 ΜΩ	1,222 g (43.10 oz.)

Environment

Maximum altitude	2,000 m (800 mbar) (at 25 °C ambient temperature)
Pollution Degree	2

Indoor use only.

Operating Environment

Ambient temperature range	0 °C to 50 °C
Relative humidity range	10% to 90%, noncondensing

Storage Environment

Ambient temperature range	-40 °C to 71 °C
Relative humidity range	5% to 95%, noncondensing

Shock and Vibration

Operating shock	30 g peak, half-sine, 11 ms pulse
Random vibration	
Operating	5 Hz to 500 Hz, 0.3 g _{rms}
Nonoperating	5 Hz to 500 Hz, 2.4 g _{rms}

Compliance and Certifications

Safety Compliance Standards

This product is designed to meet the requirements of the following electrical equipment safety standards for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 61010-1, CSA C22.2 No. 61010-1



Note For safety certifications, refer to the product label or the <u>Product</u> <u>Certifications and Declarations</u> section.

Electromagnetic Compatibility

This product meets the requirements of the following EMC standards for electrical equipment for measurement, control, and laboratory use:

- EN 61326-1 (IEC 61326-1): Class A emissions; Basic immunity
- EN 55011 (CISPR 11): Group 1, Class A emissions
- EN 55022 (CISPR 22): Class A emissions
- EN 55024 (CISPR 24): Immunity
- AS/NZS CISPR 11: Group 1, Class A emissions
- AS/NZS CISPR 22: Class A emissions

- FCC 47 CFR Part 15B: Class A emissions
- ICES-001: Class A emissions



Note In the United States (per FCC 47 CFR), Class A equipment is intended for use in commercial, light-industrial, and heavy-industrial locations. In Europe, Canada, Australia, and New Zealand (per CISPR 11), Class A equipment is intended for use only in heavy-industrial locations.



Note Group 1 equipment (per CISPR 11) is any industrial, scientific, or medical equipment that does not intentionally generate radio frequency energy for the treatment of material or inspection/analysis purposes.



Note For EMC declarations, certifications, and additional information, refer to the <u>Product Certifications and Declarations</u> section.

Product Certifications and Declarations

Refer to the product Declaration of Conformity (DoC) for additional regulatory compliance information. To obtain product certifications and the DoC for NI products, visit <u>ni.com/product-certifications</u>, search by model number, and click the appropriate link.

Environmental Management

NI is committed to designing and manufacturing products in an environmentally responsible manner. NI recognizes that eliminating certain hazardous substances from our products is beneficial to the environment and to NI customers.

For additional environmental information, refer to the **Engineering a Healthy Planet** web page at <u>ni.com/environment</u>. This page contains the environmental regulations and directives with which NI complies, as well as other environmental information not included in this document.

EU and UK Customers

• A Waste Electrical and Electronic Equipment (WEEE)—At the end of the product life cycle, all NI products must be disposed of according to local laws and regulations. For more information about how to recycle NI products in your region, visit <u>ni.com/environment/weee</u>.

电子信息产品污染控制管理办法(中国 RoHS)

• ◎ ● 中国 RoHS— NI 符合中国电子信息产品中限制使用某些有害物 质指令(RoHS)。关于 NI 中国 RoHS 合规性信息,请登录 ni.com/environment/ rohs_china。(For information about China RoHS compliance, go to ni.com/ environment/rohs_china.)

 $\frac{1}{2}$ 50 Ω input only.

² Signals exceeding the maximum input overload may cause damage to the device.

 $\frac{3}{2}$ Within ±3 °C of self-calibration temperature.

⁴ Used to calculate errors when temperature changes more than ±3 °C since the last self-calibration.

⁵ Measured on one channel with test signal applied to other channel. Same range settings used on both channels.

⁶ Normalized to 50 kHz.

 7_1 M Ω input tested using a 50 Ω source and a 50 Ω feed through terminator connected at the input.

 $^{8}_{-}$ 50% FS input pulse, 23°C ± 10°C.

 9 AC coupling available on 1 M Ω only.

 $\frac{10}{10}$ For ≤ 100 MHz, -1 dBFS input signal corrected to FS. For >100 MHz, -2 dBFS input signal corrected to FS.

¹¹ For 10 MHz, -1 dBFS input signal corrected to FS. For 300 MHz, -2 dBFS input signal corrected to FS. Includes the 2nd through the 5th harmonics. 18 kHz resolution bandwidth (RBW).

 $\frac{12}{12}$ For 10 MHz, -1 dBFS input signal corrected to FS. For 300 MHz, -2 dBFS input signal corrected to FS. Includes the 2nd through the 5th harmonics. 18 kHz resolution bandwidth (RBW).

 $\frac{13}{50} \Omega$ terminator connected to input. 23°C ± 10°C.

 $\frac{14}{50}$ Ω terminator connected to input. 23°C ± 10°C.

 $\frac{15}{15}$ Internal Sample clock is locked to the PXIe_CLK100 Reference clock.

¹⁶ Divide by **n** decimation from 6.25 GS/s used for all rates less than maximum sample rate. For more information about Sample clock and decimation, refer to the **NI High-Speed Digitizers Help**.

 $\frac{17}{2}$ With one channel enabled, stepped in multiples of 12.5 GS/s. With two channels enabled, stepped in multiples of 6.25 GS/s.

 $\frac{18}{18}$ Includes the effects of the converter aperture uncertainty and the clock circuitry jitter. Excludes trigger jitter.

 $\frac{19}{19}$ Phase-locked to Reference clock. The chassis clock or external Reference clock must be accurate to 25 parts per million (ppm), or (1 × 10⁻⁶).

 $\frac{20}{20}$ Divide by **n** decimation available where $1 \le \mathbf{n} \le 65535$. For more information about Sample clock and decimation, refer to the **NI High-Speed Digitizers Help.** The effective sample rate can be $1 \times$ Input Frequency or $2 \times$ Input Frequency when acquiring on two channels, or $1 \times$ Input Frequency, $2 \times$ Input Frequency or $4 \times$ Input Frequency when acquiring on one channel; use the Sample Clock Timebase Multiplier property or the NISCOPE_ATTR_SAMP_CLK_TIMEBASE_MULT attribute to specify. $\frac{21}{2}$ The PLL Reference clock frequency must be accurate to ±25 ppm.

 $\frac{22}{2}$ The PLL Reference clock frequency must be accurate to ±25 ppm.

 $\frac{23}{2}$ Holdoff set to 0.

 $\frac{24}{2}$ Within ±5 °C of self-calibration temperature.

²⁵ When same impedance settings used on both input channels. For more information about functionality when using mixed impedances between the input channels, visit <u>ni.com/kb</u> and enter 5W8CFE8P.

²⁶ Caused by clock and analog path delay differences. No manual adjustment performed.

 $\frac{27}{2}$ Synchronized triggers are synchronized to ±1 Sample clock timebase.

 $\frac{28}{2}$ Onboard memory is shared between all enabled channels.

²⁹ Single-record and multirecord acquisitions.

³⁰ You can exceed these numbers if you fetch records while acquiring data. For more information, refer to the **NI High-Speed Digitizers Help**.