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**for Education**

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# Conventions

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The following conventions are used in this manual:

»

The » symbol leads you through nested menu items and dialog box options to a final action. The sequence **Tools»Clear ERC Markers»Entire design** directs you to pull down the **Tools** menu, select the **Clear ERC Markers** item, and select **Entire design** from the resulting dialog box.



This icon denotes a tip, which alerts you to advisory information.



This icon denotes a note, which alerts you to important information.



This icon denotes a caution, which advises you of precautions to take to avoid injury, data loss, or a system crash.

**bold**

Bold text denotes items that you must select or click in the software, such as menu items and dialog box options. Bold text also denotes parameter names.

*italic*

Italic text denotes variables, emphasis, a cross-reference, or an introduction to a key concept. Italic text also denotes text that is a placeholder for a word or value that you must supply.

monospace

Text in this font denotes text or characters that you should enter from the keyboard, sections of code, programming examples, and syntax examples. This font is also used for the proper names of disk drives, paths, directories, programs, subprograms, subroutines, device names, functions, operations, variables, filenames, and extensions.

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## Appendix A

### Technical Support and Professional Services

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# Educators' Guide

Multisim is the schematic capture and simulation application of National Instruments Circuit Design Suite, a suite of EDA (Electronics Design Automation) tools that assists you in carrying out the major steps in the circuit design flow. Multisim is designed for schematic entry, simulation, and feeding to downstage steps, such as PCB layout.

In addition to the professional features that are detailed in the *Multisim Help*, there are a number of education-specific features that are outlined in this manual.

This chapter describes the tools that Multisim offers to let you exercise greater control over the program's interface and functionality when sharing designs with students, as well as to set certain aspects of a design's behavior for instructional purposes.

Some of the described features may not be available in your edition of Multisim. Refer to the *NI Circuit Design Suite Release Notes* for a description of the features available in your edition.

## Design Creator's Name

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Multisim provides a feature by which the name of the creator of each design is stored with that design. Educators can take advantage of this feature to identify the student who, for example, created the design being submitted as the answer to an assignment (provided that the student uses his/her own copy of the program to create the design). The name appears in the **Circuit Restrictions** dialog box, which you can view as long as no passwords have been set. Refer to the [Setting Circuit Restrictions](#) section for more information.

# Using Restrictions

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Restrictions are useful in a number of ways:

- when you are designing circuits for demonstration purposes and want to limit the functionality available to students.
- when you are sharing designs with students and want:
  - to prevent them from being able to edit the design in any way.
  - to limit the types of modifications they can make to a design.
  - to limit the types of analyses they can perform on it.
  - to limit the information they can see about certain parts of the design (for example, the value of a resistor you want them to calculate).

You can set global-level restrictions, which become default Multisim settings, or circuit-level restrictions, which affect only specific designs.

To ensure that only you can set or modify restrictions, you can use passwords which can protect both global and circuit restrictions. It is important that you set passwords immediately when using restrictions that you want to keep secure against any modification by students. The password for global restrictions is encrypted and stored in the Multisim program file. The password for circuit restrictions (for restricting only a particular design) is encrypted and stored in the design file.

## Setting Global Restrictions

Use global restrictions to set the basic level of functionality of Multisim available to students in all designs with which they will work. You can select a default path where designs are to be saved, hide databases and the **In Use List**, and determine whether students may edit components or place instruments.

You can also hide complicated instruments and analysis options from the menus by using the simplified version. Refer to the [Simplified Version](#) section for more information.



**Note** Global restrictions are overridden by circuit restrictions if the circuit restrictions are saved with the design. Refer to the [Setting Circuit Restrictions](#) section for more information.

## General Global Restrictions

Complete the following steps to set general global restrictions:

1. Choose **Options»Global restrictions**. The **Password** dialog box appears.



**Note** The **Password** dialog also appears if you select **Options»Circuit restrictions**, if you have previously set a password by clicking **Password** from the **Circuit Restrictions** dialog box. Refer to the [Setting Circuit Restrictions](#) section for information about the **Circuit Restrictions** dialog box.

2. Enter the default password “Rodney” (this is case sensitive) and click **OK**. The **Global Restrictions** dialog box appears.



**Note** You should change the default password. Refer to the [Setting Passwords for Restrictions](#) section for more information.

3. Click the **General** tab.
4. Set the default path and location where students find and save files in the **Design Path** field.
5. Set the following as desired in the **Toolbars** box:
  - **Disable Instruments toolbar**—Makes instruments unavailable to be placed in the design.
  - **Disable In-Use List toolbar**—Hides the **In Use List**.
6. Set the following as desired in the **Databases** box:
  - **Disable database editing**—Ensures that students cannot edit components in the database.
  - **Disable Master database component access**—Hides the Multisim Master database and component groups and families from the interface.
  - **Disable Corporate database component access**—Hides the corporate database and component groups and families from the interface.
  - **Disable User database component access**—Hides the “user” database and component groups and families from the interface.
7. Click **OK**. Your options are immediately set for all designs, unless you have set circuit restrictions. Refer to the [Setting Circuit Restrictions](#) section for more information.

## Simplified Version

The simplified version restricts students to only certain instruments and analyses. The simplified version can also be locked, preventing students from turning it off with **Options»Simplified version** and having access to all analyses and instruments.

Complete the following steps to set up the simplified version:

1. Display the **General** tab of the **Global Restrictions** dialog box.
2. Set your options by enabling one of the following options:
  - **Lock simplified**—Disables the **Options»Simplified version** menu option.
  - **Simplified version**—Changes the interface display by hiding the more complex functions and restricting the available instruments and analyses. If the simplified version is restricted, it will be greyed out in the **Options** menu.
  - **Full version**—Displays the full default interface without restrictions.
3. Click **OK**.

Your options are immediately set for all designs, unless you have set circuit restrictions. Refer to the [Setting Circuit Restrictions](#) section for more information.

## Global Analyses Restrictions

Complete the following steps to set global analyses restrictions:

1. From the **Global Restrictions** dialog box, click the **Analysis** tab.
2. Enable the desired analyses by selecting their checkboxes and click **OK**. Only the analyses you check will be enabled in the **Simulate»Analyses** menu or when the student clicks the **Grapher/Analyses List** button in the **Main** toolbar.



**Note** Refer to the **Analysis** section of the *Multisim Help* for more information on analyses.

These options are immediately set for all designs, unless you have set circuit restrictions. Refer to the [Setting Circuit Restrictions](#) section for more information.

## Setting Circuit Restrictions

Use circuit restrictions to set restrictions on individual designs. Circuit restrictions override global restrictions. They are saved with your design and invoked each time the design is loaded. In addition to hiding databases and setting available analyses, you can set a schematic to be read-only (not editable by students), you can hide components' values, faults and uses in analyses, and you can lock subcircuits to make them unavailable for opening by students.



**Note** Remember that circuit restrictions only apply to the current design; when you create a new design, only the global restrictions will apply. Refer to the [Setting Global Restrictions](#) section for more information. If you want circuit restrictions to apply to a new design, you will need to reset those restrictions each time you create a new design.

Complete the following steps to set general circuit restrictions:

1. Choose **Options»Circuit restrictions**. If you have created a password, you will be prompted for it. Refer to the [Setting Passwords for Restrictions](#) section for more information. Enter your password in the **Password** dialog box, and click **OK**. The **Circuit Restrictions** dialog box appears.
2. Click the **General** tab and set the desired options by enabling the appropriate checkboxes. Select from the following options:
  - **Schematic read-only**—Prevents students from saving the design, and hides components bins. Students will only be able to draw wires between instruments and an open pin on an existing connector. Also, they can only remove wires that are between an instrument and a connector.
  - **Description read-only**—Prevents students from changing the contents of the **Description Box**.
  - **Hide component values**—Marks the **Values** tab of components' properties dialog boxes with an "X" and hides values. You may wish to provide false values using labels.
  - **Hide component faults**—Marks the **Faults** tab of components' properties dialog boxes with an "X", and hides faults.
  - **Lock subcircuits**—Prevents students from opening subcircuits and hierarchical blocks and seeing their contents. Students must measure the input and output of a hidden subsheet to determine its contents.
  - **Disable Instruments toolbar**—Makes instruments unavailable to be placed on the design.

- **Disable In-Use List toolbar**—Disables the In-Use List for the current design.
- **Disable Master database component access**—Hides the Multisim Master database and components groups and families from the current design.
- **Disable Corporate database component access**—Hides the corporate database and components groups and families from the interface.
- **Disable User database component access**—Hides the user database and components groups and families from the current design.



**Note** The **Design creator name** is taken from the operating system.

3. Click **OK**. The options you select are immediately invoked in the design.
4. To have the restrictions apply each time the design is opened, choose **File»Save** to save the restrictions in the design file.

Complete the following steps to set design analyses restrictions:

1. From the **Circuit Restrictions** dialog box, click the **Analysis** tab.
2. Enable the desired analyses by selecting their checkboxes and click **OK**. Only the analyses you check will be enabled in the **Simulate»Analyses** menu or when the student clicks the **Grapher/Analyses List** button in the **Main** toolbar.



**Note** Refer to the **Analysis** section in the *Multisim Help* for more information on analyses.

3. To have these analyses apply each time the design is opened, choose **File»Save** to save the restrictions.

Complete the following steps to set design breadboard restrictions:

1. From the **Circuit Restrictions** dialog box, click the **Breadboard** tab.
2. Set the following as desired:
  - **Highlight target holes**—Disable if you do not wish to see where the targets for jumper wires are when placing them on the breadboard.
  - **Completion feedback**—Disable if you do not wish components and wires on the schematic to change color as they are placed and wired on the breadboard.
3. Click **OK**.



**Note** For details on breadboarding, refer to Chapter 2, *Breadboarding*.

## Setting Passwords for Restrictions

When using restrictions, you should create a password immediately to ensure that your settings are secure.

Complete the following steps to create/change a password:

1. For global restrictions, choose **Options»Global restrictions**.  
*Or*  
For circuit restrictions, choose **Options»Circuit restrictions**.
2. Enter a password if prompted to do so.



**Note** The default password for global restrictions is “Rodney” (this is case sensitive). Circuit restrictions *do not* have a default password.

3. From the restrictions dialog box that appears, click **Password**. The **Change Password** dialog box appears.
4. If you are choosing a password for the first time, leave the **Old password** field blank.
5. If you are changing a password, enter the old password in the **Old password** field.
6. Enter your (new) password in the **New password** field.
7. Confirm your new password by entering it again in the **Confirm password** field.
8. Click **OK**.



**Note** If you want to change global or circuit restrictions, you will need to enter the respective password. Be sure to keep your passwords for both the **Global restrictions** and **Circuit restrictions** dialogs written down and in a safe place, as you will not be able to retrieve them from the program or design files, where they are stored in encrypted form.



**Note** A design password is not automatically transferred to a new design when you go to set circuit restrictions for it, so you will need to recreate the password every time you create circuit restrictions that you want to keep secure.

## Link to Education Resources

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**Note** This function is hidden when the simplified version option is selected. Refer to the *Simplified Version* section for more information.



To go to the National Instruments Academic website, click the **Education web site** button or select **Tools»Education web site**.

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# Breadboarding

This chapter describes Multisim's breadboarding feature.

Some of the described features may not be available in your edition of Multisim. Refer to the *NI Circuit Design Suite Release Notes* for a description of the features available in your edition.

## Breadboarding Overview

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The **Breadboarding** feature provides a technical aid for educators who wish to illustrate breadboarding as a means of prototyping designs. It also gives students exposure to the breadboarding process, and shows in 3D what the resulting breadboard will look like when completed.

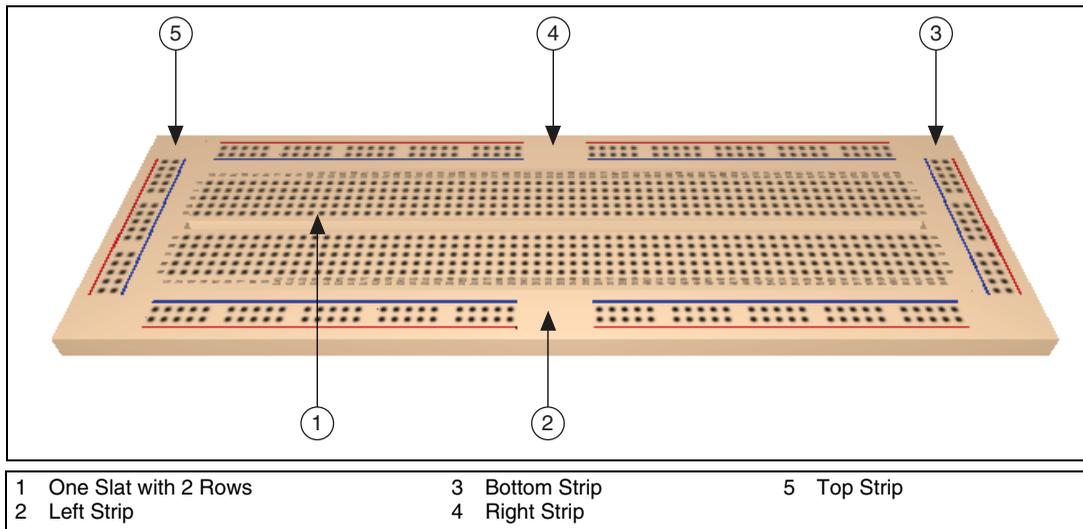
# Breadboard Settings

The default breadboard is shown in the screen capture below. If you wish to change the default settings, use the following procedure.

Complete the following steps to change the breadboard's settings:



1. Select **Tools»View breadboard** from the main Multisim menu. The **Breadboard View** displays. The default breadboard appears as shown below.



As shown in the figure above, the default breadboard contains: one slat with two rows (1); one left strip (2); one bottom strip (3); one right strip (4); one top strip (5).



2. Select **Options»Breadboard settings** to display the **Breadboard Settings** dialog box.
3. Enter the desired parameters for the breadboard:
  - **Number of slats**—The number of slats to appear on the breadboard.
  - **Rows in a slat**—The number of rows in each slat.
  - **Top strip** checkbox—Select to include a top strip on the breadboard.
  - **Bottom strip** checkbox—Select to include a bottom strip on the breadboard.

- **Left strip** checkbox—Select to include a left strip on the breadboard.
- **Right strip** checkbox—Select to include a right strip on the breadboard.



**Note** Refer to the figure in step 1 for an illustration of the above parts of the breadboard.

4. Click **OK**. The view of the breadboard changes to reflect your settings.

## 3D Options

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The 3D viewing options for the **Breadboard View** are set in the **3D Options** tab of the **Global Preferences** dialog box.

Complete the following steps to change the 3D options:

1. Select **Options»Global preferences** and click on the **3D Options** tab.
2. Optionally, click on **Background color** to display a standard **Color** dialog box where you can adjust the background color as desired.
3. In the **Info box** area:
  - **Info box**—Disable this checkbox if you do not wish to see the box at the top of the **Breadboard View** that shows components information.
  - **Left**—Select to place the components information box at the top-left of the **Breadboard View**.
  - **Center**—Select to place the components information box at the top-center of the **Breadboard View**.
  - **Right**—Select to place the components information box at the top-right of the **Breadboard View**.
4. Disable the **Show target holes** checkbox if you do not wish to see where the targets for jumper wires are when placing them. Refer to the [Placing a Jumper](#) section for more information.
5. Disable the **Show completion feedback** checkbox if you do not wish components and wires on the schematic to change color as they are placed and wired on the breadboard.
6. In the **3D performance** box:
  - Move the slider as desired to improve graphic performance. **More Details** cause a slower screen refresh rate.
  - Enable the **User Defined** checkbox and disable the 3D features that you do not wish to see (**Show Breadboard Numbers**, **Show Lights**, **Show Reflections**, **Show Transparent Indicators**).

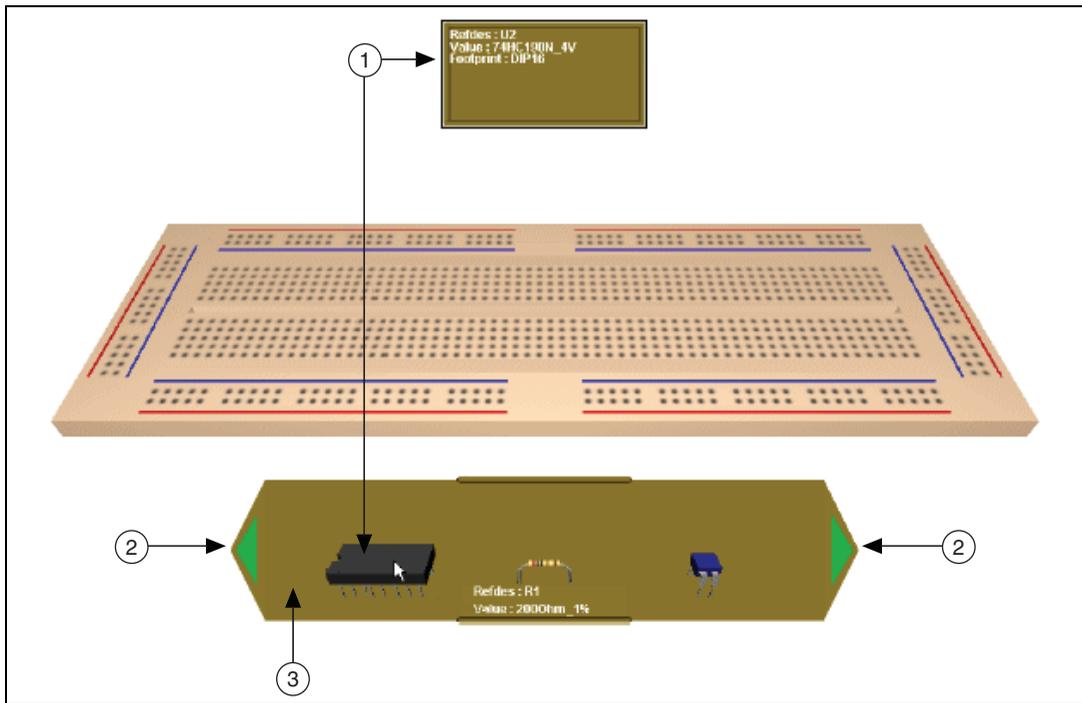


**Tip** Disabling **Show Breadboard Numbers** will result in a much quicker refresh rate.

## Placing Components on the Breadboard

Complete the following steps to place components on a breadboard:

1. Create a schematic diagram of the desired design in the usual manner.
2. Select **Tools»Show breadboard** from the main Multisim menu. The **Breadboard View** displays similar to the following example.

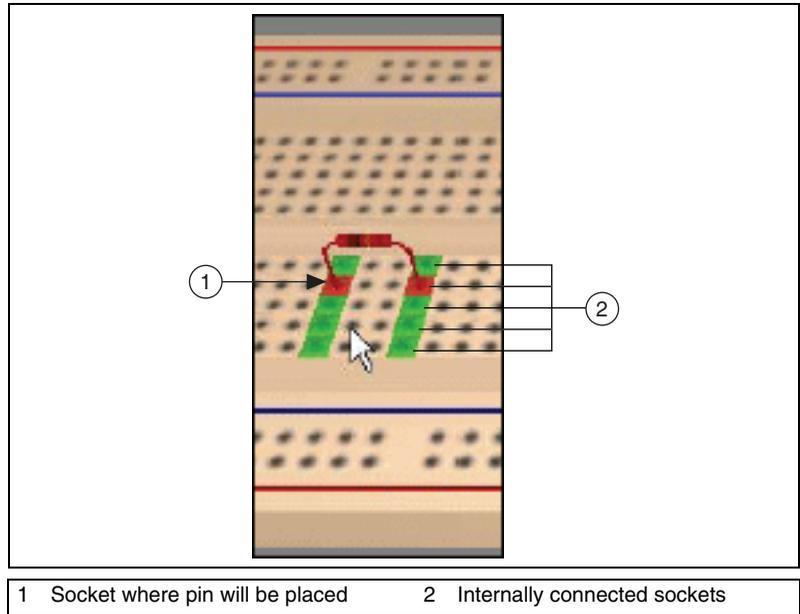


- 1 Hover cursor over component to see description
- 2 Click arrows to view other components

- 3 Place Component Bar contains components waiting to be placed on breadboard.

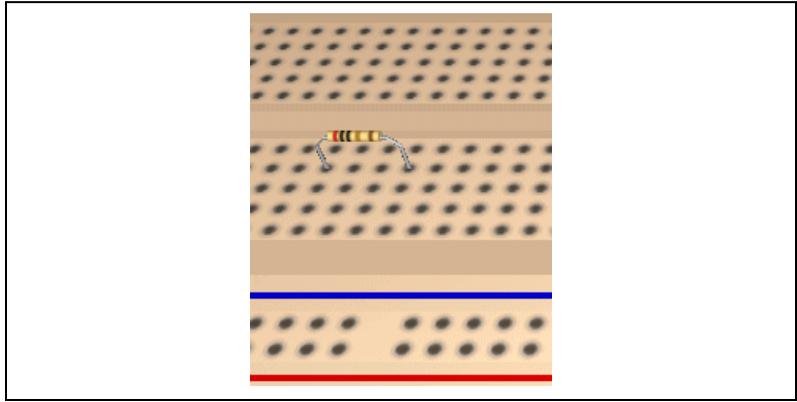
- Click on a component in the **Place Component Bar** and drag it to the desired location on the breadboard. As the component passes over the breadboard, sockets change color as shown below.

Red sockets (1) indicate where the component's pins will be placed when the mouse button is released. All of the sockets labelled (2) are connected. Green indicates sockets that are internally connected to the red socket in the same row on the breadboard.

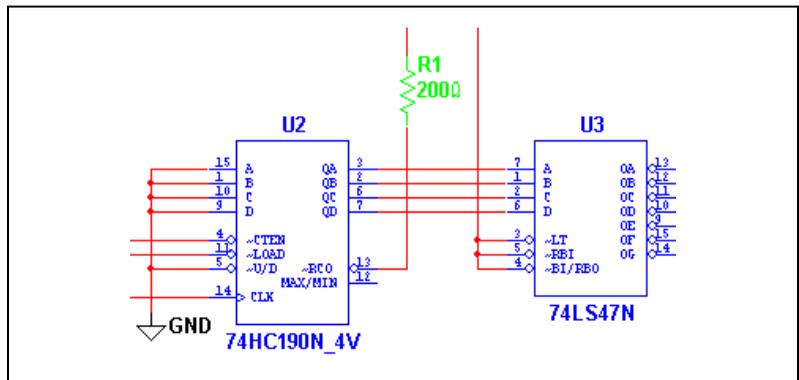


**Tip** Select <Ctrl-R> to rotate a selected component 90 degrees clockwise or <Ctrl-Shift-R> to rotate it 90 degrees counter-clockwise.

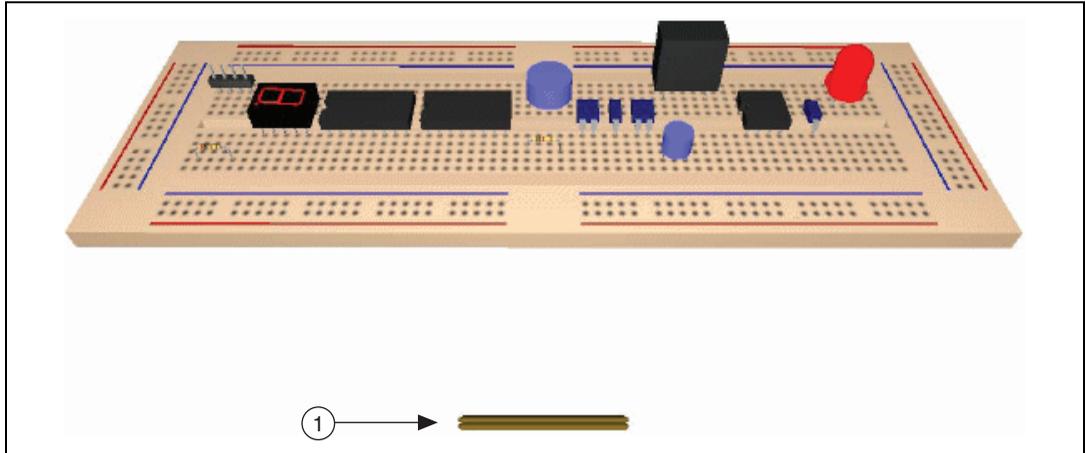
- Release the mouse button to place the component. Notice that the colored (red and green) sockets on the breadboard no longer appear.



- Return to the schematic view and note that the color of the placed component has changed as shown in the example below (R1).



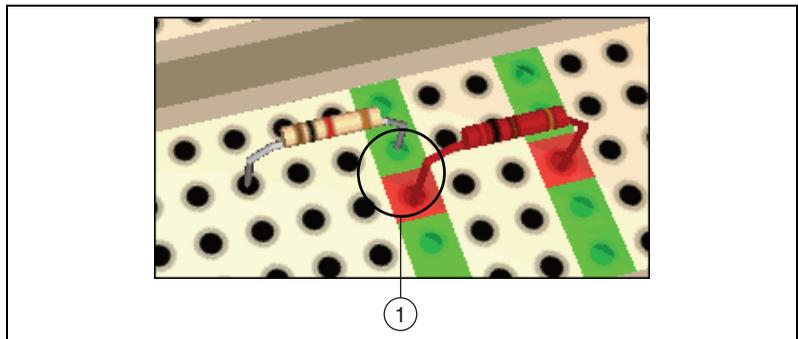
6. Continue placing the design's components on the breadboard. When all the components have been placed, the **Place Component Bar** collapses as shown below (1).



1 Collapsed Place Component Bar



**Tip** Where pins of components are connected on the schematic, you can place them in connected sockets on the breadboard as shown below. This technique can reduce the number of jumper wires required. Refer to the *Placing a Jumper* section for more information about jumpers.

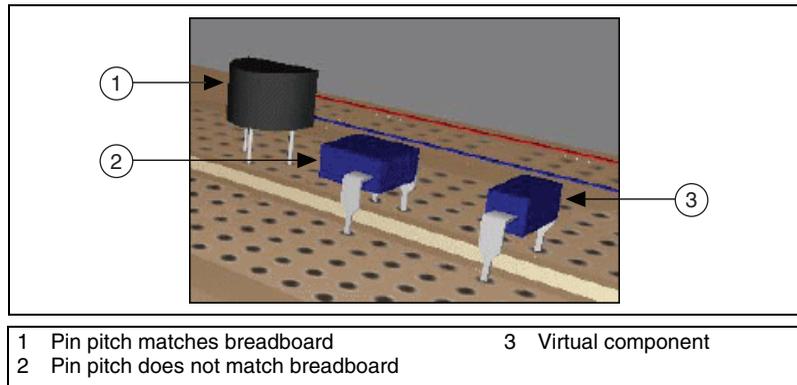


1 Connected pins

## Appearance of 3D Components

The appearance of the 3D component is dependant on the footprint that is selected from the **Select a Component** browser during schematic capture in the **Footprint manufacturer/type** list.

Some virtual components have a default 3D view that appears as a blue 3D rectangle or cube. “Real” components that have pin pitch (spacing) that does not fit the pin pitch on the breadboard will also appear as 3D rectangles or cubes, with properly spaced pins.



**Notes** Certain virtual components, including 3D components, also appear as 3D rectangles or cubes.

To view footprint information, hover the cursor over the desired component. Refer to the [Viewing Component Information](#) section for more information.

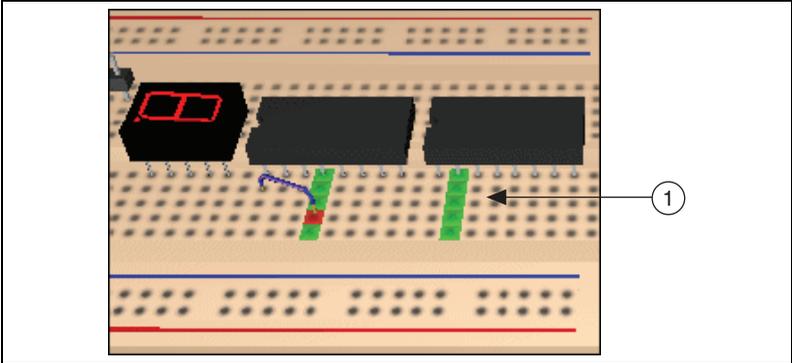
## Wiring Placed Components

By placing component pins that are connected on the schematic into sockets that are internally connected, much of the “wiring” can be done at the same time components are placed. However, in most designs, it will also be necessary to place jumpers to complete the wiring of the placed components.

# Placing a Jumper

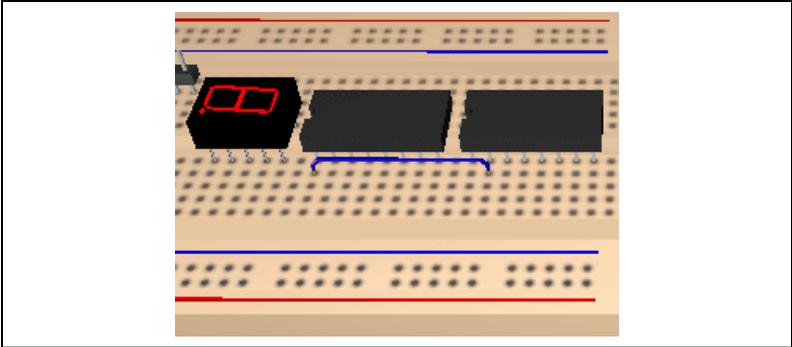
Complete the following steps to place a jumper wire:

1. Click on a socket connected to the pin where you wish to start the jumper and begin moving the cursor. Legitimate “target” pins display as shown below (1).

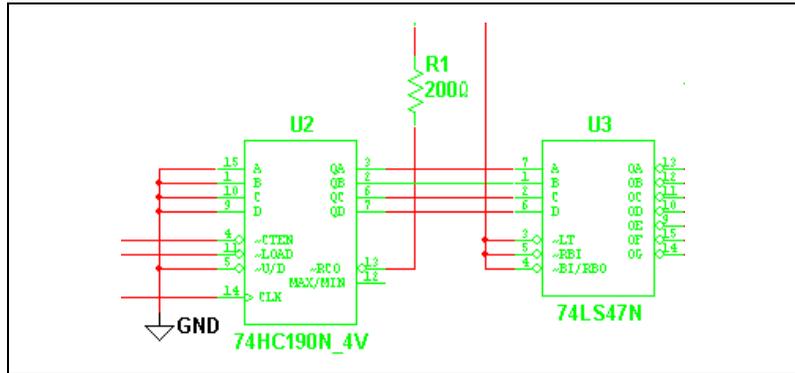


1 Target pins

2. Click to place the jumper in the desired socket.



- Return to the schematic view and note that the color of the wire connecting the two pins has changed to green to indicate a connection has been made, as shown in the figure below, between pin 2 of U2, and pin 1 of U3.



**Note** If a net contains more than two connections, all must be connected before any of the wires in the net change color.

- Continue placing jumpers until all schematic connections have been made.



**Tip** Run a **Design Rules Check** and **Connectivity Check** to see if there are any errors in your breadboard. Refer to the *DRC and Connectivity Check* section for more information.

## Changing Jumper Wire Color

Complete the following steps to change jumper wire color:



- Select **Edit»Breadboard wire color**.
- Select the desired color from the **Colors** dialog box that appears.

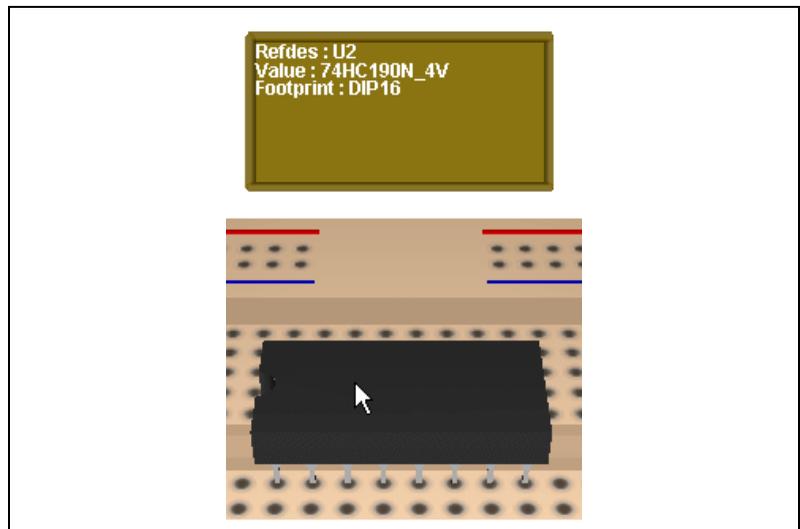


**Note** The color of previously placed wires is not affected. The new color will be applied to any subsequently placed wires.

## Viewing Component Information

Complete the following steps to view information about a specific component:

1. Hover the cursor over the component. The information box is populated as shown below.

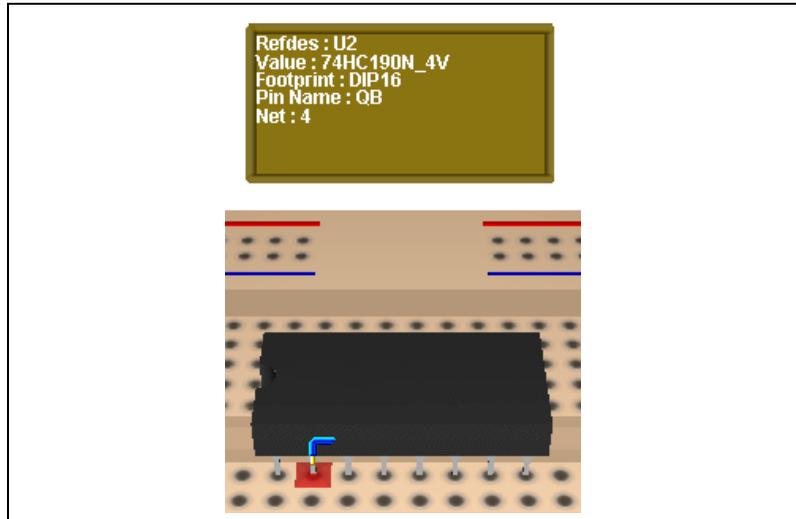


Complete the following steps to see pin information:

1. Hover the cursor over the “metal” part of the desired pin. The information box now includes the pin name and the schematic net to which the pin should be connected.



**Note** This only works for placed components.



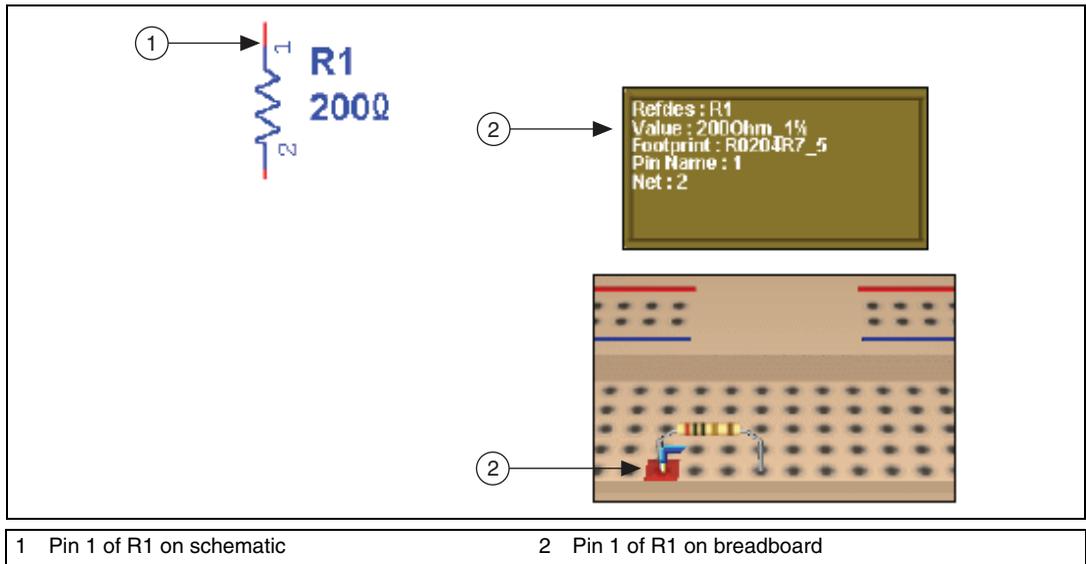
## Two-terminal Components

Two-terminal non-directional components like resistors have symbol pin names (1 and 2) that automatically swap if they are connected the “wrong way” according to the pin name that is on the schematic.

Complete the following steps to view the pin names for all devices on the schematic:

1. Select **Options»Sheet properties** and click the **Sheet** tab of the **Sheet Properties** dialog box.
2. Click the **Symbol pin names** checkbox until the checkbox contains a checkmark instead of a solid color.
3. Click **OK** to close the dialog.

In the example below, (1) shows pin 1 of R1 on the schematic, and pin 1 of R1 on the breadboard (2). If Pin 1 is connected to a pin that should be connected to Pin 2, the pin names automatically swap. (Pin 1 becomes Pin 2 and vice versa).



## Manipulating the Breadboard View

You can manipulate the view of the breadboard in a number of ways.



To make the breadboard appear larger, select **View»Zoom in**.



To make the breadboard appear smaller, select **View»Zoom out**.



**Tip** Use your mouse's center wheel to zoom in or out. (This must be set up in the **General** tab of the **Global Preferences** dialog box. For details, refer to the *Multisim Help*.)



To view the entire breadboard, select **View»Zoom full**.



To rotate the breadboard 180 degrees, select **View»Rotate view 180°**.

*Or*

Press <Shift-R> on your keyboard.



**Tip** Rotate the breadboard in any direction by dragging the mouse from a blank area of the **Breadboard View**.

To pan the breadboard, press <Shift> and use any of the arrow keys.

*Or*

Press <Ctrl-Shift> and drag the mouse.

*Or*

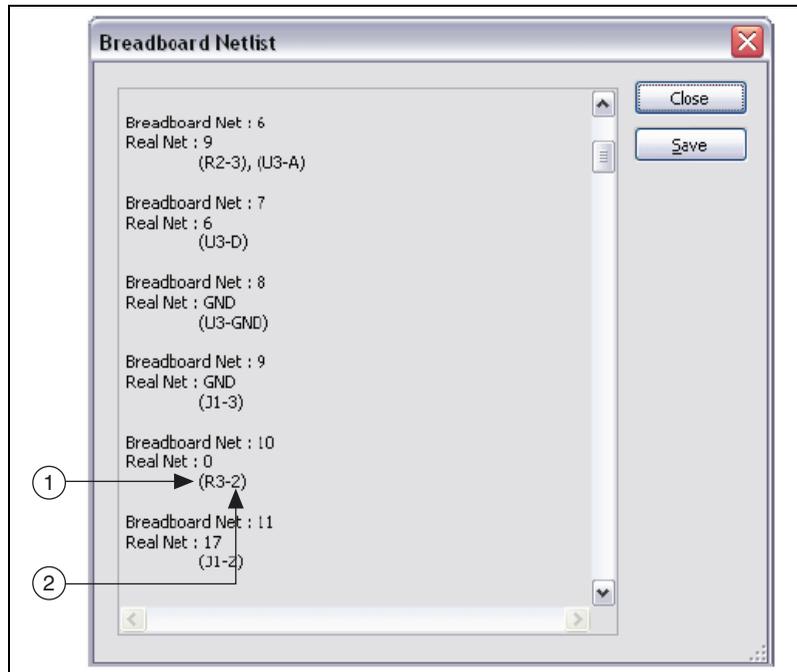
Hold down your mouse-wheel and drag the mouse.

## Breadboard Netlist dialog box

Complete the following steps to display a netlist for the placed components and jumpers:



1. Select **Tools»Show breadboard netlist**. The **Breadboard Netlist** dialog box appears.



1 RefDes

2 Pin name

2. Optionally, click **Save** to save the breadboard netlist as a .txt or .csv file.



**Note** These nets are breadboard connections, and are not necessarily numbered in correspondence to the schematic nets.

## DRC and Connectivity Check

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You can run a **Design Rules and Connectivity Check** to see if there are any errors on your breadboard.

To run a DRC and Connectivity Check, select **Tools»DRC and connectivity check**. The results appear in the **Results** tab of the **Spreadsheet View**.

**Design Rule Errors**—Indicate connections that are on the breadboard that are not on the schematic.

**Connectivity Errors**—Indicate component pins that are connected to schematic nets whose connections are not all completed.

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# Virtual NI ELVIS and NI myDAQ

This chapter describes Multisim's virtual NI ELVIS feature.

Some of the described features may not be available in your edition of Multisim. Refer to the *NI Circuit Design Suite Release Notes* for a description of the features available in your edition.

## Overview

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Virtual NI ELVIS emulates much of the behavior of its real-world counter-part, the NI Educational Laboratory Virtual Instrumentation Suite (NI ELVIS). Planning, prototyping and testing of instructors' projects can be carried out on students' PCs before moving on to the real NI ELVIS I or NI ELVIS II workstation in the lab.

Multisim emulates the original NI ELVIS I and NI ELVIS II. NI ELVIS II contains more instruments than the original. However, you should use whichever version you have in your lab. For details, refer to *The Virtual NI ELVIS I Schematic* and *The Virtual NI ELVIS II Schematic* sections.

## The Virtual NI ELVIS I Schematic

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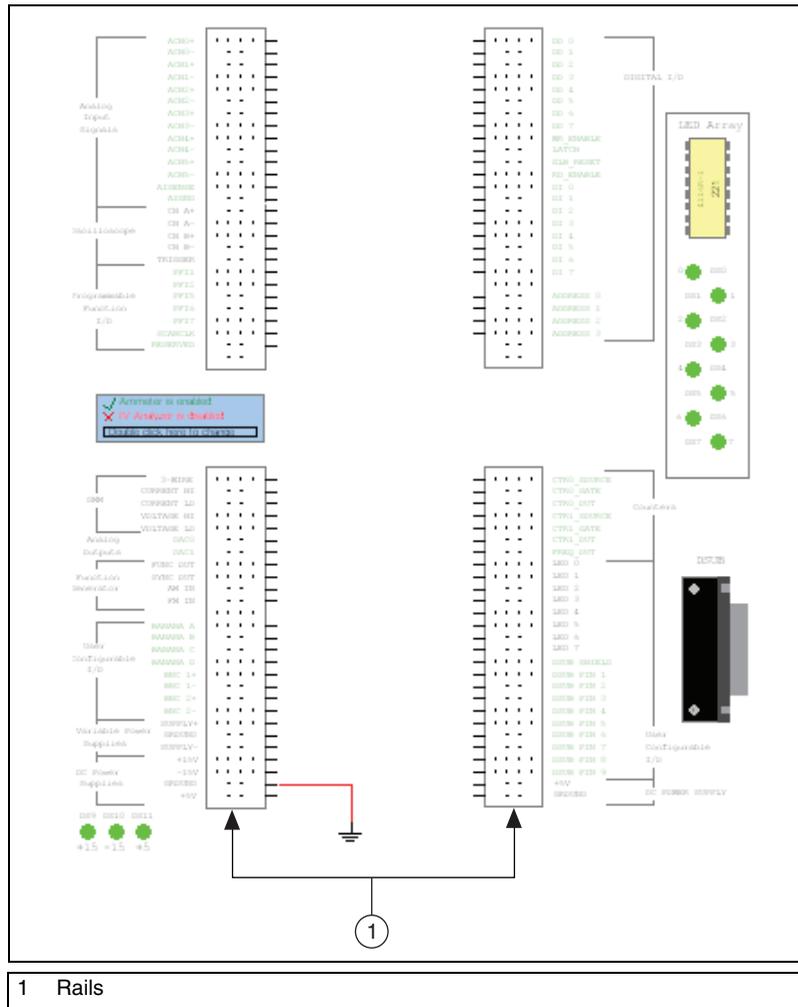
A virtual NI ELVIS I schematic contains a number of items that correspond to elements of the real-world NI ELVIS workstation. The connection and control of these elements is described in this section.



**Note** This section describes the behavior of Multisim's original NI ELVIS I schematic. Refer to *The Virtual NI ELVIS II Schematic* section for information on Multisim's NI ELVIS II functionality.

Complete the following steps to create a new virtual NI ELVIS I schematic:

1. Select **File>New>NI ELVIS I design**. The schematic appears as shown below:



**Note** The ground connector that appears at the bottom left of the diagram is the reference point for measurements taken during simulation, and must not be removed.

2. Place and wire components in the virtual NI ELVIS I schematic in the same manner as other Multisim schematics. For details, refer to the *Multisim Help*.

The prototyping board rails (see 1 in the figure above) found to the left and right of the main workspace correspond to rails on the prototyping board of the real-world version of NI ELVIS, and are labelled in the same manner.

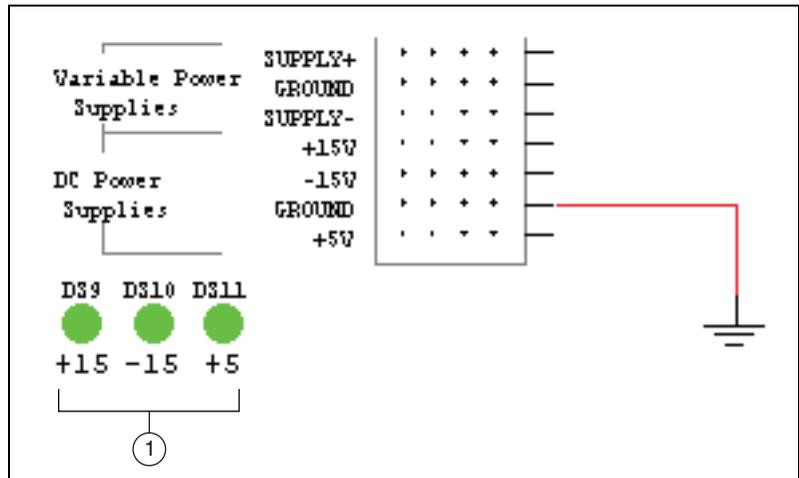
Rows on the rails that are shown with green labels are not enabled for simulation in Multisim. However, they can be used for schematic capture and viewing of the completed virtual NI ELVIS I schematic in the 3D view.

Unlike other Multisim components, these rails cannot be moved to other places on the workspace.



To connect to an LED, place a wire from one of the LED rows (**LED 0** through **LED 7**) to the desired point in your schematic.

There are also three power supply LEDs in the lower-left section of any virtual NI ELVIS I schematic, as shown in the figure below (1).



1 Power Supply LEDs

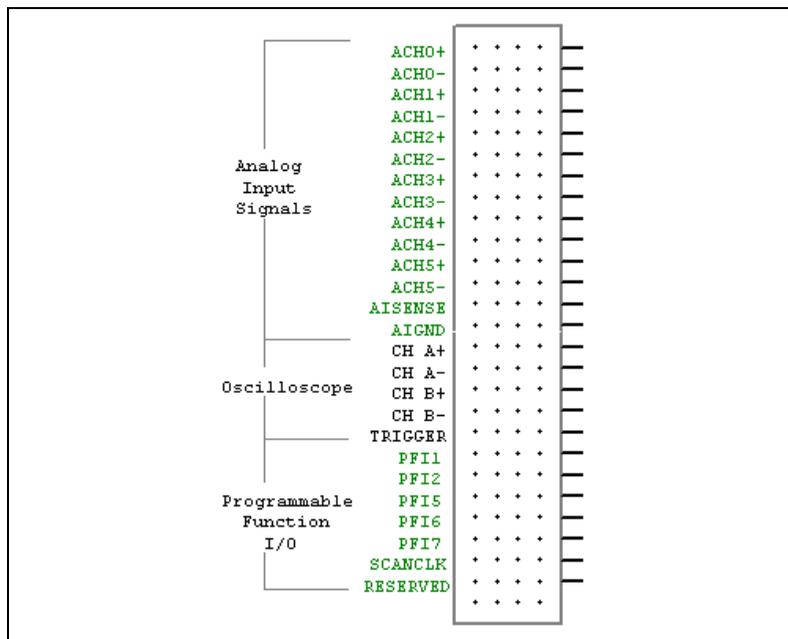
During simulation, these LEDs light whether or not connections have been made to their corresponding pins in the prototyping rail. They indicate that power is available to the respective connections.

## NI ELVIS I Instruments

One instance of each of the following NI ELVIS instruments is found in the virtual NI ELVIS I schematic:

- *Oscilloscope*—This instrument is a two-channel oscilloscope.
- *IV Analyzer and Multimeter*—This instrument can be enabled as either an IV analyzer, or a digital multimeter.
- *Function Generator*—This instrument generates sine, square or triangle waves.
- *Power Supplies*—This device is a variable power supply.

## Oscilloscope



The connections to the virtual NI ELVIS oscilloscope are found in the upper-left prototyping rail.

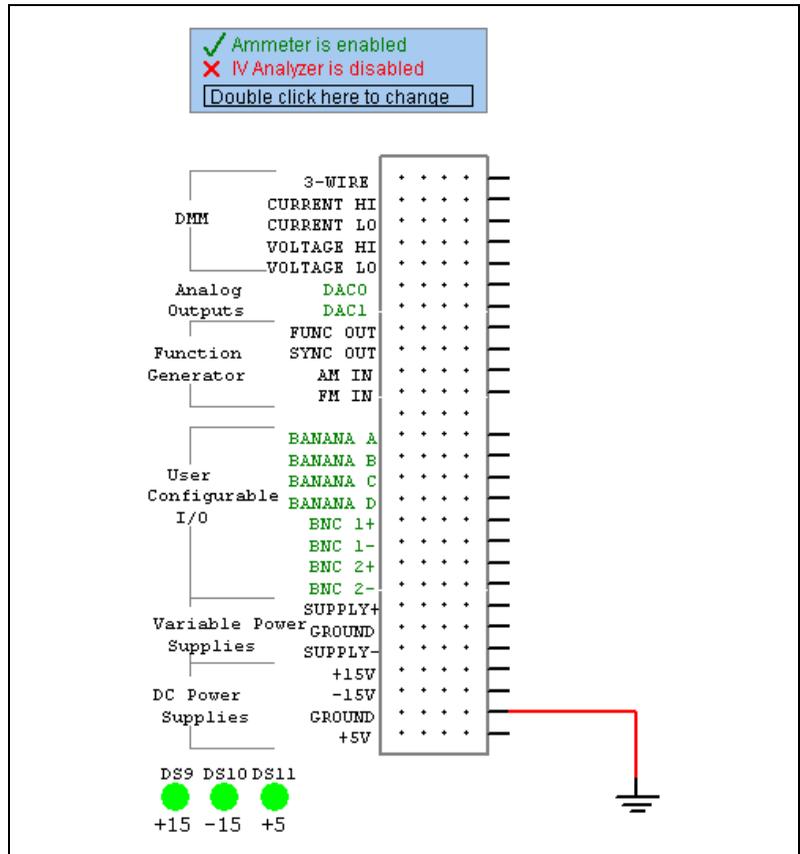
To connect the oscilloscope, place wires from the points in your schematic that you wish to measure to any of the pins on the **CH A+**, **CH A-**, **CH B+**, **CH B-** or **TRIGGER** rows beside **Oscilloscope**. These rows correspond to the terminals of the oscilloscope.

- **CH A+** —Positive input of channel A.
- **CH A-** —Negative input of channel A.
- **CH B+** —Positive input of channel B.
- **CH B-** —Negative input of channel B.
- **TRIGGER**—Trigger input signal.

Complete the following steps to access the oscilloscope's controls:

1. Double-click on the the **Oscilloscope** label in the upper-left prototyping rail. The instrument face for the Multisim virtual oscilloscope displays.
2. Refer to the *Multisim Help* for details on the use of this instrument.

## IV Analyzer and Multimeter



When a new virtual NI ELVIS I schematic is opened, the **IV Analyzer** is disabled, and the **Ammeter** is enabled as shown in the above figure.

To disable the **Ammeter** and enable the **IV Analyzer**, double-click where indicated on the virtual NI ELVIS I schematic.

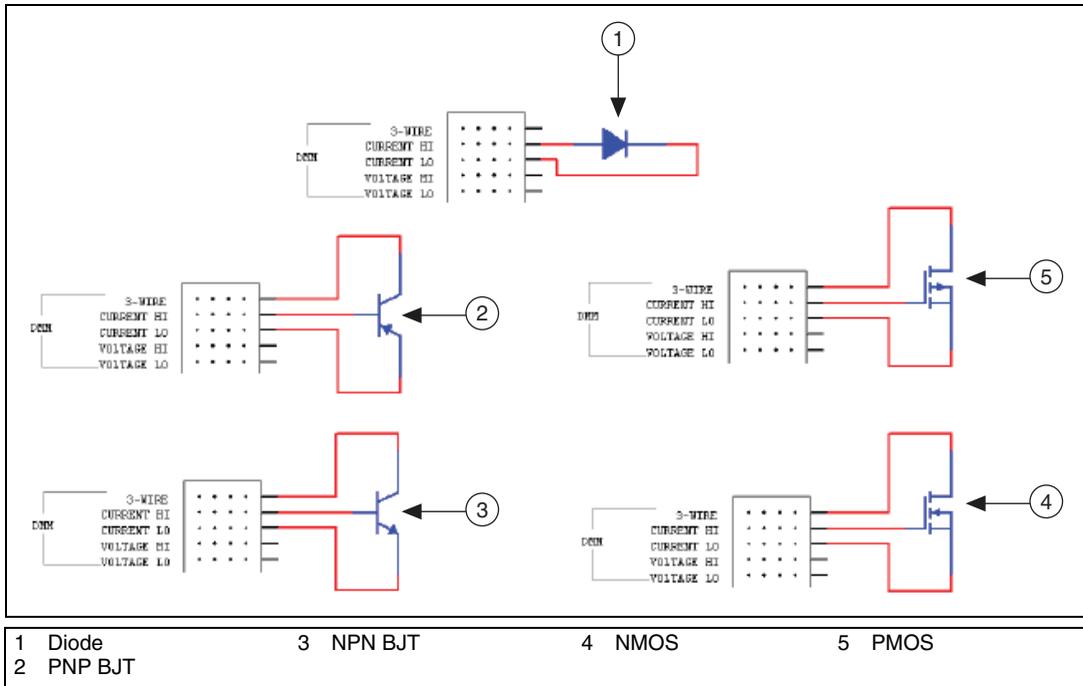
To disable the **IV Analyzer** and enable the **Ammeter**, double-click again.



**Note** When the **IV Analyzer** is enabled, there is a slight delay when simulation is started while a **DC Sweep** is performed. If the **Ammeter** is enabled, there is no delay.

Complete the following to connect the **IV Analyzer**:

- Place wires from the component you wish to measure to the pins on the **3-WIRE**, **CURRENT HI** and **CURRENT LO** rows. These rows correspond to the inputs of the **IV Analyzer**. Refer to the figure below for connections for a diode (1); PNP BJT (2); NPN BJT (3); NMOS FET (4); PMOS FET (5).
- Disconnect any other wires from the DMM terminals.



Complete the following to connect the **Ammeter/Ohmmeter**:

- Place wires from the points in the design you wish to measure to the pins on the **CURRENT HI** and **CURRENT LO** rows. **CURRENT HI** corresponds to the + terminal of the meter and **CURRENT LO** corresponds to the – terminal.
- Disconnect any other wires from the DMM terminals.

Complete the following steps to access the controls for the enabled instrument:

1. Double-click just *above* the **DMM** label. If you have enabled the **IV Analyzer** as described earlier, that instrument's face appears. If you have enabled the **Ammeter**, an instrument containing the **Ammeter** and **Ohmmeter** functions of a multimeter appears.
2. Refer to the *Multisim Help* for details on the use of these instruments.

Complete the following to connect the **Voltmeter**:

1. Place wires from the points in the design you wish to measure to the pins on the **VOLTAGE HI** and **VOLTAGE LO** rows.  
**VOLTAGE HI** corresponds to the + terminal of the meter and **VOLTAGE LO** corresponds to the – terminal.
2. Disconnect any other wires from the DMM terminals.

Complete the following steps to access the controls for the **Voltmeter**:

1. Double-click just *below* the **DMM** label. An instrument containing the **Voltmeter** function of a multimeter appears.
2. Refer to the *Multisim Help* for details on the use of this instrument.

## Function Generator

Complete the following to connect the **Function Generator**:

1. Place wires from the pins on the **FUNC OUT**, **SYNC OUT**, **AM IN** and **FM IN** rows to the desired points in your schematic.
  - **FUNC OUT**—Output signal.
  - **SYNC OUT**—Outputs a TTL-compatible clock signal of the same frequency as the output waveform.
  - **AM IN**—A signal input here controls the amplitude of the signal at **FUNC OUT**.
  - **FM IN**—A signal input here controls the frequency of the signal at **FUNC OUT** and **SYNC OUT**.

Complete the following steps to access the controls for the **Function Generator**:

1. Double-click on the **Function Generator** label. The properties dialog for the **NI ELVIS Function Generator** appears.
2. Click on the **Value** tab and enter the desired output parameters.
3. Click **OK** to close the **Function Generator**'s properties dialog box.



**Note** This instrument can be used for transient analysis only. It does not function for frequency-domain analyses. To run a frequency-domain analysis, use an AC source from the Multisim **Master database**. For more information on analyses, refer to the *Multisim Help*.

## Power Supplies

The lower-left prototyping rail contains the following fixed DC power supplies:

- **+15 V**
- **-15 V**
- **+5 V** (also found in the lower-right prototyping rail).

Variable Power Supplies are also available:

- **SUPPLY+** (+12 V max)
- **SUPPLY-** (-12 V max).

To connect to any of the power supplies, place wires from the pin on the corresponding row to the desired point in the design.

Complete the following steps to access the controls for the variable power supply:

1. Double-click on **Variable Power Supplies**. The properties dialog box for the NI ELVIS power supply appears.
2. Click on the **Value** tab and enter the desired parameters.
3. Click **OK** to close the properties dialog box.

## The Virtual NI ELVIS II Schematic

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A virtual NI ELVIS II schematic contains a number of items that correspond to elements of the real-world NI ELVIS II workstation. The connection and control of these elements is described in this section.



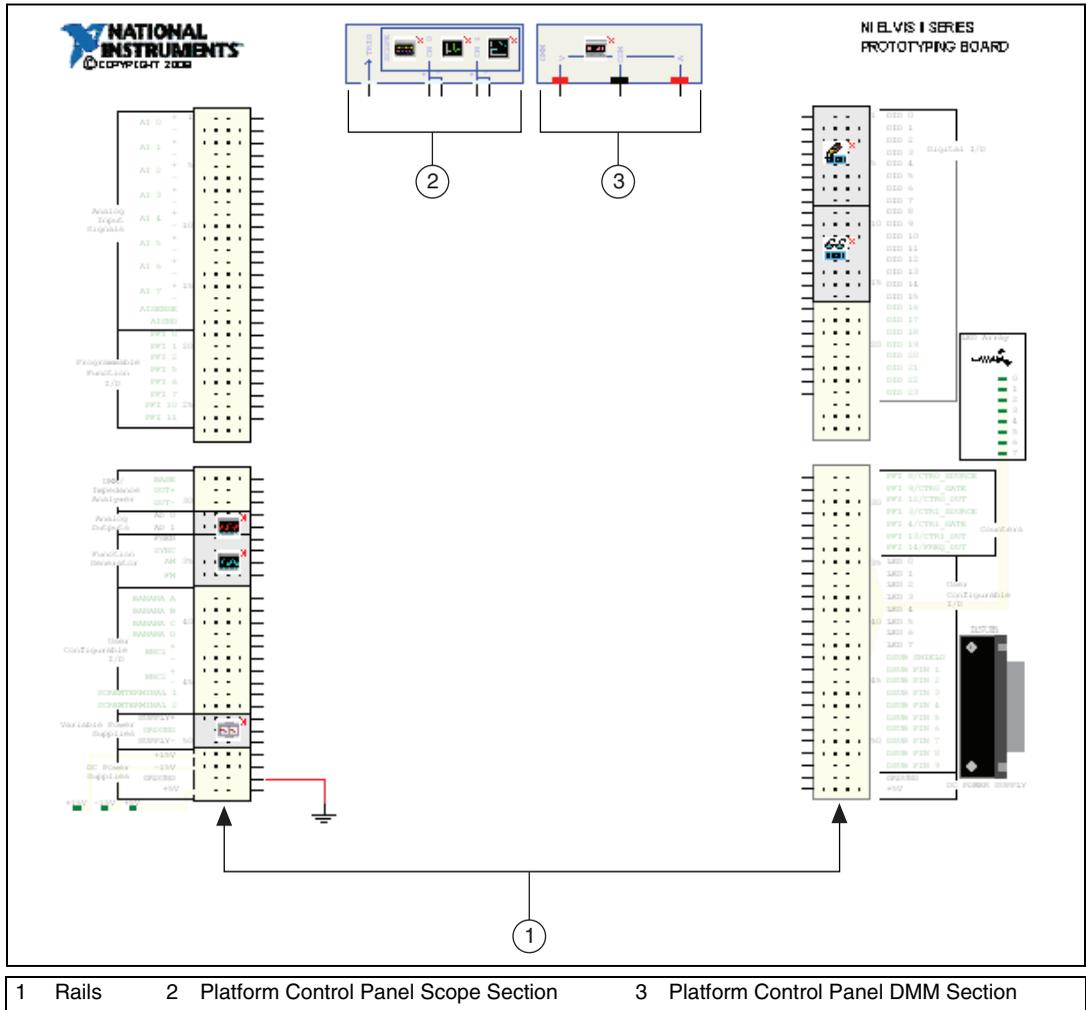
**Note** This section describes the behavior of Multisim's NI ELVIS II schematic. Refer to *The Virtual NI ELVIS I Schematic* section for information on Multisim's original NI ELVIS I functionality.



**Note** During NI Circuit Design Suite (NI CDS) installation, the installer prompts you for the NI ELVISmx installation CD, which is included in your NI CDS package. NI ELVISmx enables the NI ELVIS II functionality in Multisim. If you do not install this software, the NI ELVIS II functionality will be disabled in Multisim.

Complete the following steps to create a new virtual NI ELVIS II schematic:

1. Select **File»New»NI ELVIS II design**. When first opened, a virtual NI ELVIS II schematic appears as shown below.



**Note** The ground connector that appears at the bottom left of the diagram is the reference point for measurements taken during simulation, and must not be removed.

2. Place and wire components in the virtual NI ELVIS II schematic in the same manner as other Multisim schematics. For details, refer to the *Multisim Help*.

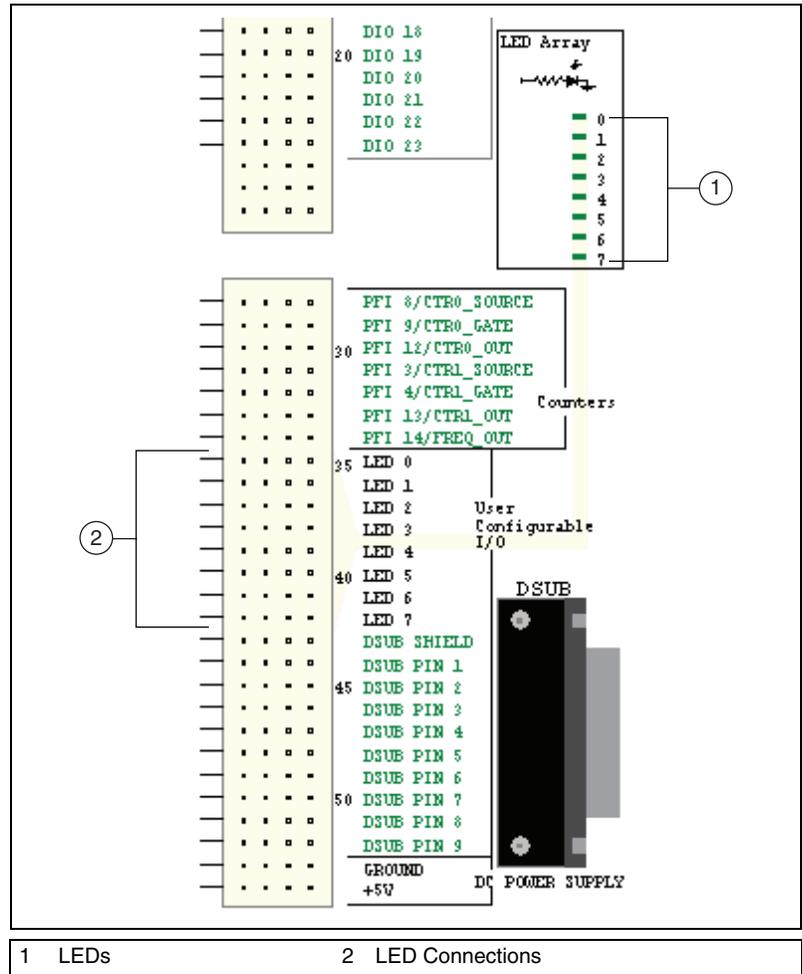
The prototyping board rails (see 1 in the figure above) found to the left and right of the main workspace correspond to rails on the prototyping board of the real-world version of NI ELVIS II, and are labelled in the same manner. At the top in the control panel sections (see 2 and 3 in the figure above), there are icons for connecting to the oscilloscope, dynamic signal analyzer, bode analyzer and digital multimeter. These instruments are isolated and are not available in the rails of the prototyping board. They are found on the main real-world NI ELVIS II unit.

Rows on the rails that are shown with green labels are not enabled for simulation in Multisim. However, they can be used for schematic capture and viewing of the completed virtual NI ELVIS II schematic in the 3D view.

Unlike other Multisim components, these rails and instrument icons cannot be moved to other places on the workspace.

## LEDs

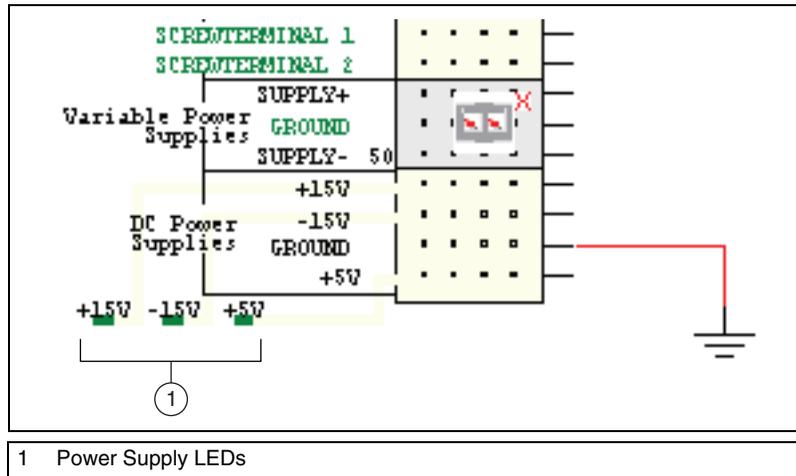
Connections to the eight LEDs on the right side of the NI ELVIS II schematic are found in the NI ELVIS II Right-Bottom Rail Section, as shown in the figure below (2). During simulation, any of these LEDs (1) that are correctly driven will light.



Complete the following to connect to an LED:

- Place a wire from one of the LED rows (**LED 0** through **LED 7**) to the desired point in your schematic.

There are also three power supply LEDs in the lower-left section of any virtual NI ELVIS II schematic, as shown in the figure below (1):

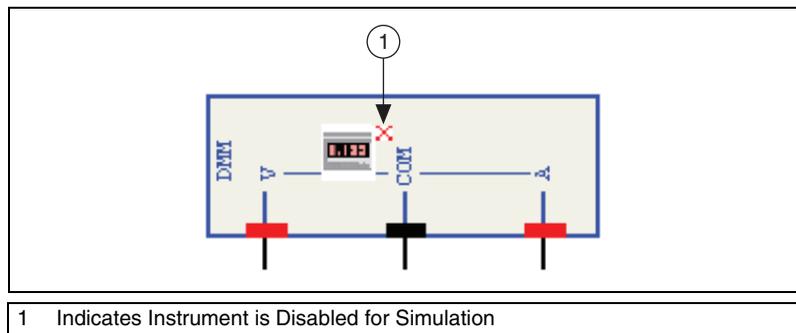


During simulation, these LEDs will light whether or not connections have been made to their corresponding pins in the prototyping rail. They indicate that power is available to the respective connections.

## Enabling NI ELVIS II Schematic Instruments for Simulation

NI ELVISmx instruments on the NI ELVIS II schematic can be enabled or disabled for simulation on an individual basis. Each enabled instrument consumes system resources, so setting unused instruments to disabled improves simulation speed.

When an NI ELVISmx instrument is disabled, a small red “X” appears next to the upper-right corner of the instrument icon on the schematic, as shown in the figure below (1). By default, all instruments in a new NI ELVIS II schematic begin as disabled.





**Note** NI ELVISmx instruments that are placed directly onto a workspace from the **NI ELVISmx Instruments** toolbar cannot be disabled for simulation. Refer to the [NI ELVISmx Instruments Toolbar](#) section for more information.

NI ELVISmx instruments' enabled state for simulation may be modified in any one of three ways:

- Double-click on a disabled instrument to display its SFP. If simulation is running, a warning displays advising you to stop simulation before you enable the instrument.
- Right-click on the instrument to display a context menu that includes the item **NI ELVIS II Instrument Enabled in Simulation**. Select this menu item to toggle its check mark and switch the instrument from enabled to disabled and back again. This command is unavailable during simulation.
- Select **Simulate»NI ELVIS II simulation settings** to display the **NI ELVIS II Simulation Settings** dialog box. This lists the NI ELVIS instruments on the rails and platform control panel, with a check box next to each one. Check/uncheck the instrument name to enable/disable the instrument on the schematic. This menu item is disabled during simulation.



**Note** This menu item is only active when an NI ELVIS II schematic is selected as the active workspace.

After enabling the desired instruments, run the simulation in the usual manner.



**Note** Refer to the *Multisim Help* for information about simulation.

## NI ELVIS II Instruments

The following NI ELVIS II instruments are available in Multisim:

- *Oscilloscope*—This instrument is a two-channel oscilloscope.
- *Dynamic Signal Analyzer*—This instrument computes and displays the RMS averaged power spectrum of a single channel.
- *Bode Analyzer*—This instrument measures the gain and phase shift versus frequency for passive or active linear designs.
- *Digital Multimeter*—This instrument is a digital multimeter.
- *Arbitrary Waveform Generator*—This instrument generates user-specified waveforms.

- **Function Generator**—This instrument generates sine, square or triangle waves.
- **Variable Power Supply**—This device is a variable DC power supply.
- **Digital Reader**—This instrument reads digital data.
- **Digital Writer**—This instrument updates the digital output on the NI ELVIS II Prototyping Board with user-specific digital patterns.

There are three ways to access NI ELVIS II instruments:

- Use the pre-placed icons found on the NI ELVIS II schematic rails and platform control panel sections.
- Place them from the menu onto any Multisim workspace using **Simulate»Instruments»NI ELVISmx instruments»<instrument>**.
- Place them from the **NI ELVISmx Instruments** toolbar onto any Multisim workspace. Refer to the *NI ELVISmx Instruments Toolbar* section for more information.

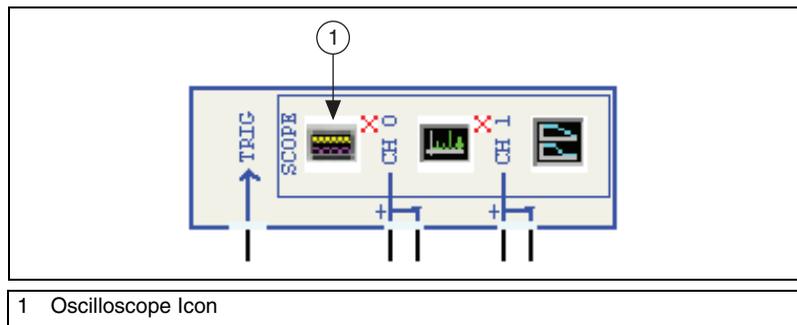
An NI ELVIS II instrument soft front panel (SFP) is where you find that instrument’s controls. To access any NI ELVIS II instrument’s SFP, double-click on its icon.

For information about any of the NI ELVIS II instruments, click the **Help** button on the instrument’s SFP to display the *NI ELVISmx Help*.

## Oscilloscope

This instrument is a two-channel oscilloscope.

In NI ELVIS II schematics, this instrument’s pre-placed icon is located in the NI ELVIS II Platform Control Panel Scope Section of the NI ELVIS II schematic, as shown in the figure below (1).



Complete the following step to connect the instrument:

1. Place wires from the desired points in your schematic to the pins on the NI ELVIS II Platform Control Panel Scope Section described below:
  - **TRIG**—Trigger input.
  - **CH 0+** —Positive input of channel 0.
  - **CH 0-** —Negative input of channel 0.
  - **CH 1+** —Positive input of channel 1.
  - **CH 1-** —Negative input of channel 1.

Complete the following steps to access the SFP:

1. Double-click the instrument's icon, shown in the figure above (1). The SFP appears.
2. Change the settings in the SFP as desired.

Complete the following steps to place this instrument directly onto *any* Multisim workspace:

1. Select **Simulate»Instruments»NI ELVISmx instruments»NI ELVISmx Oscilloscope**.
2. Click to place the instrument icon in the desired location on the workspace.
3. Wire in the same manner as any other Multisim instrument.



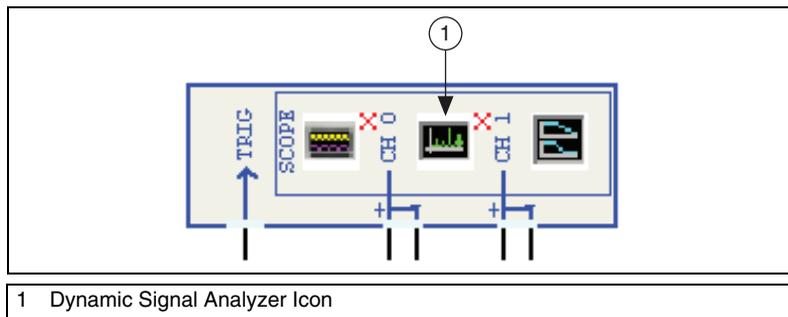
**Note** You can also use the **NI ELVISmx Instruments** toolbar to place this instrument. Refer to the [NI ELVISmx Instruments Toolbar](#) section for more information.

For information about using this instrument, click the **Help** button on its SFP to display the *NI ELVISmx Help*.

## Dynamic Signal Analyzer

The **NI ELVIS Dynamic Signal Analyzer** computes and displays the RMS averaged power spectrum of a single channel. A variety of windowing and averaging modes can be applied to the signal. It also detects the peak frequency component and estimates the actual frequency and power.

In NI ELVIS II schematics, this instrument's icon is located in the NI ELVIS II Platform Control Panel Scope Section of the NI ELVIS II schematic, as shown in the figure below (1).



Complete the following step to connect the instrument:

- Place wires from the desired points in your schematic to the pins on the NI ELVIS II Platform Control Panel Scope Section described below:
  - TRIG**—Trigger input.
  - CH 0+**—Positive input of channel 0.
  - CH 0-**—Negative input of channel 0.



**Note** **CH 1+** and **CH 1-** are not used for this device.

Complete the following steps to access the SFP:

- Double-click the instrument's icon, shown in the figure above (1). The SFP appears.
- Change the settings in the SFP as desired.

Complete the following steps to place this instrument directly onto *any* Multisim workspace:

- Select **Simulate»Instruments»NI ELVISmx instruments»NI ELVISmx Dynamic Signal Analyzer**.
- Click to place the instrument icon in the desired location on the workspace.
- Wire in the same manner as any other Multisim instrument.



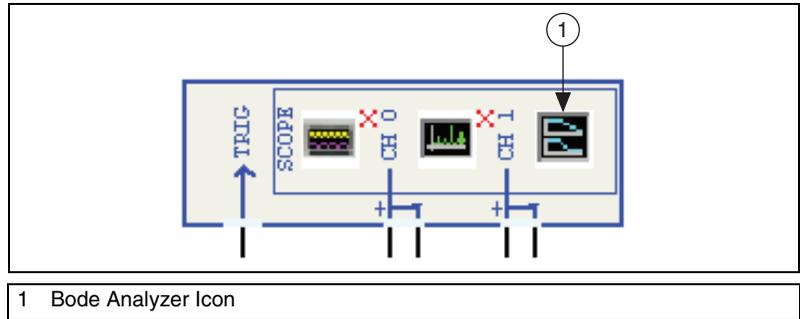
**Note** You can also use the **NI ELVISmx Instruments** toolbar to place this instrument. Refer to the [NI ELVISmx Instruments Toolbar](#) section for more information.

For information about using this instrument, click the **Help** button on its SFP to display the *NI ELVISmx Help*.

## Bode Analyzer

The NI ELVISmx **Bode Analyzer** measures the gain and phase shift versus frequency for passive or active linear designs.

In NI ELVIS II schematics, this instrument's icon is located in the NI ELVIS II Platform Control Panel Scope Section of the NI ELVIS II schematic, as shown in the figure below (1).



1 Bode Analyzer Icon

Complete the following step to connect the instrument:

- Place wires from the desired points in your schematic to the pins on the NI ELVIS II Platform Control Panel Scope Section described below:
  - CH 0+** —Positive Stimulus.
  - CH 0-** —Negative Stimulus.
  - CH 1+** —Positive Response.
  - CH 1-** —Negative Response.

Complete the following steps to access the SFP:

- Double-click the instrument's icon, shown in the figure above (1). The SFP appears.
- Change the settings in the SFP as desired.

Complete the following steps to place this instrument directly onto *any* Multisim workspace:

- Select **Simulate»Instruments»NI ELVISmx instruments»NI ELVISmx Bode Analyzer**.
- Click to place the instrument icon in the desired location on the workspace.
- Wire in the same manner as any other Multisim instrument.



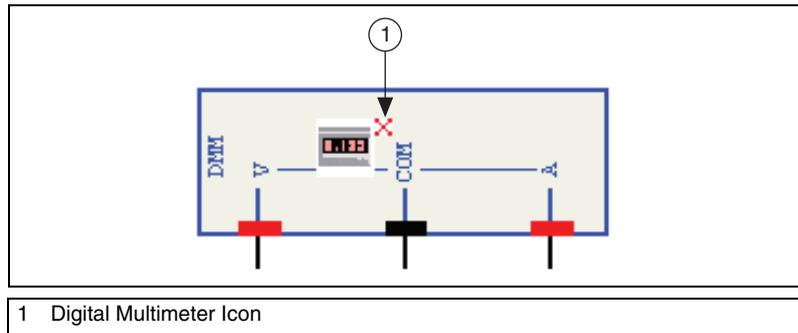
**Note** You can also use the **NI ELVISmx Instruments** toolbar to place this instrument. Refer to the [NI ELVISmx Instruments Toolbar](#) section for more information.

For information about using this instrument, click the **Help** button on its SFP to display the *NI ELVISmx Help*.

## Digital Multimeter

This instrument is a digital multimeter (DMM).

In NI ELVIS II schematics, this instrument's icon is located in the NI ELVIS II Platform Control Panel DMM Section of the NI ELVIS II schematic, as shown in the figure below (1).



Complete the following step to connect the instrument:

- Place wires from the desired points in your schematic to the pins on the NI ELVIS II Platform Control Panel DMM Section described below:
  - V**—Voltmeter input.
  - COM**—Common input.
  - A**—Ammeter input.

Complete the following steps to access the SFP:

- Double-click the instrument's icon, shown in the figure above (1). The SFP appears.
- Change the settings in the SFP as desired.

Complete the following steps to place this instrument directly onto *any* Multisim workspace:

- Select **Simulate»Instruments»NI ELVISmx instruments»NI ELVISmx Digital Multimeter**.
- Click to place the instrument icon in the desired location on the workspace.
- Wire in the same manner as any other Multisim instrument.



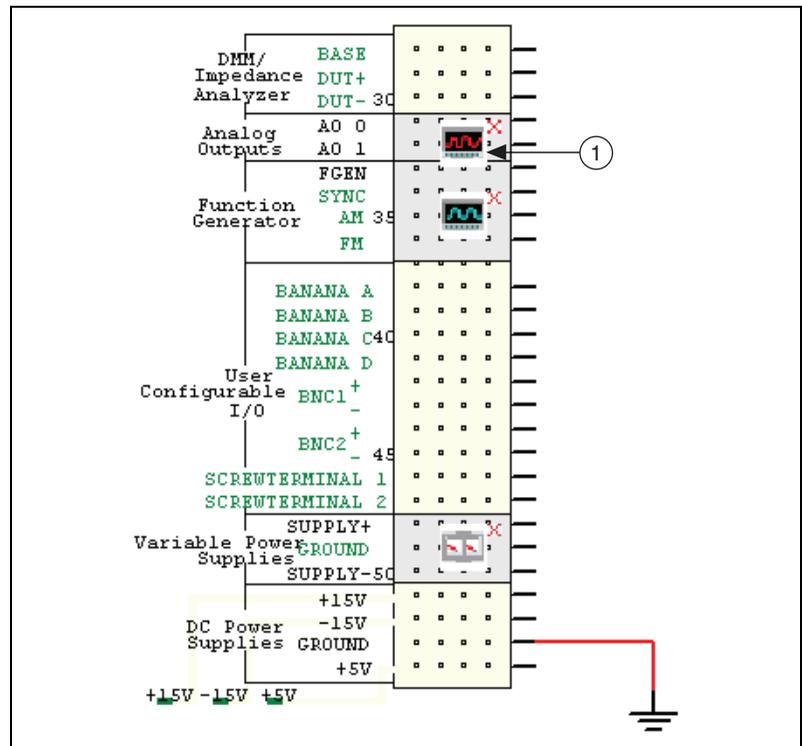
**Note** You can also use the **NI ELVISmx Instruments** toolbar to place this instrument. Refer to the *NI ELVISmx Instruments Toolbar* section for more information.

For information about using this instrument, click the **Help** button on its SFP to display the *NI ELVISmx Help*.

## Arbitrary Waveform Generator

This instrument generates user-specified waveforms.

In NI ELVIS II schematics, this instrument's icon is located in the NI ELVIS II Left-Bottom Rail Section of the NI ELVIS II schematic, as shown in the figure below (1).



1 Arbitrary Waveform Generator Icon

Complete the following step to connect the instrument:

1. Place wires from the desired points in your schematic to the pins on the NI ELVIS II Left-Bottom Rail Section described below:
  - **AO 0**—Output pin 0.
  - **AO 1**—Output pin 1.

Complete the following steps to access the SFP:

1. Double-click the instrument's icon, shown in the figure above (1). The SFP appears.
2. Change the settings in the SFP as desired.

Complete the following steps to place this instrument directly onto *any* Multisim workspace:

1. Select **Simulate»Instruments»NI ELVISmx instruments»NI ELVISmx Arbitrary Waveform Generator**.
2. Click to place the instrument icon in the desired location on the workspace.
3. Wire in the same manner as any other Multisim instrument.



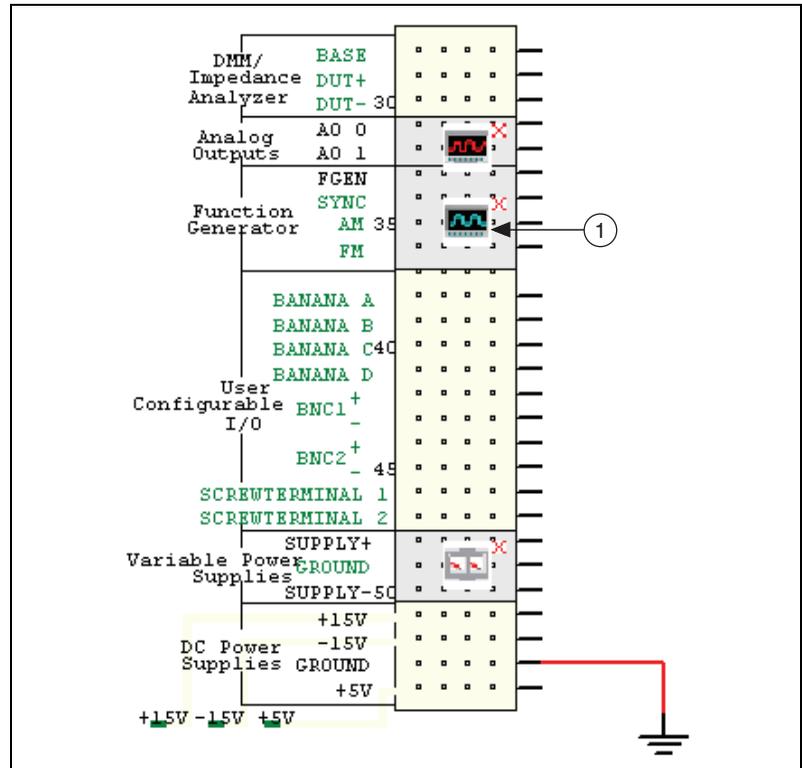
**Note** You can also use the **NI ELVISmx Instruments** toolbar to place this instrument. Refer to the [NI ELVISmx Instruments Toolbar](#) section for more information.

For information about using this instrument, click the **Help** button on its SFP to display the *NI ELVISmx Help*.

## Function Generator

This instrument generates sine, square or triangle waves.

In NI ELVIS II schematics, this instrument's icon is located in the NI ELVIS II Left-Bottom Rail Section of the NI ELVIS II schematic, as shown in the figure below (1).



1 Function Generator Icon

Complete the following step to connect the instrument:

- Place wires from the desired points in your schematic to the pin on the NI ELVIS II Left-Bottom Rail Section described below:
  - FGEN**—Output from the device.

Complete the following steps to access the SFP:

1. Double-click the instrument's icon, shown in the figure above (1). The SFP appears.
2. Change the settings in the SFP as desired.

Complete the following steps to place this instrument directly onto *any* Multisim workspace:

1. Select **Simulate»Instruments»NI ELVISmx instruments»NI ELVISmx Function Generator**.
2. Click to place the instrument icon in the desired location on the workspace.
3. Wire in the same manner as any other Multisim instrument.



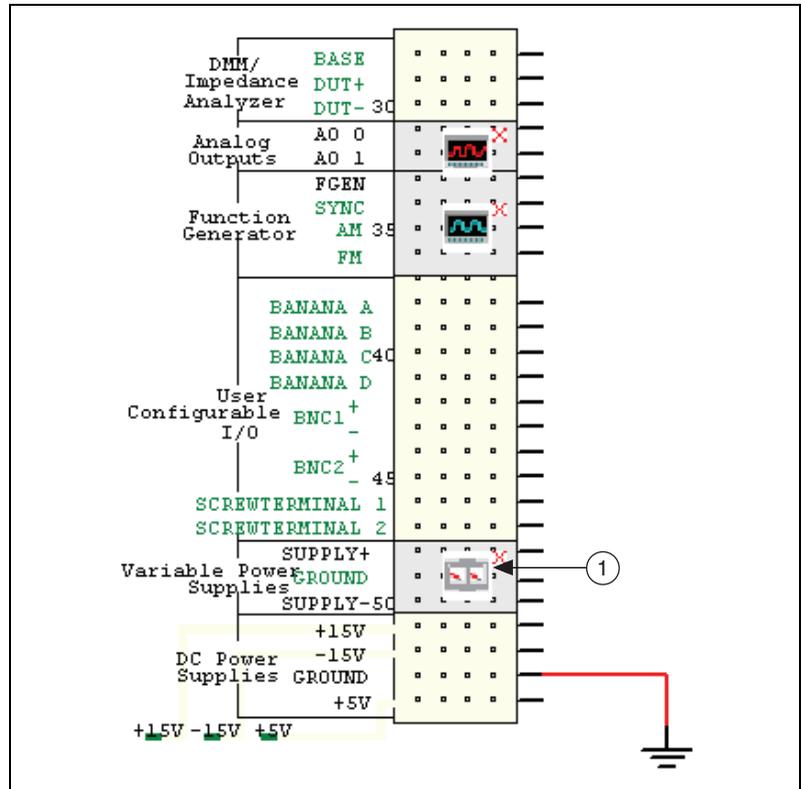
**Note** You can also use the **NI ELVISmx Instruments** toolbar to place this instrument. Refer to the [NI ELVISmx Instruments Toolbar](#) section for more information.

For information about using this instrument, click the **Help** button on its SFP to display the *NI ELVISmx Help*.

## Variable Power Supply

This device is a variable DC power supply.

In NI ELVIS II schematics, this instrument's icon is located in the NI ELVIS II Left-Bottom Rail Section of the NI ELVIS II schematic, as shown in the figure below (1).



1 Variable Power Supply Icon

Complete the following step to connect the device:

- Place wires from the desired points in your schematic to the pins on the NI ELVIS II Left-Bottom Rail Section described below:
  - SUPPLY+** —Positive output.
  - SUPPLY-** —Negative output.

Complete the following steps to access the SFP:

1. Double-click the instrument's icon, shown in the figure above (1). The SFP appears.
2. Change the settings in the SFP as desired.

Complete the following steps to place this instrument directly onto *any* Multisim workspace:

1. Select **Simulate»Instruments»NI ELVISmx instruments»NI ELVISmx Variable Power Supply**.
2. Click to place the instrument icon in the desired location on the workspace.
3. Wire in the same manner as any other Multisim instrument.



**Note** You can also use the **NI ELVISmx Instruments** toolbar to place this instrument. Refer to the [NI ELVISmx Instruments Toolbar](#) section for more information.

For information about using this instrument, click the **Help** button on its SFP to display the *NI ELVISmx Help*.

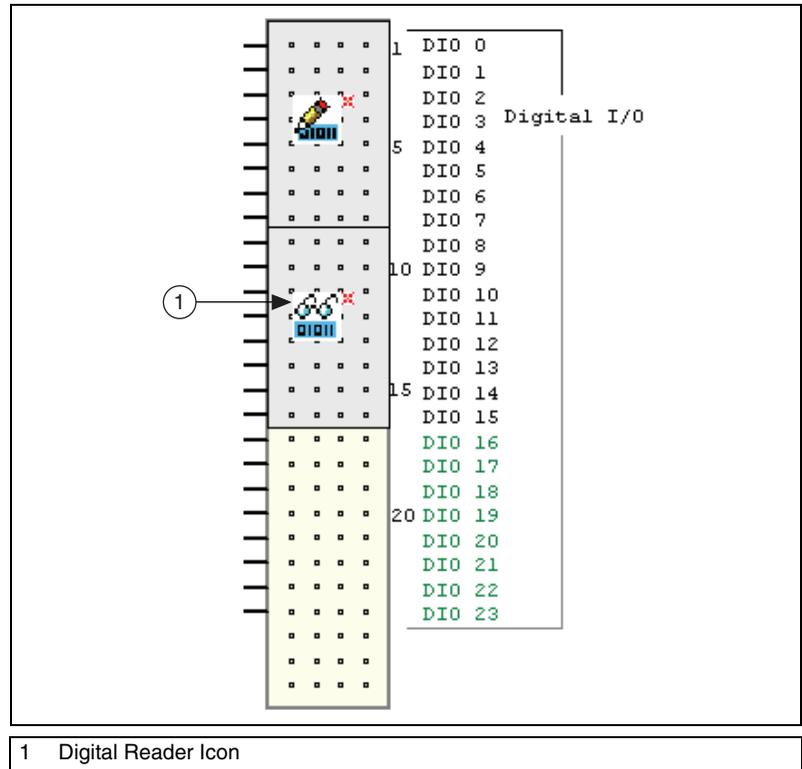
The left-bottom rail also contains the following fixed DC power supplies:

- **+15 V**
- **-15 V**
- **+5 V**

## Digital Reader

This instrument reads digital data.

In NI ELVIS II schematics, this instrument's icon is located in the NI ELVIS II Right-Top Rail Section of the NI ELVIS II schematic, as shown in the figure below (1).



Complete the following step to connect the instrument:

- Place wires from the desired points in your schematic to the pins on the NI ELVIS II Right-Top Rail Section described below:
  - DIO 8–DIO 15**—The inputs for the device.

Complete the following steps to access the SFP:

- Double-click the instrument's icon, shown in the figure above (1). The SFP appears.
- Change the settings in the SFP as desired.

Complete the following steps to place this instrument directly onto *any* Multisim workspace:

1. Select **Simulate»Instruments»NI ELVISmx instruments»NI ELVISmx Digital Reader**.
2. Click to place the instrument icon in the desired location on the workspace.
3. Wire in the same manner as any other Multisim instrument.



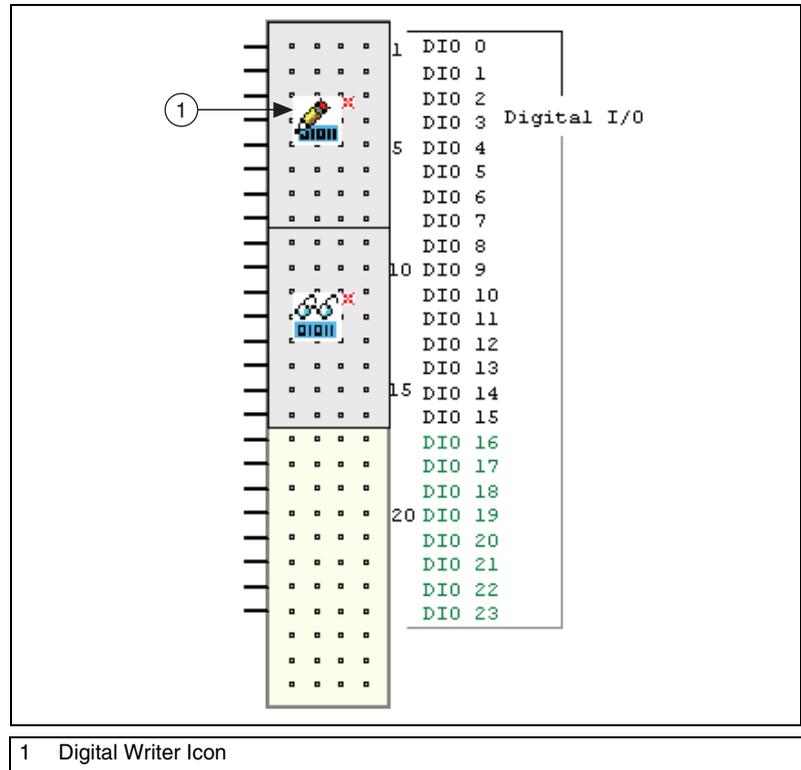
**Note** You can also use the **NI ELVISmx Instruments** toolbar to place this instrument. Refer to the [NI ELVISmx Instruments Toolbar](#) section for more information.

For information about using this instrument, click the **Help** button on its SFP to display the *NI ELVISmx Help*.

## Digital Writer

This instrument updates the digital output on the NI ELVIS Prototyping Board with user-specific digital patterns.

In NI ELVIS II schematics, this instrument's icon is located in the NI ELVIS II Right-Top Rail Section of the NI ELVIS II schematic, as shown in the figure below (1).



Complete the following step to connect the instrument:

- Place wires from the desired points in your schematic to the pins on the NI ELVIS II Right-Top Rail Section described below:
  - DIO 0–DIO 7**—The outputs for the device.

Complete the following steps to access the SFP:

- Double-click the instrument's icon, shown in the figure above (1). The SFP appears.
- Change the settings in the SFP as desired.

Complete the following steps to place this instrument directly onto *any* Multisim workspace:

1. Select **Simulate»Instruments»NI ELVISmx instruments»NI ELVISmx Digital Writer**.
2. Click to place the instrument icon in the desired location on the workspace.
3. Wire in the same manner as any other Multisim instrument.



**Note** You can also use the **NI ELVISmx Instruments** toolbar to place this instrument. Refer to the *NI ELVISmx Instruments Toolbar* section for more information.

For information about using this instrument, click the **Help** button on its SFP to display the *NI ELVISmx Help*.

## NI ELVISmx Instruments Toolbar

The buttons in the **NI ELVISmx Instruments** toolbar are described below. In each case, the button places a specific NI ELVISmx instrument on the workspace.

Button	Description
	<b>NI ELVISmx Arbitrary Waveform Generator</b> button. Places an NI ELVISmx arbitrary waveform generator on the workspace. Refer to the <i>Arbitrary Waveform Generator</i> section for more information.
	<b>NI ELVISmx Digital Reader</b> button. Places an NI ELVISmx digital reader on the workspace. Refer to the <i>Digital Reader</i> section for more information.
	<b>NI ELVISmx Digital Writer</b> button. Places an NI ELVISmx digital writer on the workspace. Refer to the <i>Digital Writer</i> section for more information.
	<b>NI ELVISmx Digital Multimeter</b> button. Places an NI ELVISmx digital multimeter on the workspace. Refer to the <i>Digital Multimeter</i> section for more information.
	<b>NI ELVISmx Dynamic Signal Analyzer</b> button. Places an NI ELVISmx dynamic signal analyzer on the workspace. Refer to the <i>Dynamic Signal Analyzer</i> section for more information.

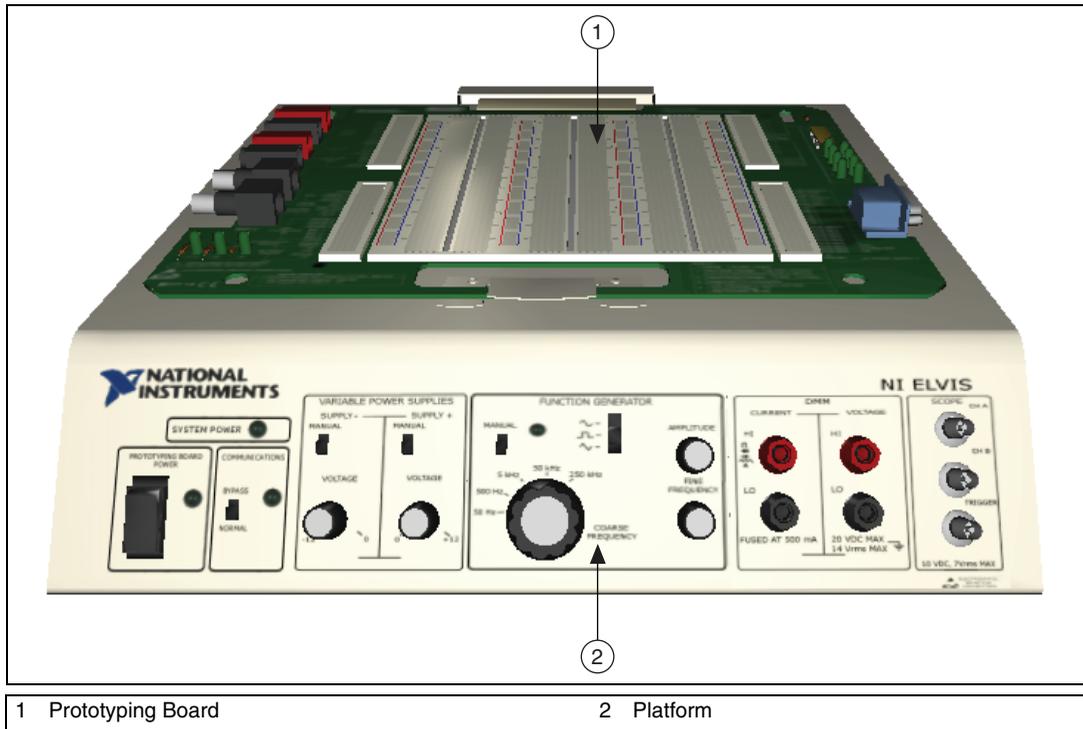
Button	Description
	<b>NI ELVISmx Function Generator</b> button. Places an NI ELVISmx function generator on the workspace. Refer to the <i>Function Generator</i> section for more information.
	<b>NI ELVISmx Oscilloscope</b> button. Places an NI ELVISmx oscilloscope on the workspace. Refer to the <i>Oscilloscope</i> section for more information.
	<b>NI ELVISmx Variable Power Supply</b> button. Places an NI ELVISmx variable power supply on the workspace. Refer to the <i>Variable Power Supply</i> section for more information.
	<b>NI ELVISmx Bode Analyzer</b> button. Places an NI ELVISmx bode analyzer on the workspace. Refer to the <i>Bode Analyzer</i> section for more information.

## NI ELVIS Prototyping Boards

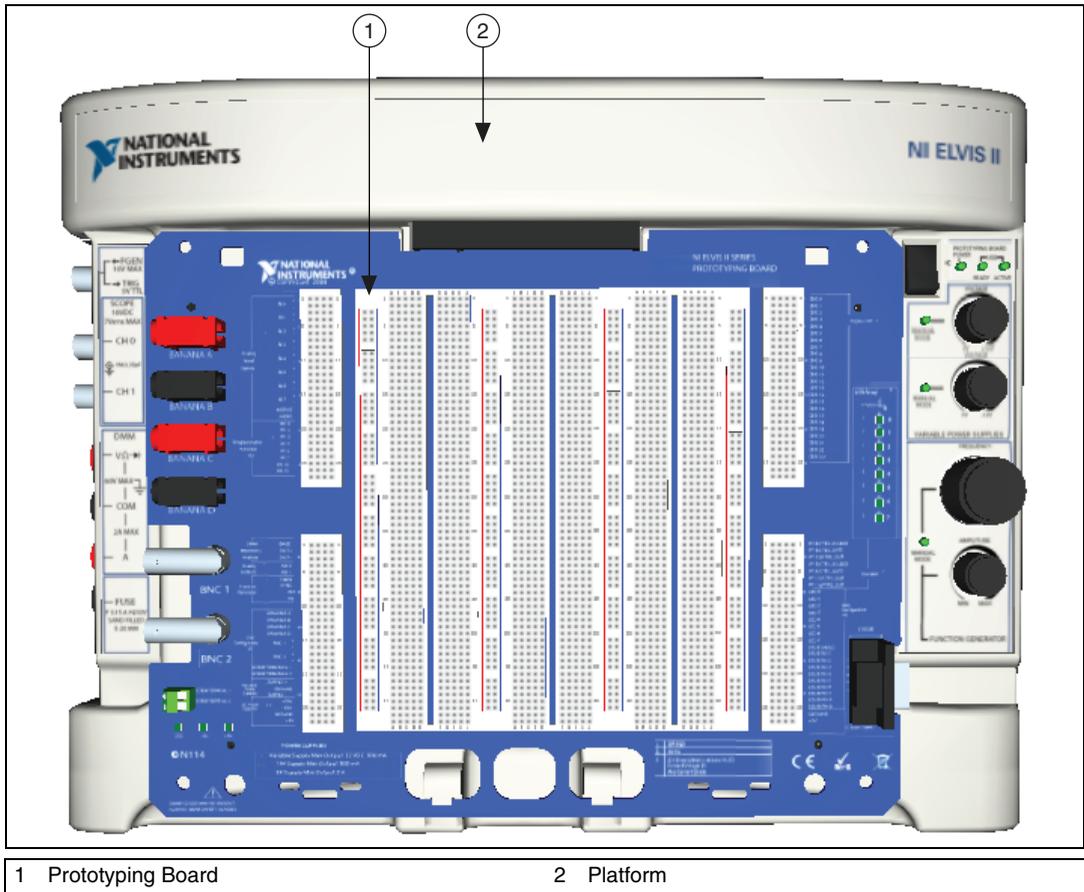
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Once you have completed the virtual NI ELVIS I or NI ELVIS II schematic, you are ready to place the components on the 3D rendering of the prototyping board.

The figure below shows the virtual NI ELVIS I 3D prototyping board (1) and platform (2) with no placed components.



The figure below shows the virtual NI ELVIS II 3D prototyping board (1) and platform (2) with no placed components.



**Note** The controls that appear on the NI ELVIS I and the NI ELVIS II 3D platforms are inactive. Interactive simulation is accomplished via the schematic view. For details on simulation, refer to the *Multisim Help*.



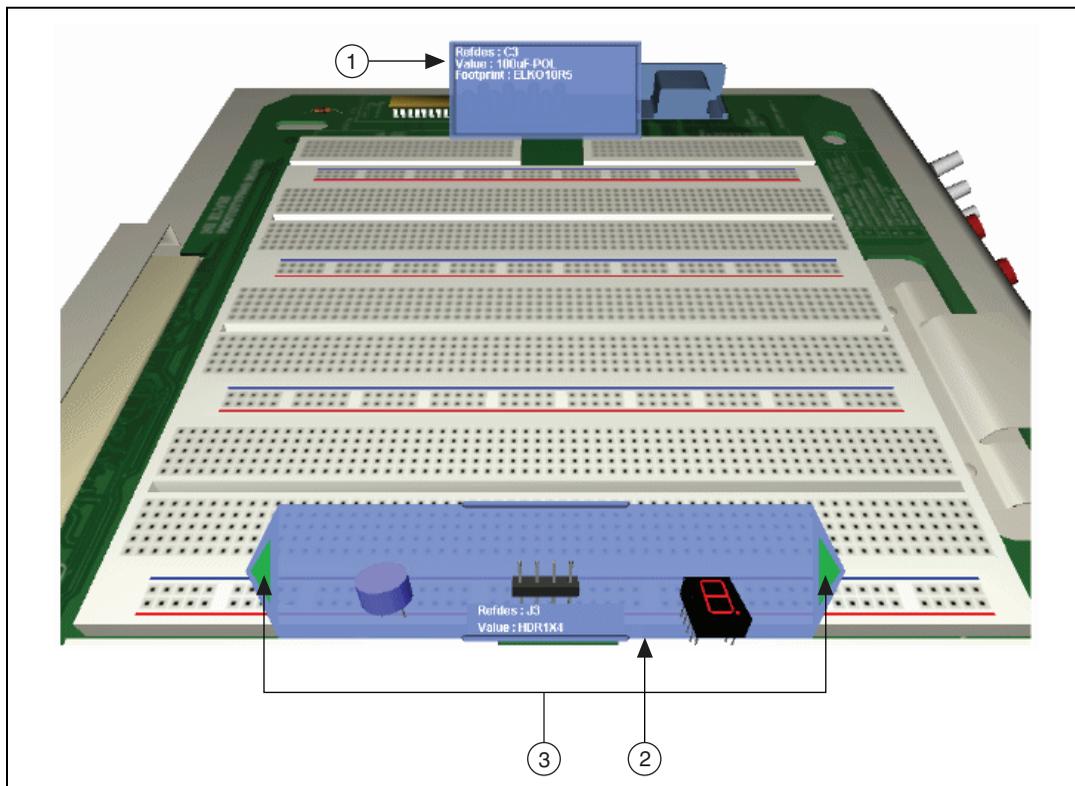
**Tip** For information about changing the 3D view, refer to the *Manipulating the Breadboard View* section of Chapter 2, *Breadboarding*.

Complete the following steps to place components on the 3D prototyping board:



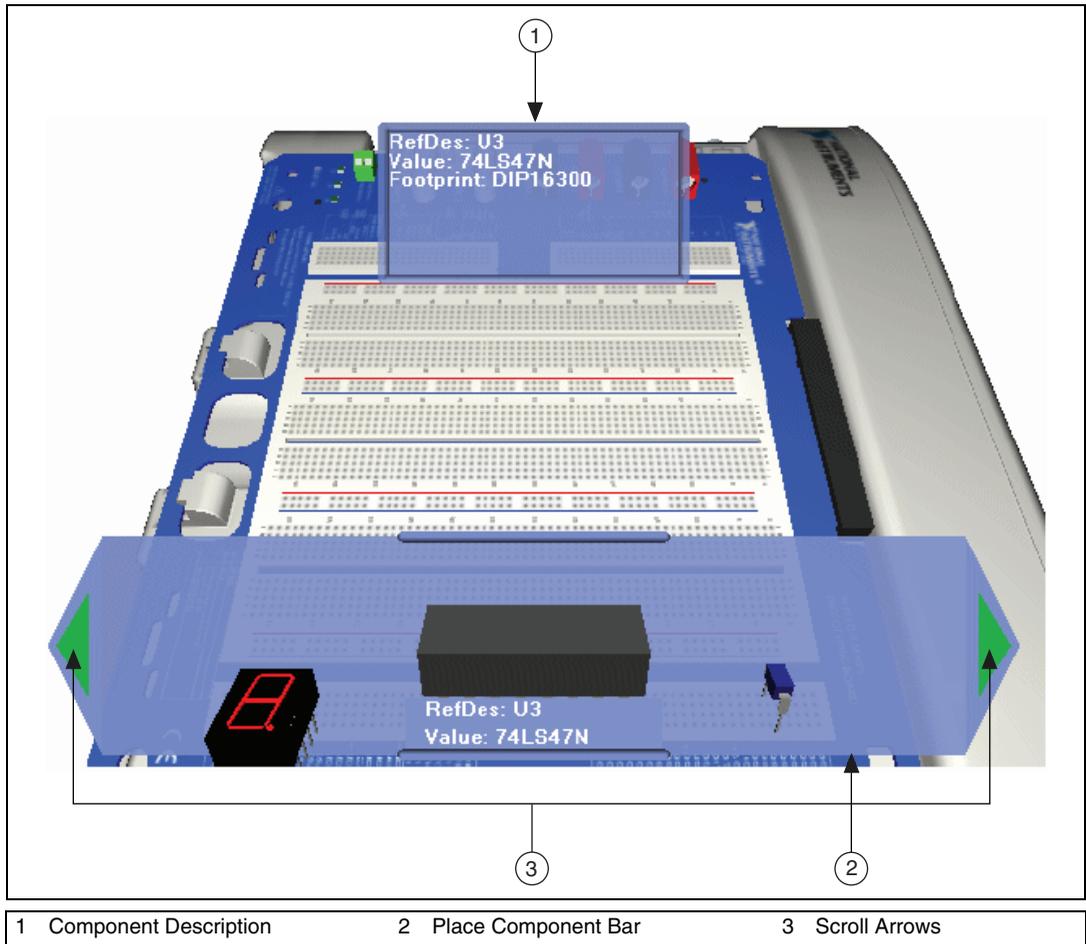
1. Select **Tools»View breadboard** from the main Multisim menu.

For NI ELVIS I designs, the 3D prototyping board appears similar to the example shown in the figure below:



1	Component Description	2	Place Component Bar	3	Scroll Arrows
---	-----------------------	---	---------------------	---	---------------

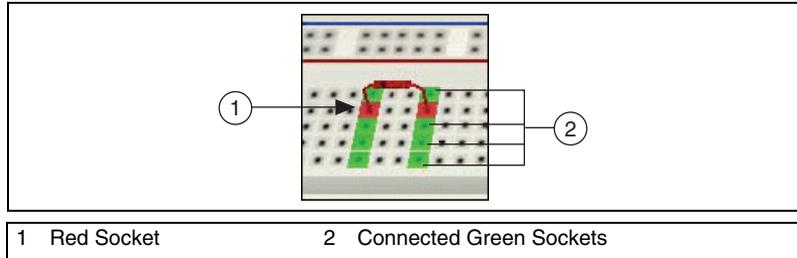
For NI ELVIS II designs, the 3D prototyping board appears similar to the example shown in the figure below:



**Note** The **Place Component Bar**, shown in the figures above (2), is where components waiting to be placed on the prototyping board appear. To view other components, click the scroll arrows (3). To see a description of a component (for example, (1) in the above figure), hover the cursor over the component. 3D viewing options are set in the **Global Preferences** dialog box. Refer to the [3D Options](#) section of Chapter 2, [Breadboarding](#) for more information.

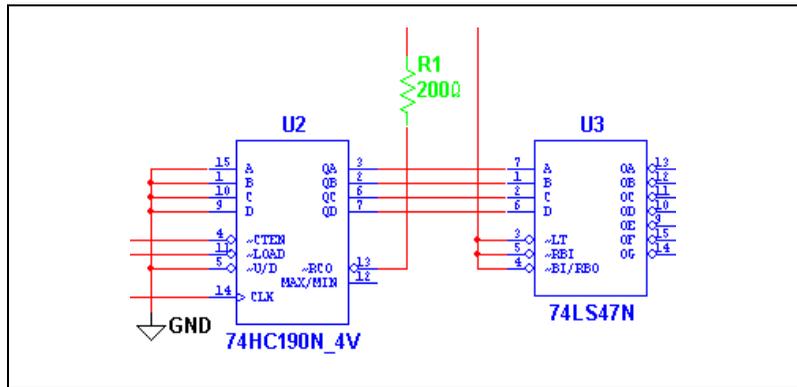
- Click on a component in the **Place Component Bar** and drag it to the desired location on the board. As the component passes over the board, sockets change color as shown in the figure below.

Red sockets (1) indicate where the component's pins will be placed when the mouse button is released. Green (2) indicates sockets that are internally connected to the red socket in the same row on the board.



**Tip** Select <Ctrl-R> to rotate a selected component 90 degrees clockwise or <Ctrl-Shift-R> to rotate it 90 degrees counter-clockwise.

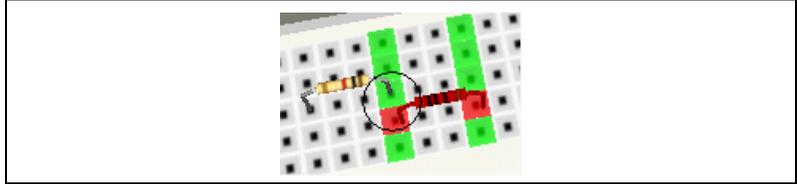
- Release the mouse button to place the component. The colored (red and green) sockets on the board no longer appear.
- Return to the schematic view and note that the color of the placed component has changed as shown in the example below (R1).



- Continue placing the design's components on the board. When all the components have been placed, the **Place Component Bar** collapses.



**Tip** Where pins of components are connected on the schematic, you can place them in connected sockets as circled in the figure below. This technique can reduce the number of jumper wires required.



**Note** Refer to the *Appearance of 3D Components* section of Chapter 2, *Breadboarding*, for more information.

## Wiring Placed Components in 3D Mode



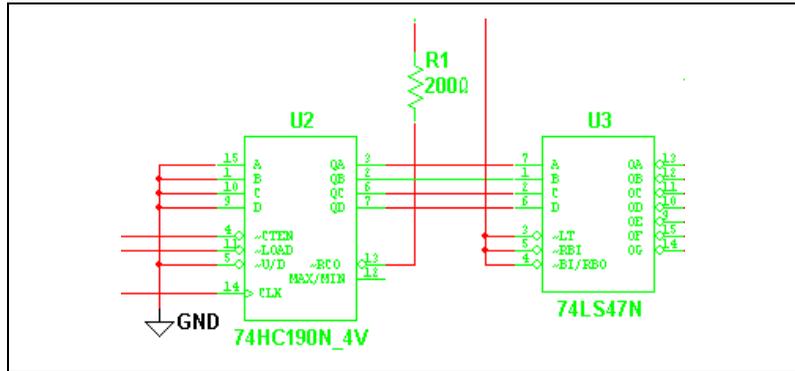
**Note** This section applies to both NI ELVIS I and NI ELVIS II schematics.

By placing component pins that are connected on the schematic into sockets on the 3D prototyping board that are internally connected, much of the “wiring” can be done at the same time components are placed. However, in most designs, it will also be necessary to place jumpers on the 3D prototyping board to complete the wiring of the placed components.

Complete the following steps to place a jumper wire:

1. Click on a socket connected to the pin where you wish to start the jumper and begin moving the cursor. Legitimate “target” pins (green) display as you move the cursor.
2. Click to place the jumper in the desired socket.

- Return to the schematic view and note that the color of the wire connecting the two pins has changed to green to indicate a connection has been made, as shown in the figure below, between pin 2 of U2, and pin 1 of U3.



**Note** If a net contains multiple connections, all must be connected before any of the wires in the net change color.

- Continue placing jumpers until all schematic connections have been made.



**Tip** Run a **Design Rules and Connectivity Check** from the 3D prototyping view to see if there are any errors in your board. Refer to the *DRC and Connectivity Check* section of Chapter 2, *Breadboarding*, for more information.



**Note** You may also wish to refer to the *Viewing Component Information* and *Breadboard Netlist dialog box* sections of Chapter 2, *Breadboarding*.

## Virtual NI myDAQ

NI myDAQ is a low-cost, portable data acquisition device that students can use to do laboratory-style measurements outside of the lab.

A virtual NI myDAQ schematic contains a number of items that correspond to elements of the real-world NI myDAQ. The connection and control of these elements is described in this section.

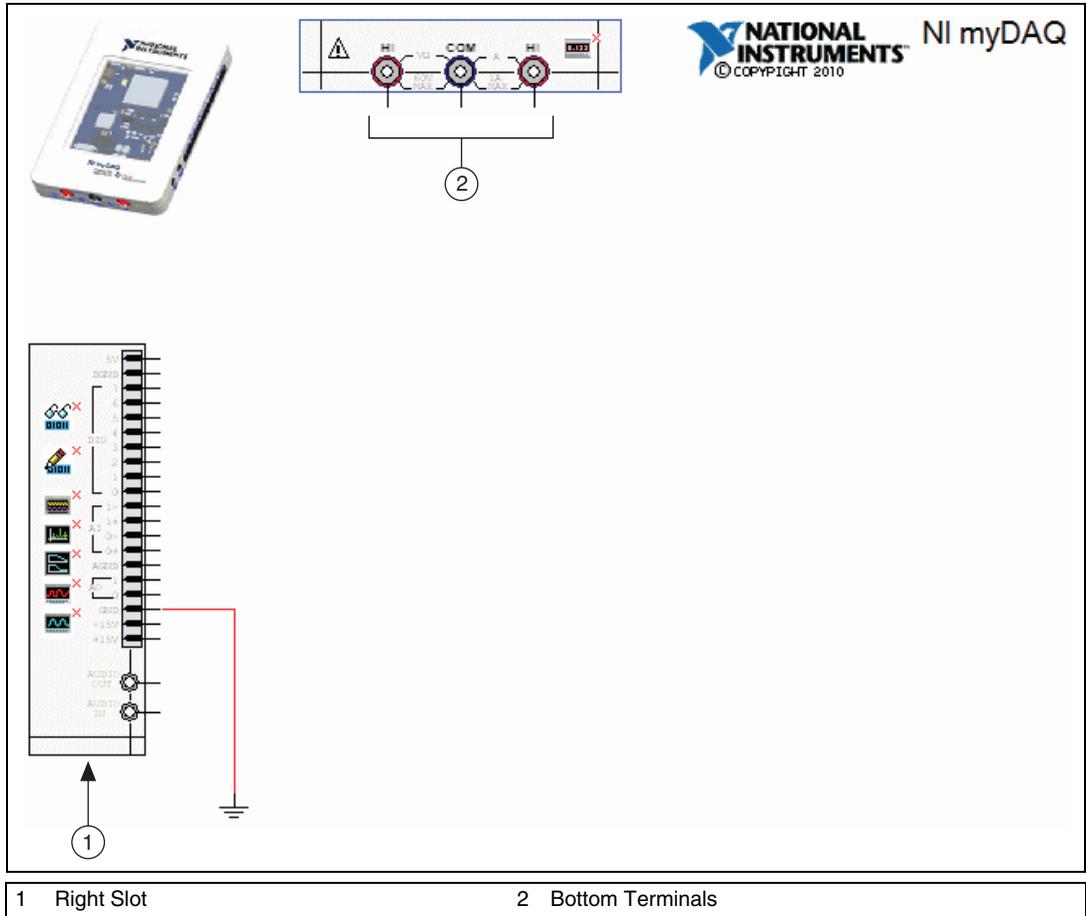


**Note** During NI Circuit Design Suite (NI CDS) installation, the installer prompts you for the NI ELVISmx installation CD, which is included in your NI CDS package. NI ELVISmx

enables the NI myDAQ functionality in Multisim. If you do not install this software, the NI myDAQ functionality will be disabled in Multisim.

Complete the following steps to create a new virtual NI myDAQ design:

1. Select **File»New»NI myDAQ design**. When first opened, a virtual NI myDAQ schematic appears as shown below.



**Note** The ground connector that appears at the bottom left of the diagram is the reference point for measurements taken during simulation, and must not be removed.

2. Place and wire components in the virtual NI myDAQ schematic in the same manner as other Multisim schematics. For details, refer to the *Multisim Help*.

The connectors (see 1 in the figure above) found on the workspace correspond to the connectors in the right slot of the real-world version of the NI myDAQ, and are labelled in the same manner. In the bottom terminals section of the workspace (see 2 in the figure above), there is an icon for connecting to the digital multimeter.

Rows in the right slot that are shown with green labels are for schematic capture only and are not available for simulation in Multisim.

The right slot section of the NI myDAQ schematic also contains the following fixed DC power supplies:

- **-15 V**
- **+15 V**

## Enabling NI myDAQ Schematic Instruments for Simulation

NI ELVISmx instruments on the NI myDAQ schematic can be enabled or disabled for simulation on an individual basis. Each enabled instrument consumes system resources, so setting unused instruments to disabled improves simulation speed.

When an NI ELVISmx instrument is disabled, a small red “X” appears next to the upper-right corner of the instrument icon on the schematic. By default, all instruments in a new NI myDAQ schematic begin as disabled.

NI ELVISmx instruments may be enabled for simulation in these ways:

- Double-click on a disabled instrument to display its SFP. This automatically enables it. If simulation is running, a warning displays advising you to stop simulation before you enable the instrument.
- Right-click on the instrument to display a context menu that includes the item **NI myDAQ Instrument Enabled in Simulation**. Select this menu item to toggle the instrument from enabled to disabled and back again. This command is unavailable during simulation.
- Select **Simulate»NI myDAQ simulation settings** to display the **NI myDAQ Simulation Settings** dialog box. This lists the **NI ELVISmx** instruments with a check box next to each one. Check/uncheck the instrument name to enable/disable the instrument on the schematic. This menu item is disabled during simulation.



**Note** This menu item is only active when an NI myDAQ schematic is selected as the active workspace.

After enabling the desired instruments, run the simulation in the usual manner.



**Note** Refer to the *Multisim Help* for information about simulation.

## NI ELVISmx Instruments in Virtual NI myDAQ

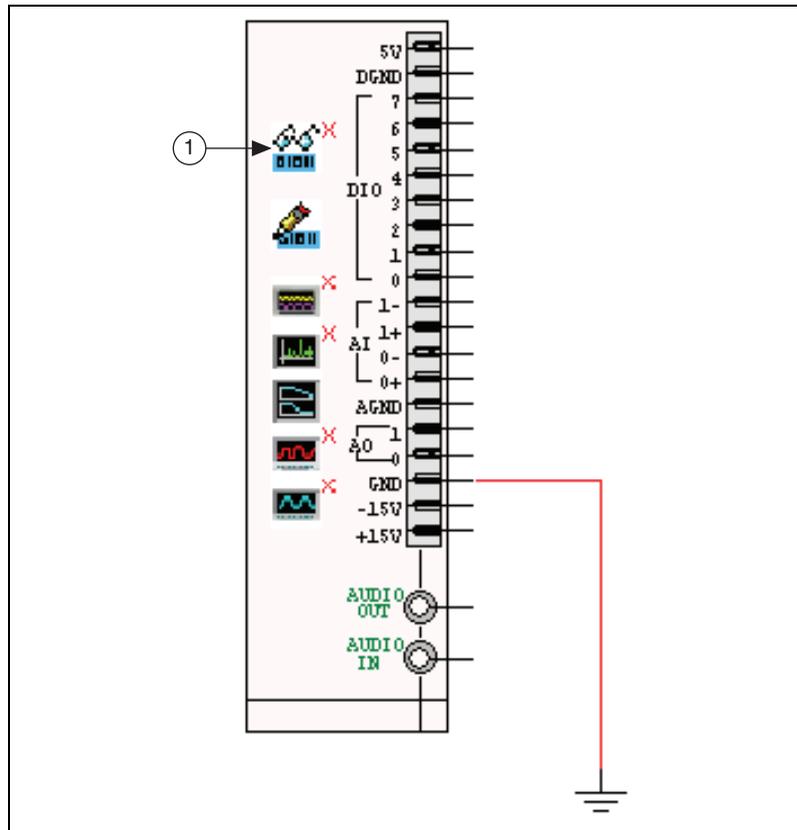
The following NI ELVISmx instruments are available in Multisim:

- *Digital Reader*—This instrument reads digital data.
- *Digital Writer*—This instrument updates the digital I/O (DIO) lines with user-specified digital patterns.
- *Oscilloscope*—This instrument is a two-channel oscilloscope.
- *Dynamic Signal Analyzer*—This instrument computes and displays the RMS averaged power spectrum of a single channel.
- *Bode Analyzer*—This instrument measures the gain and phase shift versus frequency for passive or active linear designs.
- *Arbitrary Waveform Generator*—This instrument generates user-specified waveforms.
- *Function Generator*—This instrument generates sine, square or triangle waves.
- *Digital Multimeter*—This instrument is a digital multimeter.

## Digital Reader

This instrument reads digital data.

This instrument's pre-placed icon is located in the NI myDAQ right slot section of the NI myDAQ schematic, as shown in the figure below (1).



1 Digital Reader Icon

Complete the following step to connect the instrument:

1. Place wires from the desired points in your schematic to the pins on the NI myDAQ right slot section described below:
  - **DIO 4–DIO 7**—The inputs for the device.

Complete the following steps to access the SFP:

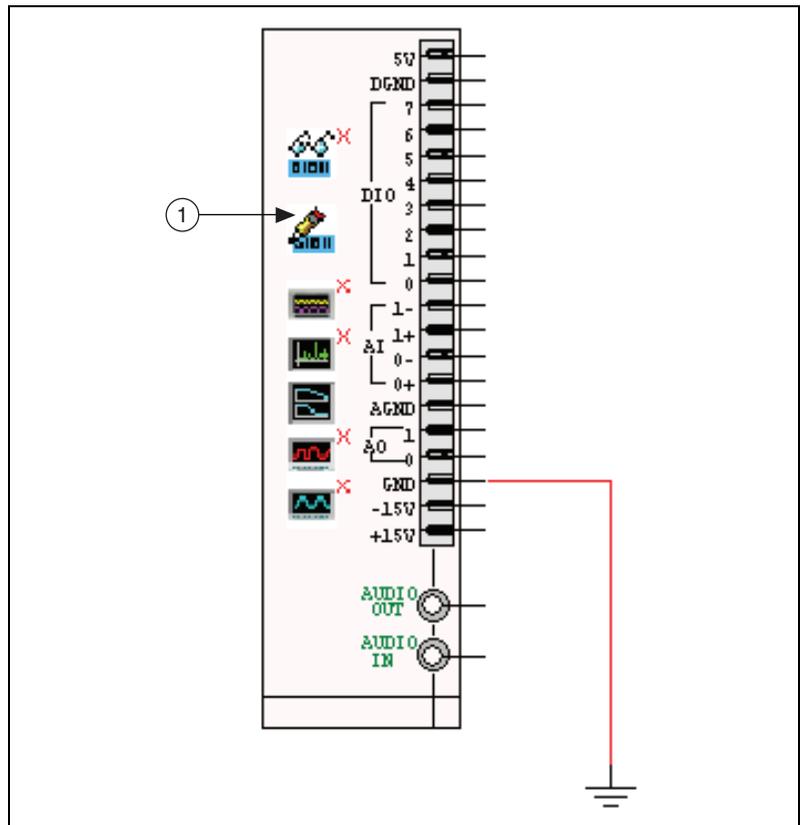
1. Double-click the instrument's icon, shown in the figure above (1). The SFP appears.
2. Change the settings in the SFP as desired.

For information about using this instrument, click the **Help** button on its SFP to display the *NI ELVISmx Help*.

## Digital Writer

This instrument updates the digital I/O (DIO) lines with user-specified digital patterns.

This instrument's pre-placed icon is located in the NI myDAQ right slot section of the NI myDAQ schematic, as shown in the figure below (1).



1 Digital Reader Icon

Complete the following step to connect the instrument:

1. Place wires from the desired points in your schematic to the pins on the NI myDAQ right slot section described below:
  - **DIO 0–DIO 3**—The inputs for the device.

Complete the following steps to access the SFP:

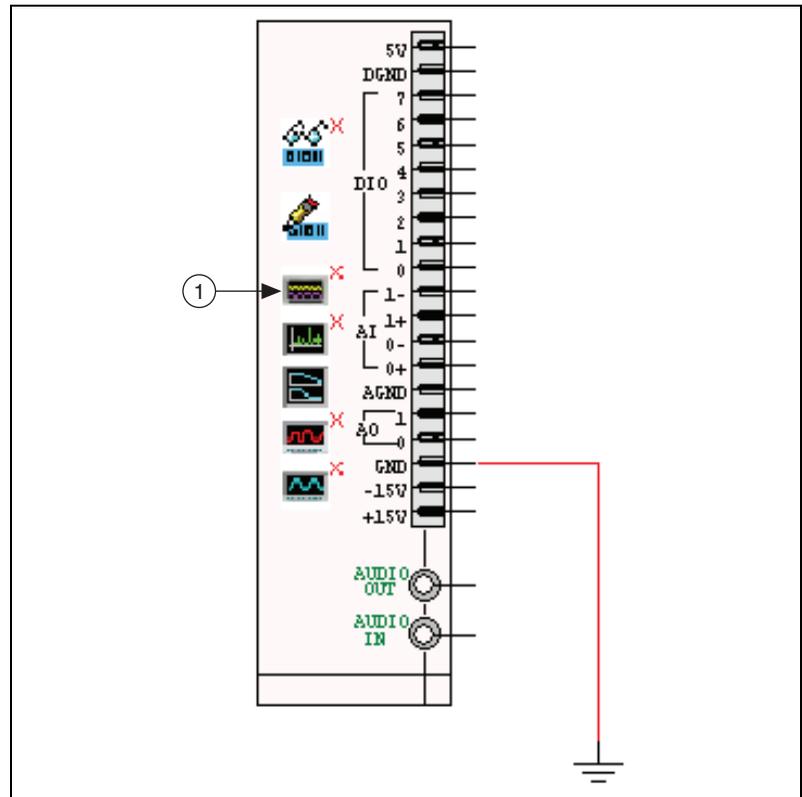
1. Double-click the instrument's icon, shown in the figure above (1). The SFP appears.
2. Change the settings in the SFP as desired.

For information about using this instrument, click the **Help** button on its SFP to display the *NI ELVISmx Help*.

## Oscilloscope

This instrument is a two-channel oscilloscope.

This instrument's pre-placed icon is located in the NI myDAQ right slot section of the NI myDAQ schematic, as shown in the figure below (1).



1 Oscilloscope Icon

Complete the following step to connect the instrument:

- Place wires from the desired points in your schematic to the pins on the NI myDAQ right slot section described below:
  - **AI 0+** —Positive input of channel 0.
  - **AI 0-** —Negative input of channel 0.
  - **AI 1+** —Positive input of channel 1.
  - **AI 1-** —Negative input of channel 1.



**Note** These pins are shared with the **Bode Analyzer** and the **Dynamic Signal Analyzer**.

Complete the following steps to access the SFP:

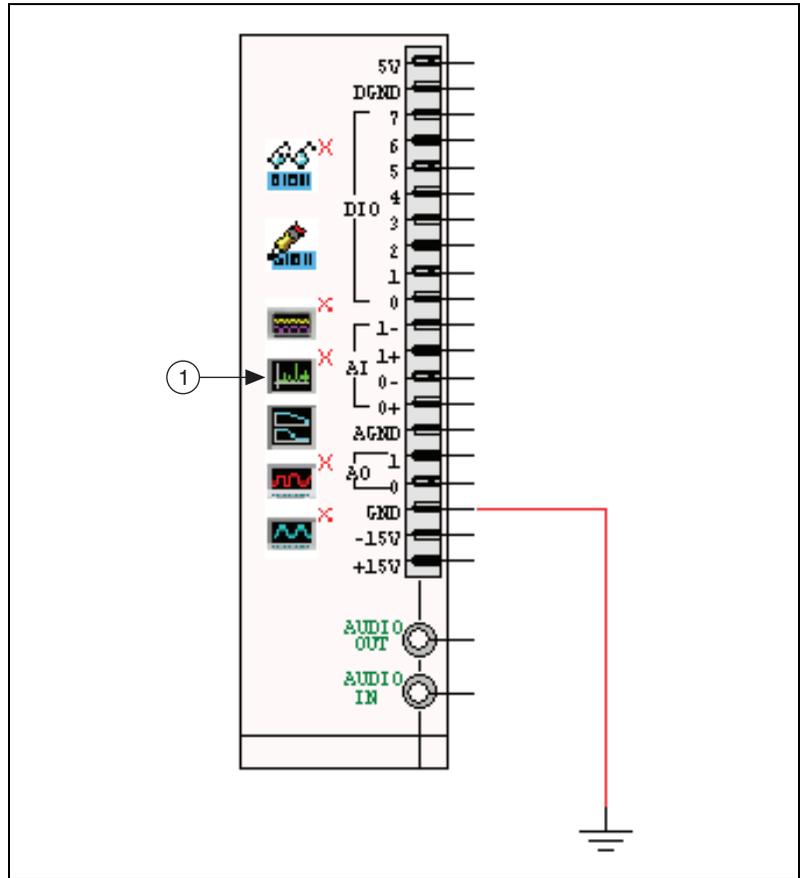
1. Double-click the instrument's icon, shown in the figure above (1). The SFP appears.
2. Change the settings in the SFP as desired.

For information about using this instrument, click the **Help** button on its SFP to display the *NI ELVISmx Help*.

## Dynamic Signal Analyzer

This instrument computes and displays the RMS averaged power spectrum of a single channel. A variety of windowing and averaging modes can be applied to the signal. It also detects the peak frequency component and estimates the actual frequency and power.

This instrument's pre-placed icon is located in the NI myDAQ right slot section of the NI myDAQ schematic, as shown in the figure below (1).



1 Dynamic Signal Analyzer Icon

Complete the following step to connect the instrument:

1. Place wires from the desired points in your schematic to the pins on the NI myDAQ right slot section described below:
  - **AI 0+** —Positive input of channel 0.
  - **AI 0-** —Negative input of channel 0.
  - **AI 1+** —Positive input of channel 1.
  - **AI 1-** —Negative input of channel 1.



**Note** These pins are shared with the **Bode Analyzer** and the **Oscilloscope**.

Complete the following steps to access the SFP:

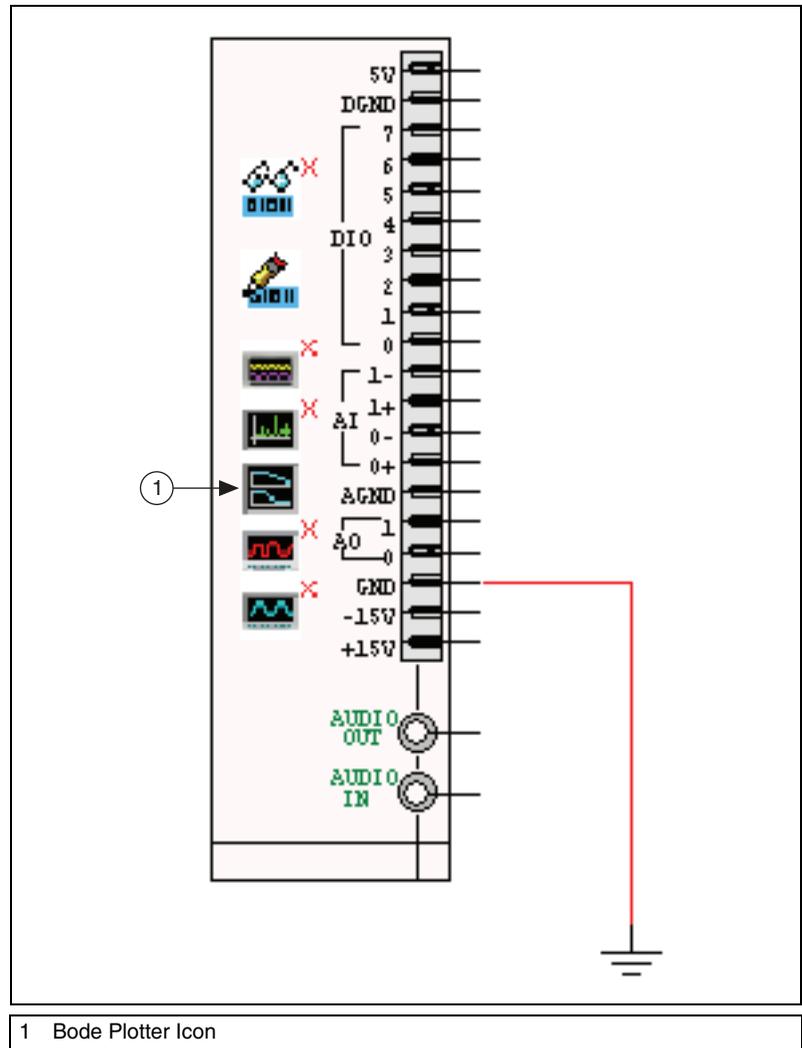
1. Double-click the instrument's icon, shown in the figure above (1). The SFP appears.
2. Change the settings in the SFP as desired.

For information about using this instrument, click the **Help** button on its SFP to display the *NI ELVISmx Help*.

## Bode Analyzer

This instrument measures the gain and phase shift versus frequency for passive or active linear designs.

This instrument's pre-placed icon is located in the NI myDAQ right slot section of the NI myDAQ schematic, as shown in the figure below (1).



Complete the following step to connect the instrument:

1. Place wires from the desired points in your schematic to the pins on the NI myDAQ right slot section described below:
  - **AI 0+** —Positive input of channel 0 (stimulus).
  - **AI 0-** —Negative input of channel 0 (stimulus).
  - **AI 1+** —Positive input of channel 1 (response).
  - **AI 1-** —Negative input of channel 1 (response).



**Note** These pins are shared with the **Oscilloscope** and the **Dynamic Signal Analyzer**.

Complete the following steps to access the SFP:

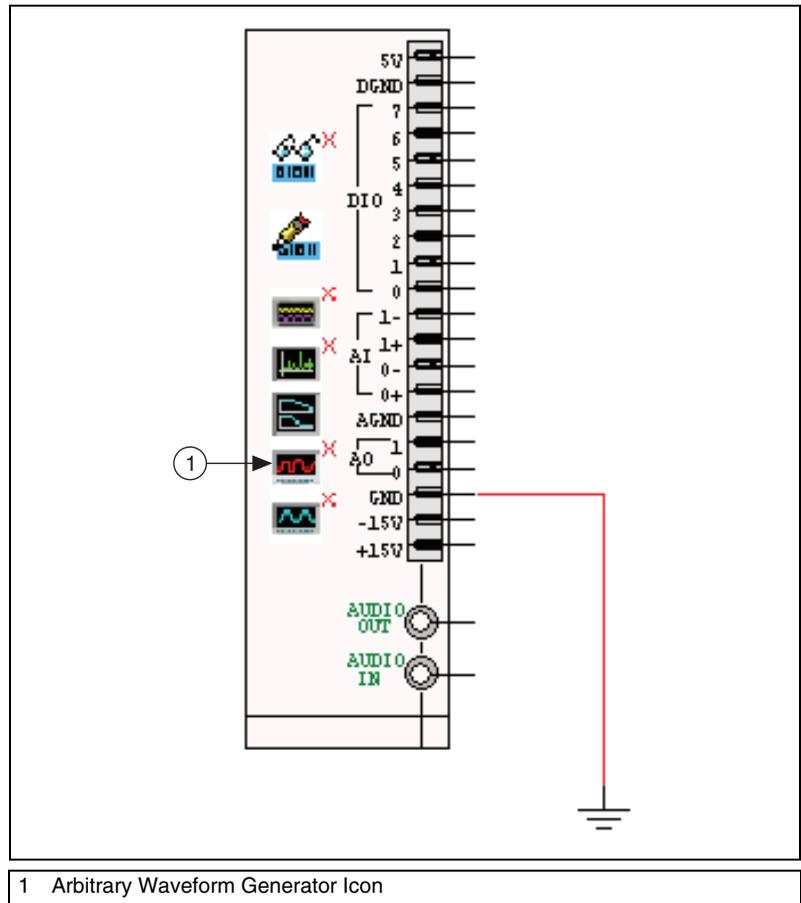
1. Double-click the instrument's icon, shown in the figure above (1). The SFP appears.
2. Change the settings in the SFP as desired.

For information about using this instrument, click the **Help** button on its SFP to display the *NI ELVISmx Help*.

## Arbitrary Waveform Generator

This instrument generates user-specified waveforms.

This instrument's pre-placed icon is located in the NI myDAQ right slot section of the NI myDAQ schematic, as shown in the figure below (1).



Complete the following step to connect the instrument:

1. Place wires from the desired points in your schematic to the pins on the NI myDAQ right slot section described below:
  - **AO 0**—Output pin 0.
  - **AO 1**—Output pin 1.



**Note** These pins are shared with the **Function Generator**, so only one of these instruments can be active at a time.

Complete the following steps to access the SFP:

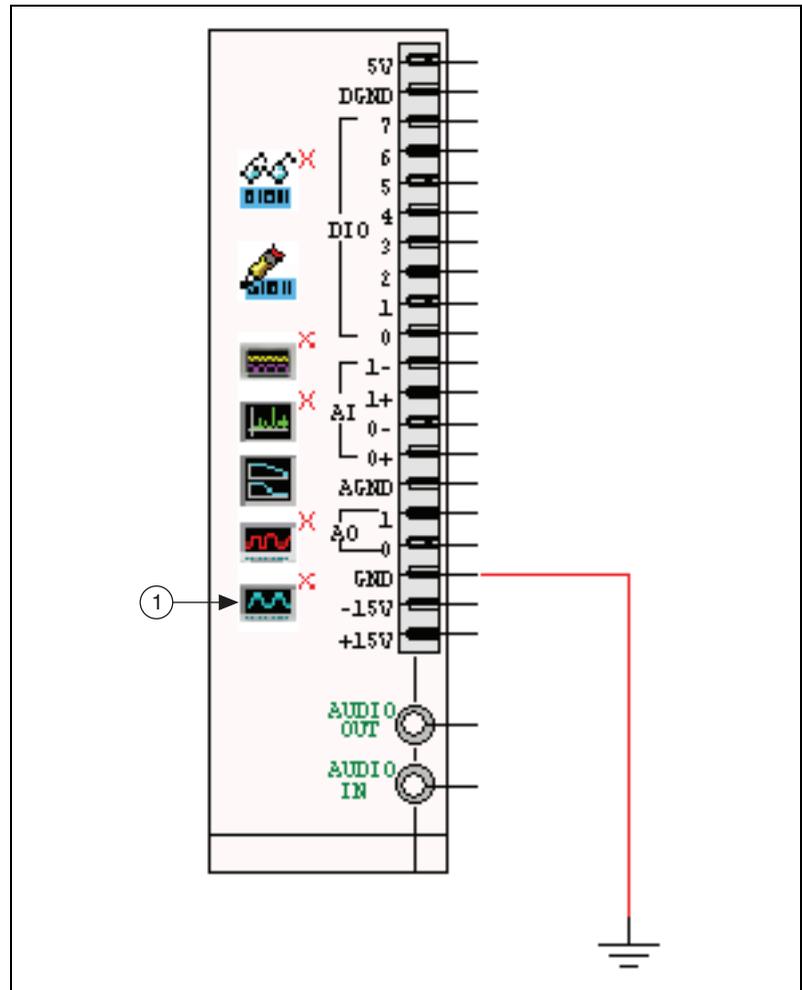
1. Double-click the instrument's icon, shown in the figure above (1). The SFP appears.
2. Change the settings in the SFP as desired.

For information about using this instrument, click the **Help** button on its SFP to display the *NI ELVISmx Help*.

## Function Generator

This instrument generates sine, square or triangle waves.

This instrument's pre-placed icon is located in the NI myDAQ right slot section of the NI myDAQ schematic, as shown in the figure below (1).



1 Function Generator Icon

Complete the following step to connect the instrument:

- Place wires from the desired points in your schematic to the pins on the NI myDAQ right slot section described below:
  - AO 0**—Output pin 0.



**Note** This pin is shared with the **Arbitrary Waveform Generator**, so only one of these instruments can be active at a time.

Complete the following steps to access the SFP:

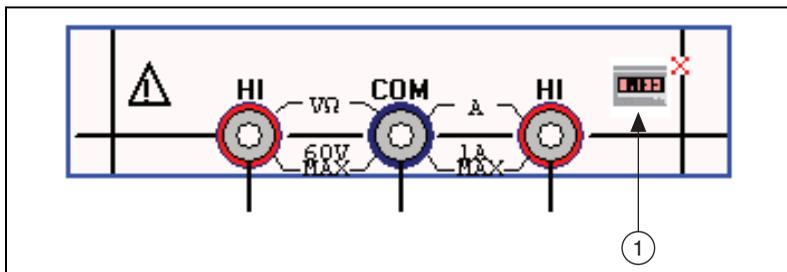
- Double-click the instrument's icon, shown in the figure above (1). The SFP appears.
- Change the settings in the SFP as desired.

For information about using this instrument, click the **Help** button on its SFP to display the *NI ELVISmx Help*.

## Digital Multimeter

This instrument is a digital multimeter (DMM).

This instrument's pre-placed icon is located in the NI myDAQ bottom terminals section of the NI myDAQ schematic, as shown in the figure below (1).



1 Digital Multimeter Icon

Complete the following step to connect the instrument:

- Place wires from the desired points in your schematic to the pins on the NI myDAQ bottom terminals section described below:
  - HI**—Voltmeter and ohmmeter input.
  - COM**—Common input.
  - HI**—Ammeter input.

Complete the following steps to access the SFP:

1. Double-click the instrument's icon, shown in the figure above (1). The SFP appears.
2. Change the settings in the SFP as desired.

For information about using this instrument, click the **Help** button on its SFP to display the *NI ELVISmx Help*.

## Virtual NI myDAQ Designs in the Breadboard View

As with other Multisim designs, you can view a virtual NI myDAQ design in the **Breadboard View**.



**Note** The NI myDAQ bottom terminals that appear at the top of the myDAQ design, and the NI myDAQ right slot that appears at the left of the myDAQ design appear as generic ICs in the **Breadboard View**. These ICs can be placed on the breadboard.

Refer to Chapter 2, *Breadboarding*, for more information.

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# PLD Schematics

The following sections describe how to graphically define the internal structure of a PLD (programmable logic device). They also describe how to export the PLD design to VHDL files or programming files, and how to program a connected PLD.

Some of the described features may not be available in your edition of Multisim. Refer to the *NI Circuit Design Suite Release Notes* for a description of the features available in your edition.

## Overview

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A PLD schematic defines the internal logical behavior of a PLD and the interface to external logical connections. PLD schematics can be exported to VHDL files, a programming file, or used to program a connected PLD (FPGA).

A PLD schematic contains specialized components that define the operation of the individual logic blocks of the PLD.

These PLD components include both SPICE models and VHDL export data. This allows the components to be simulated in Multisim, and then exported with VHDL-only data. Refer to the [Editing a Component's VHDL Export Data](#) section for information about the VHDL export data.



**Note** The PLD components are not compatible with older MultiVHDL components and models. If you have a legacy copy of MultiVHDL, you can continue to use it. However, co-simulation has been discontinued with version 11 of Circuit Design Suite.

Some additional diagnostic components such as digital probes and Multisim instruments can also be placed on a PLD schematic. These components do not change the PLD topology and are not exported when an **Export to PLD** command is executed.

The PLD schematic:

- restricts the components that can be placed to those that can be mapped for VHDL export, and to special diagnostic components.
- has special port connectors that map the external nets to internal signals and identify the signal modes.
- may enable programming of a connected PLD.
- may enable generation and saving of a programming file.
- enables export to VHDL.



**Note** You cannot export a PLD schematic to Ultiboard, or any other PCB layout application. The PLD device in a Multisim schematic has no layout information.

## Components

Only a special category of components are allowed for PLD designs. Valid components include exportable and diagnostic devices. They are located in the **PLD Logic**, **Sources**, **Indicators**, and **Misc** groups of the database.

When a PLD schematic is active, the **Select a Component** dialog box name changes to **Select a Component (PLD Mode)**. Only valid components appear in the dialog.

In the **Select a Component (PLD Mode)** dialog box, **Model manufacturer/ID** displays the SPICE model manufacturer, and **VHDL export manufacturer/Name** displays the source of the VHDL model.

Search functionality from the **Select a Component (PLD Mode)** dialog box additionally allows searching for VHDL export data and only finds valid PLD components. Titles on all search dialogs are appended with **PLD Mode**.

Refer to the *Multisim Help* for more information.

## Port Connectors

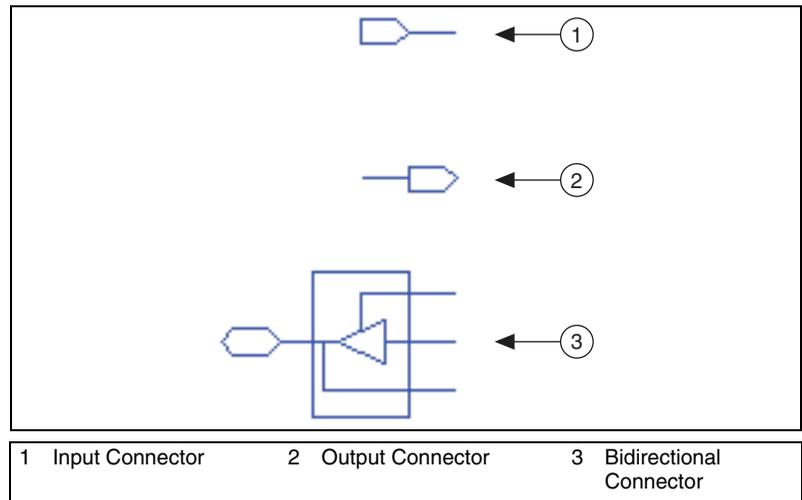
Port connectors represent the FPGA pins that are used by the PLD design. You must define how the logic connects to the device pins by wiring the internal design to the port connectors.

A port connector can be set to input, output, or bidirectional mode. The mode defines the behaviors in simulation and PLD export. Input and output modes allow input or output to the PLD, respectively. The bidirectional mode may act as either an input or output, depending on the state of the

control pin. When the signal on the control pin is high, the connector acts as an output from the PLD. When the signal on the control pin is low, the connector acts as an input to the PLD.

You cannot place global connectors on a PLD schematic. External nets cannot be connected directly to internal PLD schematic nets. They must go through port connectors.

A connector's symbol changes based on its mode, as shown in the figure below.



You can define the connectors before creating your design if you know the properties of the connectors you will use. Multisim will then allow you to select these defined connectors when creating your design. Refer to the [Standard PLD Configuration File](#) and [Port Connectors Tab](#) sections for more information.

This is particularly useful if you know in advance how VHDL signal names will be mapped to pins, for example, if the PLD is on an evaluation board. Unlike undefined connectors, defined connectors retain their properties and can be exported even when not placed on the schematic.

Refer to the [Adding Port Connectors to a PLD Schematic](#) and [Port Connector Dialog Box](#) sections for more information.

## PLD Toolbar

The table below describes the buttons found in the **PLD** toolbar.

Button	Description
	<p><b>Input Connector</b> button. Displays the <b>Input Connector</b> dialog box. Use this to place an input connector on a PLD schematic. Refer to the <a href="#">Adding Port Connectors to a PLD Schematic</a> section for more information.</p>
	<p><b>Output Connector</b> button. Displays the <b>Output Connector</b> dialog box. Use this to place an output connector on a PLD schematic. Refer to the <a href="#">Adding Port Connectors to a PLD Schematic</a> section for more information.</p>
	<p><b>Bidirectional Connector</b> button. Displays the <b>Bidirectional Connector</b> dialog box. Use this to place a bidirectional connector on a PLD schematic. Refer to the <a href="#">Adding Port Connectors to a PLD Schematic</a> section for more information.</p>
	<p><b>PLD Settings</b> button. Displays the <b>PLD Settings</b> dialog box. Refer to the <a href="#">PLD Settings Dialog Box</a> section for more information.</p>
	<p><b>PLD Topology Check</b> button. Runs a topology check on the selected PLD design. Refer to the <a href="#">Running a Topology Check</a> section for more information.</p>
	<p><b>Export to PLD</b> button. Displays the <b>PLD Export</b> dialog box. Refer to the <a href="#">Exporting to PLD</a> section for more information.</p>

## PLD Components Toolbar

The table below describes the buttons found in the **PLD Components** toolbar. Refer to the [Adding Components to a PLD Schematic](#) section for more information.

Button	Description
	<p><b>Place Logic Gate</b> button. Displays the <b>Select a Component (PLD Mode)</b> dialog box with the <b>Logic Gates Family</b> selected. Select the desired logic gate in the <b>Component</b> list and click <b>OK</b> to place it on the PLD schematic.</p>
	<p><b>Place Buffer</b> button. Displays the <b>Select a Component (PLD Mode)</b> dialog box with the <b>Buffers Family</b> selected. Select the desired buffer in the <b>Component</b> list and click <b>OK</b> to place it on the PLD schematic.</p>
	<p><b>Place Latch</b> button. Displays the <b>Select a Component (PLD Mode)</b> dialog box with the <b>Latches Family</b> selected. Select the desired latch in the <b>Component</b> list and click <b>OK</b> to place it on the PLD schematic.</p>
	<p><b>Place Flip-Flop</b> button. Displays the <b>Select a Component (PLD Mode)</b> dialog box with the <b>Flip-Flops Family</b> selected. Select the desired flip-flop in the <b>Component</b> list and click <b>OK</b> to place it on the PLD schematic.</p>
	<p><b>Place Encoder</b> button. Displays the <b>Select a Component (PLD Mode)</b> dialog box with the <b>Encoders Family</b> selected. Select the desired encoder in the <b>Component</b> list and click <b>OK</b> to place it on the PLD schematic.</p>
	<p><b>Place Decoder</b> button. Displays the <b>Select a Component (PLD Mode)</b> dialog box with the <b>Decoders Family</b> selected. Select the desired decoder in the <b>Component</b> list and click <b>OK</b> to place it on the PLD schematic.</p>
	<p><b>Place Counter</b> button. Displays the <b>Select a Component (PLD Mode)</b> dialog box with the <b>Counters Family</b> selected. Select the desired counter in the <b>Component</b> list and click <b>OK</b> to place it on the PLD schematic.</p>

Button	Description
	<p><b>Place Adder</b> button. Displays the <b>Select a Component (PLD Mode)</b> dialog box with the <b>Adders Family</b> selected. Select the desired adder in the <b>Component</b> list and click <b>OK</b> to place it on the PLD schematic.</p>
	<p><b>Place Comparator</b> button. Displays the <b>Select a Component (PLD Mode)</b> dialog box with the <b>Comparators Family</b> selected. Select the desired comparator in the <b>Component</b> list and click <b>OK</b> to place it on the PLD schematic.</p>
	<p><b>Place Multiplexer</b> button. Displays the <b>Select a Component (PLD Mode)</b> dialog box with the <b>Multiplexers Family</b> selected. Select the desired multiplexer in the <b>Component</b> list and click <b>OK</b> to place it on the PLD schematic.</p>
	<p><b>Place Demultiplexer</b> button. Displays the <b>Select a Component (PLD Mode)</b> dialog box with the <b>Demultiplexers Family</b> selected. Select the desired demultiplexer in the <b>Component</b> list and click <b>OK</b> to place it on the PLD schematic.</p>
	<p><b>Place Shift Register</b> button. Displays the <b>Select a Component (PLD Mode)</b> dialog box with the <b>Shift Registers Family</b> selected. Select the desired shift register in the <b>Component</b> list and click <b>OK</b> to place it on the PLD schematic.</p>
	<p><b>Place Generator</b> button. Displays the <b>Select a Component (PLD Mode)</b> dialog box with the <b>Generators Family</b> selected. Select the desired generator in the <b>Component</b> list and click <b>OK</b> to place it on the PLD schematic.</p>

Button	Description
	<p><b>Place Digital Source</b> button. Displays the <b>Select a Component (PLD Mode)</b> dialog box with the <b>Digital Sources Family</b> selected. Select the desired digital source in the <b>Component</b> list and click <b>OK</b> to place it on the PLD schematic.</p>
	<p><b>Place Probe</b> button. Displays the <b>Select a Component (PLD Mode)</b> dialog box with the <b>Probe Family</b> selected. Select the desired probe in the <b>Component</b> list and click <b>OK</b> to place it on the PLD schematic.</p>

## Creating a PLD Schematic

The **New PLD Design** wizard guides you through the steps of creating and configuring the PLD schematic. You can create a PLD schematic as an independent document, as a subcircuit, or as a hierarchical block in a standard schematic.

Complete the following steps to create a new PLD schematic:

1. Select **File»New»PLD design**.

*Or*

Select **Place»New PLD subcircuit**.

*Or*

Select **Place»New PLD hierarchical block**.

Refer to the [Placing PLDs as Subcircuits and Hierarchical Blocks](#) section for more information.

With any of the above actions, step 1 of the **New PLD Design** wizard appears.

2. Select one of the following as desired:
  - **Use standard configuration**—Select one of the following from the drop-down list: **NI Digital Electronics FPGA Board**, **NI Digital Electronics FPGA Board (7 segment)**. Select one of the standard configuration files if you want to use Multisim with the NI Digital Electronics FPGA board. Refer to the [Standard PLD Configuration File](#) section for more information.
  - **Use custom configuration file**—Select if you wish to use a non-standard configuration file that you have created.

- **Create empty PLD**—Select if you wish to create a PLD using saved default settings (will contain no defined connectors), or if you wish to define connectors after creating the schematic.



**Note** When you select a PLD configuration file, Multisim indicates if generating a programming file and programming a PLD will be enabled. This functionality cannot be enabled for a design after the design has been created.

3. Click **Next** to display step 2 of the **New PLD Design** wizard.
4. Complete the following as desired:
  - **PLD design name or PLD subcircuit name or Choose a file name**—Defaults to **Programmable Logic Device 1**, **Programmable Logic Device 2**, and so on. Edit as desired.
  - **PLD part number (optional)**—Defaults to the FPGA named in the configuration file that is referenced in step 1. If there is no referenced configuration file, or the file has no part number named, this field defaults to the last value selected. Edit to specify the part number to show in the **Bill of Materials** report.



**Note** If you picked a PLD configuration file in step 1 of the **New PLD Design** wizard that has programming information that includes a specific device, “(optional)” will not appear in the field name and the field will not be editable.

5. Click **Next** to display step 3 of the **New PLD Design** wizard.  
*Or*  
Click **Finish** to close the **New PLD Design** dialog box and open the new PLD schematic without modifying **Default operating voltages** or changing the defined connectors.
6. If you clicked **Next**, step 3 of the **New PLD Design** wizard displays. Edit the following in the **Default operating voltages** box as desired:
  - **Input connector**—The default operating voltage for all new undefined input connectors in the PLD.
  - **Output connector**—The default operating voltage for all new undefined output connectors in the PLD.
  - **Bidirectional connector**—The default operating voltage for all new undefined bidirectional connectors in the PLD.

7. If you selected either **Use standard configuration** or **Use custom configuration file** in step 1 of the wizard, the **Select the defined connectors to place on the PLD** list also displays in step 3 of the wizard. Use the checkboxes to select which defined connectors to place on the PLD.
8. Click **Finish** to close the **New PLD Design** dialog box and open the new PLD schematic.

## Standard PLD Configuration File

The standard PLD configuration files describe general properties of the PLD on the NI Digital Electronics FPGA Board. Multisim includes two PLD configuration files, which differ only by which port connectors are placed on the schematic by default.

Select **Digital Electronics FPGA Board (7 Segment)** if you will be using the 7 segment displays in your design. Otherwise, select **Digital Electronics FPGA Board**.

Standard PLD configuration files are found in the `pldconfig` folder in the install directory. The standard files are accessed from the **Use standard configuration** drop-down list in step 1 of the **New PLD Design** wizard.

## Subcircuits and Hierarchical Blocks

You can place PLD subcircuits (SCs) and hierarchical blocks (HBs) inside a standard schematic. You can also place them in an existing PLD schematic.



**Note** You cannot place standard SCs or HBs in PLD schematics.

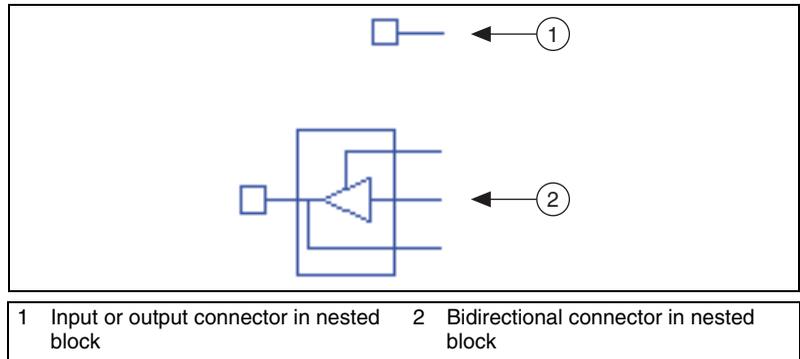
Refer to the figure below for some examples.

1 PLD schematic with no subcircuit or hierarchical block	4 PLD subcircuit in standard schematic
2 Subcircuit in PLD schematic	5 PLD hierarchical block in standard schematic
3 Hierarchical block in PLD schematic	6 Hardware device target



**Tip** Right-click on the hardware device target icon and select **Export to PLD** to display the **PLD Export** wizard. Refer to the [Exporting to PLD](#) section for more information.

Input and output connectors in nested PLD schematics do not graphically indicate their mode. In this case, the connectors have no effect on simulation and export.



## Placing PLDs as Subcircuits and Hierarchical Blocks

You can create hierarchical designs to capture the PLD's logic. Subsheets nested in a PLD do not define additional PLDs. Rather, they define reusable blocks in the PLD.

Refer to the *Multisim Help* for more information about hierarchical blocks and subcircuits.

### Placing a New PLD as a Subcircuit

Complete the following steps to place a new PLD as a subcircuit in a standard schematic:

1. Open a new or existing Multisim design.
2. Select **Place»New PLD subcircuit**. Step 1 of the **New PLD Design** wizard appears.
3. Use the wizard to create the PLD subcircuit, as detailed in the [Creating a PLD Schematic](#) section.

When you click **Finish** in either step 2 or step 3, a ghost image of the PLD appears on the cursor.

4. Click to place the PLD on the workspace.

## Placing a New PLD as a Hierarchical Block

Complete the following steps to place a new PLD as a hierarchical block in a standard schematic:

1. Open a new or existing Multisim design.
2. Select **Place»New PLD hierarchical block**. Step 1 of the **New PLD Design** dialog box appears.
3. Use the wizard to create the PLD subcircuit, as detailed in the *Creating a PLD Schematic* section.

When you click **Finish** in either step 2 or step 3 of the wizard, a ghost image of the PLD appears on the cursor.

4. Click to place the PLD on the workspace.

## Placing a New PLD Subcircuit in a PLD Schematic

Complete the following steps to place a new PLD subcircuit in a PLD schematic:

1. Open a new or existing PLD design.
2. Select **Place»New subcircuit**. The **Subcircuit Name** dialog box appears.
3. Enter a **Subcircuit Name** and click **OK** to place the subcircuit on the PLD schematic.

## Placing a New PLD Hierarchical Block in a PLD Schematic

Complete the following steps to place a new PLD hierarchical block in a PLD schematic:

1. Open a new or existing PLD design.
2. Select **Place»New hierarchical block**. The **Hierarchical Block Properties** dialog box appears.
3. Enter the **File name of hierarchical block**, **Number of input pins**, **Number of output pins**, and click **OK** to place the hierarchical block on the PLD schematic.

## Placing an Existing PLD Schematic as a Hierarchical Block in a PLD Schematic

Complete the following steps to place an existing PLD schematic as a hierarchical block in a PLD schematic:

1. Open a new or existing PLD design.
2. Select **Place»Hierarchical block from file**. A standard **Open** dialog box appears.
3. Select the desired file and click **Open**. A ghost image of the hierarchical block appears on the cursor.



**Note** Only a PLD schematic may be placed in a PLD schematic as a hierarchical block.

4. Click to place it on the workspace.

## Adding Components to a PLD Schematic

Complete the following steps to add a component to a PLD schematic:

1. Open or create a PLD design.
2. Select **Place»Component** to display the **Select a Component (PLD Mode)** dialog box.

The components that display in this dialog are limited to those that can be placed on a PLD schematic.

3. Select the desired **Group**, **Family** and **Component**, and click to place the component on the workspace.

## Adding Port Connectors to a PLD Schematic

Complete the following steps to add an input, output, or bidirectional port connector to a PLD schematic:

1. Select **Place»Connectors»Input connector**.

*Or*

Select **Place»Connectors»Output connector**.

*Or*

Select **Place»Connectors»Bidirectional connector**.



**Note** Refer to the [Standard PLD Configuration File](#) section for information on pre-defined port connectors.

- If port connectors are defined, the associated dialog box appears, otherwise, skip to step 4.

Select one of the following radio buttons:

- **Create defined connector**—This button is active if there are defined connectors that have not been placed. Select one of these connectors from the list below the radio button.
  - **Create default connector**—Select to place a new, undefined connector on the PLD schematic.
- Click **OK** to close the dialog.
  - A ghost image of the connector appears on the cursor.
  - Click in the desired location to place the connector.

## Port Connector Dialog Box

Complete the following steps to change the properties of a placed port connector:

- Double-click on the placed connector to display the **Port Connector** dialog box. The **Value** tab displays.
- Select a new **Name** from the drop-down list. This list displays all available defined reference designators.

*Or*

Type a new value in the **Name** field. The **RefDes** defines the name of the signal in exported VHDL.

- Select one of **Input**, **Output**, or **Bidirectional** from the **Mode** drop-down list.
- Change the **Operating voltage** as desired. This value is used for simulation only. It is not exported to VHDL.



**Note** In simulation, a signal is interpreted as low when the voltage level is less than half of the operating voltage, and high when it is above half of the operating voltage.

- Optionally, click the **Display** tab and select one of:
  - **Use schematic global setting**—Check to use the **Port names** setting in the **Connectors** box in the **Sheet** tab of the **Sheet Properties** dialog box.
  - **Show name**—Check to display the selected connector's name on the workspace. You must uncheck **Use schematic global setting** first.
- Click **OK** to close the dialog box.



**Note** You can set the default values for the operating voltages of all undefined PLD connectors in the **General** tab of the **PLD Settings** dialog box. Refer to the [General Tab](#) section for more information.

## PLD Settings Dialog Box

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Use the **PLD Settings** dialog box to adjust port connector and general settings for your PLD schematic.

### Port Connectors Tab

Complete the following steps to make changes to the port connector settings of a PLD schematic:

1. Select the desired PLD schematic.
2. Select **Options»PLD settings** to display the **PLD Settings** dialog box.
3. Select the **Port connectors** tab. The following columns are for information only, and cannot be edited.
  - **Defined**—A green indicator in this column means that the corresponding port connector is defined for the PLD schematic and retains its settings even when not placed on the schematic. If you place a default connector as described in [Adding Port Connectors to a PLD Schematic](#), the indicator does not appear.
  - **In use**—A green indicator in this column means that the corresponding port connector is on the PLD schematic.
4. Edit the following as desired:
  - **Name**—The name the connector has on the PLD schematic. The **Name** also defines the name of the signal in exported VHDL.
  - **Mode** drop-down list—Select **Input**, **Output**, or **Bidirectional**.
  - **General purpose** checkbox—Select if you wish this connector to be able to assume any mode during placement. This may only be specified for defined connectors.
  - **Operating voltage**—The operating voltage of the connector. This value is used for simulation only. It is not exported to VHDL.
  - **Always export** checkbox—Select to export a connector when an **Export to PLD** command is executed, whether or not it is **In Use**. This may only be specified for defined connectors. Refer to the [Exporting to PLD](#) section for more information.

5. Optionally, in the **Defined connectors** box:
  - **Add** button—Click to display the **Add Defined Connector** dialog box. Refer to the *Add Defined Connector dialog box* section for details.
  - **Delete** button—Click to delete the selected port connector. You cannot delete a connector that is **In Use**.
6. Optionally, in the **In use connectors** box:
  - **Set defined** button—Click to set the selected undefined connector as defined. The green indicator in the **Defined** column appears.



**Tip** When creating a PLD, you can define the port connectors (name and properties) that will be used in your design before creating the design. This is particularly useful if you know in advance how VHDL signal names will be mapped to pins, for example, if the PLD is on an evaluation board. Unlike undefined connectors, defined connectors retain their properties and can be exported even when not placed on the schematic.

- **Set undefined** button—Click to set the selected connector as “undefined”. The green indicator in the **Defined** column disappears. Use this button if you inadvertently set a connector to “defined”.



**Note** The **Set as default** checkbox applies to the **General** tab only. Refer to the *General Tab* section for more information.

## Add Defined Connector dialog box

The **Add Defined Connector** dialog box displays when you click the **Add** button in the **Port connectors** tab of the **PLD Settings** dialog box. Refer to the *Port Connectors Tab* section for more information.

Complete the following steps to add a defined port connector to a PLD design:

1. Select **Options»PLD settings** to display the **PLD Settings** dialog box.
2. Select the **Port connectors** tab.
3. Click **Add**. The **Add Defined Connector** dialog box displays.
4. Set the following as desired:
  - **Name**—Edit as desired.
  - **Mode** drop-down list—Select **Input**, **Output**, or **Bidirectional**.
  - **Operating voltage**—The operating voltage of the connector. This value is used for simulation only. It is not exported to VHDL.

- **General purpose** checkbox—Select to allow the connector to assume any mode. When selected, the connector appears in the **Input Connector**, **Output Connector**, and **Bidirectional Connector** dialog boxes. Refer to the [Adding Port Connectors to a PLD Schematic](#) section for information.
  - **Always export** checkbox—Select to export the connector, even if it is not used in the design.
5. Click **Add**. The new connector appears in the **Port connectors** tab.
  6. Continue adding connectors as described above, or click **Done** to close the **Add Defined Connector** dialog box.

## General Tab

Complete the following steps to make changes to the general settings of a top-level PLD schematic:

1. Select the desired PLD schematic.



**Note** Changes made in the following steps apply only to the top level of the selected PLD schematic. Settings in subsheets such as hierarchical blocks are not changed.

2. Select **Options»PLD settings** to display the **PLD Settings** dialog box.
3. Select the **General** tab.
4. Edit the **PLD part number** to specify the part number shown in the **Bill of Materials**. This is the **PLD part number** selected in step 2 of the **New PLD Design** wizard.



**Note** You cannot edit this if you selected a PLD configuration file that has programming information in step 1 of the **New PLD Design** wizard when you created the PLD design.

5. Set the following in the **Default operating voltages** box as desired:
  - **Input connector**—The default operating voltage of all new undefined input connectors in the PLD schematic.
  - **Output connector**—The default operating voltage of all new undefined output connectors in the PLD schematic.
  - **Bidirectional connector**—The default operating voltage of all new undefined bidirectional connectors in the PLD schematic.

6. Select the following checkboxes in the **Port connectors** box as desired:
  - **Lock port connector names**—Select to display a warning when you attempt to rename a port connector.
  - **Unconnected port connectors generate warning in topology check**—Refer to the [Running a Topology Check](#) section for more information.
  - **Unconnected output pins generate warning in topology check**—Refer to the [Running a Topology Check](#) section for more information.
  - **Export unconnected port connectors**—Placed, unconnected port connectors will be exported when an **Export to PLD** command is executed.
  - **Export unplaced defined port connectors**—Select to export port connectors that are defined in the PLD schematic file, but have not been placed on the PLD schematic.
  - **Export port connector buffers automatically**—Select to connect buffers from all input and output connectors to the internal PLD design logic when an **Export to PLD** command is executed. This prevents some errors from occurring when you synthesize the exported VHDL.



**Note** Refer to the [Exporting to PLD](#) section for more information.

7. Set the following in the **Advanced** box as desired:
  - **Source library**—Component export data is added to the source library. This must be the name of the source library (normally **work**) in your VHDL synthesizer where you will add the exported VHDL file.
8. Optionally, select the **Set as default** checkbox.
 

This checkbox applies to the **General** tab only. If you specified a PLD configuration file when you created the PLD schematic, this file may have operating voltages and port connector names locked. When creating a new PLD using a configuration file that defines these, the values in the configuration file take precedence. These settings take precedence over the selection made in the **General** tab of the **PLD Settings** dialog box.

# Exporting to PLD

---

After you have completed your design, you can export the PLD device for use in another application.

When you select **Transfer»Export to PLD**, one of two dialog boxes displays:

- **PLD Export** wizard—The configuration file used in step 1 of the **New PLD Design** wizard must have hardware device target information defined for this dialog box to display. Refer to the *PLD Export Dialog Box* section for details.

This selection uses Xilinx tools which you must obtain and install separately. Only Xilinx devices are supported to compile, synthesize, and program from within Multisim.

Multisim supports Xilinx 10.1 SP3 or later, as well as versions 12.x and 13.x.

National Instruments supports the Xilinx Spartan 3E FPGA on the NI Digital Electronics FPGA board.



**Note** Refer to the *Enabling Programming for Unsupported PLDs* section for information on how to create custom configuration files to enable programming a Xilinx hardware device target.

- **Export PLD to VHDL** dialog box—If the configuration file used in step 1 of the **New PLD Design** wizard did not have hardware device target information defined, or if no configuration file was used, this dialog box displays. Refer to the *Export PLD to VHDL Dialog Box* section for details.

## PLD Export Dialog Box

If the configuration file used in step 1 of the **New PLD Design** wizard defined hardware device target information, use the following procedures to export the PLD design. Otherwise, refer to the *Export PLD to VHDL Dialog Box* section for instructions.

- *Programming a Connected PLD Device*—Follow these instructions if you want to program a PLD and the PLD device is connected to your computer.
- *Generating a PLD Programming File*—Follow these instructions if you want to program a PLD and the PLD device is not connected to your computer, or if you want to program a PLD at a later time. You

must use Xilinx iMPACT to load the exported programming file onto the PLD.

- **Generating VHDL Files**—Follow these instructions if you want to directly use third party tools for synthesis/simulation or you want to view the generated VHDL.

## Programming a Connected PLD Device

Complete the following steps to program a PLD device that is connected to your computer.



**Note** National Instruments supports the Xilinx Spartan 3E FPGA on the NI Digital Electronics FPGA board.



**Note** If you wish to program a PLD using a PLD design that was created in Multisim 11.0, you must recreate the design in Multisim 11.0.1 or higher, using a standard configuration file from the **New PLD Design** wizard. Otherwise, the **Export PLD to VHDL** dialog box appears when you select **Transfer»Export to PLD**. Refer to the [Export PLD to VHDL Dialog Box](#) section for more information.

1. Select **Transfer»Export to PLD** to run a **Topology Check** and display step 1 of the **PLD Export** wizard.

Results of the **Topology Check** appear in the **Results** tab of the **Spreadsheet View**. You can also manually run a **Topology Check** at any time. Refer to the [Running a Topology Check](#) section for information.

Correct any errors before proceeding.

We recommend that you also fix any warnings.

2. Select **Program the connected PLD**. You must connect the required hardware device target to your computer, otherwise an error message will display when you click **Finish** to begin the programming process.
3. Optionally, select the **Save generated programming file** checkbox to save the generated programming file for later use in Xilinx iMPACT.
4. Click **Next** to display step 2 of the **PLD Export** wizard.
5. Complete the following as required:
  - **Xilinx tool**—Select one of:
    - **Xilinx ISE Design Suite 13.1 32-bit**—This will change depending on your installed version of Xilinx.
    - **Automatically detect tool**—Select to automatically search your computer for installed Xilinx tools. If more than

one version is found, the **Automatically Detect Tool** dialog box displays. Use this dialog box to select one of the found versions of the Xilinx tool.



**Note** Any non-supported versions of the Xilinx tool that are installed will also be detected, and listed as unsupported. Multisim supports Xilinx 10.1 SP3 or later, as well as versions 12.x and 13.x.

- **Manually select tool**—Displays a file browser where you navigate to the installation directory of the desired version of the Xilinx tool.
- **Programming file**—This only appears if you selected **Save generated programming file** in the previous step. You can type the file path and name, or click **Browse** to navigate to a different location.
- **PLD part number** drop-down list—Select the PLD from the drop-down list. The contents of this list come from the PLD configuration file that you used to set up your PLD design.
- **Refresh** button—Click to determine the **Device status** if **Not checked** is displayed. If **Not detected** displays, be sure that the device is connected before proceeding.



**Note** If this button is greyed-out, Xilinx tools are not installed/found.

- **Advanced settings** table—Select a row in table to see a description appear. Exercise caution when making changes.
6. Click **Finish**. A **PLD Export** dialog box displays the status of the steps involved in the process. For example, *Step 7 of 11: Map*.

More detailed messages, warnings, and any errors appear in the **Results** tab as the selected Xilinx tool programs the connected PLD. These messages are supplied from the Xilinx tool. For information about these, refer to the Xilinx help.

At the same time, an indicator consisting of moving zeroes and ones appears below the hardware device target icon in the **Design Toolbox**.

If you cancel the PLD export, this indicator continues to move until the current step is fully terminated.

If you click **Hide**, the **PLD Export** dialog box disappears, but the indicator continues to move until the export completes. To show the **PLD Export** dialog box again, select **Transfer»View export progress**.

To cancel the PLD export, select **Transfer»Cancel export**.

## Generating a PLD Programming File

Complete the following steps to generate a programming file from a PLD design:



**Note** If you wish to generate a PLD programming file using a PLD design that was created in Multisim 11.0, you must recreate the design in Multisim 11.0.1 or higher, using a standard configuration file from the **New PLD Design** wizard. Otherwise, the **Export PLD to VHDL** dialog box appears when you select **Transfer»Export to PLD**. Refer to the [Export PLD to VHDL Dialog Box](#) section for more information.

1. Select **Transfer»Export to PLD** to run a **Topology Check** and display step 1 of the **PLD Export** wizard.

Results of the **Topology Check** appear in the **Results** tab of the **Spreadsheet View**. You can also manually run a **Topology Check** at any time. Refer to the [Running a Topology Check](#) section for information.

Correct any errors before proceeding.

We recommend that you also fix any warnings.

2. Select **Generate and save programming file**.
3. Click **Next** to display step 2 of the **PLD Export** wizard.
4. Complete the following as required:
  - **Xilinx tool**—Select one of:
    - **Xilinx ISE Design Suite 13.1 32-bit**—This will change depending on your installed version of Xilinx.
    - **Automatically detect tool**—Select to automatically search your computer for installed Xilinx tools. If more than one version is found, the **Automatically Detect Tool** dialog box displays. Use this dialog box to select one of the found versions of the Xilinx tool.



**Note** Any non-supported versions of the Xilinx tool that are installed will also be detected, and listed as unsupported. Multisim supports Xilinx 10.1 SP3 or later, as well as versions 12.x and 13.x.

- **Manually select tool**—Displays a file browser where you navigate to the desired version of the Xilinx tool.
- **Programming file**—You can type a file path and name, or click **Browse** to navigate to a different location.

- **PLD part number** drop-down list—Select the PLD part from the drop-down list.
  - **Advanced settings** table—Select a row in the table to see a description appear. Exercise caution when making changes.
5. Click **Finish**. A **PLD Export** dialog box displays the status of the steps involved in the process. For example, *Step 3 of 9: Check syntax*.

More detailed messages, warnings, and any errors appear in the **Results** tab as the Xilinx tool generates and saves the programming file. These messages are supplied from the selected Xilinx tool. For information about these, refer to the Xilinx help.

At the same time, an indicator consisting of moving zeroes and ones appears below the hardware device target icon in the **Design Toolbox**.

If you cancel the PLD export, this indicator continues to move until the current step is fully terminated.

If you click **Hide**, the **PLD Export** dialog box disappears, but the indicator continues to move until the export completes. To show the **PLD Export** dialog box again, select **Transfer»View export progress**.

To cancel the PLD export, select **Transfer»Cancel export**.

## Generating VHDL Files

Complete the following steps to generate VHDL files from a PLD design that conform to IEEE VHDL specification Std 1076-2002:

1. Select **Transfer»Export to PLD** to run a **Topology Check** and display step 1 of the **PLD Export** wizard.

Results of the **Topology Check** appear in the **Results** tab of the **Spreadsheet View**. You can also manually run a **Topology Check** at any time. Refer to the *Running a Topology Check* section for information.

Correct any errors before proceeding.

We recommend that you also fix any warnings.

2. Select **Generate and save VHDL** files.
3. Click **Next** to display step 2 of the **PLD Export** wizard.
4. Optionally, type a new file path and file name in the **Top level module file** field, or click **Browse** and navigate to the desired location for the design file.

This file contains the topology of the PLD schematic.



**Note** If port connector names are not locked, Multisim prompts you to lock them. Port connectors are locked by default if you use one of the standard PLD configurations.

5. Select the **Customize package file name** checkbox if you wish to enter your own file path and file name for the package file. Type a new file path and file name in the **Package file** field, or click **Browse** and navigate to the desired location.

*Or*

Deselect the **Customize package file name** checkbox if you wish to automatically generate a name for the package file on export.

The package file contains definitions of all components in the PLD schematic.



**Tip** Right-click in the active **Top level module file** or **Package file** field and select **Show on Disk** to go to where the generated files will be placed.

6. Click **Finish**. Multisim exports two VHDL files—a top level module file and a package file.

The top level module file (for example, `ProgrammableLogicDevice1.vhd`) defines the top level for the design. The package file contains the component definitions for the PLD device. By default, these files are saved to the same directory as the Multisim design.

The package file (for example, `ProgrammableLogicDevice1_pkg.vhd`) is assumed to be in the library **work**—the default library for most synthesizers. If this is incorrect, you can change it in the **PLD Settings** dialog box. You can specify VHDL export options in the **General** tab. Refer to the [General Tab](#) section for details.

Multisim uses the port connector names to generate top-level signal names. To prevent conflicts, and to ensure valid VHDL code, the signal and entity names in the exported files may not always match the names in the design. For example, a net may have the name `1`, which is not valid in VHDL. It is renamed to a similar but valid name, for example, `\1\`.

## Export PLD to VHDL Dialog Box

If the configuration file used in step 1 of the **New PLD Design** wizard did not define hardware device target information, or if no configuration file was used, use this procedure to export the PLD design to VHDL.

Otherwise, refer to the [PLD Export Dialog Box](#) section for instructions.

You may export VHDL to use with any FPGA. The generated VHDL files conform to IEEE VHDL specification Std 1076-2002.

Complete the following steps to export the PLD design to VHDL:

1. Select **Transfer»Export to PLD** to run a **Topology Check** and display the **Export PLD to VHDL** dialog box.

Results of the **Topology Check** appear in the **Results** tab of the **Spreadsheet View**. You can also manually run a **Topology Check** at any time. Refer to the *Running a Topology Check* section for information.

2. Optionally, type a new file path and file name in the **Top level module file** field, or click **Browse** and navigate to the desired location for the design file.

This file contains the topology of the PLD schematic.



**Note** If port connector names are not locked, Multisim prompts you to lock them.

3. Select the **Customize package file name** checkbox if you wish to enter your own file path and file name for the package file. Type a new file path and file name in the **Package file** field, or click **Browse** and navigate to the desired location.

*Or*

Deselect the **Customize package file name** checkbox if you wish to automatically generate a name for the package file on export.

The package file contains definitions of all components in the PLD schematic.



**Tip** Right-click in the active **Top level module file** or **Package file** field and select **Show on Disk** to go to where the generated files will be placed.

4. Click **OK** to export. Multisim exports two VHDL files—a design file and a package file.

The top level module file (for example, `ProgrammableLogicDevice1.vhd`) defines the top level for the design. The package file contains the component definitions for the PLD device. By default, these files are saved to the same directory as the Multisim design.

The package file (for example, `ProgrammableLogicDevice1_pkg.vhd`) is assumed to be in the library **work**—the default library for most synthesizers. If this is

incorrect, you can change it in the **PLD Settings** dialog box. You can specify VHDL export options in the **General** tab. Refer to the *General Tab* section for details.

Multisim uses the port connector names to generate top-level signal names. To prevent conflicts, and to ensure valid VHDL code, the signal and entity names in the exported files may not always match the names in the design. For example, a net may have the name 1, which is not valid in VHDL. It is renamed to a similar but valid name, for example, \1\.

## Running a Topology Check

A **Topology Check** identifies errors and warnings in a PLD design.

Errors verify that:

- there is at least one used port connector in the design.
- port connectors are not directly connected to another port connector.

Warnings:

- verify that all pins on a PLD component are connected to other PLD components or to a port connector. Unconnected pins are marked open in the VHDL netlist.
- check for unconnected port connectors. To disable this warning, uncheck **Unconnected port connectors generate warning in topology check** in the **General** tab of the **PLD Settings dialog** box.
- check for unconnected output pins. To disable this warning, uncheck **Unconnected output pins generate warning in topology check** in the **General** tab of the **PLD Settings dialog** box.
- identify components that are not exportable such as diagnostic components.
- check that all nets have at least one input and one output pin.

Complete the following steps to run a manual **Topology Check**:

1. Select **Tools»PLD topology check**.

Any errors and warnings display in the **Results** tab of the **Spreadsheet View** with appropriate descriptive text.

2. Right-click on an error or warning and select **Go to** from the context menu that appears. Depending on the error, the source of the selected error or warning may be highlighted on the workspace.

## Editing a Component's VHDL Export Data

Each PLD component includes VHDL export data as well as a standard SPICE model.

You can edit the VHDL export data from the **VHDL export** tab of the **Component Properties** dialog box. This tab is only available for PLD components.



**Note** PLD components do not have footprints or electronic parameters. Consequently, the **Footprint** and **Electronic param** tabs in the **Component Properties** dialog box do not display for PLD components. Refer to the *Multisim Help* for more information about the **Component Properties** dialog box.

Complete the following steps to display a placed component's export properties:

1. Double-click on the placed component to display its properties dialog box.
2. Click the **Value** tab.
3. Click **Edit component in DB**. The **Component Properties** dialog box appears.
4. Click the **VHDL export** tab. The following appear in this tab:
  - **VHDL export name** area—Displays the VHDL export models associated with the selected component. This field cannot be edited directly. Use **Add/Edit** or **Delete export data** if you wish to modify the contents of this field.
  - **VHDL export data** area—Displays the VHDL export model data of the selected component. This field cannot be edited directly. Its contents change based on the selection in the **VHDL export name** area.
  - **Symbol pins** column—Found in the **Pin mapping table**. Displays the names of the pins associated with the symbol.
  - **VHDL export ports** column—Found in the **Pin mapping table**. Use to map the component's **Symbol pins** to its **VHDL export ports**. Edit with care.
  - **Add from comp** button—Click to select a component, whose VHDL export model you wish to use, from the existing Multisim database.
  - **Add/Edit** button—Use to add or edit a new or existing VHDL export model in the Multisim database.

- **Delete export data** button—Clears the contents of the tab.
- **Show template** button—Use to display the **Symbol to port mapping table**. Edit with care.

## Enabling Programming for Unsupported PLDs

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National Instruments supports the Xilinx Spartan 3E FPGA on the NI Digital Electronics FPGA Board. If you select one of the supplied PLD configuration files when creating the PLD design, you can generate a programming file for this FPGA or directly program the connected board.

However, you can create a custom PLD configuration file to enable programming of additional FPGAs. Note that National Instruments does not support additional FPGAs.

By creating a custom PLD configuration file, you can enable generation of a programming file and programming of a connected PLD for unsupported PLDs. Though unsupported, you can expect this functionality to work for unsupported PLDs if the device is a Xilinx FPGA, and it can be compiled and synthesized with 32 bit Xilinx ISE Design Suite 10.1 SP3 or later, Xilinx ISE Design Suite 12.x, or Xilinx ISE Design Suite 13.x.

### Custom PLD Configuration Files

PLD configuration files describe general properties of a PLD and the connections you can make to the PLD. PLD configuration files may also contain information on how to generate a programming file and program a connected PLD.

Files with the extension `.mspc` are Multisim PLD configuration files. To create a new PLD configuration file, you can:

- create a PLD schematic with the desired PLD connectors, and export it as a PLD configuration file. From PLD design, select **Transfer»Export to PLD configuration**.
- create the PLD configuration in another application and save the file with a `.mspc` extension. Refer to the [Creating a Custom PLD Configuration File in Another Application](#) section for more information.

Once you have created a custom PLD configuration file, you can select it in the **Use custom configuration file** field in step 1 of the **New PLD Design** wizard. Refer to the [Creating a PLD Schematic](#) section for more information.

Alternatively, you can add the custom PLD configuration file to the same directory as the standard PLD configuration files. These files become available in the **Use standard configuration** drop-down list. Refer to the [Standard PLD Configuration File](#) and [Creating a PLD Schematic](#) sections for more information.

## Creating a Custom PLD Configuration File in Another Application

You can create a custom PLD configuration file in another application. This is useful if you need to change information that cannot be set in the Multisim user interface. For example, to enable generating a programming file and programming a connected PLD other than the NI Digital Electronics FPGA Board.

PLD configuration files use an XML format. The format is documented in `PLDConfigurationSchema.xsd`, which is found in the `pldconfig` folder in the install directory.

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# Ladder Diagrams

This chapter describes Multisim's ladder diagram functionality.

Some of the described features may not be available in your edition of Multisim. Refer to the *NI Circuit Design Suite Release Notes* for a description of the features available in your edition.

## Overview

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You can use the Education edition of Multisim to create and simulate **Ladder Diagrams**. These diagrams are electrically based, as opposed to the binary/digital representations employed by ladder *logic*. Diagrams of this type are used extensively for industrial motor control designs.

**Ladder Diagrams** are able to drive output devices or take input data from regular schematics and embed the instructions on how input states affect output states. This can be done in either the same schematic or separate hierarchical blocks or subcircuits that contain the **Ladder Diagram**.



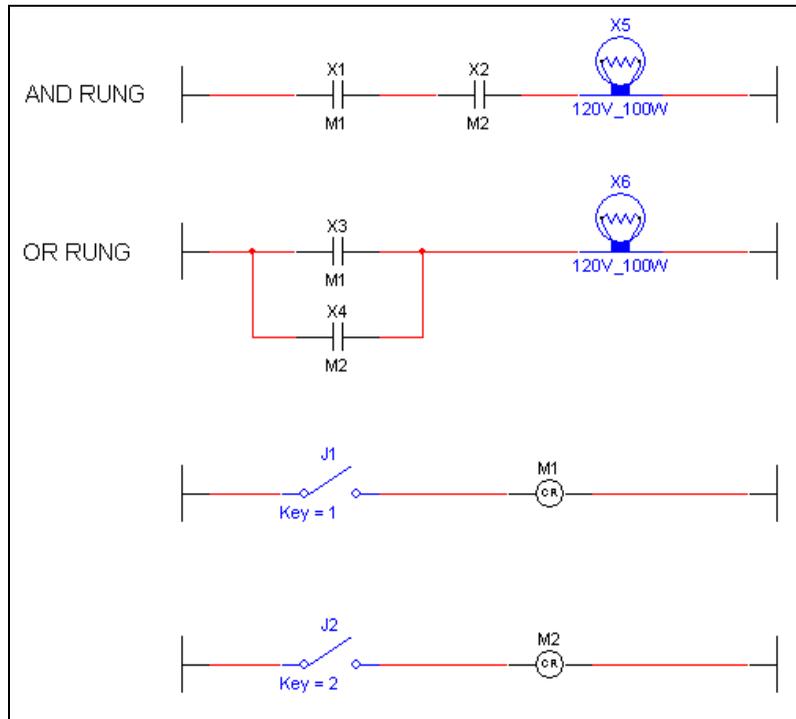
**Note** Refer to the *Multisim Help* for a complete description of hierarchical blocks and subcircuits.

## Creating a Ladder Diagram

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This section describes the steps required to make a simple **Ladder Diagram**. You should understand the concepts described here before reviewing the more complex designs found in this chapter.

This section describes how to build the **Ladder Diagram** that is used in the *AND Rungs and OR Rungs* section.



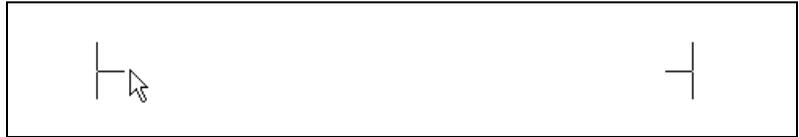
Notes about the above design:

- The relays (X1-X4) are normally open relays. When their controlling coils (M1 or M2) are energized they close. The controlling coils are set in the **Value** tab of each relay's properties dialog box.
- Both X1 AND X2 must be closed for the lamp in the AND rung (X5) to light up.
- Either X3 OR X4 must be closed for the lamp in the OR rung (X6) to light up.
- Coil M1 controls the relays with M1 as their reference. (X1 and X3).
- Coil M2 controls the relays with M2 as their reference. (X2 and X4).
- Use keys 1 and 2 on your keyboard to open and close switches J1 and J2, or hover your cursor over the desired switch and click on the button that appears.

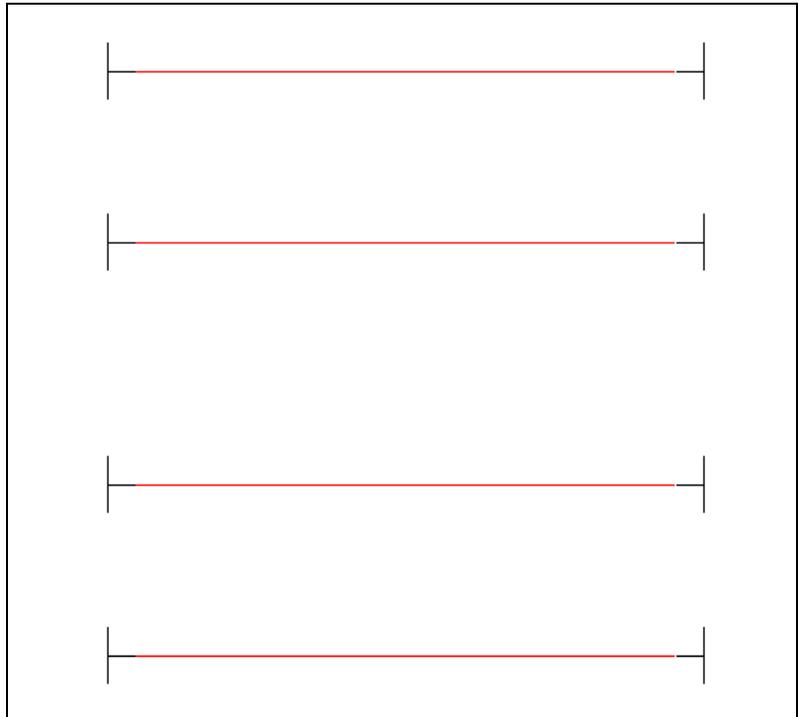
Complete the following steps to add the diagram's rungs:



1. Select **Place»Ladder rungs**. The cursor appears with the rung's left and right terminators attached.



2. Click to place the first rung and continue clicking and placing until you have placed four rungs as shown below. Right-click to stop placing rungs.



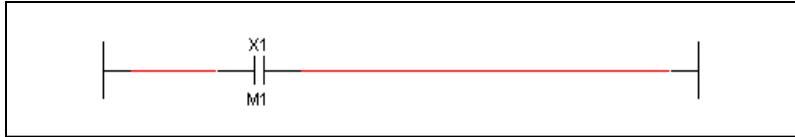
Complete the following steps to add components to the rungs:

1. Select **Place»Component**, navigate to the Normally Open Relay Contact (**RELAY\_CONTACT\_NO**) and click **OK**.

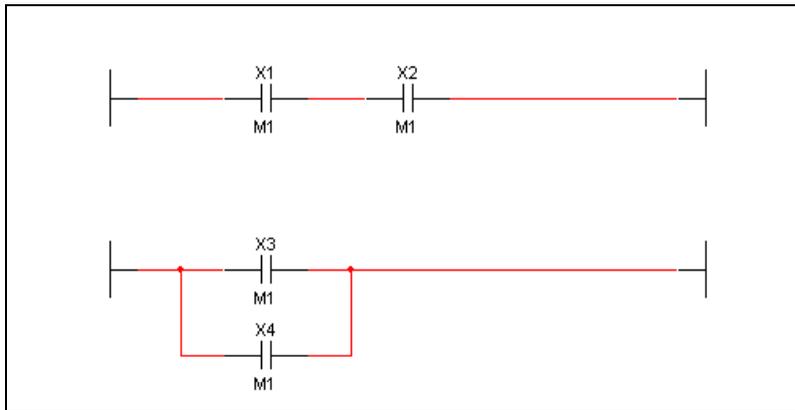


**Note** This device is found in the **Ladder Diagrams Group, Ladder Contacts Family**.

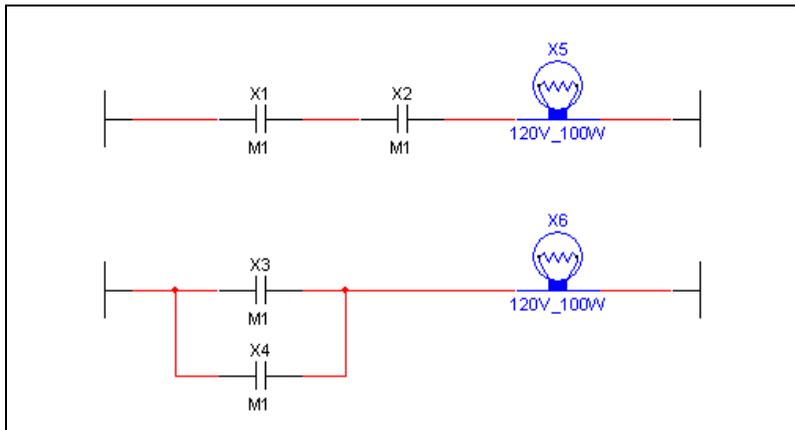
- Drop the relay contact directly onto the first rung.



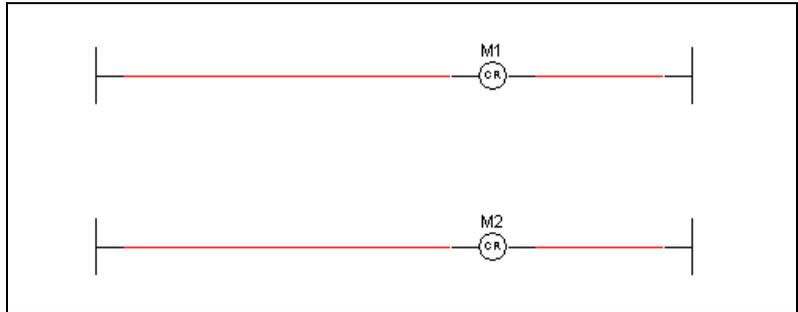
- Continue in this manner until all relay contacts have been placed. (X4 must be placed and then wired separately).



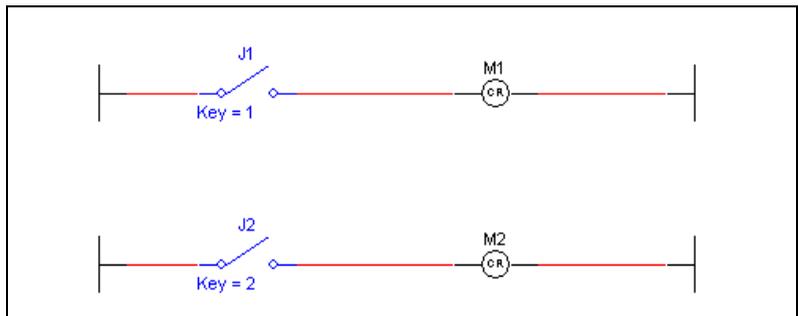
- Place the lamps (**Group-Indicators, Family-Lamp**).



- Place relay coils M1 and M2 on the third and fourth rungs (Group-Ladder Diagrams, Family-Ladder Relay Coils).



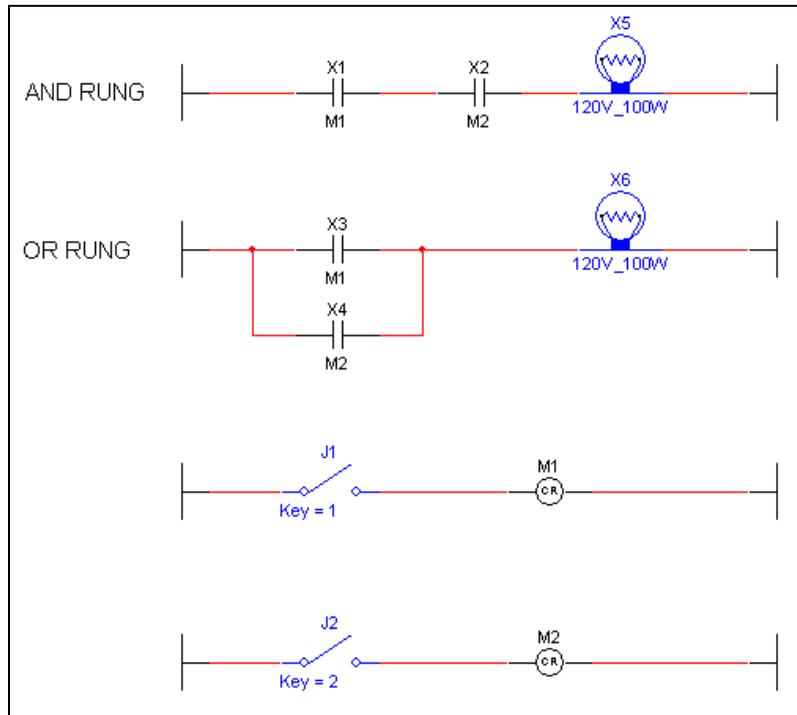
- Place switches J1 and J2.
- Double-click on each switch, select the **Value** tab, and change the **Key for toggle** for J1 to 1 and the **Key for toggle** for J2 to 2.



Complete the following steps to change the controlling device reference for X2 and X4:

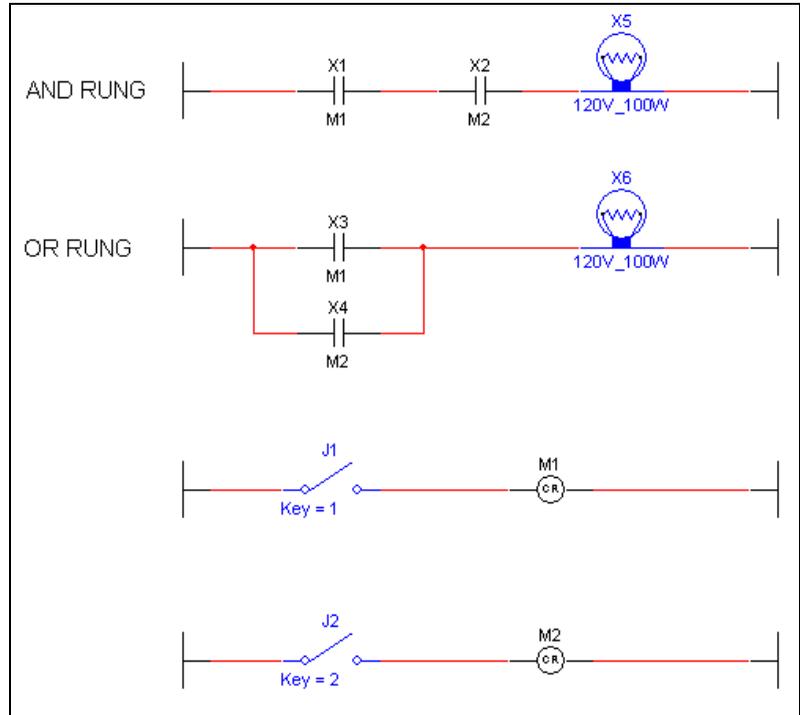
1. Double-click on X2 and click the **Value** tab.
2. Enter M2 in the **Coil Reference** field and click **OK**.

Repeat for X4. The completed **Ladder Diagram** appears as shown below.



# AND Rungs and OR Rungs

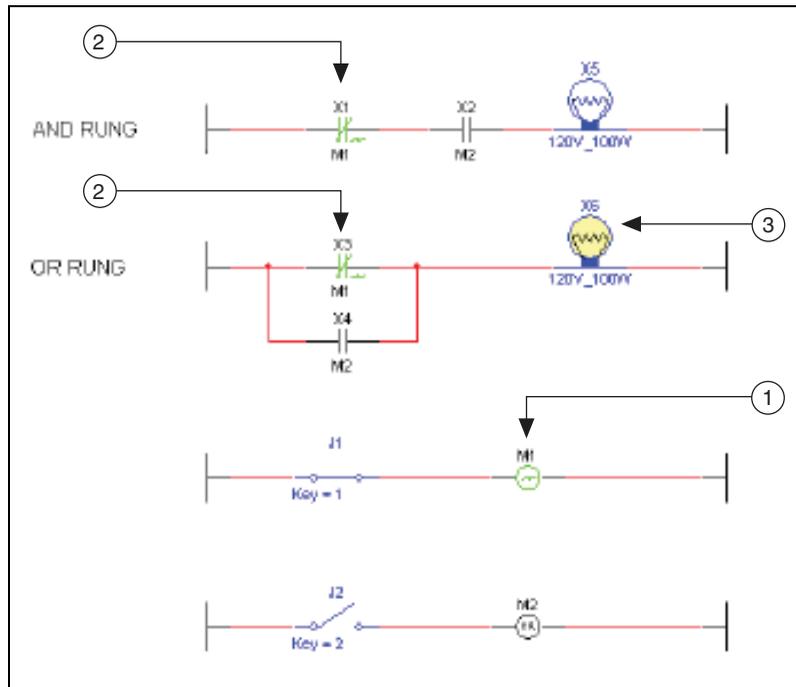
This section illustrates the difference between AND rungs and OR rungs that are found in **Ladder Diagrams**. You should understand the concepts described here before reviewing the more complex designs found in this chapter.



Complete the following steps to activate the lamp in the OR rung:

1. Select **Simulate»Run** to start simulation of the design.
2. Press 1 on your keyboard to close J1 (or hover your cursor over J1 and click the button that appears).

As shown in the figure below, pressing 1, closes J1 which activates coil M1 (1). All relays with M1 as their reference are energized (2). X6 lights because only X3 or X4 need to be energized to complete the circuit (3).



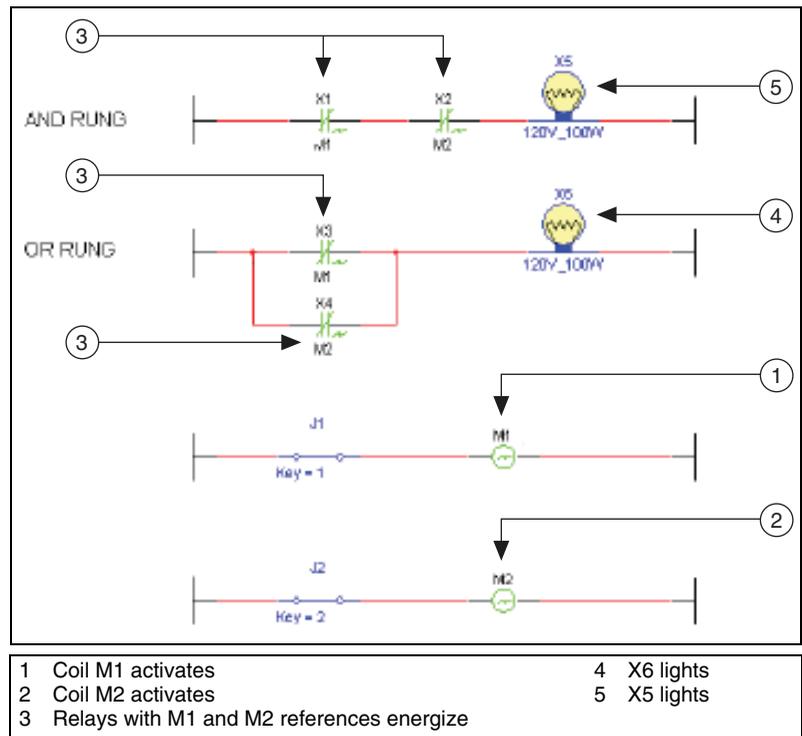
- |                                    |             |
|------------------------------------|-------------|
| 1 Coil M1 activates                | 3 X6 lights |
| 2 Coils with M1 reference energize |             |

If you press 2 on your keyboard (or hover your cursor over J2 and click the button that appears), J2 closes which activates coil M2. X6 lights because X4 is energized.

Complete the following steps to activate the lamp in the AND rung:

1. Select **Simulate»Run** to start simulation of the design.
2. Press 1 and 2 on your keyboard to close J1 and J2.

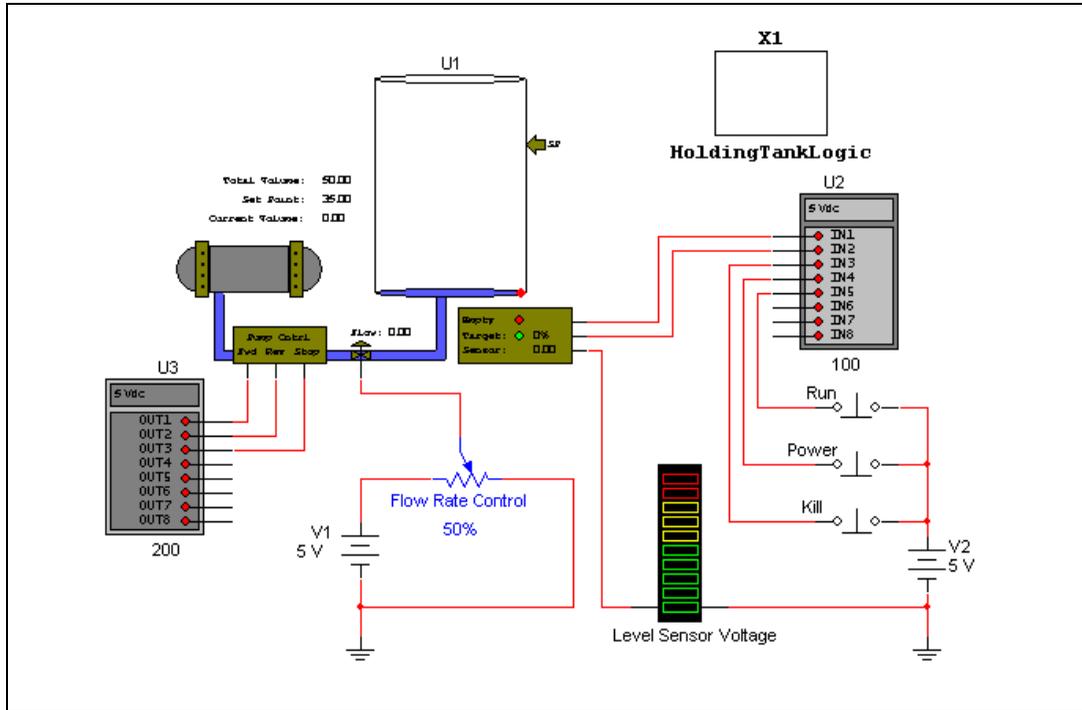
As shown in the figure below, pressing 1, closes J1 which activates coil M1 (1). Pressing 2 closes J2 which activates coil M2 (2). All relays with M1 and M2 as their references are energized (3). X6 lights because X3 OR X4 is energized and the circuit is complete (4). X5 lights because X1 AND X2 are energized and the circuit is complete (5).

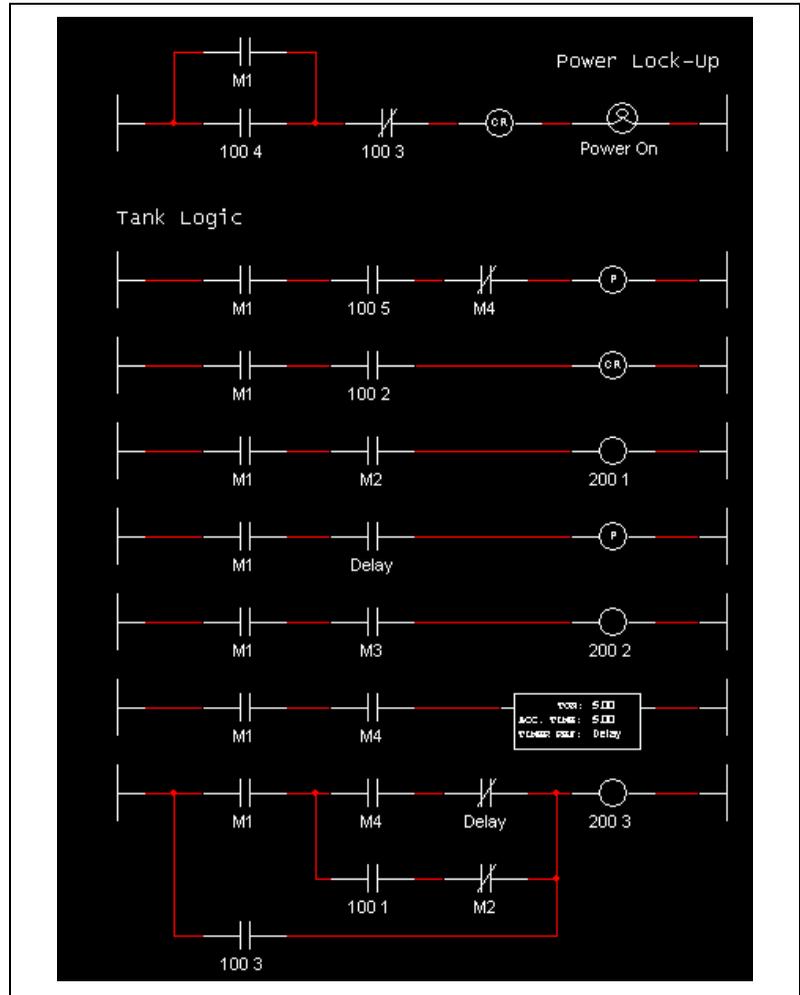


# Sample Designs

## Holding Tank

This section contains an example of a logic diagram that drives a design that fills and then empties a fluid holding tank.



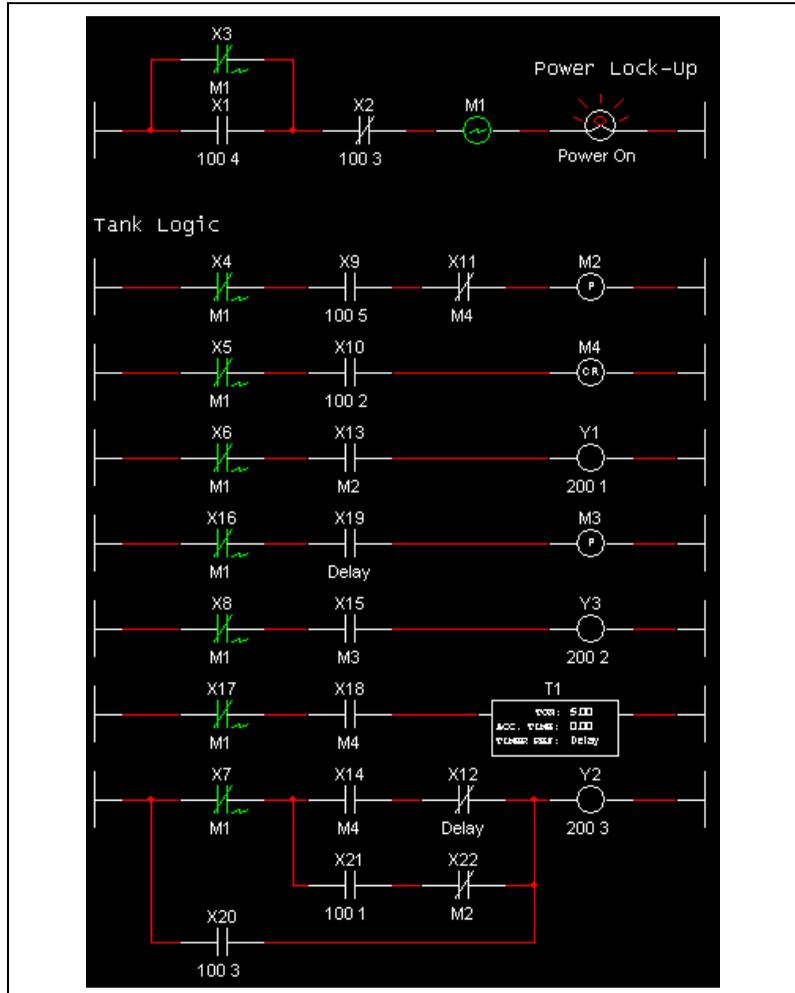


**Note** The Ladder Diagram is contained in a separate Hierarchical Block called HoldingTankLogic. For details on hierarchical blocks, refer to the *Multisim Help*.

Complete the following steps to activate this design:

1. Select **Simulate»Run** to begin simulation.
2. Press P on your keyboard to activate the Power temporary switch (or hover your cursor over the Power switch and click the button that appears). This sends 5 V to pin IN4 of Input Module U2 (**Input Module Base Address = 100**) which in turn energizes Input Contact X1 in the Power Lock-up Rung of the ladder diagram. Relay Coil M1

is energized, causing all Relay Contacts with **Relay Device Reference = M1** to energize.



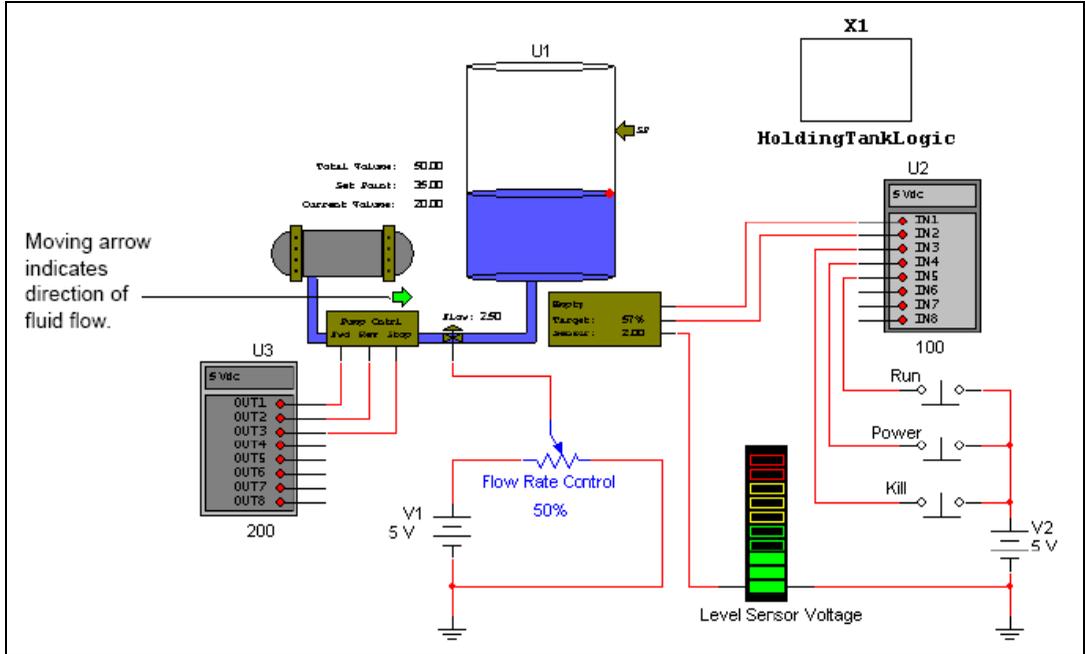
Complete the following steps to run the holding tank design:

1. Activate the design as described above.
2. Press R on your keyboard (or hover your cursor over the Run switch and click the button that appears) to activate the Run temporary switch.

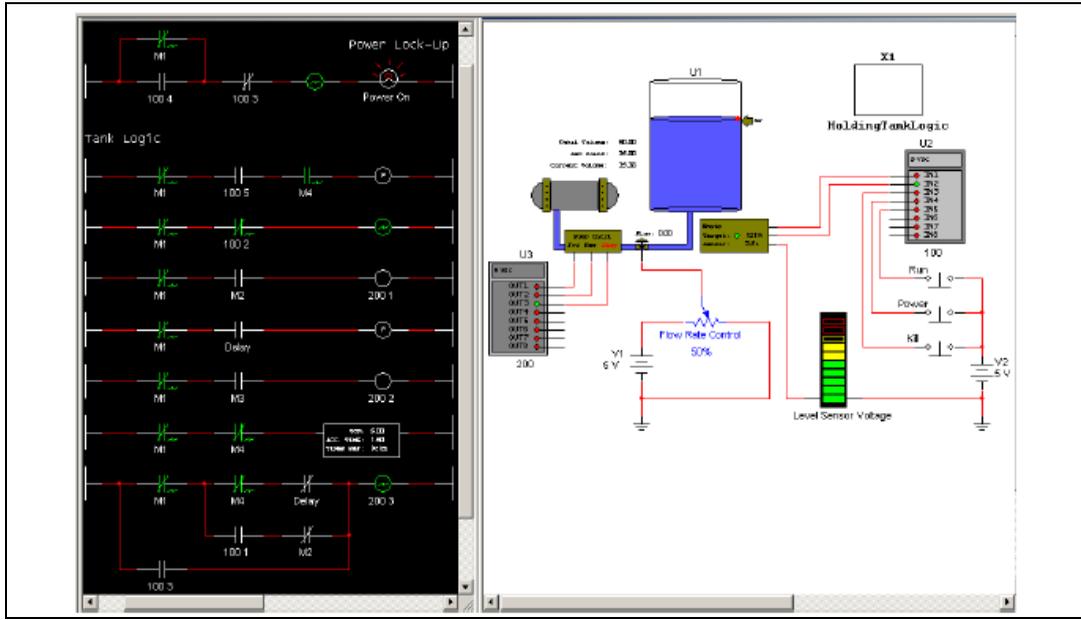


**Tip** Select **Window»Tile vertical** to view the ladder diagram and the circuit at the same time. Observe the interaction between the ladder diagram and the circuit as the simulation proceeds.

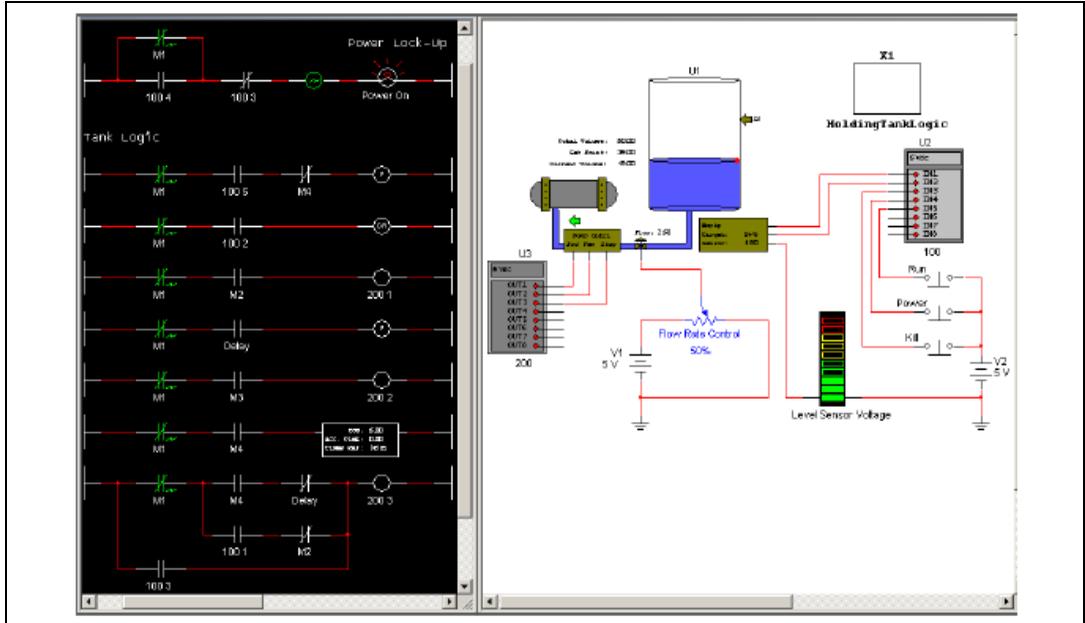
As the simulation proceeds, the tank begins to fill.



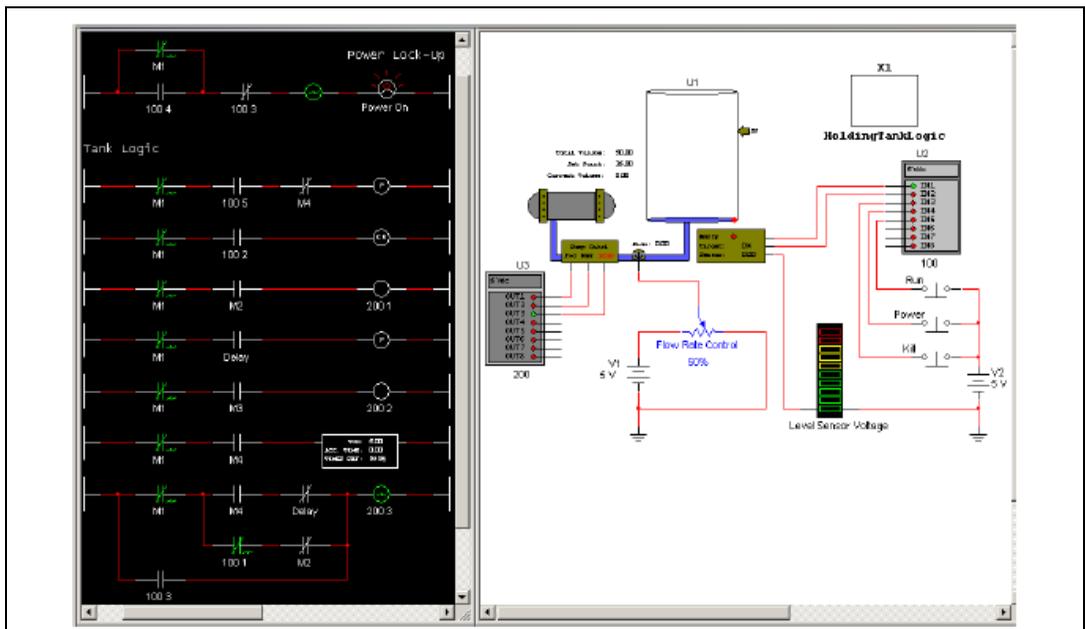
When the level of the fluid in the tank gets to the **Set Point**, fluid stops being pumped.



After a delay of five seconds, the tank begins to empty.



When the tank is empty, the flow stops.



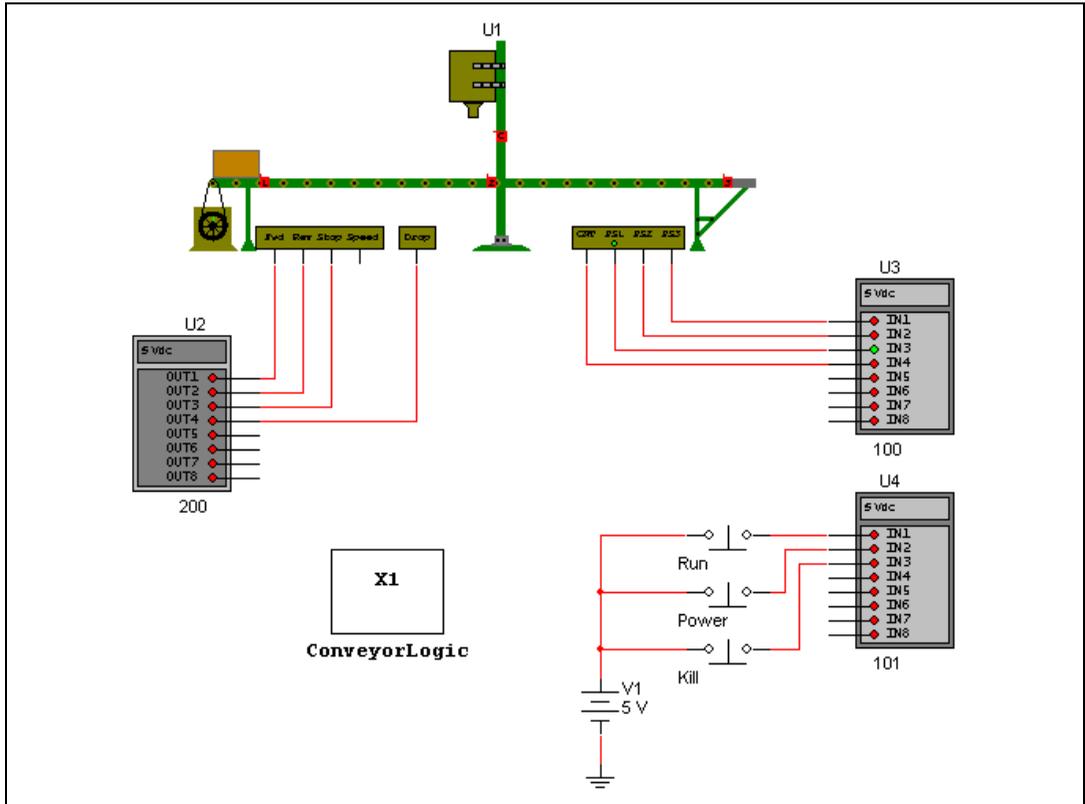
Complete the following to turn off the power at any point in the simulation:

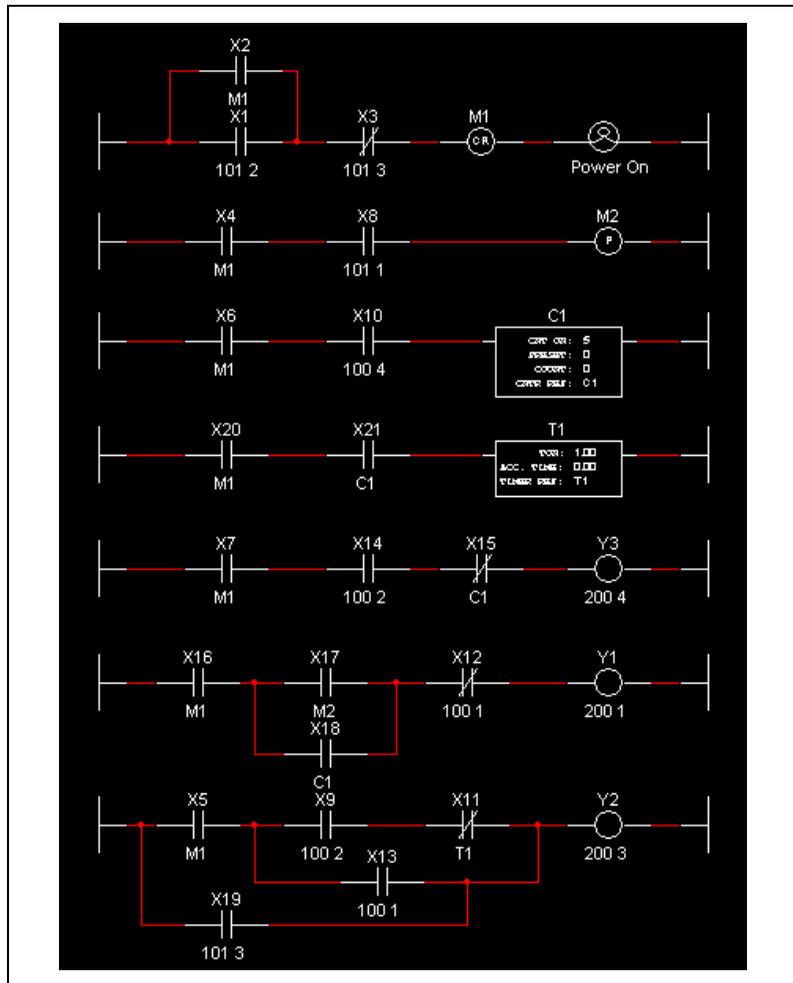
1. Press **K** on your keyboard (or hover your cursor over the Kill switch and click the button that appears) to activate the Kill temporary switch. This sends 5 V to pin IN3 of Input Module U2 (**Input Module Base Address** = 100) which in turn energizes Input Contact X2 (the contact opens). The continuity in the Power Lock-up Rung is broken and Relay Coil M1 is de-energized, which in turn switches off all Relay Contacts with **Controlling Device Reference** = M1.

When you press K, X20 is also temporarily energized, which in turn temporarily energizes Output Coil Y2, which sends a pulse to pin Out3 of Output Module U3. This is wired to the **Stop** pin of the holding tank, so the tank stops filling or emptying (depending on which is currently occurring).

# Conveyor Belt

This section contains an example of a **Ladder Diagram** that drives a conveyor belt.



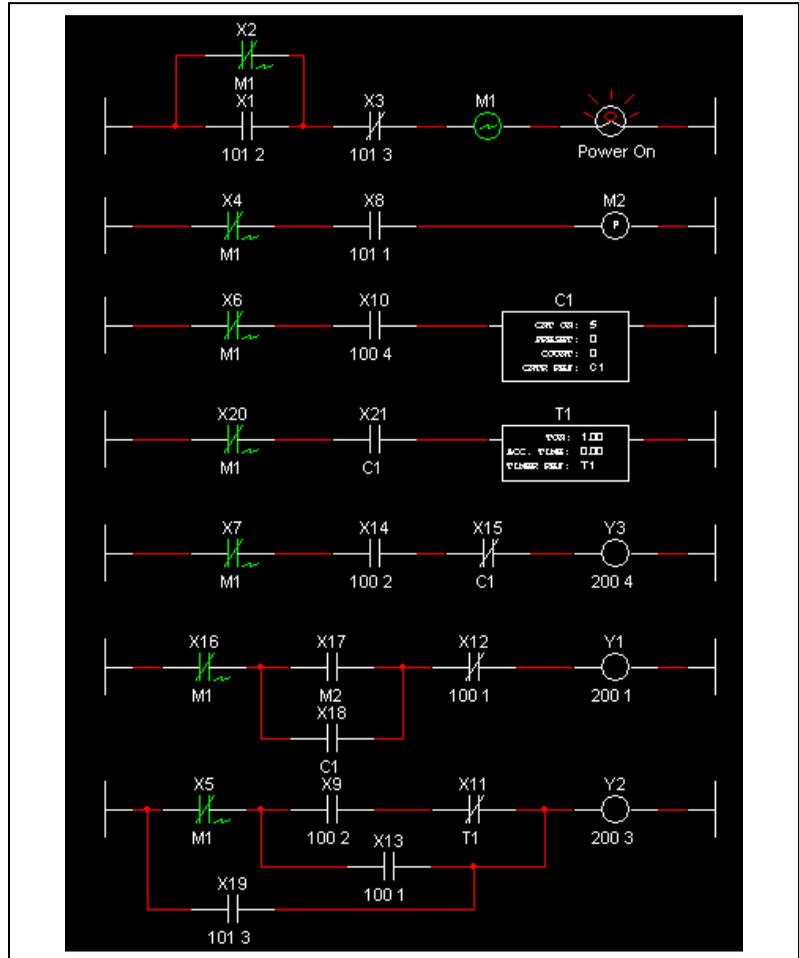


**Note** The ladder diagram is contained in a separate hierarchical block called ConveyorLogic. For details on hierarchical blocks, refer to the *Multisim Help*.

Complete the following steps to activate this design:

1. Select **Simulate»Run** to begin simulation.
2. Press P on your keyboard (or hover your cursor over the Power switch and click the button that appears) to activate the Power temporary switch. This sends 5 V to pin IN2 of Input Module U4 (**Input Module Base Address = 101**) which in turn energizes Input Contact X1 in the Power Lock-up Rung of the ladder diagram. Relay Coil M1 is

energized, causing all Relay Contacts with **Controlling Device Reference = M1** to energize.



Complete the following steps to run the conveyor belt:

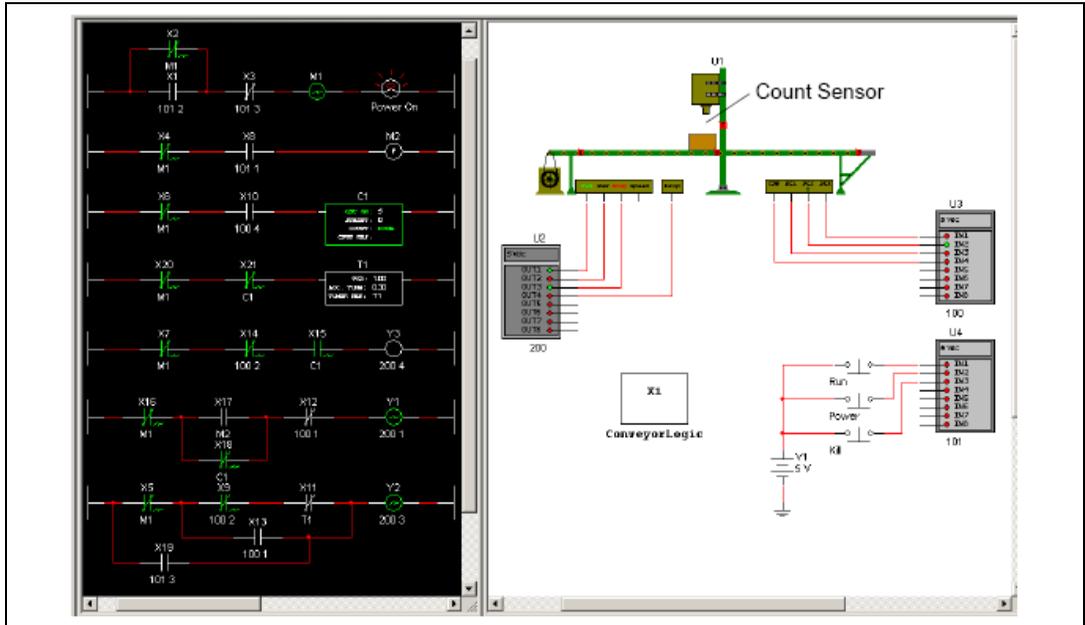
1. Activate the design as described earlier.
2. Press R on your keyboard (or hover your cursor over the Run switch and click the button that pops up) to activate the Run temporary switch.



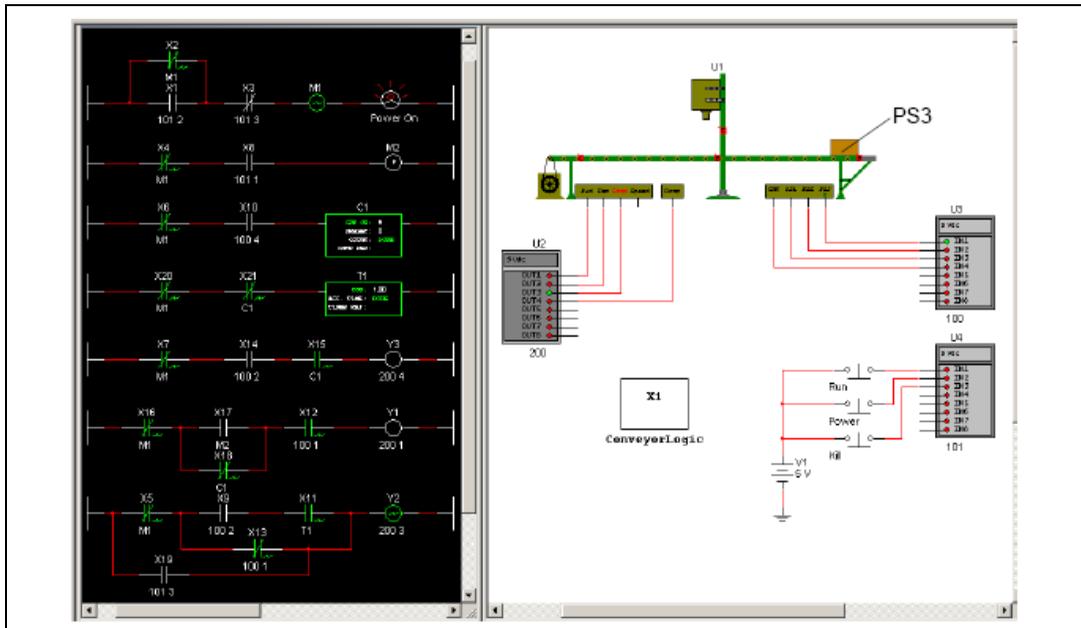
**Tip** Select **Window>Tile vertical** to view the ladder diagram and the circuit at the same time. Observe the interaction between the ladder diagram and the circuit as the simulation proceeds.



When five balls have dropped into the box (counted by Count sensor and C1), the hopper stops dropping balls.



The conveyor continues moving and stops when the box gets to Position Sensor 3 (PS3).



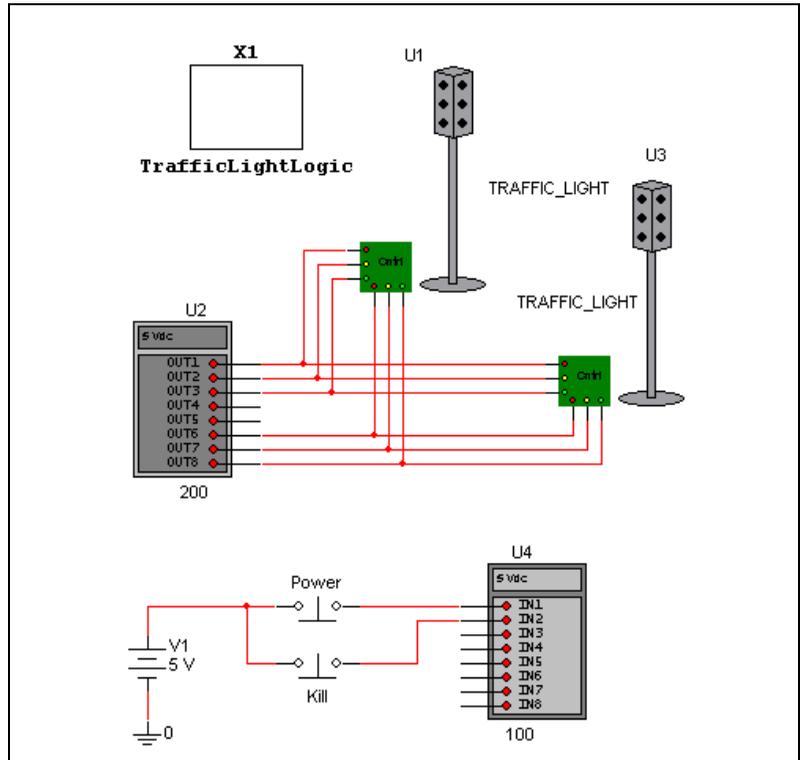
Complete the following to turn off the power at any point in the simulation:

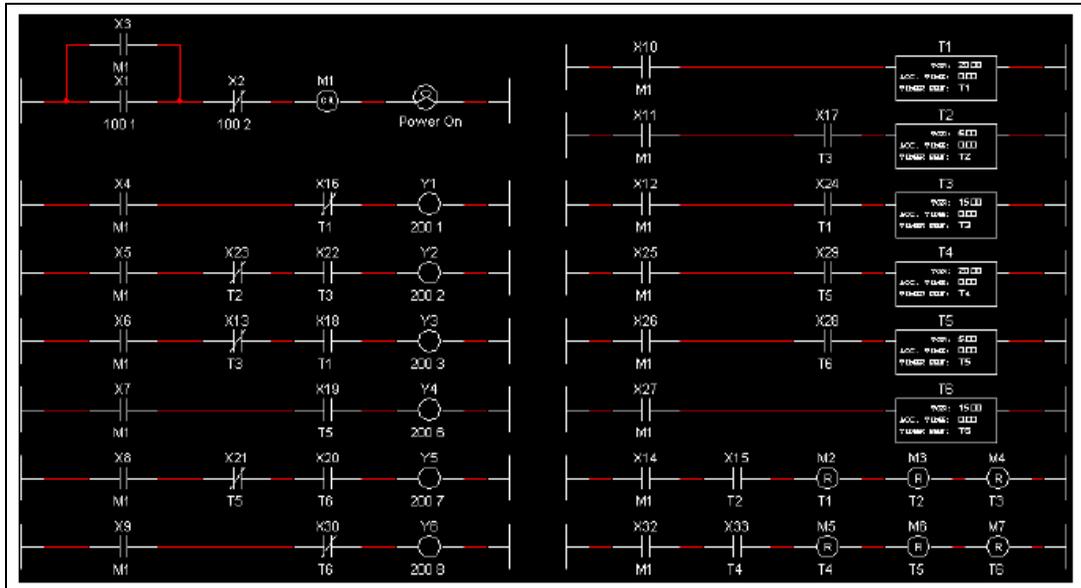
1. Press K on your keyboard (or hover your cursor over the Kill switch and click the button that appears) to activate the Kill temporary switch. This sends 5 V to pin IN3 of Input Module U4 (**Input Module Base Address = 101**) which in turn energizes Input Contact X3 (the contact opens). The continuity in the Power Lock-up Rung is broken and Relay Coil M1 is de-energized, which in turn switches off all Relay Contacts with **Relay Device Reference = M1**.

When you press K, X19 is also temporarily energized, which in turn temporarily energizes Output Coil Y2, which sends a pulse to pin Out3 of Output Module U2. This is wired to the **Stop** pin of the conveyor belt, so the belt stops.

# Traffic Light

The ladder diagram in this section runs two traffic lights.





**Note** The ladder diagram is contained in a separate hierarchical block called `TrafficLightLogic`. For details on hierarchical blocks, refer to the *Multisim Help*.

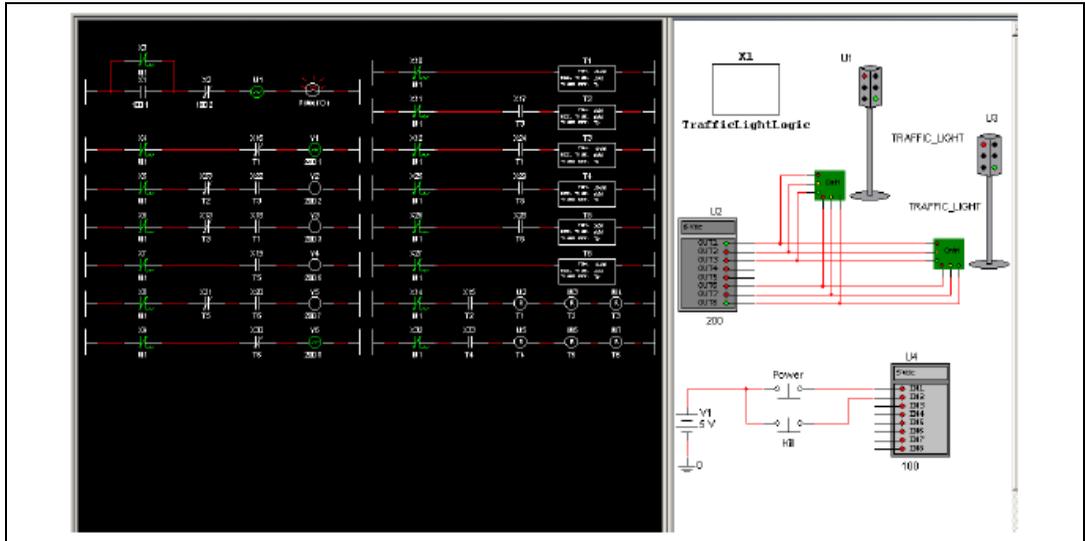
Complete the following steps to run the traffic lights:

1. Select **Simulate»Run**.
2. Press P on your keyboard (or hover your cursor over the Power switch and click the button that pops up) to activate the Power momentary switch.

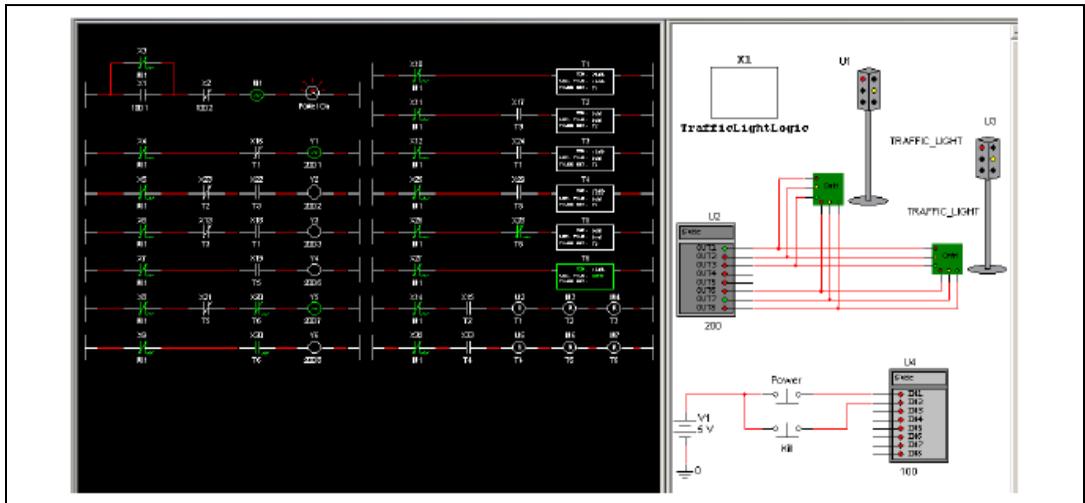


**Tip** Select **Window»Tile vertical** to view the ladder diagram and the circuit at the same time. Observe the interaction between the ladder diagram and the circuit as the simulation proceeds.

The red and green lights in traffic lights U1 and U3 light as shown below.

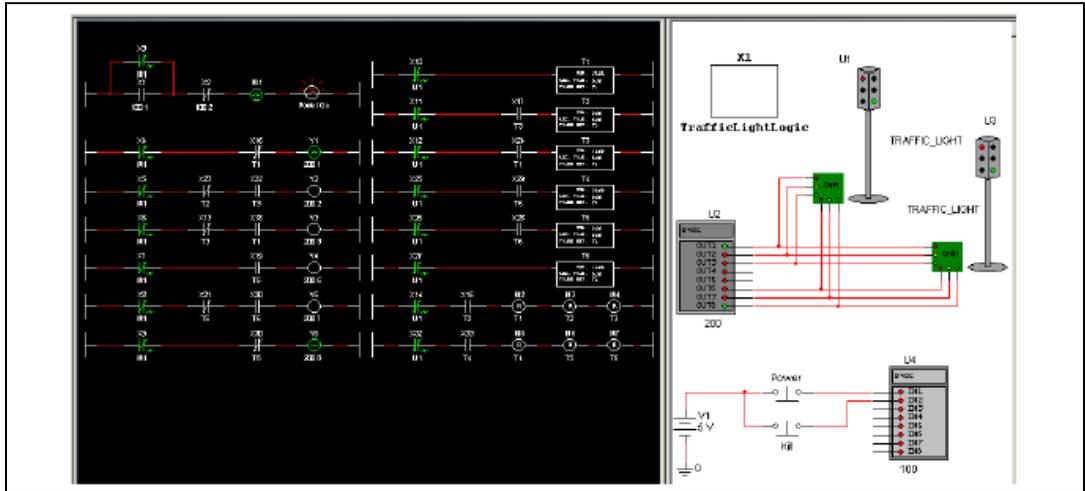


After 15 seconds, the green lights turn amber.

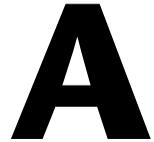




After 5 more seconds, the amber lights turn red and the red lights turn green.



3. The cycle continues in this way until you stop the simulation, or press <K> (or hover your cursor over the Kill switch and click the button that appears) to activate the Kill momentary switch.



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