Datasheet

DS001038

AS7343L

13-Channel Multi-Spectral Sensor

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Content Guide

1 General Description

The ams OSRAM AS7343L[1] is a 13-channel spectrometer designed for spectral identification of lateral flow particle markers. It is highly versatile sensor targeted to enable new laboratory applications. It is optimized for reflective, transmissive and emissive measurements including lateral flow test applications, fluid or reagent analysis, color matching, and spectral identification in the visible range.

13 individual channels cover the spectral range from approximately 380 nm to 1000 nm. 11 channels are centered in the visible spectrum (VIS), plus one near-infrared (NIR) and a clear channel. Allowing a full spectral re-construction of the incoming light.

AS7343L integrates high-precision optical filters onto standard CMOS silicon via deposited interference filter technology. A built-in aperture controls the light entering the sensor array to increase accuracy. A programmable digital GPIO and LED driver enable light source and trigger/sync control. Device control and spectral data access is implemented through a serial I²C interface. The device is available in an ultra-low profile package with dimensions of 3.1 mm x 2 mm x 1 mm.

1.1 Key Benefits & Features

The benefits and features of AS7343L, 13-Channel Multi-Spectral Sensor, are listed below:

Figure 1:
Added Value of Using AS7343L

Benefits	Features
Highly versatile spectral sensor	● 13 channels between 380 nm and 1000 nm ● Reflective, transmissive and emissive applications ● Fluorescence and luminescence measurements ● Spectral re-construction
Highest sensitivity	● Enables ultra-low light operation (e.g. chemiluminescence applications) ● Enables operation behind additional external filters
Low power consumption and minimum I²C traffic	● 1.8 V VDD operation ● Configurable sleep mode ● Interrupt-driven device
Ultra-high integration	● On chip interference filter technology ● Integrated LED driver and 6 integrated ADCs ● 3.1 mm x 2 mm x 1 mm package outline

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[1] L = Lateral flow

Benefits	Features
Electronic shutter/external trigger functionality	GPIO can be configured to function as external trigger input to enable fluorescence measurements

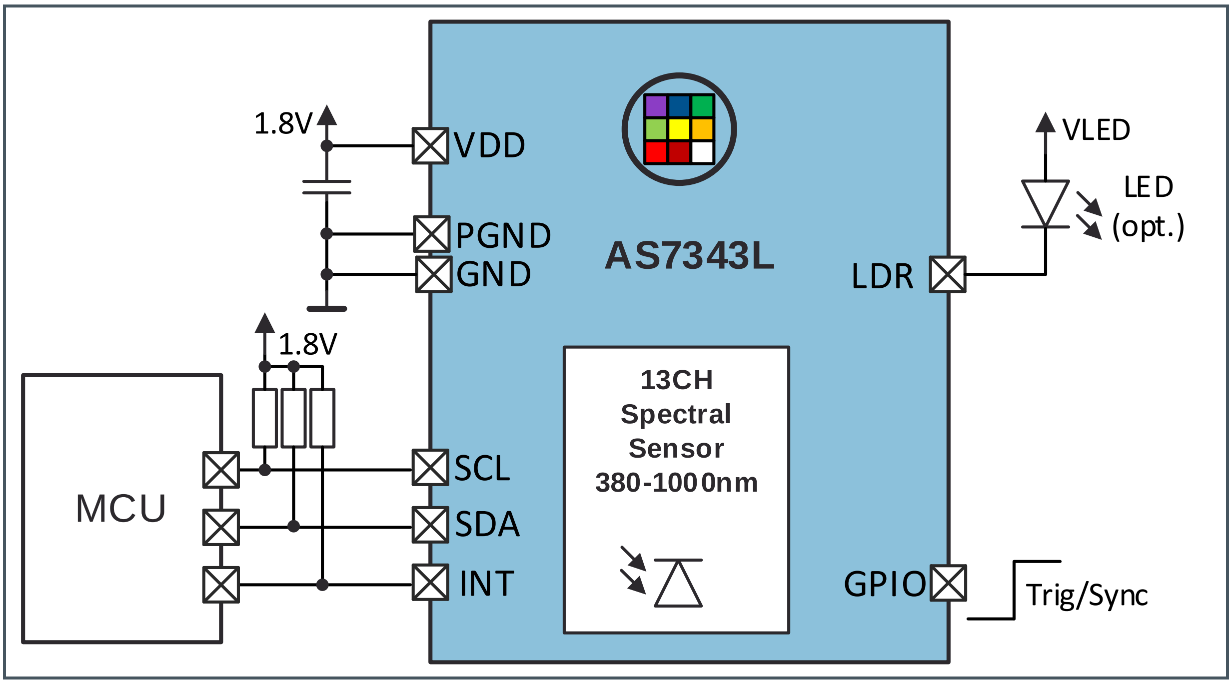
1.2 Applications

- Multi-analyte detection
- Fluorescent-based measurement applications
- Luminescence-based measurement applications
- Reflection- or transmissivity-based color detection (e.g. lateral flow strips)

1.3 Block Diagram

The functional blocks of this device are shown below:

Figure 2:
Functional Blocks of AS7343L



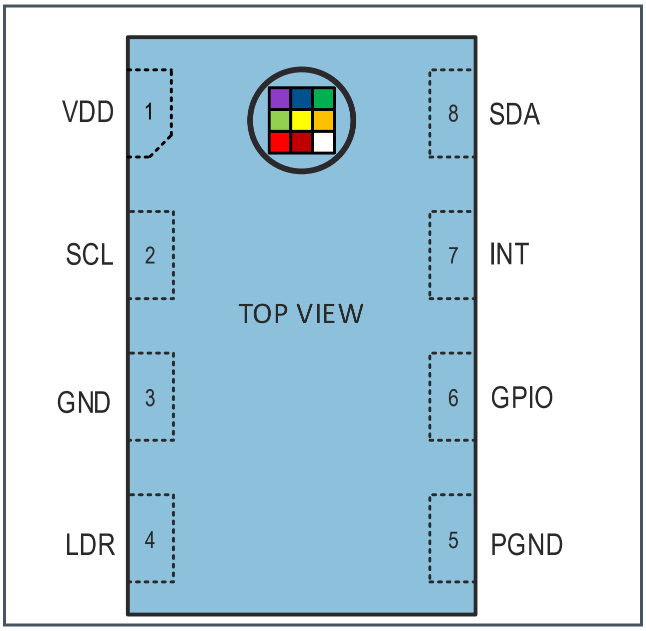
2 Ordering Information

Ordering Code	Package	Delivery Form	Delivery Quantity
AS7343L-DLGT	OLGA-8	Tape & Reel 13-inch	5000 pcs/reel
AS7343L-DLGM	OLGA-8	Tape & Reel 7-inch	500 pcs/reel

3 Pin Assignment

3.1 Pin Diagram

Figure 3:
Pin Assignment of AS7343L (TOP VIEW)



3.2 Pin Description

Figure 4:
Pin Description of AS7343L

Pin Number	Pin Name	Pin Type[(1)]	Description
1	VDD	P	Positive supply voltage terminal
2	SCL	DI	Serial interface clock signal line for I²C interface. Connect pull up resistor to 1.8 V.
3	GND	P	Ground. All voltages referenced to GND
4	LDR	A_I/O	LED current sink input. If not used leave pin unconnected.
5	PGND	P	Ground. All voltages referenced to GND
6	GPIO	D_I/O	General purpose input/output. Default output open drain. If not used leave pin unconnected.
7	INT	DO_OD	Interrupt. Open drain output active low. Connect pull up resistor to 1.8 V. If not used leave pin unconnected.

Pin Number	Pin Name	Pin Type(1)	Description
8	SDA	D_I/O	Serial interface data signal line for I²C interface. Connect pull up resistor to 1.8 V.

(1) Explanation of abbreviations:

DI	Digital Input
D_I/O	Digital Input/Output
DO_OD	Digital Output, open drain
P	Power pin
A_I/O	Analog pin

4 Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under “Operating Conditions” is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. All voltages with respect to GND/PGND. Device parameters are guaranteed at V_{DD}=1.8 V and T_A=25 °C unless otherwise noted.

Figure 5:
Absolute Maximum Ratings of AS7343L

Symbol	Parameter	Min	Max	Unit	Comments
Electrical Parameters					
V_{DD} / V_{GND}	Supply Voltage to Ground	-0.3	1.98	V	Applicable for pin VDD
V_{ANA_MAX}	Analog Pins	-0.3	3.6	V	Applicable for pin LDR
V_{DIG_MAX}	Digital Pins	-0.3	3.6	V	Applicable for pins SCL,SDA,GPIO and INT
I_{SCR}	Input Current (latch-up immunity)	± 100		mA	AEC-Q100-004E
I_O	Output Terminal Current	-1	20	mA	
Electrostatic Discharge					
ESD_{HBM}	Electrostatic Discharge HBM	± 2000		V	JS-001-2017
ESD_{CDM}	Electrostatic Discharge CDM	± 500		V	JS-002-2018
Temperature Ranges and Storage Conditions					
T_A	Operating Ambient Temperature	-30	85	°C	
T_{STRG}	Storage Temperature Range	-40	85	°C	
T_{BODY}	Package Body Temperature		260	°C	IPC/JEDEC J-STD-020(1)
RH_{NC}	Relative Humidity (non-condensing)	5	85	%	
MSL	Moisture Sensitivity Level	3			Maximum floor life time of 168h

(1) The reflow peak soldering temperature (body temperature) is specified according to IPC/JEDEC J-STD-020 “Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices.” The lead finish for Pb-free leaded packages is “Matte Tin” (100% Sn)

5 Electrical Characteristics

All limits are guaranteed. The parameters with Min and Max values are guaranteed with production tests or SQC (Statistical Quality Control) methods. All voltages with respect to GND/PGND. Device parameters are guaranteed at VDD=1.8 V and T_A=25 °C unless otherwise noted.

Figure 6:
Electrical Characteristics of AS7343L

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VDD	Supply Voltage		1.7	1.8	1.98	V
TA	Operating free-air temperature(1)		-30	25	85	°C
Power Consumption						
IDD	Supply Current(2)	VDD=1.8 V; T_A =25 °C Active mode(3)		210	280	µA
		VDD=1.8 V; T_A =25 °C Idle mode(4)		40	60	µA
		VDD=1.8 V; T_A =25 °C Sleep mode(5)		0.7	5	µA
Digital Pins						
VIH	SCL,SDA input high voltage		1.26			V
VIL	SCL,SDA input low voltage				0.54	V
VOL	INT, SDA output low voltage	6 mA sink current			0.4	V
CI	Input pin capacitance				10	pF
Ileak	Leakage current into SCL,SDA,INT pins		-5		5	µA
GPIO						
CLOAD	Maximum capacitive load GPIO				20	pF
LED Driver						
V_LDR	LDR compliance voltage	I_LDR= 4 mA ; LED_HALF = “0”			240	mV
		I_LDR= 4 mA ; LED_HALF = “1”			130	
		I LDR 134 mA ; LED_HALF = “0”			280	mV
		I LDR 134 mA ; LED_HALF = “1”			180	

(1) While the device is operational across the temperature range, functionality will vary with temperature.
(2) Supply current values are shown at the VDD pin and do not include current through pin LDR.
(3) Active state occurs during active integration. (PON = “1” ; SP_EN = “1”) If wait is enabled (WEN = “1”), supply current is lower during the wait period
(4) Idle state occurs when PON = “1” and all functions are disabled
(5) Sleep state occurs when PON = “0” and I²C bus is idle. If I²C traffic is active device automatically enters idle mode.

6 Optical Characteristics

All limits are guaranteed. The parameters with Min and Max values are guaranteed with production tests or SQC (Statistical Quality Control) methods. All voltages with respect to GND/PGND. Device parameters are guaranteed at VDD=1.8 V and T_A=25 °C unless otherwise noted.

Figure 7:
AS7343L Optical Channel Summary

Channel	Peak Wavelength [nm][1][2]			Full Width Half Maximum [nm]
	(min)	λp (typ)	(max)	(typ)
F1	395	405	415	30
F2	415	425	435	22
FZ	440	450	460	55
F3	465	475	485	30
F4	505	515	525	40
FY	545	555	565	100
F5	540	550	560	35
FXL	590	600	610	80
F6	630	640	650	50
F7	680	690	700	55
F8	735	745	755	60
NIR	845	855	865	54

(1) Parameter measured on a production ongoing sample bases on glass using diffused light. The table above is valid for full sensor response including diffuser, package and photodiode response.

(2) Peak Wavelength is validated by smoothed/averaged monochromator measurement data

Figure 8:
Optical Characteristics of Spectral Channels, AGAIN: 1024x, Integration Time: 27.8 ms

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{e_F1}	Irradiance responsivity channel F1	LED_396nm ; Ee= 155 mW/m² LED_408nm ; Ee= 155 mW/m²	4311	5749	7186	counts
R_{e_F2}	Irradiance responsivity channel F2	LED_408nm ; Ee= 155 mW/m² LED_448nm ; Ee= 155 mW/m²	1317	1756	2196	counts
R_{e_FZ}	Irradiance responsivity channel FZ	LED_428nm ; Ee= 155 mW/m² LED_480nm ; Ee= 155 mW/m²	1627	2169	2711	counts
R_{e_F3}	Irradiance responsivity channel F3	LED_448nm ; Ee= 155 mW/m² LED_500nm ; Ee= 155 mW/m²	577	770	962	counts
R_{e_F4}	Irradiance responsivity channel F4	LED_500nm ; Ee= 155 mW/m² LED_534nm ; Ee= 155 mW/m²	2356	3141	3926	counts
R_{e_FY}	Irradiance responsivity channel FY	LED_534nm ; Ee= 155 mW/m² LED_593nm ; Ee= 155 mW/m²	2810	3747	4684	counts
R_{e_F5}	Irradiance responsivity channel F5	LED_531nm ; Ee= 155 mW/m² LED_594nm ; Ee= 155 mW/m²	1180	1574	1967	counts
R_{e_FXL}	Irradiance responsivity channel FXL	LED_593nm ; Ee= 155 mW/m² LED_628nm ; Ee= 155 mW/m²	3582	4776	5970	counts
R_{e_F6}	Irradiance responsivity channel F6	LED_618nm ; Ee= 155 mW/m² LED_665nm ; Ee= 155 mW/m²	2502	3336	4170	counts
R_{e_F7}	Irradiance responsivity channel F7	LED_685nm ; Ee= 155 mW/m² LED_715nm ; Ee= 155 mW/m²	4095	5435	6774	counts
R_{e_F8}	Irradiance responsivity channel F8	LED_715nm ; Ee= 155 mW/m² LED_766nm ; Ee= 155 mW/m²	648	864	1080	counts
R_{e_NIR}	Irradiance responsivity channel NIR	LED_849nm ; Ee= 155 mW/m² LED_903nm ; Ee= 155 mW/m²	7936	10581	13226	counts

Figure 9:
Optical Characteristics of Broadband Channels, AGAIN: 1024x, FD_GAIN: 64x, Integration Time: 27.8 ms

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{e_FD}	Irradiance responsivity channel Flicker	LED_593nm ; Ee= 155 mW/m² LED_766nm ; Ee= 155 mW/m² FD_GAIN=64x	3233	4311	5389	counts
R_{e_VIS}	Irradiance responsivity channel VIS	LED_396nm ; Ee= 155 mW/m² LED_766nm ; Ee= 155 mW/m² 2 VIS PDs read-out	749	999	1248	counts

Figure 10:
Optical Characteristics of AS7343L, AGAIN: 128x, Integration Time: 11 ms (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Dark_$_1$(1)	Dark ADC count value	Ee = 0 µW/cm^2 AGAIN: 512x Integration time: 98 ms		0	5	counts
Gain(2) ratio	Optical gain ratios, relative to 64x gain setting	AGAIN: 0.5x	7.49	7.9	8.28	See note(3)
		AGAIN: 1x	15	15.8	16.5	
		AGAIN: 2x	30	31.6	33.2	
		AGAIN: 4x	61	64	67	
		AGAIN: 8x	117	124	130	
		AGAIN: 16x	235	247	259	
		AGAIN: 32x	0.475	0.5	0.525	
		AGAIN: 64x		1		
		AGAIN: 128x	1.9	2	2.1	
		AGAIN: 256x	3.9	4.1	4.3	
		AGAIN: 512x	8.1	8.6	9.1	
		AGAIN: 1024x	15.2	16.9	18.6	
		AGAIN: 2048x	28.2	34.75	41.3	
ADC noise(4)		White LED, 2700 K Integration time: 100 ms		0.05		% full scale
t_{int}	Typical integration time(5)	ASTEP = 599 ATIME = 29		50		ms
t_{ASTEP}	Integration time step size	ASTEP = 999		2.78		ms
h_{ca}	Half cone angle	On the sensor		40		deg

(1) The typical 3-sigma distribution is between 0 and 1 counts for AGAIN setting of 16x.

(2) The gain ratios are relative to 64x gain setting and are calculated relative to the response with integration time: 11 ms and AGAIN: 128x.

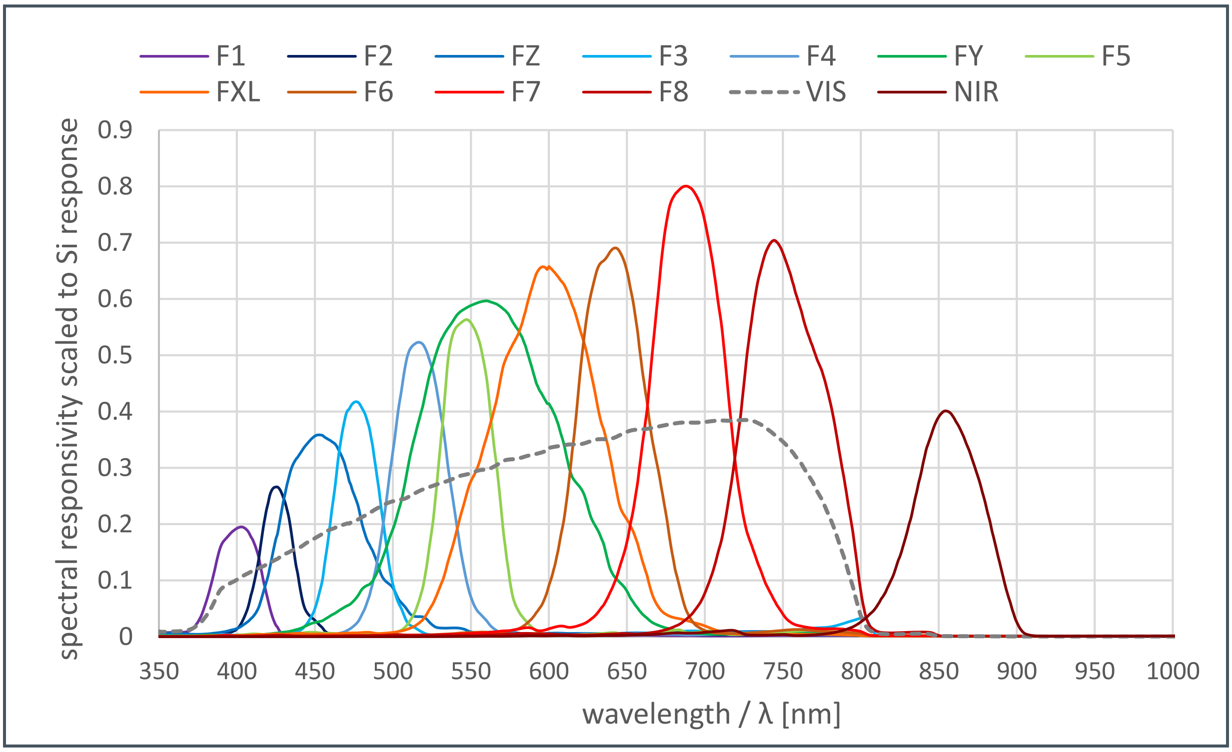
(3) ADC noise is calculated as the standard deviation of relative to full scale.

(4) Integration time, in milliseconds, is equal to: (ATIME + 1) x (ASTEP + 1) x 2.78 µs

(5) AGAIN ratio 0.5x to 16x is multiplied by 1000 for easier readability

7 Typical Operating Characteristics

Figure 11:
Typical Spectral Responsivity

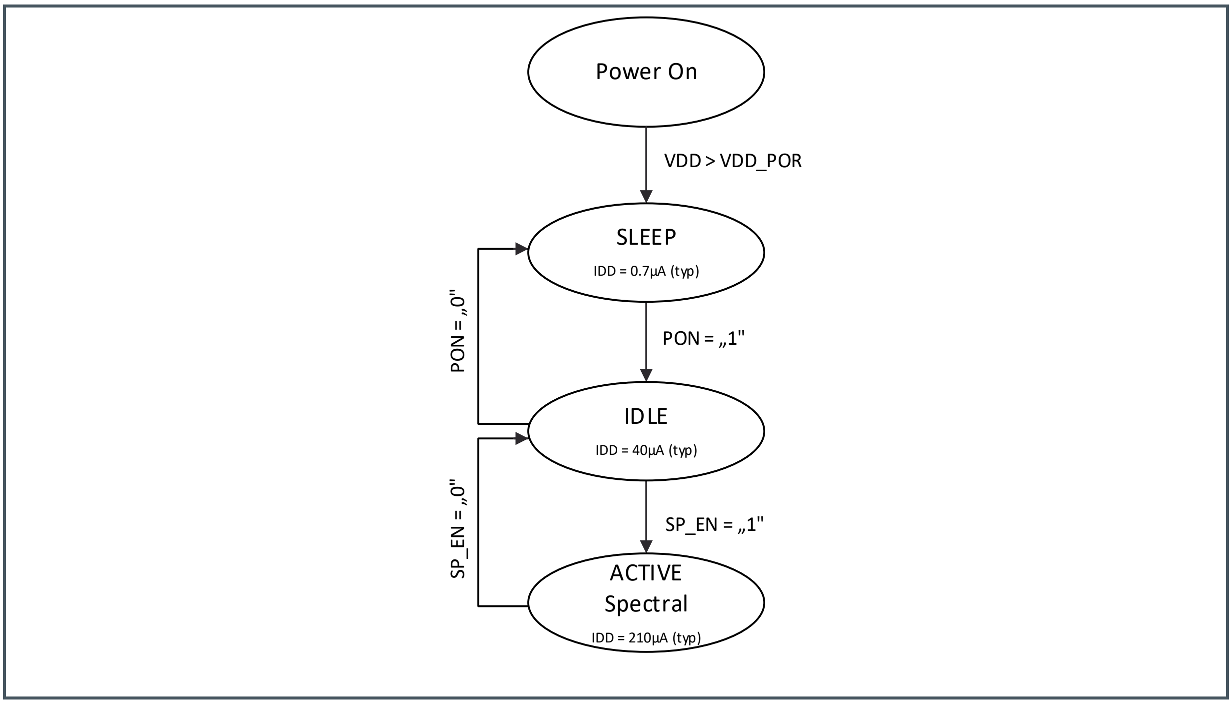


8 Functional Description

Upon power-up (POR), the device initializes. During initialization (typically 200 µs), the device will deterministically send NAK on I²C and cannot accept I²C transactions. All communication with the device must be delayed and all outputs from the device must be ignored including interrupts. After initialization, the device enters the SLEEP state. In this operational state, the internal oscillator and other circuitry are not active, resulting in ultra-low power consumption. If an I²C transaction occurs during this state, the I²C core wakes up temporarily to service the communication. Once the Power ON bit, "PON", is enabled, the device enters the IDLE state in which the internal oscillator and attendant circuitry are active, but power consumption remains low. Whenever the spectral measurement is enabled (SP_EN = "1") the device enters the ACTIVE state. If the spectral measurement is disabled (SP_EN = "0") the device returns to the IDLE state. The figure below describes a simplified state diagram and the typical supply currents in each state.

If Sleep after Interrupt is enabled (SAI = "1" in register 0xAC), the state machine will enter SLEEP when an interrupt occurs. Entering SLEEP does not automatically change any of the register settings (e.g. PON bit is still high, but the normal operational state is over-ridden by SLEEP state). SLEEP state is terminated when the SAI_ACTIVE bit is cleared (the status bit is in register 0xA7 and the clear status bit is in register 0xFA).

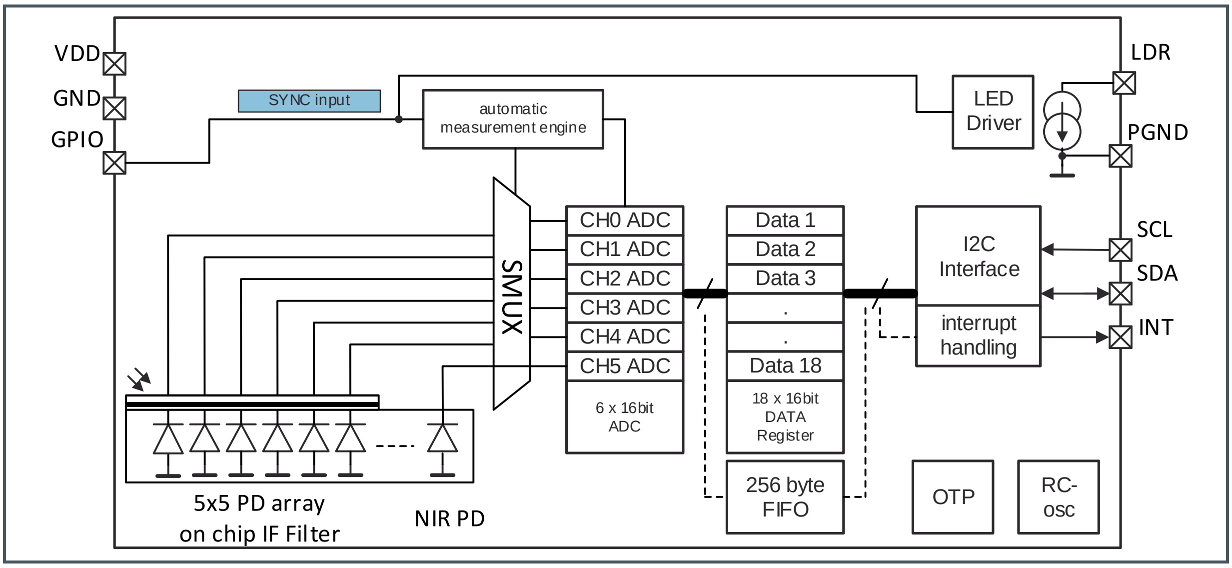
Figure 12:
Simplified State Diagram



8.1 Device Architecture

The device features six independent 16-bit ADCs. Gain and integration time of the six ADCs can be adjusted with the I^{2}C interface. A wait time can be programed to automatically set a delay between two consecutive spectral measurements and to reduce overall power consumption. Once a measurement is started, the device is automatically processing the channels and storing the measurement data on chip in the corresponding data registers.

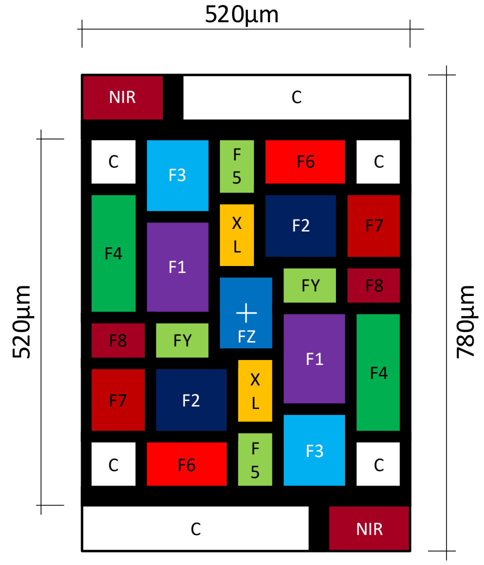
Figure 13:
Simplified Block Diagram



8.2 Sensor Array

The device features a 5x5-photodiode array and two near- infrared response (“NIR”) sense fields and two large clear photodiodes (“C”).

Figure 14:
Sensor Array



8.3 GPIO

The GPIO can be used synchronization input to start/stop the spectral measurement. It also allows synchronizing the LED driver (LDR) with an external start/stop signal. Default state of the GPIO is “output”.

8.4 Interrupt (INT)

The interrupt (INT) can be used to define thresholds and read-out the device only when the channel threshold has been reached. The pin is active low.

8.5 LED Driver (LDR)

The LED driver is programmable and can be used to drive external LEDs. It is also possible to synchronize the LED driver with an external start/stop signal via pin GPIO.

9 I²C Interface

The device uses I²C serial communication protocol for communication. The device supports 7-bit chip addressing and both standard and full-speed clock frequency modes. Read and Write transactions comply with the standard set by Philips (now NXP). Internal to the device, an 8-bit buffer stores the register address location of the desired byte to read or write. This buffer auto-increments upon each byte transfer and is retained between transaction events (i.e. valid even after the master issues a STOP command and the I²C bus is released). During consecutive Read transactions, the future/repeated I²C Read transaction may omit the memory address byte normally following the chip address byte; the buffer retains the last register address +1. All 16-bit fields have a latching scheme for reading and writing. In general, it is recommended to use I²C bursts whenever possible, especially in this case when accessing two bytes of one logical entity. When reading these fields, the low byte must be read first, and it triggers a 16-bit latch that stores the 16-bit field. The high byte must be read immediately afterwards. When writing to these fields, the low byte must be written first, immediately followed by the high byte. Reading or writing to these registers without following these requirements will cause errors.

9.1 I²C Address

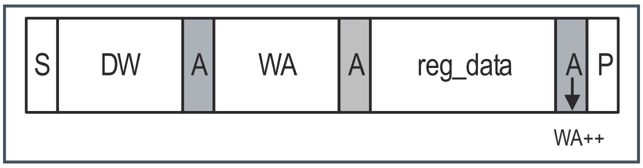
Figure 15:
AS7343L I²C Slave Address

Device	I²C Address
AS7343L	0x39

9.2 I²C Write Transaction

A Write transaction consists of a START, CHIP-ADDRESSWRITE, REGISTER-ADDRESS WRITE, DATA BYTE(S), and STOP (P). Following each byte (9TH clock pulse) the slave places an ACKNOWLEDGE/NOT- ACKNOWLEDGE (A/N) on the bus. If the slave transmits N, the master may issue a STOP.

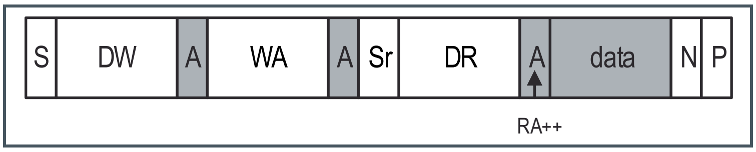
Figure 16:
I²C Byte Write



9.3 I^{2}C Read Transaction

A Read transaction consists of a START, CHIP-ADDRESSWRITE, REGISTER-ADDRESS, RESTART, CHIP-ADDRESSREAD, DATA BYTE(S), and STOP. Following all but the final byte the master places an ACK on the bus (9TH clock pulse). Termination of the Read transaction is indicated by a NACK being placed on the bus by the master, followed by STOP.

Figure 17:
I^{2}C Read



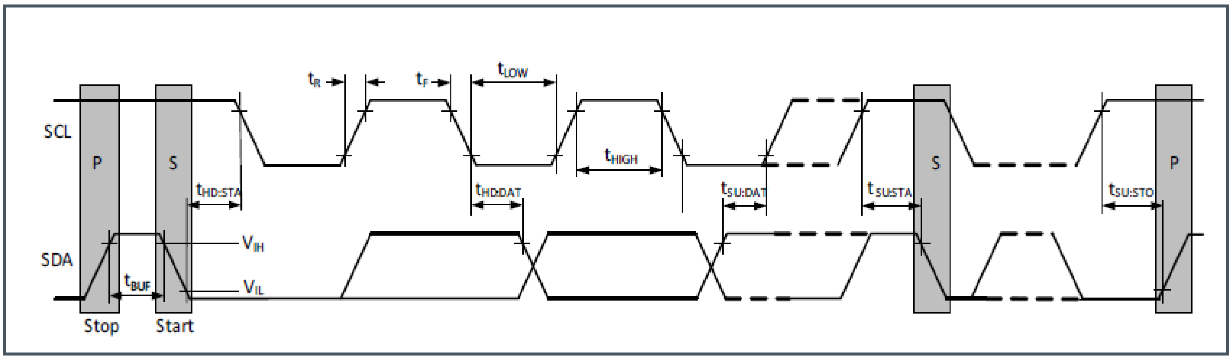
9.4 Timing Characteristics

Figure 18:
I^{2}C Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
f_{SCL}	I^{2}C clock frequency			1	MHz
t_{BUF}	Bus free time between start and stop condition	1.3			µs
$t_{HS;STA}$	Hold time after (repeated) start condition. After this period, the first clock is generated.	0.6			
$t_{SU;STA}$	Repeated start condition setup time	0.6			
$t_{SU;STO}$	Stop condition setup time	0.6			
t_{LOW}	SCL clock low period	1.3			
t_{HIGH}	SCL clock high period	0.6			
$t_{HD;DAT}$	Data hold time	0			ns
$t_{SU;DAT}$	Data setup time	100			
t_F	Clock/data fall time			300	
t_R	Clock/data rise time			300	

9.5 Timing Diagrams

Figure 19:
I²C Slave Timing Diagram



10 Register Description

The device is controlled and monitored by registers accessed through the I²C serial interface. These registers provide device control functions and can be read to determine device status and acquire device data.

The register set is summarized below. The values of all registers and fields that are listed as reserved or are not listed must not be changed at any time. Two-byte fields are always latched with the low byte followed by the high byte. The “Name” column illustrates the purpose of each register by highlighting the function associated to each bit. The bits are shown from MSB (D7) to LSB (D0). GRAY fields are reserved and their values must not be changed at any time.

In order to access registers from 0x60 to 0x74 bit REG_BANK in register CFG0 (0xA9) needs to be set to “1”.

10.1 Register Overview

Figure 20:
Register Overview

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
0x58	AUXID					AUXID [3:0]			
0x59	REVID						REVID [2:0]		
0x5A	ID	ID [7:0]							
0x66	CFG12						SP_TH_CH [2:0]		
0x80	ENABLE				SMUXEN	WEN		SP_EN	PON
0x81	ATIME	ATIME [7:0]							
0x83	WTIME	WTIME [7:0]							
0x84	SP_TH_L	SP_TH_L_LSB [7:0]							
0x85		SP_TH_L_MSB [7:0]							
0x86	SP_TH_H	SP_TH_H_LSB [7:0]							
0x87		SP_TH_H_MSB [7:0]							
0x93	STATUS	ASAT				AINT	FINT		SINT
0x94	ASTATUS	ASAT_ STATUS				AGAIN_STATUS [3:0]			
0x95	DATA_0	DATA_0_L [7:0]							
0x96		DATA_0_H [7:0]							
0x97	DATA_1	DATA_1_L [7:0]							
0x98		DATA_1_H [7:0]							
0x99	DATA_2	DATA_2_L [7:0]							
0x9A		DATA_2_H [7:0]							

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
0x9B	DATA_3	DATA_3_L [7:0]							
0x9C		DATA_3_H [7:0]							
0x9D	DATA_4	DATA_4_L [7:0]							
0x9E		DATA_4_H [7:0]							
0x9F	DATA_5	DATA_5_L [7:0]							
0xA0		DATA_5_H [7:0]							
0xA1	DATA_6	DATA_6_L [7:0]							
0xA2		DATA_6_H [7:0]							
0xA3	DATA_7	DATA_7_L [7:0]							
0xA4		DATA_7_H [7:0]							
0xA5	DATA_8	DATA_8_L [7:0]							
0xA6		DATA_8_H [7:0]							
0xA7	DATA_9	DATA_9_L [7:0]							
0xA8		DATA_9_H [7:0]							
0xA9	DATA_10	DATA_10_L [7:0]							
0xAA		DATA_10_H [7:0]							
0xAB	DATA_11	DATA_11_L [7:0]							
0xAC		DATA_11_H [7:0]							
0xAD	DATA_12	DATA_12_L [7:0]							
0xAE		DATA_12_H [7:0]							
0xAF	DATA_13	DATA_13_L [7:0]							
0xB0		DATA_13_H [7:0]							
0xB1	DATA_14	DATA_14_L [7:0]							
0xB2		DATA_14_H [7:0]							
0xB3	DATA_15	DATA_15_L [7:0]							
0xB4		DATA_15_H [7:0]							
0xB5	DATA_16	DATA_16_L [7:0]							
0xB6		DATA_16_H [7:0]							
0xB7	DATA_17	DATA_17_L [7:0]							
0xB8		DATA_17_H [7:0]							
0x90	STATUS 2		AVALID		ASAT_DIG	ASAT_ANA			
0x91	STATUS 3			INT_SP_H	INT_SP_L				
0xBB	STATUS 5						SINT_SMUX		
0xBC	STATUS 4	FIFO_OV		OVTEMP			SP_TRIG	SAI_ACT	INT_BUSY
0xBF	CFG 0			LOW_POWER	REG_BANK		WLONG		
0xC6	CFG1				AGAIN[4:0]				
0xC7	CFG3				SAI				

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
0xF5	CFG6				SMUX_CMD[4:3]				
0xC9	CFG8	FIFO_TH [7:6]							
0xCA	CFG9				SIEN_SMUX				
0x65	CFG10								
0xCF	PERS					APERS [3:0]			
0x6B	GPIO					GPIO_INV	GPIO_IN_EN	GPIO_OUT	GPIO_IN
0xD4	ASTEP	ASTEP [7:0]							
0xD5		ASTEP [15:8]							
0xD6	CFG20		auto_SMUX						
0xCD	LED	LED_ACT	LED_DRIVE [6:0]						
0xD7	AGC_GAIN_MAX	AGC_FD_GAIN_MAX [7:4]							
0xDE	AZ_CONFIG	AT_NTH_ITERATION [7:0]							
0xF9	INTENAB	ASIEN				SP_IEN	FIEN		SIEN
0xFA	CONTROL					SW_RESET	SP_MAN_AZ	FIFO_CLR	CLEAR_SAI_ACT
0xFC	FIFO_MAP		FIFO_WRITE_CH5_DATA – FIFO_WRITE_CH0_DATA [6:1]						ASTATUS
0xFD	FIFO_LVL	FIFO_LVL [7:0]							
0xFE	FDATA	FDATA _L[7:0]							
0xFF		FDATA_H [15:8]							

10.2 Detailed Register Description

For easier readability, the detailed register description is done in groups of registers related to dedicated device functions. This is not necessarily related to its register address.

Explanation of register access abbreviations:
RW = read or write
R = read only
W = write only
SC = self-clearing after access

10.2.1 Enable and Configuration Registers

The following registers are needed to power up and configure the device. To operate the device set bit PON = "1" first (register 0x80) after that configure the device and enable interrupts before setting SP_EN = "1". Changing configuration while SP_EN = "1" may result in invalid results.

ENABLE Register (Address 0x80)

Figure 21:
ENABLE Register

Addr: 0x80		ENABLE		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:5	Reserved	0	RW	Reserved
4	SMUXEN	0	RW	**SMUX Enable.** 1: Starts SMUX command Note: This bit gets cleared automatically as soon as SMUX operation is finished
3	WEN	0	RW	**Wait Enable.** 0: Wait time between two consecutive spectral measurements disabled 1: Wait time between two consecutive spectral measurements enabled
2	Reserved	0	RW	Reserved
1	SP_EN	0	RW	**Spectral Measurement Enable.** 0: Spectral Measurement Disabled 1: Spectral Measurement Enabled
0	PON	0	RW	**Power ON.** 0: AS7343L disabled 1: AS7343L enabled Note: When bit is set, internal oscillator is activated, allowing timers and ADC channels to operate.

GPIO Register (Address 0x6B)

Figure 22:
GPIO Register

Addr: 0x6B		GPIO		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:4	Reserved	0		Reserved
3	GPIO_INV	0	RW	**GPIO Invert.** If set, the GPIO output is inverted.
2	GPIO_IN_EN	0	RW	**GPIO Input Enable.** If set, the GPIO pin accepts a non-floating input.
1	GPIO_OUT	1	RW	**GPIO Output.** If set, the output state of the GPIO is active directly.
0	GPIO_IN	0	R	**GPIO Input.** Indicates the status of the GPIO input if GPIO_IN_EN is set.

LED Register (Address 0xCD)

Figure 23:
LED Register

Addr: 0xCD		LED		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	LED_ACT	0	RW	**LED Control.** 0: External LED connected to pin LDR off 1: External LED connected to pin LDR on
6:0	LED_DRIVE	000 0100	RW	**LED Driving Strength.** 000 0000: 4 mA 000 0001: 6 mA 000 0010: 8 mA 000 0011: 10 mA **000 0100:** 12 mA …… 111 1110: 256 mA 111 1111: 258 mA

INTENAB Register (Address 0xF9)

Figure 24:
INTENAB Register

Addr: 0xF9		INTENAB		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	ASIEN	0	RW	**Spectral and Flicker Detect Saturation Interrupt Enable.** When asserted permits saturation interrupts to be generated.
6:4	Reserved			Reserved
3	SP_IEN	0	RW	**Spectral Interrupt Enable.** When asserted permits interrupts to be generated, subject to the spectral thresholds and persistence filter. Bit is mirrored in the ENABLE register.
2	F_IEN	0	RW	**FIFO Buffer Interrupt Enable.** When asserted permits interrupt to be generated when FIFO_LVL exceeds the FIFO threshold condition.
1	Reserved	0		Reserved
0	SIEN		RW	**System Interrupt Enable.** When asserted permits system interrupts to be generated. Indicates that flicker detection status has changed or SMUX operation has finished.

CONTROL Register (Address 0xFA)

Figure 25:
CONTROL Register

Addr: 0xFA		CONTROL		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:4	Reserved	0		Reserved
3	SW_RESET	0	RW	**Software Reset.** When set the device will force a power on reset.
2	SP_MAN_AZ	0	RW	**Spectral Engine Manual Autozero.** Starts a manual autozero of the spectral engines. Set SP_EN = 0 before starting a manual autozero for it to work.
1	FIFO_CLR	0	RW	**FIFO Buffer Clear.** Clears all FIFO data, FINT, FIFO_OV, and FIFO_LVL.
0	CLEAR_SAI_ACT	0	RW	**Clear Sleep-After-Interrupt Active.** Clears SAI_ACTIVE, ends sleep, and restarts device operation.

10.2.2 ADC Timing Configuration / Integration Time

The integration time is set using the ATIME (0x81) and ASTEP (0xD4, 0xD5) registers. The integration time, in milliseconds, is equal to:

Equation 1: Setting the integration time

$$t_{int} = (ATIME + 1) \times (ASTEP + 1) \times 2.78\mu s$$

It is not allowed that both settings –ATIME and ASTEP – are set to “0”.

The integration time also defines the full-scale ADC value, which is equal to:

Equation 2: ADC full scale value[2]

$$ADC_{fullscale} = (ATIME + 1) \times (ASTEP + 1)$$

ATIME Register (Address 0x81)

Figure 26:
ATIME Register

<table>
<tr><th colspan="2">Addr: 0x81</th><th colspan="4">ATIME</th></tr>
<tr><th>Bit</th><th>Bit Name</th><th>Default</th><th>Access</th><th colspan="2">Bit Description</th></tr>
<tr><td rowspan="5">7:0</td><td rowspan="5">ATIME</td><td rowspan="5">0x00</td><td rowspan="5">RW</td><td colspan="2">Integration Time.
Sets the number of integration steps from 1 to 255.</td></tr>
<tr><td>Value</td><td>Integration Time</td></tr>
<tr><td>0</td><td>ASTEP</td></tr>
<tr><td>n</td><td>ASTEP x (n+1)</td></tr>
<tr><td>255</td><td>ASTEP x 256</td></tr>
</table>

---

[2] The maximum ADC count is 65535. Any ATIME/ASTEP field setting resulting in higher ADC full-scale values would result in a full-scale of 65535.

ASTEP Register (Address 0xD4, 0xD5)

Figure 27:
ASTEP Register

<table>
<tr><th colspan="2">Addr: 0xD4, 0xD5</th><th colspan="4">ASTEP</th></tr>
<tr><th>Bit</th><th>Bit Name</th><th>Default</th><th>Access</th><th colspan="2">Bit Description</th></tr>
<tr><td rowspan="4">7:0</td><td rowspan="4">ASTEP 0xCA</td><td rowspan="9">999</td><td rowspan="9">RW</td><td colspan="2">Integration Time Step Size.
Sets the integration time per step in increments of 2.78 µs. The default value is 999.</td></tr>
<tr><td>VALUE</td><td>STEP SIZE</td></tr>
<tr><td>0</td><td>2.78 µs</td></tr>
<tr><td>n</td><td>2.78 µs x (n+1)</td></tr>
<tr><td rowspan="5">15:8</td><td rowspan="5">ASTEP 0xCB</td><td>599</td><td>1.67 ms</td></tr>
<tr><td>999</td><td>2.78 ms</td></tr>
<tr><td>17999</td><td>50 ms</td></tr>
<tr><td>65534</td><td>182 ms</td></tr>
<tr><td>65535</td><td>Reserved, do not use</td></tr>
</table>

WTIME Register (Address 0x83)

If wait is enabled (WEN = “1” register 0x80), each new measurement is started based on WTIME. It is necessary for WTIME to be sufficiently long for spectral integration and any other functions to be completed within the period. The device will warn the user if the timing is configured incorrectly. If WTIME is too short, then SP_TRIG in register STATUS6 (ADDR: 0xA7) will be set to “1”.

Figure 28:
WTIME Register

<table>
<tr><th colspan="2">Addr: 0x83</th><th colspan="5">WTIME</th></tr>
<tr><th>Bit</th><th>Bit Name</th><th>Default</th><th>Access</th><th colspan="3">Bit Description</th></tr>
<tr><td rowspan="6">7:0</td><td rowspan="6">WTIME</td><td rowspan="6">0x00</td><td rowspan="6">RW</td><td colspan="3">Spectral Measurement Wait Time.
8-bit value to specify the delay between two consecutive spectral measurements.</td></tr>
<tr><td>Value</td><td>Wait Cycles</td><td>Wait Time</td></tr>
<tr><td>0x00</td><td>1</td><td>2.78 ms</td></tr>
<tr><td>0x01</td><td>2</td><td>5.56 ms</td></tr>
<tr><td>n</td><td>n</td><td>2.78 ms x (n+1)</td></tr>
<tr><td>0xff</td><td>256</td><td>711 ms</td></tr>
</table>

10.2.3 ADC Configuration

The following registers provide configuration for the 6 integrated ADCs (CH0 to CH5). It is possible to adjust the gain and setup the auto zero compensation for the ADCs.

CFG1 Register (Address 0xC6)

Figure 29:
CFG1 Register

<table>
<tr><th colspan="3">Addr: 0xC6</th><th colspan="3">CFG1</th></tr>
<tr><th>Bit</th><th>Bit Name</th><th>Default</th><th>Access</th><th colspan="2">Bit Description</th></tr>
<tr><td>7:5</td><td>Reserved</td><td>0</td><td></td><td colspan="2">Reserved</td></tr>
<tr><td rowspan="15">4:0</td><td rowspan="15">AGAIN</td><td rowspan="15">9</td><td rowspan="15">RW</td><td colspan="2">Spectral Engines Gain Setting.
Sets the spectral sensitivity.</td></tr>
<tr><td>VALUE</td><td>GAIN</td></tr>
<tr><td>0</td><td>0.5x</td></tr>
<tr><td>1</td><td>1x</td></tr>
<tr><td>2</td><td>2x</td></tr>
<tr><td>3</td><td>4x</td></tr>
<tr><td>4</td><td>8x</td></tr>
<tr><td>5</td><td>16x</td></tr>
<tr><td>6</td><td>32x</td></tr>
<tr><td>7</td><td>64x</td></tr>
<tr><td>8</td><td>128x</td></tr>
<tr><td>9</td><td>256x</td></tr>
<tr><td>10</td><td>512x</td></tr>
<tr><td>11</td><td>1024x</td></tr>
<tr><td>12</td><td>2048x</td></tr>
</table>

AZ_CONFIG Register (Address 0xDE)

The following register configures how often the spectral engine offsets are reset (auto zero) to compensate for changes of the device temperature. The typical time auto zero needs to be completed is 15 ms.

Figure 30:
AZ_CONFIG Register

<table>
<tr><th>Addr: 0xDE</th><th></th><th colspan="4">AZ_CONFIG</th></tr>
<tr><th>Bit</th><th>Bit Name</th><th>Default</th><th>Access</th><th colspan="2">Bit Description</th></tr>
<tr><td rowspan="8">7:0</td><td rowspan="8">AZ_NTH_ITERATION</td><td rowspan="8">255</td><td rowspan="8">RW</td><td colspan="2">**AUTOZERO FREQUENCY.**
Sets the frequency at which the device performs auto zero of the spectral engines.</td></tr>
<tr><td>**VALUE**</td><td>**AUTOZERO FREQUENCY**</td></tr>
<tr><td>0</td><td>Never (not recommended)</td></tr>
<tr><td>1</td><td>Every integration cycle</td></tr>
<tr><td>2</td><td>Every 2 cycles</td></tr>
<tr><td>…</td><td>Every “AZ_NTH_ITERATION” cycle</td></tr>
<tr><td>254</td><td>Every 254 cycles</td></tr>
<tr><td>255</td><td>Only before first measurement cycle</td></tr>
</table>

CFG8 Register (Address 0xC9)

Figure 31:
CFG8 Register

<table>
<tr><th>Addr: 0xC9</th><th></th><th colspan="4">CFG8</th></tr>
<tr><th>Bit</th><th>Bit Name</th><th>Default</th><th>Access</th><th colspan="2">Bit Description</th></tr>
<tr><td rowspan="6">7:6</td><td rowspan="6">FIFO_TH</td><td rowspan="6">2</td><td rowspan="6">RW</td><td colspan="2">**FIFO Threshold.**
Sets a threshold on the FIFO level that triggers the first FIFO buffer interrupt (FINT).</td></tr>
<tr><td>**VALUE**</td><td>**FIFO_LVL**</td></tr>
<tr><td>0</td><td>1</td></tr>
<tr><td>1</td><td>4</td></tr>
<tr><td>2</td><td>8</td></tr>
<tr><td>3</td><td>16</td></tr>
<tr><td>5:0</td><td>Reserved</td><td>0</td><td></td><td colspan="2">Reserved</td></tr>
</table>

10.2.4 Device Identification

The following registers provided device identification. Device ID, revision ID and auxiliary ID are read only.

AUXID Register (Address 0x58)

Figure 32:
AUXID Register

Addr: 0x58		AUXID		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:4	Reserved			Reserved
3:0	AUXID	0000	R	**Auxiliary Identification.**

REVID Register (Address 0x59)

Figure 33:
REVID Register

Addr: 0x59		REVID		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:3	Reserved			Reserved
2:0	REV_ID	000	R	**Revision Number Identification.**

ID Register (Address 0x5A)

Figure 34:
ID Register

Addr: 0x5A		ID		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	ID	10000001	R	**Part Number Identification.** Value 10000001

10.2.5 Spectral Interrupt Configuration

The spectral interrupt threshold registers provide 16-bit values to be used as the high and low thresholds for comparison to the 16-bit CH0_DATA values (ADC CH0). If SP_IEN (register 0xF9) is enabled and CH0_DATA is not between the two thresholds for the number of consecutive measurements specified in APERS (register 0xBD) an interrupt is set.

SP_TH_L_LSB Register (Address 0x84)

Figure 35:
SP_TH_L_LSB Register

Addr: 0x84		SP_TH_L_LSB		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	SP_TH_L_LSB	0x00	RW	**Spectral Low Threshold LSB.** This register provides the low byte of the low interrupt threshold (CH0).

SP_TH_L_MSB Register (Address 0x85)

Figure 36:
SP_TH_L_MSB Register

Addr: 0x85		SP_TH_L_MSB		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	SP_TH_L_MSB	0x00	RW	**Spectral Low Threshold MSB.** This register provides the high byte of the low interrupt threshold (CH0). Both SP_TH_L registers are combined to a 16-bit threshold. If the value captured by channel 0 is below the low threshold and the APERS value is reached the bit SP_IEN is set and an interrupt is generated. There is an 8-bit data latch implemented that stores the written low byte until the high byte is written. Both bytes will be applied at the same time to avoid an invalid threshold. Note: The LSB register cannot be changed without writing to the MSB register. It is recommended to write to SP_TH_L_LSB and SP_TH_L_MSB within one I^{2}C command.

SP_TH_H_LSB Register (Address 0x86)

Figure 37:
SP_TH_H_LSB Register

Addr: 0x86		SP_TH_H_LSB		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	SP_TH_H_LSB	0x00	RW	**Spectral High Threshold LSB.** This register provides the low byte of the high interrupt threshold (CH0).

SP _TH_H_MSB Register (Address 0x87)

Figure 38:
SP_TH_H_MSB Register

Addr: 0x87		SP_TH_H_MSB		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	SP_TH_H_MSB	0x00	RW	**Spectral High Threshold MSB.** This register provides the high byte of the high interrupt threshold (CH0). Both SP_TH_H registers are combined to a 16-bit threshold. If the value captured by channel 0 is above the high threshold and the APERS value is reached the bit SP_IEN is set and an interrupt is generated.

CFG12 Register (Address 0x66)

Figure 39:
CFG12 Register

<table>
<tr><th colspan="2">Addr: 0x66</th><th colspan="3">CFG12</th></tr>
<tr><th>Bit</th><th>Bit Name</th><th>Default</th><th>Access</th><th>Bit Description</th></tr>
<tr><td>7:3</td><td>Reserved</td><td>0</td><td></td><td>Reserved</td></tr>
<tr><td>2:0</td><td>SP_TH_CH</td><td>0</td><td>RW</td><td>Spectral Threshold Channel.
Sets the channel used for interrupts and persistence, if enabled, to determine device status and gain settings.
<table>
<tr><th>VALUE</th><th>CHANNEL</th></tr>
<tr><td>0</td><td>CH0</td></tr>
<tr><td>1</td><td>CH1</td></tr>
<tr><td>2</td><td>CH2</td></tr>
</table></td></tr>
</table>

Addr: 0x66		CFG12			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
				3	CH3
				4	CH4
				5	CH5

10.2.6 Device Status Registers

The following registers provide status of the device and indicate details about saturation, interrupts, over temperature, device execution and ambient light flicker detection.

STATUS Register (Address 0x93)

The primary status register for AS7343L indicates if there are saturation or interrupt events that need to be handled by the user. This register is self-clearing, meaning that writing a “1” to any bit in the register clears that status bit. In this way, the user should read the STATUS register, handle all indicated event(s) and then write the register value back to STATUS to clear the handled events. Writing “0” will not clear those bits if they have a value of “1”, which means that new events that occurred since the last read of the STATUS register will not be accidentally cleared. In case channel saturation has happened (ASAT) it is recommended to discard the measurement results and re-configure device configuration such as AGAIN and Integration Time to avoid saturation.

Figure 40:
STATUS Register

Addr: 0x93		STATUS		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	ASAT	0	R, SC	**Spectral and Flicker Detect Saturation.** If ASIEN is set, indicates Spectral saturation. Check STATUS2 register to distinguish between analog or digital saturation.
6:4	Reserved	0	R	Reserved
3	AINT	0	R, SC	**Spectral Channel Interrupt.** If SP_IEN is set, indicates that a spectral event that met the programmed thresholds and persistence (APERS) occurred.
2	FINT	0	R, SC	**FIFO Buffer Interrupt.** If FIEN is set, indicates that the FIFO_LVL fulfills the threshold condition. If cleared by writing 1, the interrupt will be asserted again as more data is collected. To fully clear this interrupt, all data must be read from the FIFO buffer.
1	Reserved	0	R	Reserved
0	SINT	0	R, SC	**System Interrupt.**

Addr: 0x93		STATUS		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
				If SIEN is set, indicates that system interrupt is set. Refer to Status5 register.

STATUS 2 Register (Address 0x90)

Figure 41:
STATUS 2 Register

Addr: 0x90		STATUS 2		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	Reserved	0		Reserved
6	AVALID	0	R	**Spectral Valid**. Indicates that the spectral measurement has been completed
5	Reserved	0		Reserved
4	ASAT_DIGITAL	0	R	**Digital Saturation**. Indicates that the maximum counter value has been reached. Maximum counter value depends on integration time set in the ATIME register.
3	ASAT_ANALOG	0	R	**Analog Saturation**. Indicates that the intensity of ambient light has exceeded the maximum integration level for the spectral analog circuit.
2:0	Reserved	0	R	Reserved

STATUS 3 Register (Address 0x91)

Figure 42:
STATUS 3 Register

Addr: 0x91		STATUS 3		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	Reserved	0		Reserved
5	INT_SP_H	0	R	**Spectral Interrupt High.** Indicates that a spectral interrupt occurred because the data exceeded the high threshold.
4	INT_SP_L	0	R	**Spectral Interrupt Low**. Indicates that a spectral interrupt occurred because the data is below the low threshold.
3:0	Reserved	0		Reserved

STATUS 5 Register (Address 0xBB)

Figure 43:
STATUS 5 Register

Addr: 0xBB		STATUS 5		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:3	Reserved	0		Reserved
2	SINT_SMUX	0	R	**SMUX Operation Interrupt.** Indicates that SMUX command execution has finished.
1:0	Reserved	0		Reserved

STATUS 4 Register (Address 0xBC)

Figure 44:
STATUS 4 Register

Addr: 0xBC		STATUS 4		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	FIFO_OV	0	R	**FIFO Buffer Overflow.** Indicates that the FIFO buffer overflowed and information has been lost. Bit is automatically cleared when the FIFO buffer is read
6	Reserved	0	R	Reserved
5	OVTEMP	0	R	**Over Temperature Detected.** Indicates the device temperature is too high. Write 1 to clear this bit.
4:3	Reserved	0		Reserved
2	SP_TRIG	0	R	**Spectral Trigger Error.** Indicates that there is a timing error. The WTIME is too short for the selected ATIME.
1	SAI_ACTIVE	0	R	**Sleep after Interrupt Active.** Indicates that the device is in SLEEP due to an interrupt. To exit SLEEP mode, clear this bit.
0	INT_BUSY	0	R	**Initialization Busy.** Indicates that the device is initializing. This bit will remain 1 for about 300 µs after power on. Do not interact with the device until initialization is complete.

10.2.7 Spectral Data and Status

The ASTATUS register provides saturation and gain status associated to each set of spectral data. Reading the ASTATUS register (0x94) latches all 36 spectral data bytes to that status read. Reading these bytes consecutively (0x94 to 0xB8) ensures that the data is concurrent. All spectral data are stored as 16-bit values. The ASTATUS and spectral data registers are read only.

ASTATUS Register (Address 0x94)

Figure 45:
ASTATUS Register

Addr: 0x94		ASTATUS		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	ASAT_STATUS	0	R, SC	**Saturation Status.** Indicates if the latched data is affected by analog or digital saturation.
6:4	Reserved	0	R	Reserved
3:0	AGAIN_STATUS	0	R, SC	**Gain Status.** Indicates the gain applied for the spectral data latched to this ASTATUS read.

DATA Register (Address 0x95/0xB8)

Figure 46:
DATA_L Register

Addr: 0x95/97/99..B7		DATA_N_L		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	DATA_L	0	R	Spectral Data – low byte

Figure 47:
DATA_H Register

Addr: 0x96/98/9A..B8		DATA_N_H		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	DATA_H	0	R	Spectral Data – high byte

10.2.8 Miscellaneous Configuration

CFG0 Register (Address 0xBF)

Figure 48:
CFG 0 Register

Addr: 0xBF		CFG0		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	Reserved	0		Reserved
5	LOW_POWER	0	RW	**Low Power Idle.** When asserted, the device will automatically run in a low power mode whenever all functions are in wait states or disabled.
4	REG_BANK	0	RW	**Register Bank Access.** 0: Register access to register 0x80 and above 1: Register access to register 0x20 to 0x7F Note: Bit needs to be set to access registers 0x20 to 0x7F. If registers 0x80 and above needs to be accessed bit needs to be set to “0”.
3	Reserved	0		Reserved
2	WLONG	0	RW	**Trigger Long.** Increases the WTIME setting by a factor of 16.
1:0	Reserved	0		Reserved

CFG3 Register (Address 0xC7)

Figure 49:
CFG 3 Register

Addr: 0xC7		CFG3		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:5	Reserved	0		Reserved
4	SAI	0	RW	**Sleep After Interrupt.** If set, the oscillator is turned off whenever an interrupt is active. SAI_ACTIVE is set in this event. To activate the oscillator again, clear all interrupts and clear the SAI_ACTIVE bit.
3:0	Reserved	0xC		Reserved

CFG6 Register (Address 0xF5)

Figure 50:
CFG6 Register

<table>
<tr><th>Addr: 0xF5</th><th></th><th colspan="4">CFG6</th></tr>
<tr><th>Bit</th><th>Bit Name</th><th>Default</th><th>Access</th><th colspan="2">Bit Description</th></tr>
<tr><td rowspan="6">4:3</td><td rowspan="6">SMUX_CMD</td><td rowspan="6">2</td><td rowspan="6">RW</td><td colspan="2">SMUX Command.
Selects the SMUX command to execute when setting SMUXEN gets set. Do not change during ongoing SMUX operation.</td></tr>
<tr><td>VALUE</td><td>SMUX_CMD</td></tr>
<tr><td>0</td><td>ROM code initialization of SMUX</td></tr>
<tr><td>1</td><td>Read SMUX configuration to RAM from SMUX chain</td></tr>
<tr><td>2</td><td>Write SMUX configuration from RAM to SMUX chain</td></tr>
<tr><td>3</td><td>Reserved, do not use</td></tr>
</table>

CFG9 Register (Address 0xCA)

Figure 51:
CFG9 Register

Addr: 0xCA		CFG9		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:5	Reserved	0		Reserved
4	SIEN_SMUX	0	RW	**System Interrupt SMUX Operation.** Enables system interrupt when SMUX command has finished
3:0	Reserved			Reserved

CFG20 Register (Address 0xD6)

Figure 52:
CFG20 Register

Addr: 0xD6		CFG20		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	Reserved			Reserved

Addr: 0xD6		CFG20		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
6:5	auto_smux	0	RW	**Automatic Channel Read-Out.** **0:** 6 Channel FZ, FY, FXL, NIR, 2xVIS, Clear **1:** Reserved **2:** Automatic 12 channel Cycle 1: FZ, FY, FXL, NIR, 2xVIS, Clear Cycle 2: F2, F3, F4, F6, 2xVIS, Clear **3:** Automatic 18 channel Cycle 1: FZ, FY, FXL, NIR, 2xVIS, Clear Cycle 2: F2, F3, F4, F6, 2xVIS, Clear Cycle 3: F1, F5, F7, F8, 2xVIS, Clear Note: The bit “auto_smux” should only be changed before a measurement is started. Once a measurement is started the device is automatically processing the channels as per definition above and storing the measurement results in the eighteen data registers. 2xVIS: Per default the “Top Left” and “Bot Right” VIS/CLEAR PD is read-out
4:0	Reserved			Reserved

PERS Register (Address 0xCF)

Figure 53:
PERS Register

<table>
<tr><th colspan="2">Addr: 0xCF</th><th colspan="4">PERS</th></tr>
<tr><th>Bit</th><th>Bit Name</th><th>Default</th><th>Access</th><th colspan="2">Bit Description</th></tr>
<tr><td>7:4</td><td>Reserved</td><td>0</td><td></td><td colspan="2">Reserved</td></tr>
<tr><td rowspan="8">3:0</td><td rowspan="8">APERS</td><td rowspan="8">0</td><td rowspan="8">RW</td><td colspan="2">Spectral Interrupt Persistence.
Defines a filter for the number of consecutive occurrences that spectral data must remain outside the threshold range between SP_TH_L and SP_TH_H before an interrupt is generated. The spectral data channel used for the persistence filter is set by SP_TH_CHANNEL. Any sample that is inside the threshold range resets the counter to 0.</td></tr>
<tr><td>VALUE</td><td>CHANNEL</td></tr>
<tr><td>0</td><td>Every spectral cycle generates an interrupt</td></tr>
<tr><td>1</td><td>1</td></tr>
<tr><td>2</td><td>2</td></tr>
<tr><td>3</td><td>3</td></tr>
<tr><td>4</td><td>5</td></tr>
<tr><td>5</td><td>10</td></tr>
</table>

Addr: 0xCF		PERS			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
				…	5 x (APERS – 3)
				14	55
				15	60

10.2.9 FIFO Buffer Data and Status

The FIFO buffer is used to poll spectral data with fewer I²C read and write transactions. The FIFO buffer is 256 bytes of RAM containing 128 two-byte datasets. If the FIFO overflows (i.e. 129 datasets before host reads data from the FIFO buffer), an overflow flag will be set and new data will be lost. The Host acquires data by reading addresses: 0xFE – 0xFF. The register address pointer automatically wraps from 0xFF to 0xFE as data are read. Data can be read one byte at a time or in blocks, (there is no block-read length limit). When reading single bytes, the internal FIFO read pointer and the FIFO Buffer Level, FIFO_LVL, are updated each time register 0xFF is read. For block-reads, the internal FIFO read pointer and the FIFO Buffer Level, FIFO_LVL update for each two-byte entry. If the FIFO continues to be accessed after FIFO_LVL = 0, the device will return 0 for all data. The FINT interrupt indicates when there is valid data in the FIFO buffer. The amount of unread data is indicated by the FIFO_LVL.

FIFO_MAP Register (Address 0xFC)

Figure 54:
FIFO_MAP Register

Addr: 0xFC		FIFO_MAP		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	Reserved	0		Reserved
6	FIFO_WRITE_CH5_DATA	0	RW	**FIFO Write CH5 Data.** If set, CH5 data is written to the FIFO Buffer. (two bytes per sample)
5	FIFO_WRITE_CH4_DATA	0	RW	**FIFO Write CH4 Data.** If set, CH4 data is written to the FIFO Buffer. (two bytes per sample)
4	FIFO_WRITE_CH3_DATA	0	RW	**FIFO Write CH3 Data.** If set, CH3 data is written to the FIFO Buffer. (two bytes per sample)
3	FIFO_WRITE_CH2_DATA	0	RW	**FIFO Write CH2 Data.** If set, CH2 data is written to the FIFO Buffer. (two bytes per sample)
2	FIFO_WRITE_CH1_DATA	0	RW	**FIFO Write CH1 Data.** If set, CH1 data is written to the FIFO Buffer. (two bytes per sample)
1	FIFO_WRITE_CH0_DATA	0	RW	**FIFO Write CH0 Data.** If set, CH0 data is written to the FIFO Buffer. (two bytes per sample)
0	FIFO_WRITE_ASTATUS	0	RW	**FIFO Write Status.** If set, ASTATUS (one byte per sample) is written to the FIFO Buffer.

FIFO_LVL Register (Address 0xFD)

Figure 55:
FIFO_LVL Register

Addr: 0xFD		FIFO_LVL		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	FIFO_LVL	0	R	**FIFO Buffer Level.** Indicates the number of entries (each are 2 bytes) available in the FIFO buffer waiting for readout. The FIFO RAM is 256byte, the FIFO_LVL range is from 0 entries to 128 entries.

FDATA Register (Address 0xFE and 0xFF)

Figure 56:
FDATA_L Register

Addr: 0xFE		FDATA_L		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	FDATA	0	R	FIFO Buffer Data

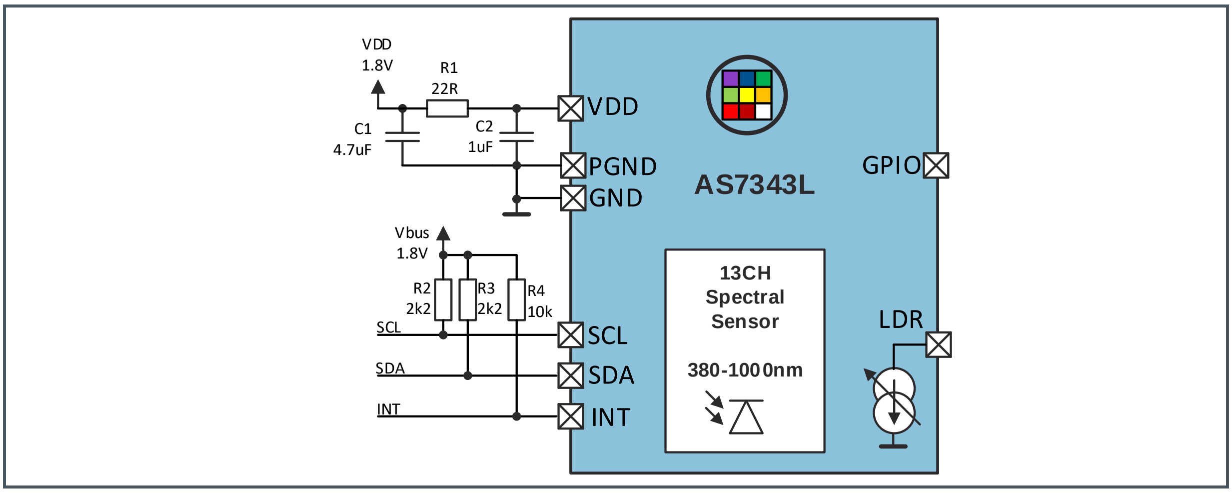
Figure 57:
FDATA_H Register

Addr: 0xFF		FDATA_H		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
15:8	FDATA	0	R	FIFO Buffer Data

11 Application Information

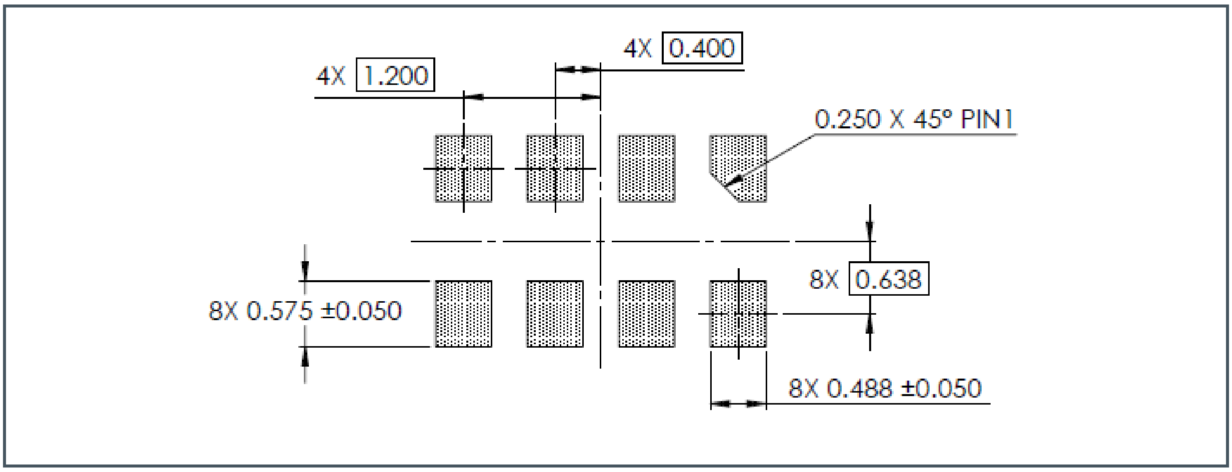
11.1 Schematic

Figure 58:
Application Example



11.2 PCB Pad Layout

Figure 59:
Recommended PCB Pad Layout

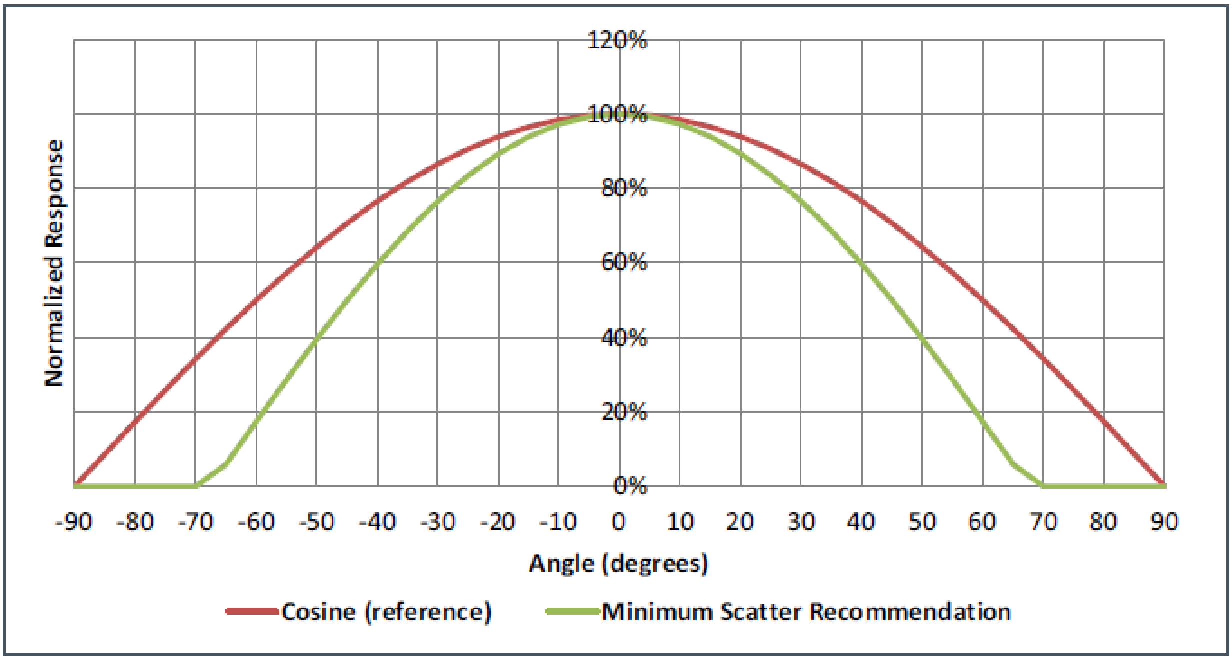


(1) All dimensions are in millimeters.
(2) Dimension tolerances are 0.05 mm unless otherwise noted.
(3) This drawing is subject to change without notice.

11.3 Application Optical Requirements

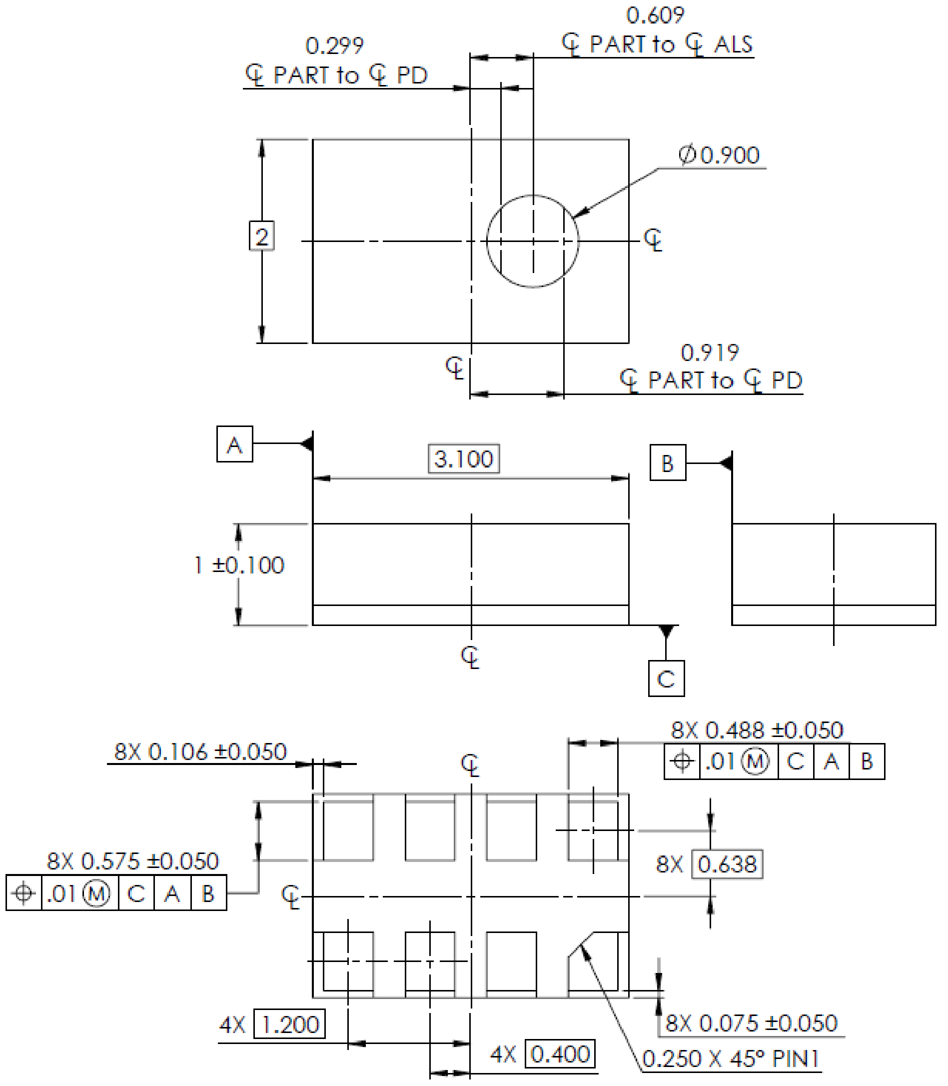
For optimal performance, an achromatic diffuser shall be placed above the device aperture. The recommended solution is a bulk diffuser that meets the minimum recommended scattering characteristic shown below. For more details refer to the optical design guide or contact ams OSRAM.

Figure 60:
Diffuser Characteristics



12 Package Drawings & Markings

Figure 61:
OLGA8 Package Outline Drawing



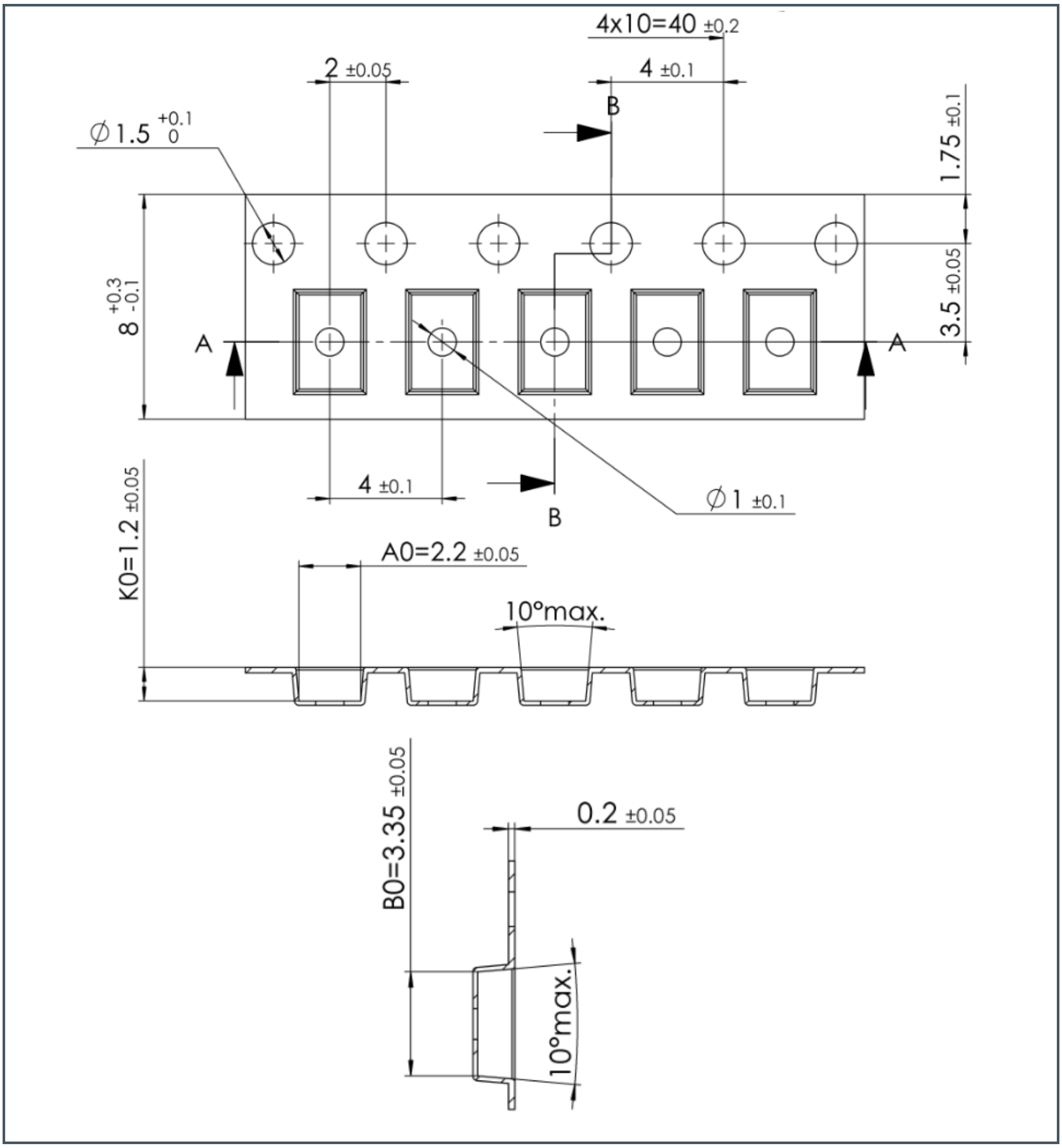
RoHS

Green

(1) All dimensions are in millimeters. Angles in degrees.
(2) Dimensioning and tolerance conform to ASME Y14.5M-1994.
(3) This package contains no lead (Pb).
(4) This drawing is subject to change without notice.

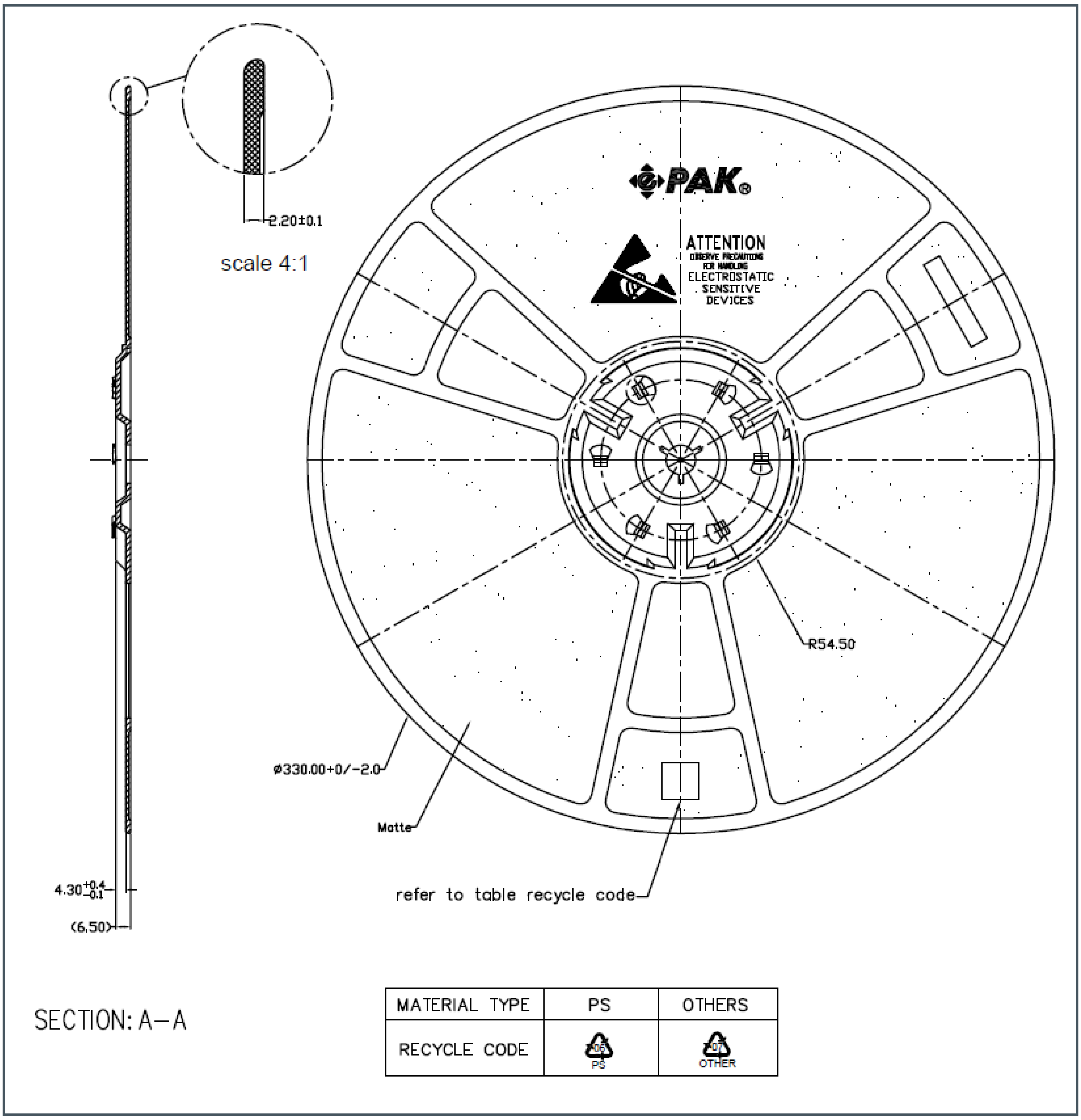
13 Tape & Reel Information

Figure 62:
AS7343L OLGA8 Tape Dimensions



(1) All dimensions are in millimeters. Angles in degrees.
(2) This drawing is subject to change without notice.

Figure 63:
AS7343L OLGA8 Reel Dimensions



MATERIAL TYPE	PS	OTHERS
RECYCLE CODE	06 PS	07 OTHER

(1) All dimensions are in millimeters. Angles in degrees.

(2) This drawing is subject to change without notice.

14 Soldering & Storage Information

The module has been tested and has demonstrated an ability to be reflow soldered to a PCB substrate. The solder reflow profile describes the expected maximum heat exposure of components during the solder reflow process of product on a PCB. Temperature is measured on top of component. The components should be limited to a maximum of three passes through this solder reflow profile.

Figure 64:
Solder Reflow Profile Graph

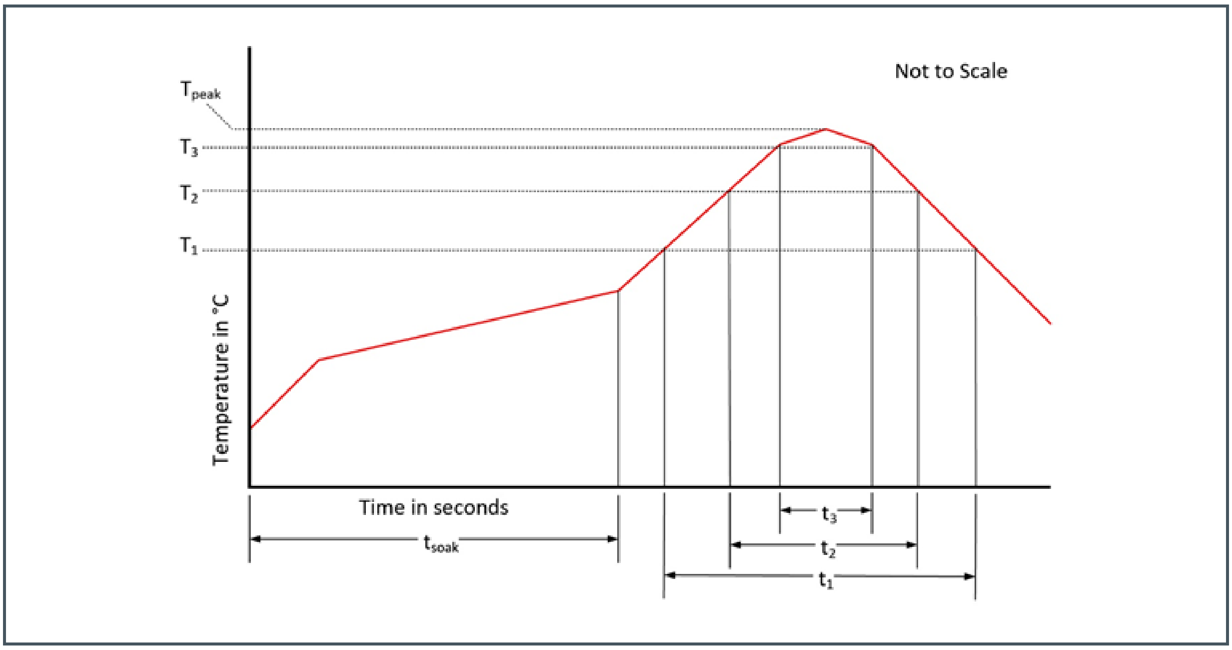


Figure 65:
Solder Reflow Profile

Parameter	Reference	Device
Average temperature gradient in preheating		2.5 °C/s
Soak time	t_{soak}	2 to 3 minutes
Time above 217 °C (T1)	t_1	Max 60 s
Time above 230 °C (T2)	t_2	Max 50 s
Time above T_{peak} – 10 °C (T3)	t_3	Max 10 s
Peak temperature in reflow	T_{peak}	260 °C
Temperature gradient in cooling		Max −5 °C/s

14.1 Storage Information

14.1.1 Moisture Sensitivity

Optical characteristics of the device can be adversely affected during the soldering process by the release and vaporization of moisture that has been previously absorbed into the package.

To ensure the package contains the smallest amount of absorbed moisture possible, each device is baked prior to being dry packed for shipping. Devices are dry packed in a sealed aluminized envelope called a moisture-barrier bag with silica gel to protect them from ambient moisture during shipping, handling, and storage before use.

14.1.2 Shelf Life

The calculated shelf life of the device in an unopened moisture barrier bag is 12 months from the date code on the bag when stored under the following conditions:

- Shelf Life: 12 months
- Ambient Temperature: <40 °C
- Relative Humidity: <90%

Rebaking of the devices will be required if the devices exceed the 12 month shelf life or the Humidity Indicator Card shows that the devices were exposed to conditions beyond the allowable moisture region.

14.1.3 Floor Life

The module has been assigned a moisture sensitivity level of MSL 3. As a result, the floor life of devices removed from the moisture barrier bag is 168 hours from the time the bag was opened, provided that the devices are stored under the following conditions:

- Floor Life: 168 hours
- Ambient Temperature: <30°C
- Relative Humidity: <60%

If the floor life or the temperature/humidity conditions have been exceeded, the devices must be rebaked prior to solder reflow or dry packing.

14.1.4 Rebaking Instructions

When the shelf life or floor life limits have been exceeded, rebake at 50 °C for 12 hours.

15 Revision Information

Document Status	Product Status	Definition
Product Preview	Pre-Development	Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice
Preliminary Datasheet	Pre-Production	Information in this datasheet is based on products in the design, validation or qualification phase of development. The performance and parameters shown in this document are preliminary without any warranty and are subject to change without notice
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Datasheet (discontinued)	Discontinued	Information in this datasheet is based on products which conform to specifications in accordance with the terms of ams-OSRAM AG standard warranty as given in the General Terms of Trade, but these products have been superseded and should not be used for new designs

Changes from previous version to current revision v2-00	Page
Document security class is updated to “Public” in the footer	

- Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
- Correction of typographical errors is not explicitly mentioned.

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