Product Change Notification / SYST-31MBNE432

Date:

05-Sep-2022

Product Category:

8-bit Microcontrollers

PCN Type:

Document Change

Notification Subject:

ERRATA - ATmega32A Silicon Errata and Data Sheet Clarifications

Affected CPNs:

SYST-31MBNE432_Affected_CPN_09052022.pdf
SYST-31MBNE432_Affected_CPN_09052022.csv

Notification Text:

SYST-31MBNE432

Microchip has released a new Errata for the ATmega32A Silicon Errata and Data Sheet Clarifications of devices. If you are using one of these devices please read the document located at ATmega32A Silicon Errata and Data Sheet Clarifications.

Notification Status: Final

Description of Change: Initial document release. • Content moved from the data sheet and restructured to the new document template • Updated the die revision list to reflect die revisions in production Data Sheet Clarifications added: • Errata section in data sheet is no longer valid • 3.2. Watchdog Timer • 3.3. WDTCR

Impacts to Data Sheet: None

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 05 Sep 2022

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices:N/A

Attachments:

ATmega32A Silicon Errata and Data Sheet Clarifications

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Affected Catalog Part Numbers (CPN)

ATMEGA32A-PU
ATMEGA32A-MU
ATMEGA32A-AU
ATMEGA32A-PN
ATMEGA32A-MN
ATMEGA32A-AN
ATMEGA32A-MNR
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ATMEGA32A-AUR
ATMEGA32A-AURA5

ATmega32A

ATmega32A Silicon Errata and Data Sheet Clarification

Introduction

The ATmega32A devices you have received conform functionally to the current device data sheet (DS40002072), except for the anomalies described in this document. The errata described in this document will likely be addressed in future revisions of the ATmega32A devices.

Note:

- This document summarizes all the silicon errata issues from all silicon revisions, previous and current.

Table of Contents

1. Silicon Issue Summary

- Erratum is not applicable.

X Erratum is applicable.

Peripheral	Short Description	Valid for Silicon Revision		
		Rev. G(1)	Rev. I	Rev. K
Analog Comparator	2.2.1. First Analog Comparator Conversion May be Delayed	X	X	X
Timer	2.3.1. Interrupts May Be Lost When Writing the Timer Registers in the Asynchronous Timer (Timer/Counter 2)	X	X	X
JTAG Interface	2.4.1. IDCODE Masks Data From TDI Input	X	X	X
Memories	2.5.1. Reading EEPROM by Using ST or STS to Set EERE Bit Triggers Unexpected Interrupt Request	X	X	X

Note:

1. This revision is the initial release of the silicon.

2. Silicon Errata Issues

2.1 Errata Details

- Erratum is not applicable.

X Erratum is applicable.

2.2 Analog Comparator

2.2.1 First Analog Comparator Conversion May be Delayed

If a slow-rising V_{CC} powers the device, the first Analog Comparator conversion will take longer than expected on some devices.

Work Around

When the device has been powered or reset, disable and enable the Analog Comparator before the first conversion.

Affected Silicon Revisions

ATmega32A		
Rev. G	**Rev. I**	**Rev. K**
X	**X**	**X**

2.3 Interrupts

2.3.1 Interrupts May Be Lost When Writing the Timer Registers in the Asynchronous Timer (Timer/Counter 2)

The interrupt will be lost if writing one of the registers Timer/Counter 2 Control Register (TCCR2), Timer/Counter 2 Register (TCNT2), or Timer/Counter 2 Output Compare Register (OCR2) when the Timer/Counter 2 Register is `0x00`.

Work Around

Always check that the asynchronous Timer/Counter register (TCNT2) neither has the value `0xFF` nor `0x00` before writing to the Timer/Counter 2 Control Register (TCCR2), Timer/Counter 2 Register (TCNT2), or Timer/Counter 2 Output Compare Register (OCR2).

Affected Silicon Revisions

ATmega32A		
Rev. G	**Rev. I**	**Rev. K**
X	**X**	**X**

2.4 JTAG Interface

2.4.1 IDCODE Masks Data From TDI Input

The JTAG instruction IDCODE is not working correctly. Data to succeeding devices are replaced by all-ones during Update-DR.

Work Around

- The problem is not visible if ATmega32A is the only device in the scan chain
- Select the Device ID Register of the ATmega32A by issuing the IDCODE instruction or by entering the Test-Logic-Reset state of the TAP controller to read out the contents of its Device ID Register and possibly data from succeeding devices of the scan chain. Issue the BYPASS instruction to the ATmega32A while reading the Device ID Registers of preceding devices of the boundary scan chain
- If the Device IDs of all devices in the boundary scan chain are captured simultaneously, the ATmega32A must be the first device in the chain

Affected Silicon Revisions

ATmega32A		
Rev. G	Rev. I	Rev. K
X	X	X

2.5 Memories

2.5.1 Reading EEPROM by Using ST or STS to Set EERE Bit Triggers Unexpected Interrupt Request

Reading EEPROM using the ST or STS command to set the EERE bit in the EECR register triggers an unexpected EEPROM interrupt request.

Work Around

Always use OUT or SBI to set EERE in EECR.

Affected Silicon Revisions

ATmega32A		
Rev. G	Rev. I	Rev. K
X	X	X

3. Data Sheet Clarifications

Note the following typographic corrections and clarifications for the latest version of the device data sheet (DS40002072).

Note: Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

3.1 Errata Section in Data Sheet is no Longer Valid

A clarification for the Errata section in the device data sheet has been made.

The errata content has been moved to a separate document, *ATmega32A Silicon Errata and Data Sheet Clarification* (this document).

See the *Silicon Errata Issues* section of this document for the latest errata.

3.2 Watchdog Timer

A clarification has been made for the typical Watchdog Timer oscillator frequency.

The Watchdog Timer is clocked from a separate On-chip Oscillator which runs at **1.25 MHz**. A typical value at V_{CC} = 5V and a temperature of 25°C. See characterization data for typical values at other V_{CC} levels and/or temperatures. The Watchdog Reset interval can be adjusted by controlling the Watchdog Timer prescaler, as shown in Table 11-1 on page 50. The WDR – Watchdog Reset – instruction resets the Watchdog Timer. The Watchdog Timer is also reset when it is disabled and when a Chip Reset occurs. Eight different clock cycle periods can be selected to determine the reset period. If the reset period expires without another Watchdog Reset, the ATmega32A resets and executes from the Reset Vector. For timing details on the Watchdog Reset, refer to page 47.

3.3 Watchdog Timer Control Register

Name: WDTCR
Offset: -
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
				WDTOE	WDE	WDP[2:0]		
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bit 4 – WDTOE Watchdog Turn-off Enable

Set this bit when the WDE bit is written to logic zero. Otherwise, the Watchdog will not be disabled. Once written to one, hardware will clear this bit after four clock cycles. Refer to the description of the WDE bit for a Watchdog disable procedure.

Bit 3 – WDE Watchdog Enable

When the WDE is written to logic one, the Watchdog Timer is enabled, and if the WDE is written to logic zero, the Watchdog Timer function is disabled. WDE can only be cleared if the WDTOE bit has logic level one. Follow this procedure to disable an enabled Watchdog Timer:

1. In the same operation, write a logic one to WDTOE and WDE. Write a logic one to WDE even though it is set to one before the disable operation starts.
2. Within the following four clock cycles, write a logic 0 to WDE, which disables the Watchdog.

Bits 2:0 – WDP[2:0] Watchdog Timer Prescaler

The WDP2, WDP1, and WDP0 bits determine the Watchdog Timer prescaling when the Watchdog Timer is enabled. The table below shows the different prescaling values and their corresponding Timeout Periods.

Table 3-1. Watchdog Timer Prescale Select

WDP2	WDP1	WDP0	Number of WDT Oscillator Cycles	Typical Time-Out at V_{CC} = 3.0V	Typical Time-Out at V_{CC} = 5.0V
0	0	0	16K (16,384)	**14 ms**	**13 ms**
0	0	1	32K (32,768)	**28 ms**	**26 ms**
0	1	0	64K (65,536)	**56 ms**	**52 ms**
0	1	1	128K (131,072)	**0.11s**	**0.10s**
1	0	0	256K (262,144)	**0.22s**	**0.21s**
1	0	1	512K (524,288)	**0.45s**	**0.42s**
1	1	0	1,024K (1,048,576)	**0.89s**	**0.84s**
1	1	1	2,048K (2,097,152)	**1.8s**	**1.7s**

The following code example shows one assembly and one C function for turning off the WDT. It assumes that interrupts are controlled (e.g, by disabling interrupts globally) so that no interrupts will occur during the execution of these functions.

Assembly Code Example

```
WDT_off:
    ; reset WDT
    wdr
    ; Write logical one to WDTOE and WDE
    in r16, WDTCR
    ori r16, (1<<WDTOE)|(1<<WDE)
    out WDTCR, r16
    ; Turn off WDT
    ldi r16, (0<<WDE)
    out WDTCR, r16
    ret
```

C Code Example

```
void WDT_off(void)
{
    /* reset WDT */
    _WDR();
    /* Write logical one to WDTOE and WDE */
    WDTCR |= (1<<WDTOE) | (1<<WDE);
    /* Turn off WDT */
    WDTCR = 0x00;
}
```

4. Document Revision History

Note: The document revision is independent of the silicon revision.

4.1 Revision History

Doc Rev.	Date	Comments
A	09/2022	Initial document release. • Content moved from the data sheet and restructured to the new document template • Updated the die revision list to reflect die revisions in production Data Sheet Clarifications added: • Errata section in data sheet is no longer valid • 3.2. Watchdog Timer • 3.3. WDTCR

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