Product Change Notification / SYST-12QCOX081

Date:

14-Sep-2022

Product Category:

CAN Controller with integrated Transceiver

PCN Type:

Document Change

Notification Subject:

ERRATA - MCP251863 Silicon Errata

Affected CPNs:

SYST-12QCOX081_Affected_CPN_09142022.pdf
SYST-12QCOX081_Affected_CPN_09142022.csv

Notification Text:

SYST-12QCOX081

Microchip has released a new Errata for the MCP251863 Silicon Errata of devices. If you are using one of these devices please read the document located at MCP251863 Silicon Errata.

Notification Status: Final

Description of Change: Initial release of this document

Reason for Change: To Improve Productivity
Impacts to Data Sheet: None

Change Implementation Status: Complete

Date Document Changes Effective: 14 Sep 2022

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices::N/A

Attachments:

MCP251863 Silicon Errata

Please contact your local Microchip sales office with questions or concerns regarding this notification.

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Affected Catalog Part Numbers (CPN)

MCP251863T-H/SS
MCP251863T-H/SSVAO
MCP251863T-E/SS
MCP251863T-E/SSVAO

MCP251863

MCP251863
Silicon Errata and Data Sheet Clarification

The functionality of the MCP251863 devices is described in the Device Data Sheet (DS20006624A), except for the anomalies described below.

1. Module: SPI Module

Incorrect data for certain READ/READ_CRC commands:

There is a possibility that the transmitted data on a READ/READ_CRC is wrong when reading from the chip. A glitch on the SDO line shorter than 1 bit in length occurs and creates wrong data.

Fix/Work Around

Only use the READ_CRC command, and if a CRC mismatch occurs, re-issue the READ_CRC command.

The following registers can be affected:

CiTXIF

CiRXIF

CiCON

CiTBC

CiINT

CiRXOVIF

CiTXATIF

CiTXREQ

CiTREC

CiBDIAG0

CiBDIAG1

CiTXQSTA

CiFIFOSTAm

The occurrence can be minimized by not using FIFOs 7/15/23/31.

Bit 31 of RAM reads with CRC can also be affected. This can be avoided by reading from a receive FIFO only after the message was loaded into the FIFO, indicated by the receive flags. This is the recommended procedure independent of the issue described here.

2. Module: ECC Module

ECC Single Error Correction does not work in all cases:

Fix/Work Around:

Enable Single Error Correction (SEC) and Double Error Detection (DED) interrupts by setting SECIE and DEDIE. Handle SECIF as a detection interrupt and do not rely on the error correction. Instead, handle both interrupts as a notification that the RAM word at ERRADDR was corrupted.

3. Module: SPI Module

SFR address rollover does not work:

The SFR address rollover, from 0x3FF to 0x000 and from 0xFFF to 0xE00, does not work. Instead, the address changes from 0x3FF to 0x400 and from 0xFFF to 0x000.

The address rollover for the RAM works as described.

Fix/Work Around:

None.

4. Module: SPI/RAM Module

The SPI can write corrupted data to the RAM at fast SPI speeds:

Simultaneous activity on the CAN bus while writing data to RAM via the SPI interface, with high SCK frequency, can lead to corrupted data being written to RAM.

Fix/Work Around:

Ensure that FSCK is less than or equal to 0.85 * (FSYSCLK/2).

5. Module: SPI/GPIO Module

Writing multiple bytes to the IOCON register using one SPI `WRITE` instruction may overwrite LAT0 and LAT1:

Writing Byte 2 and Byte 3 of the IOCON register using one SPI `WRITE` instruction clears LAT0 and LAT1.

Fix/Work Around:

When setting LAT0 or LAT1, do not use a multi-data byte SPI `WRITE` instruction.

Instead, write the bit fields in the IOCON register using single data byte SFR `WRITE` instructions.

Clarifications/Corrections to the Data Sheet

In the MCP251863 Data Sheet (DS20006624A), the following clarifications and corrections should be noted.

None.

APPENDIX A: REVISION HISTORY

Revision A (September 2022)

- Initial release of this document

NOTES:

Note the following details of the code protection feature on Microchip products:

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