UM11697

$\frac{\text{RDGD31603PSMKEVM three-phase inverter kit}}{\text{Rev. 2} - \text{13 June 2022}}$

User manual

Document information

Information	Content
Keywords	GD3160, gate, driver, power, inverter, Automotive
Abstract	The RDGD31603PSMKEVM three-phase inverter is a functional hardware power inverter reference design which can be used as a foundation to develop a complete ASIL-D compliant high voltage, high-power traction motor inverter for electric vehicles. The kit can be used as a double pulse and short circuit tester to measure key switching parameters, or as a three-phase inverter for motor control. This board is compatible with eMPack power modules and application kit eMP1300MD12SC2S-APK from Semikron.



RDGD31603PSMKEVM three-phase inverter kit

Revision History

Revision history

Rev	Date	Description
UM11697 v1	20211210	Initial version
UM11697 v2	20220613	 Added last sentence to Abstract on page 1 Section 1: Added paragraph: "This board is compatible with" Section 2 Removed "on the NXP web site" from section title Added last paragraph: "All information regarding eMPack" Section 3.2 Removed from list: Compatible eMPack power module from Semikron DClink capacitor compatible with eMPack power module Added to list: Compatible with eMPack application kit (eMP1300MD12SC2S-APK, article number 19285392) from Semikron. Section 4.1, third list item: Changed to "Capability to connect to eMPack power modules family for full" from "Capability to connect to eMPack specific modules for full" Figure 8: Added description: "This board is compatible with eMPack SiC power modules (eMP1300MD12SC2S)" Added Figure 9
		 Added Figure 9 Section 4.2.9: Added "/SiC" to section title Section 4.2.9.1 First paragraph: Changed to "channel gate driver for IGBTs and SiC devices." from "channel gate driver for IGBTs." Second paragraph: Changed to "minimizes power module stress during faults." from "minimizes IGBT stress during faults. Third paragraph: Changed to "gates of most power modules." from "gates of most IGBTs." Section 4.2.9.2, ninth list item: Changed to "IGBTs/SiC, power range > 125 kW" from "IGBTs, power range > 125 kW" Removed section 4.2.10 IGBT pin connections Section 6 Removed from list: DC link capacitor compatible with eMPack module Compatible eMPack IGBT or SiC module Added to list: "Compatible eMPack application kit (power module, cooler plate and DClink capacitor) (eMP1300MD12SC2S-APK, article number 19285392) from Semikron." Section 7: Changed to "RDGD31603PSMKEVM" from "RDGD3160I3PH5EVM"

RDGD31603PSMKEVM three-phase inverter kit

Important notice

NXP provides the enclosed product(s) under the following conditions:

This reference design is intended for use of ENGINEERING DEVELOPMENT OR EVALUATION PURPOSES ONLY. It is provided as a sample IC pre-soldered to a printed circuit board to make it easier to access inputs, outputs, and supply terminals. This reference design may be used with any development system or other source of I/O signals by simply connecting it to the host MCU or computer board via off-the-shelf cables. The final device in an application will be heavily dependent on proper printed circuit board layout and heat sinking design, as well as attention to supply filtering, transient suppression, and I/O signal quality.

The goods provided may not be complete in terms of required design, marketing, and/ or manufacturing related protective considerations, including product safety measures typically found in the end product incorporating the goods. Due to the open construction of the product, it is the user's responsibility to take any and all appropriate precautions with regard to electrostatic discharge. In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards. For any safety concerns, contact NXP sales and technical support services.

RDGD31603PSMKEVM three-phase inverter kit

1 Introduction

This document is the user guide for the RDGD31603PSMKEVM reference design. It is intended for engineers involved in evaluation, design, implementation and validation using GD3160, a single-channel gate driver for insulated-gate bipolar transistor/silicon carbide (IGBT/SiC) devices.

The scope of this document is to provide the user with information to evaluate the GD3160. The kit can be used as a double pulse and short circuit tester to measure key switching parameters or used as a three phase inverter for motor control. This document covers connecting the hardware, installing the software and tools, configuring the environment and using the kit.

The RDGD31603PSMKEVM is a fully functional three-phase inverter evaluation board populated with six GD3160 gate drivers with fault management and supporting circuitry. This board supports SPI daisy chain communication for programming and communication with three high-side gate drivers and three low-side gate drivers independently.

This board is compatible with eMPack SiC power modules (EMP1300MD12SC2SV1DPD) and application kit (eMP1300MD12SC2S-APK) from Semikron.

The RDGD31603PSMKEVM has low-voltage and high-voltage isolation in conjunction with gate drive integrated galvanic signal isolation. Other supporting features on the board include desaturation short-circuit detection, IGBT/SiC temperature sensing, and DC Link bus voltage monitoring. See the GD3160 data sheet for additional gate drive features.

2 Finding kit resources and information

NXP Semiconductors provides online resources for this reference design and its supported device(s) on http://www.nxp.com.

The information page for the RDGD31603PSMKEVM reference design is at www.nxp.com/RDGD31603PSMKEVM. This page provides overview information, documentation, software and tools, parametrics, ordering information and a **Getting Started** tab. The **Getting Started** tab provides quick-reference information applicable to using the RDGD31603PSMKEVM reference design, including the downloadable assets referenced in this document.

All information regarding eMPack power modules and application kit can be found at https://www.semikron.com.

2.1 Collaborate in the NXP community

The NXP community is for sharing ideas and tips, asking and answering technical questions, and receiving input on just about any embedded design topic.

The NXP community is at http://community.nxp.com.

3 Getting started

Working with the RDGD31603PSMKEVM requires kit contents and a Windows PC workstation with FlexGUI software installed.

UM11697

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RDGD31603PSMKEVM three-phase inverter kit

3.1 Kit contents

- Assembled and tested RDGD31603PSMKEVM (three-phase inverter populated with 5.0 V compatible gate driver devices) board in an anti-static bag
- 3.3 V to 5.0 V translator board connected to FRDM-KL25Z MCU (KITGD3160TREVB) with micro-USB cable for using FlexGUI software control
- · Quick Start Guide

3.2 Additional hardware

In addition to the kit contents, the following hardware is necessary or beneficial when working with this kit.

- Microcontroller for SPI communication
- Compatible with eMPack application kit (eMP1300MD12SC2S-APK, article number 19285392) from Semikron.
- · HV power supply with protection shield and hearing protection
- · Current sensors for monitoring each phase current
- 12 V, 1.0 A DC power supply
- 4-channel oscilloscope with appropriate isolated probes

3.3 Windows PC workstation

This reference design requires a Windows PC workstation. Meeting these minimum specifications should produce great results when working with this reference design.

• USB-enabled computer with Windows 8 or Windows 10

3.4 Software

The Flex GUI software must be installed in order to use this kit. All listed software is available on the information page at http://www.nxp.com/RDGD31603PSMKEVM.

• Flex GUI software for using with KITGD3160TREVB MCU/translator board

4 Getting to know the hardware

4.1 RDGD31603PSMKEVM features

- Capability to perform double pulse and short-circuit tests on Phase U using KITGD3160TREVB and FlexGUI. See schematics for phase U and FlexGUI Pulse tab (<u>Figure 32</u> and <u>Figure 33</u>)
- Evaluation board designed for and populated with GD3160 Gate Drivers and protection circuitry
- Capability to connect to eMPack power modules family for full three-phase evaluation and development (see <u>Figure 8</u> for specific module pin placement)
- Daisy chain SPI communication (three high-side and three low-side gate drivers)
- Variable fly-back VCC power supply with GND reference and variable VEE supply
- · Easy access power, ground, and signal test points
- · Optional connection for DC bus voltage monitoring

UM11697

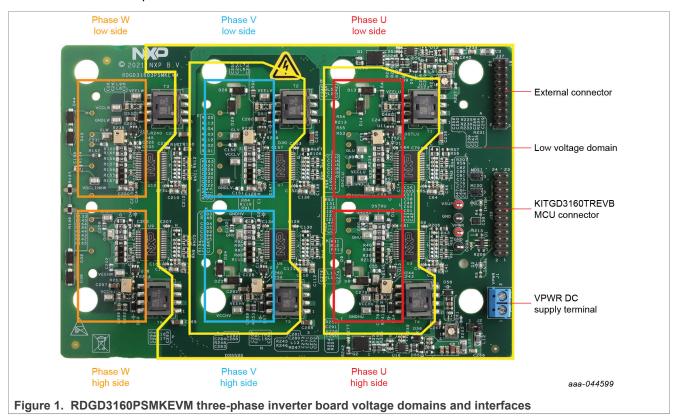
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4.2 Kit featured components

4.2.1 Voltage domains, GD3160 pinout, logic header, and IGBT pinout

The low-voltage domain is an externally supplied 12 V DC (VPWR) primary supply for non- isolated circuits, typically supplied by a vehicle battery. The low-voltage domain includes the interface between the MCU and GD3160 control registers and logic control.

The low-side driver and high-side driver domains are isolated high-voltage driver control domains for SiC MOSFET or IGBT single phase connections and control circuits. The pins on the bottom of the board are designed to easily connect to a compatible three-phase SiC MOSFET or IGBT module.



4.2.2 GD3160 pinout and MCU interface pinout

See the GD3160 advanced IGBT/SiC gate driver data sheet for specific information about pinout, pin descriptions, specifications, and operating modes. The VSUP/VPWR DC supply terminal is a low voltage input connection for supplying power to the low voltage non- isolated die and related circuitry. A GD3160 application is typically supplied by a +12 V DC vehicle battery.

The KITGD3160TREVB MCU/translator included with the kit can be attached to this board at the 24 pin dual row header pin interface. All gate drivers can be accessed via SPI control using FlexGUI software.

The external connector (20 pin) can be used for monitoring interrupts, PWM inputs, and other miscellaneous logic I/O signals from gate drive devices. See schematic for details.

RDGD31603PSMKEVM three-phase inverter kit

Note: Double pulse and short-circuit tests can be conducted on Phase U only. See FlexGUI Pulse tab, see <u>Figure 32</u> and <u>Figure 33</u>.

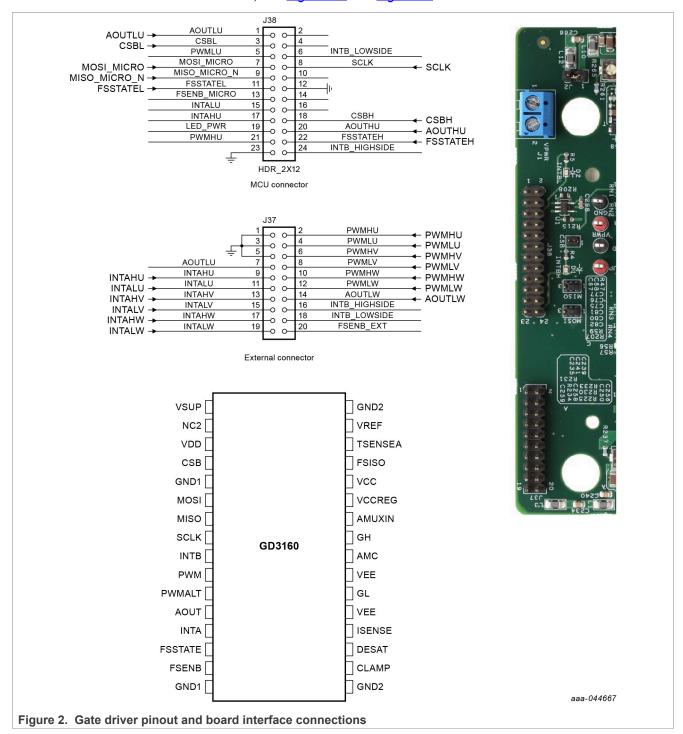


Table 1. MCU connector (J38) pin definitions

Pin	Name	Function
1	AOUTLU	GD3160 analog output signal low-side U phase
2	n.c.	not connected

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Table 1. MCU connector (J38) pin definitions...continued

Pin	Name	Function
3	CSBL	Chip select bar to low-side gate drivers
4	n.c.	not connected
5	PWMLU	Pulse width modulation low-side phase U
6	INTB LOW SIDE	GD3160 fault reporting/monitoring output pin for low-side devicees
7	MOSI_MICRO	SPI target in signal
8	SCLK	SPI clock
9	MISO_MICRO_N	SPI target out signal
10	n.c.	not connected
11	FSSTATEL	Fail-safe state low-side input
12	GND	Ground
13	FSENB_MICRO	Fail-safe enable bar input
14	n.c.	not connected
15	INTALU	GD3160 fault reporting/monitoring output pin for low-side phase U
16	n.c.	not connected
17	INTAHU	GD3160 fault reporting/monitoring output pin for high-side phase U
18	CSBH	Chip select bar to high-side gate drivers
19	LED_PWR	5 V pull-up for LED interrupt indicators
20	AOUTHU	GD3160 analog output signal high-side U phase
21	PWMHU	Pulse width modulation high-side phase U
22	FSSTATEH	Fail-safe state high-side input
23	GND	Ground
24	INTB_HIGH SIDE	GD3160 fault reporting/monitoring output pin for high-side

Table 2. External connector (J38) pin definition

Pin	Name	Function
1	GND	ground
2	PWMHU	Pulse width modulation input high-side phase U
3	GND	ground
4	PWMLU	Pulse width modulation input low-side phase U
5	GND	ground
6	PWMHV	Pulse width modulation input high-side phase V
7	AOUTLU	GD3160 duty cycle encoded analog output signal low-side U phase
8	PWMLV	Pulse width modulation input low-side phase U
9	INTAHU	GD3160 fault reporting/monitoring output pin for high-side phase U
10	PWMHW	Pulse width modulation input high-side phase W
11	INTALU	GD3160 fault reporting/monitoring output pin for low-side phase U

UM11697

User manual

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RDGD31603PSMKEVM three-phase inverter kit

Table 2. External connector (J38) pin definition...continued

Pin	Name	Function
12	PWMLW	Pulse width modulation input low-side phase W
13	INTAHV	GD3160 fault reporting/monitoring output pin for high-side phase V
14	AOUTLW	GD3160 analog output signal low-side W phase
15	INTALV	GD3160 fault reporting/monitoring output pin for low-side phase V
16	INTB_HIGH SIDE	GD3160 fault reporting output all high-side gate drivers
17	INTAHW	GD3160 fault reporting/monitoring output pin for high-side phase W
18	INTB_LOW SIDE	GD3160 fault reporting output all low-side gate drivers
19	INTALW	GD3160 fault reporting/monitoring output pin for low-side phase W
20	FSENB EXT	Active-low Fail Safe control input (leave open if unused)

4.2.3 Test points

All test points are clearly marked on the board. The following figure shows the location of various test points.

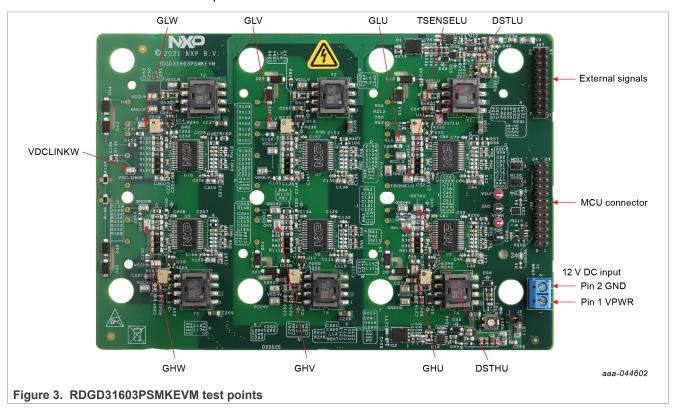


Table 3. Test points

Table 6. Test points	
Test point name	Function
DSTHU	DESAT high-side U phase VCE desaturation connected to DESAT pin circuitry
DSTLU	DESAT low-side U phase VCE desaturation connected to DESAT pin circuitry
GHU	Gate high-side U phase
GHV	Gate high-side V phase

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RDGD31603PSMKEVM three-phase inverter kit

Table 3. Test points...continued

Test point name	Function
GHW	Gate high-side W phase
GLU	Gate low-side U phase
GLV	Gate low-side V phase
GLW	Gate low-side W phase
TSENSELU	Temperature sense test point low-side U phase input to TSENSEA
VDCLINKW	DC link voltage test point low-side W phase input to AMUXIN

4.2.4 Indicators

The RDGD31603PSMKEVM evaluation board contains LEDs as visual indicators on the board.



Table 4. RDGD31603PSMKEVM indicator descriptions

Name	Description
INTBL LED	Indicates that a GD3160 INTB fault interrupt has occurred on the low side devices
INTBH LED	Indicates that a GD3160 INTB fault interrupt has occurred on the high side devices

RDGD31603PSMKEVM three-phase inverter kit

4.2.5 Connectors, jumpers and potentiometers

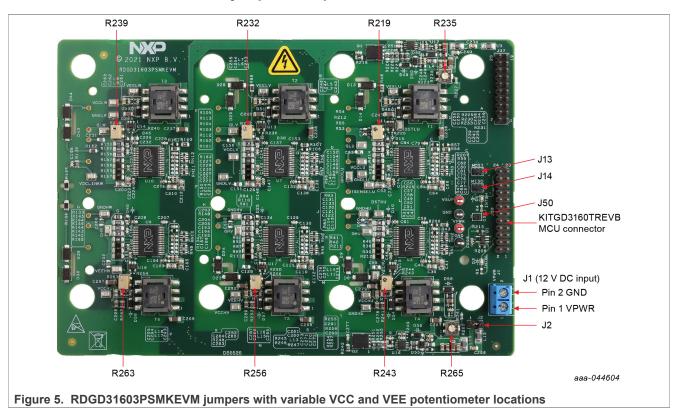


Table 5. RDGD31603PSMKEVM connector, jumper and potentiometer descriptions

Name	Description
J2	Jumper 1-2 default - DC supply for VSUP to gate drivers supplied through J1 terminal connection Jumper Open VSUP supply to gate drivers isolated
J13	Jumper 1-2 default MOSI – Normal mode three device daisy chain three device high side, three device low side (x3 – 2 channel) Jumper 2-3 MOSI - Six device daisy chain all six gate drivers daisy chained together (x6 – 1 channel)
J14	Jumper 1-2 default MISO-Normal mode three device daisy chain three device high side, three device low side (x3 – 2 channel) Jumper 2-3 MISO - Six device daisy chain all six gate drivers daisy chained together (x6 – 1 channel)
J50	Jumper open default CSB-Normal mode three device high side, three device low side (x3 - 2 channel) Jumper 1-2 CSB - Six device daisy chain all six gate drivers daisy chained together (x6 - 1 channel)
J37 External signals	Miscellaneous PWM and Interrupt signals (See schematic for details)
J38 MCU Signals	Two-row header of all MCU signals for debug and development. (See schematic for details)
J1 VPWR terminal connector	Used for external low voltage power supply connection, typically 12 V Vbatt
R265	5 k Ω pot to adjust fly-back VCC level all high-side gate drivers
R235	$5~\text{k}\Omega$ pot to adjust fly-back VCC level all low-side gate drivers

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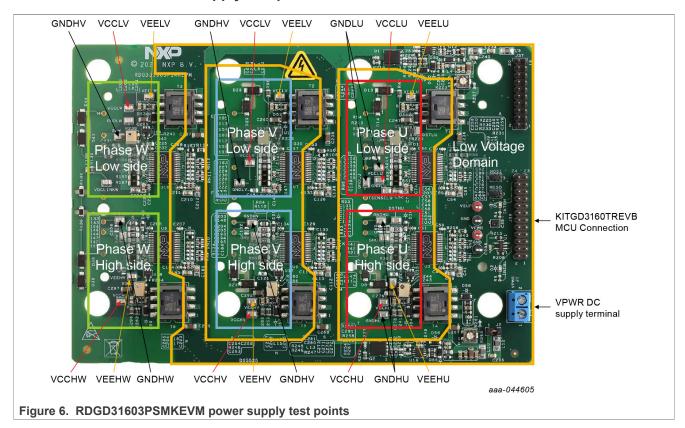
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Table 5. RDGD31603PSMKEVM connector, jumper and potentiometer descriptions...continued

Name	Description
R243	1 k Ω pot to adjust VEE level high-side phase U
R219	1 k Ω pot to adjust VEE level low-side phase U
R256	1 k Ω pot to adjust VEE level high-side phase V
R232	1 k Ω pot to adjust VEE level low-side phase V
R263	1 k Ω pot to adjust VEE level high-side phase W
R239	1 k Ω pot to adjust VEE level low-side phase W

4.2.6 Power supply test points



Name	Function
VCCHU	High-side phase U VCC voltage test point Isolated positive voltage supply (11 V to 28 V)
VEEHU	High-side phase U VEE voltage test point Isolated negative voltage supply (-1.25 V to -7.5 V)
GNDHU	High-side phase U isolated ground
VCCHV	High-side phase V VCC voltage test point Isolated positive voltage supply (11 V to 28 V)
VEEHV	High-side phase V VEE voltage test point Isolated negative voltage supply (-1.25 V to -7.5 V)
GNDHV	High-side phase V isolated ground
VCCHW	High-side phase W VCC voltage test point Isolated positive voltage supply (11 V to 28 V)

UM11697

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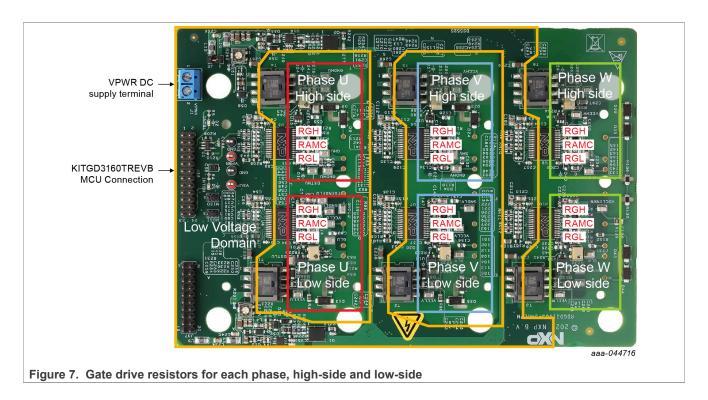
RDGD31603PSMKEVM three-phase inverter kit

Name	Function
VEEHW	High-side phase W VEE voltage test point Isolated negative voltage supply (-1.25 V to -7.5 V)
GNDHW	High-side phase V isolated ground
VCCLU	Low-side phase U VCC voltage test point Isolated positive voltage supply (11 V to 28 V)
VEELU	Low-side phase U VEE voltage test point Isolated negative voltage supply (-1.25 V to -7.5 V)
GNDLU	Low-side phase U isolated ground
VCCLV	Low-side phase V VCC voltage test point Isolated positive voltage supply (11 V to 28 V)
VEELV	Low-side phase V VEE voltage test point Isolated negative voltage supply (-1.25 V to -7.5 V)
GNDLV	Low-side phase V isolated ground
VCCLW	Low-side phase W VCC voltage test point Isolated positive voltage supply (11 V to 28 V)
VEELW	Low-side phase W VEE voltage test point Isolated negative voltage supply (-1.25 V to -7.5 V)
GNDLW	Low-side phase W isolated ground
VPWR/VSUP	+12 V DC VPWR low voltage positive supply connection (+12 V DC)
GND	VPWR/VSUP low voltage supply ground connection

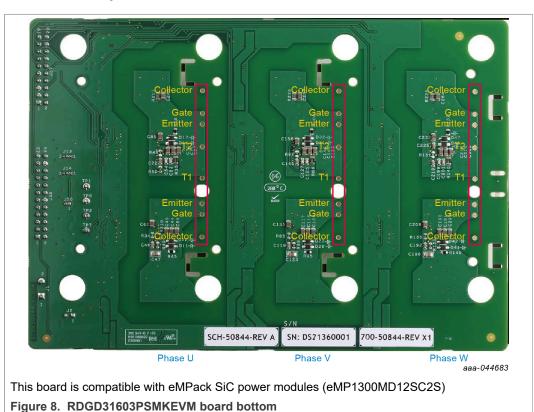
4.2.7 Gate drive resistors

- RGH-gate high resistor in series with the GH pin at the output of the GD3160 driver and SiC MOSFET gate that controls the turn on current for SiC gate.
- RGL-gate low resistor in series with the GL pin at the output of the GD3160 driver and SiC MOSFET gate that controls the turn off current for SiC gate.
- RAMC-series resistor between SiC MOSFET gate and AMC input pin of the GD3160 high-side/low-side driver for gate sensing and Active Miller clamping.

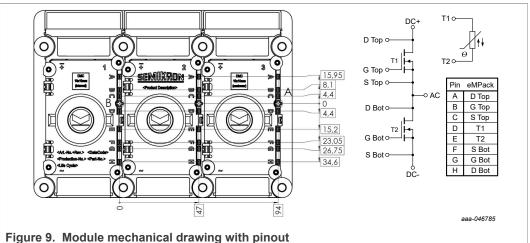
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4.2.8 Power module pin connections



RDGD31603PSMKEVM three-phase inverter kit



rigure 3. Module mechanical drawing with pino

4.2.9 Advanced IGBT/SiC gate driver

4.2.9.1 General description

The GD3160 is an advanced single channel gate driver for IGBTs and SiC devices. Integrated Galvanic isolation and low on-resistance drive transistors provide high charging and discharging current, low dynamic saturation voltage, and rail-to-rail gate voltage control.

Current and temperature sense minimizes power module stress during faults. Accurate and configurable under voltage lockout (UVLO) provides protection while ensuring sufficient gate drive voltage headroom.

The GD3160 autonomously manages severe faults and reports faults and status via the INTB pin and a SPI interface. It is capable of directly driving gates of most power modules. Self-test, control, and protection functions are included for design of high reliability systems (ASIL C/D). It meets the stringent requirements of automotive applications and is fully AEC-Q100 grade 1 qualified.

4.2.9.2 GD3160 features

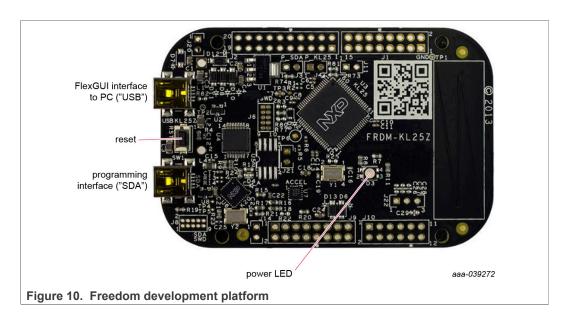
- Compatible with current sense and temp sense IGBTs
- Fast short circuit protection for IGBT/SiC with DESAT and current sense feedback
- Compliant with ASIL D ISO 26262 functional safety requirements
- · SPI interface for safety monitoring, programmability, and flexibility
- Integrated Galvanic signal isolation
- Integrated gate drive power stage capable of 15 A peak source and sink
- Interrupt pin for fast response to faults
- · Compatible with negative gate supply
- Compatible with 200 V to 1700 V IGBTs/SiC, power range > 125 kW
- AEC-Q100 grade 1 qualified

4.3 Kinetis KL25Z Freedom board

The Freedom KL25Z is an ultra-low-cost development platform for the Kinetis L series MCU built on an ARM Cortex-M0+ processor.

UM11697

RDGD31603PSMKEVM three-phase inverter kit



4.4 3.3 to 5.0 V translator board

The KITGD3160TREVB translator enables level shifting of signals from MCU 3.3 V to 5.0 V SPI communication.

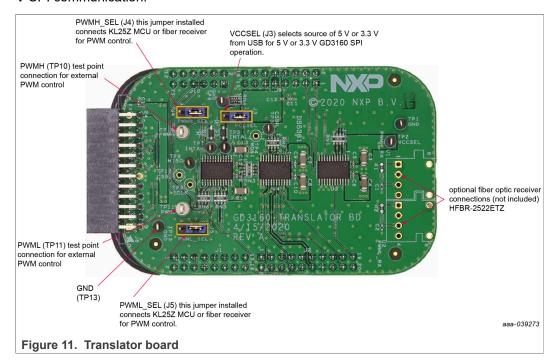


Table 6. Translator board jumper definitions

Jumper	Position	Function
VCCSEL (J3)	1-2	selects 5.0 V for 5.0 V compatible gate drive
	2-3	selects 3.3 V for 3.3 V compatible gate drive
PWMH_SEL (J4)	1-2	selects PWM high-side control from KL25Z MCU
	2-3	selects PWM high-side control from fiber optic receiver inputs

UM11697

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RDGD31603PSMKEVM three-phase inverter kit

Table 6. Translator board jumper definitions...continued

Jumper	Position	Function
PWML_SEL (J5)	1-2	selects PWM low-side control from KL25Z MCU
	2-3	selects PWM low-side control from fiber optic receiver inputs

4.5 Schematic, board layout, and bill of materials

The schematic, board layout and bill of materials for the RDGD31603PSMKEVM reference design are available at http://www.nxp.com/RDGD31603PSMKEVM.

5 Installing and configuring software and tools

Software for RDGD31603PSMKEVM is distributed with the FlexGUI tool (available on NXP.com). Necessary firmware comes pre-installed on the FRDM-KL25Z with the kit.

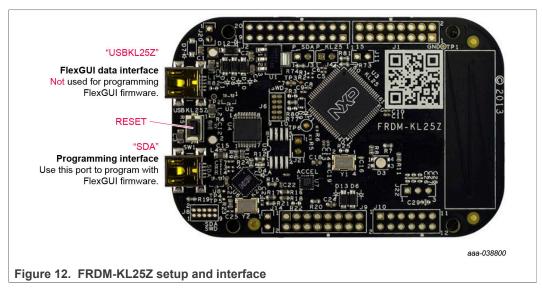
Even if the user intends to test with other software or PWM, NXP recommends installing this software as a backup, or to help with debugging.

5.1 Installing FlexGUI on your computer

The latest version of FlexGUI supports the GD3100 and GD3160. It is designed to run on any Windows 10 or Windows 8 based operating system. To install the software, do the following:

- 1. Go to www.nxp.com/FlexGUI and click Download.
- 2. When the FlexGUI software page appears, click **Download** and select the version associated with your PC operating system.
- 3. The FlexGUI wizard creates a shortcut, and an NXP FlexGUI icon appears on the desktop. By default, the FlexGUI executable file is installed at C:\flexgui-app-des-gd31xx.exe. Installing the device drivers overwrites any previous FlexGUI installation and replaces it with a current version containing the GD31xx drivers. However, configuration files (.spi) from the previous version remain intact.

5.2 Configuring the FRDM-KL25Z microcode



UM11697

RDGD31603PSMKEVM three-phase inverter kit

By default, the FRDM-KL25Z delivered with this kit is preprogrammed with the current and most up-to-date firmware available for the kit.

To quickly check that the microcode is programmed and the board is functioning properly, plug the KL25Z into the computer, open FlexGUI, and verify that the software version at the bottom is 6.4 or later (see <u>Figure 13</u>).

If functionality is lost following a board reset, reprogramming, or a corrupted data issue, the microcode may be rewritten per the following steps:

- 1. To clear the memory and place the board in bootloader mode, hold down the reset button while plugging a USB cable into the **OpenSDA** USB port.
- 2. Verify that the board appears as a BOOTLOADER device and continue with step <u>List</u> <u>item</u>. If the board appears as KL25Z, you may go to step <u>List item</u>.
- 3. Download the **Firmware Apps** .zip archive from the PEmicro OpenSDA web page (http://www.pemicro.com/opensda/).Validate your email address to access the files.
- 4. Find the most recent MDS-DEBUG-FRDM-KL25Z_Pemicro_v118.SDA and copy/ drag-and-drop into the **BOOTLOADER** device.
- 5. Reboot the board by unplugging and replugging the connection to the **OpenSDA** port. Verify now that the device appears as a KL25Z device to continue.
- Locate the most recent KL25Z firmware; which is distributed as part of the FlexGUI package.
 - a. From the FlexGUI install directory, which is located in the flexguiapp-des-gd31xx\binfolder and is named in the form "flexgui-fw-KL25Z usb hid gd31xxC vx.x.x.bin".
 - b. This .bin file is a product/family-specific configuration file for FRDM-KL25Z containing the pin definitions, SPI/PWM generation code, and pin mapping assignments necessary to interface with the translator board as part of RDGD31603PSMKEVM.
- With the KL25Z still plugged through the OpenSDA port, copy/drag-and-drop the .bin file into the KL25Z device memory. Once done, disconnect the USB and plug into the other USB port, labeled KL25Z.
 - The device may not appear as a distinct device to the computer while connected through the KL25Z USB port. This is normal.
- 8. TheFRDM-KL25Z board is now fully set up to work with RDGD31603PSMKEVM and the FlexGUI.
 - There is no software stored or present on either the driver or translator boards, only on the FRDM-KL25Z MCU board.

All uploaded firmware is stored in non-volatile memory until the reset button is hit on the FRDM-KL25Z. There is no need to repeat this process upon every power up, and there is no loss of data associated with a single unplug event.

5.3 Using the FlexGUI

The FlexGUI is available from http://www.nxp.com/FlexGUI as an evaluation tool demonstrating GD31xx-specific functionality, configuration, and fault reporting. FlexGUI also includes basic capacity for the RDGD31603PSMKEVM to control an IGBT or SiC module, enabling double pulse or short-circuit testing.

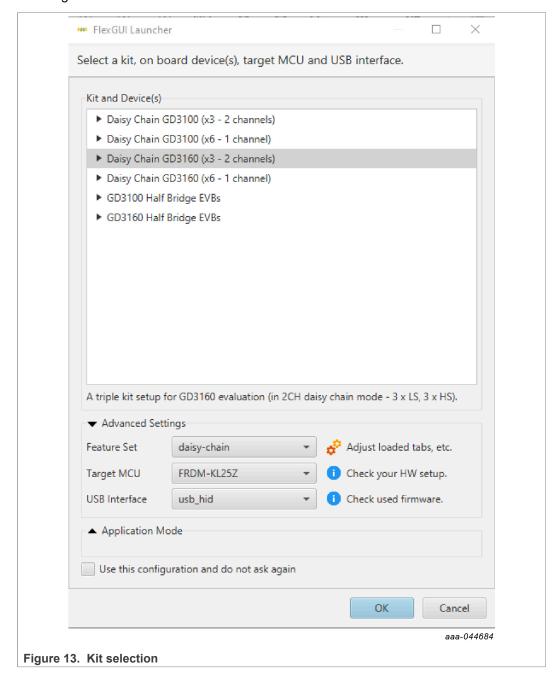
SPI messages can be realized graphically or in hexadecimal format. Chip Select Bar (CSB) is selectable to address (x6-1 channel) or (x3-2 channels) GD31xx on the board via daisy chain. See <u>Figure 14</u> to <u>Figure 33</u> or FlexGUI for GD31xx internal register read and write access.

UM11697

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Starting FlexGUI for GD31xx

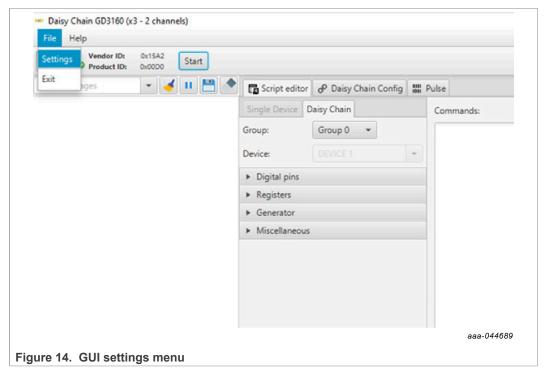
- FlexGUI install program (flexgui-app-des-gd31xx-0.x.x.exe)
- · Download FlexGUI and run the install program on your PC
- When you start the application, <u>Figure 13</u> allows you to select the target application board, feature set (standard or daisy chain), target MCU, and USB interface. Leave all settings as shown.



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FlexGUI settings

• Access settings by selecting Settings from the File menu.



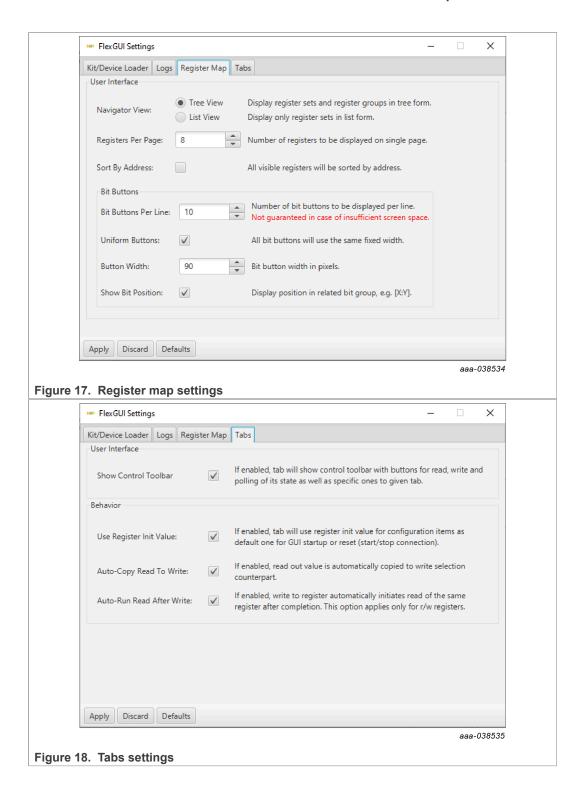
• The Loader and Logs settings are shown below:

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- Access settings by selecting Settings from the File menu.
- The Register Map and Tabs settings are shown below:

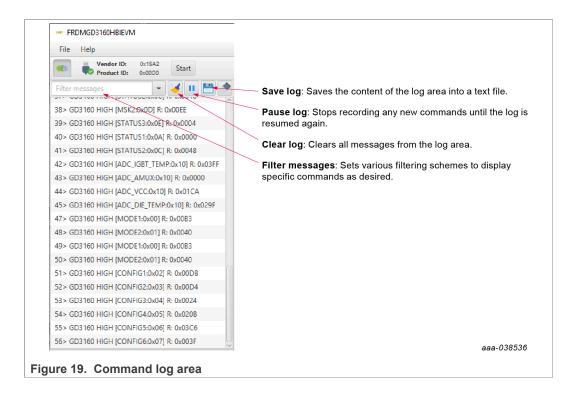
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Command Log window

• The Command Log area informs the user about application events.

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Global workspace controls

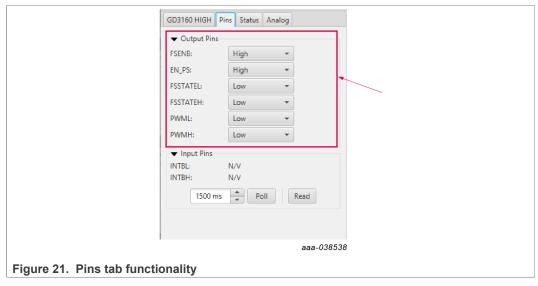
- · Always visible in the lower left corner of the main application window
 - GD3160 tab functionality
 - Switch modes between run and configuration mode
 - Set SPI frequency



Pins tab functionality

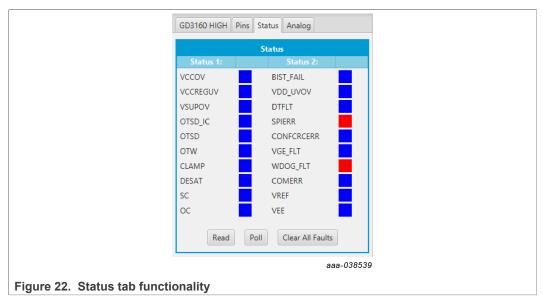
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- · Set control levels. Default values are shown
- Read and automatically poll INTB pins (INTA pins are added for GD3160)
- · Control pins set values to a default state
 - FSENB enable/disable fail-safe enable
 - EN PS enables fly-back supply on EVB at 17 V VCC on high side and low side
 - FSSTATEL and FSSTATEH set the fail-safe state when FSENB is enabled
 - PWML and PWMH set the default state PWM inputs for high side and low side



Status tab functionality

- Monitors Status 1 and Status 2 fault bits -- bits that are set are shown in red.
- · Ability to clear all faults and automatically poll status registers



Analog tab functionality

- Read and poll ADC values from the high-voltage domain
- Displays raw ADC and converted values

UM11697

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Register map

- Registers are grouped according to function; with independent lines to read and write the registers
- Registers can be set to read and write, or to read or write, by selecting Set to Read and SEND for read and Set to Write and SEND for write
- Use the copy button to copy the read values to the write line; can be set to copy automatically
- Use the reset button to undo the changes on the write line and reset to the previous value
- Global register controls perform the selected command on all registers with the check box selected



Gate Drive tab

 Allows setting of parameters related to the gate drive; controls are disabled when not in config mode

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- Provides a more intuitive visual way to set parameters
- All settings are automatically synchronized with the register controls

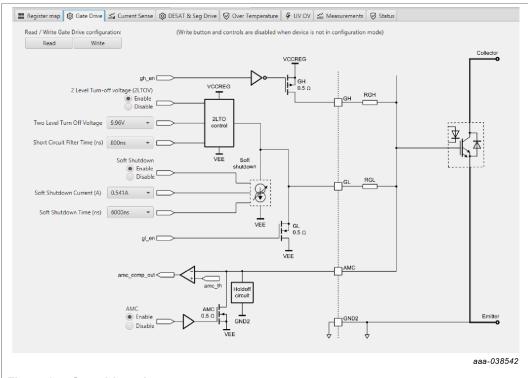
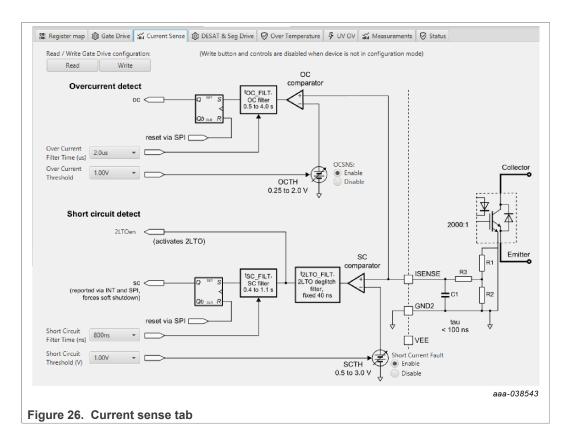


Figure 25. Gate drive tab

Current Sense tab

- · Allows setting of parameters related to current sense
- Provides a more intuitive visual way to set parameters
- All settings are automatically synchronized with the register controls

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DESAT and Seg Drive tab

DESAT and Seg Drive tab

- · Allows setting of parameters related to desat and segmented drive
- · Provides a more intuitive visual way to set parameters
- All settings are automatically synchronized with the register controls

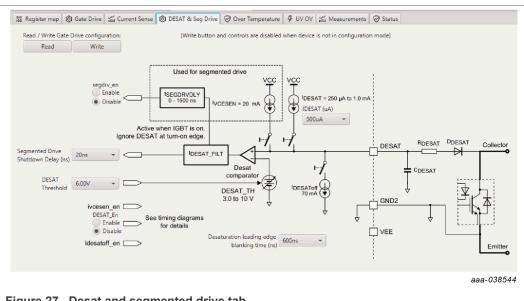
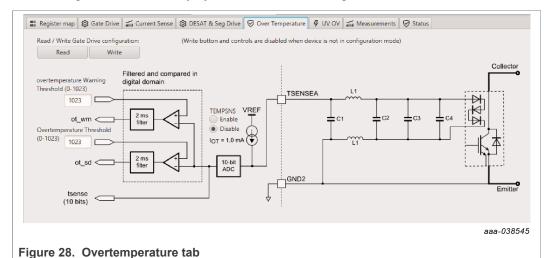


Figure 27. Desat and segmented drive tab

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Overtemperature tab

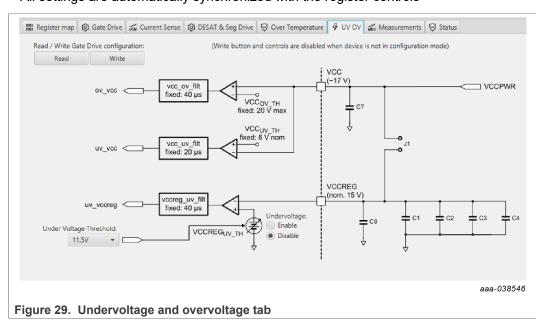
- Allows setting of parameters related to overtemperature and overtemperature warning thresholds.
- Provides a more intuitive visual way to set parameters
- · All settings are automatically synchronized with the register controls



Undervoltage threshold tab

Allows setting of parameters related to undervoltage threshold

- · Provides a more intuitive visual way to set parameters
- · All settings are automatically synchronized with the register controls



Measurements tab

· Allows monitoring and graphing of ADC and temperature values

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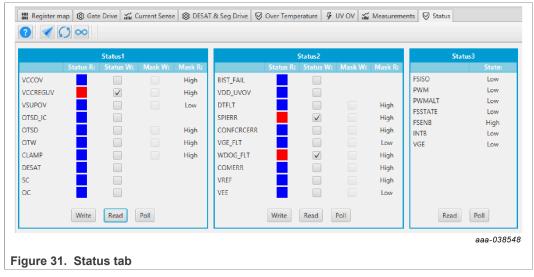
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Status tab

- Allows monitoring of Status 1, Status 2, and Status 3 register values
- · Status 1 and Status 2 faults can be cleared
- Status mask registers can be modified when in configuration mode



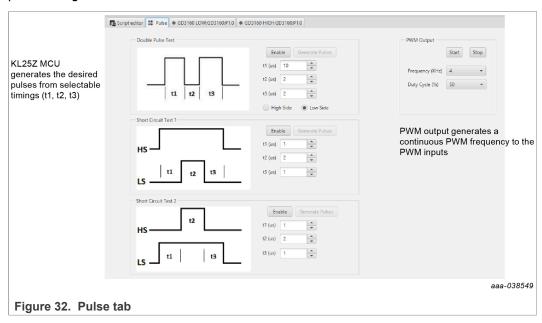
Pulse tab

- · Used for double pulse, short-circuit, and PWM testing
- Select desired T1, T2, and T3 timings for each test type; select enable, then generate pulses

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Note: Phase U can be configured for performing double-pulse and short-circuit testing. To enable short-circuit testing, two resistors (R43, R56) must be pulled from PWMALT phase U signals to disable Deadtime control on Phase U Gate drivers.



6 Configuring the hardware

RDGD31603PSMKEVM with KITGD3160TREVB attached as shown in <u>Figure 32</u> utilizing Windows based PC and FlexGUI software.

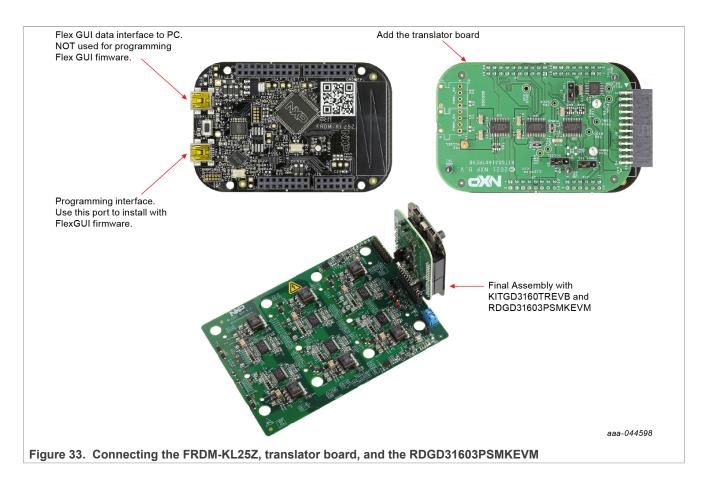
Suggested equipment needed for test:

- · Rogowski coil high-current probe
- · High-voltage differential voltage probe
- · High sample rate digital oscilloscope with probes.
- Compatible eMPack application kit (power module, cooler plate and DClink capacitor) (eMP1300MD12SC2S-APK, article number 19285392) from Semikron.
- · Windows based PC
- High-voltage DC power supply for DC link voltage
- Low-voltage DC power supply for VSUP
 +12 V DC gate drive board low-voltage domain
- Voltmeter for monitoring high-voltage DC link supply
- · Load coil for double pulse and short-circuit testing, Phase U only

Note: To enable short-circuit testing, two resistors (R43, R56) must be pulled from PWMALT phase U signals to disable Deadtime control on Phase U gate drivers.

Using the FlexGUI software, it is possible to conduct double pulse and short circuit testing on the U phase only. External PWM inputs are provided on the external connectors, should the user want to drive these pins from their own setup. When using external PWM inputs on the U phase, jumpers J4 and J5 on the translator board should be disconnected to prevent a driving conflict with the KL25Z microcontroller board.

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6.1 Start using the kit

To get started using the RDGD31603PSMKEVM:

- Assemble the KL25Z microcontroller board, the translator board and the three phase board together, as shown in <u>Figure 33</u>, on the eMPack module.
- Connect the KL25Z via USB to a computer with FlexGUI software installed.
- Supply the board with 12 V DC (1.0 A compliance current) through J1. See <u>Figure 5</u> for polarity and location.
- · Check and adjust auxiliary supplies:
- 1. Set each VEE voltage (in the range -1.25 V to -7.5 V) using the six left-most potentiometers shown in Fig.5. For example, adjust R239 to set the VEE voltage of phase W low-side, measuring between the VEELW and GNDLW test points.
- 2. Set the VCC+VEE voltage for both low-side and high-side devices, by adjusting R235 and R265 respectively, until the desired VCC voltage is achieved.

Connection with the FlexGUI software can now be started to configure and check the driver status.

6.2 Troubleshooting

Some common issues and troubleshooting procedures are detailed below. This is not an exhaustive list by any means, and additional debugging may be needed:

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Table 7. Troubleshooting

Problem	Evaluation	Explanation	Corrective action(s)
No PWM output (no fault reported).	Check PWM jumper position on translator board.	Incorrect PWM jumpers obstruct signal path but do not report fault.	Set PWMH_SEL (J4) and PWML_SEL (J5) jumpers properly,for desired control method: • 3.3 V to 5.0 V translator board reviewed in Section4.4.
	Check PWM control signal.	Ensure that proper PWM signal is reaching GD3160.	Monitor EXT_PWML (TP14) and EXT_PWMH (TP15) for commanded PWM state.
	Check FSENB status (see GD3160 pin 15, STATUS3).	PWM is disabled when FSENB = LOW.	Set pin FSENB = HIGH (pin 15) to continue
	Check CONFIG_EN bit (MODE2).	PWM is disabled when CONFIG_EN is logic 1.	Write CONFIG_EN = logic 0 to continue
No PWM output (fault reported).	Check VGE fault (VGE_FLT).	A short on IGBT or SiC module gate, or too low of VGEMON delay setting causes VGE fault, locking out PWM control of the gate.	Clear VGE_FLT bit (STATUS2) to continue. Increase VGEMON delay setting (CONFIG6). If safe operating condition can be guaranteed, set VGE_FLTM (MSK2) bit to logic 0, to mask fault.
	Check for short-circuit fault (SC) in STATUS1 register.	SC is a severe fault that disables PWM. SC fault cannot be masked.	Clear SC fault to continue. Consider adjusting SC fault settings on GD3160: • Adjust short-circuit threshold setting (CONFIG2). • Adjust short-circuit filter setting (CONFIG2).
PWM output is good, but with persistent fault reported.	Check for dead time fault (DTFLT) in STATUS2 register.	Dead time is enforced, but fault indicates that PWM controls signals are in violation.	Clear DTFLT fault bit (STATUS2). Check Phase U PWMALT weak pull-downs R206 and R57 are in place to bypass dead time faults. Consider adjusting dead time settings on GD3160: Change mandatory PWMdead time setting (CONFIG5). Mask dead time fault(MSK2).
	Check for overcurrent (OC) fault in STATUS1 register.	OC fault latches, but does not disable PWM. OC fault cannot be masked.	Clear OC fault bit (STATUS1). Adjust OC fault detection settings on GD3160: • Adjust overcurrent threshold setting (CONFIG1). • Adjust overcurrent filter setting (CONFIG1).

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Table 7. Troubleshooting...continued

Problem	Evaluation	Explanation	Corrective action(s)
PWM or FSSTATE rising edge has longer delay than falling edge.	Check translator output voltage versus GD3160 VDD voltage.	Low translator output voltage (compared with correct VDD at GD3160) causes the high threshold at the GD3160 pin to be crossed later than commanded.	Check translator output voltage selection (J233) is configured to the same level as the GD3160 VDD. Check VCCSEL supply or translator outputs on the translator board. for excessive loading or supply droop/pulldown.
WDOG_FLT reported on startup.	Check VSUP and VCC are powered.	On initialization, watchdog fault is reported when one die is powered up before the other.	Check VSUP and VCC both have power applied. Clear WDOG_FLT bit (STATUS2) to continue.
SPIERR reported on startup.	Check KL25Z/translator connection.	On initialization, SPIERR can occur when the SPI bus is open, or when GD3160 IC is powered up before the translator (which provides CSB).	Clear SPIERR fault to continue. Reinitialize power to GD3160 after translator is powered (over USB).

7 References

- [1] **RDGD31603PSMKEVM** detailed information on this board, including documentation, downloads, and software and tools:
 - http://www.nxp.com/RDGD31603PSMKEVM
- [2] **GD3160** product information on Advanced single-channel gate driver for Insulated Gate Bipolar Transistors: http://www.nxp.com/GD3160
- [3] **MPC5777C** ultra-reliable MCU for automotive and industrial engine management: http://www.nxp.com/MPC5777C
- [4] MPC5744P ultra-reliable MCU for automotive and industrial safety applications:: https://www.nxp.com/MPC574xP
- [5] MPC5775B/E-EVB http://www.nxp.com/MPC5775b-e-evb

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RDGD31603PSMKEVM three-phase inverter kit

Contents

1	Introduction	4
2	Finding kit resources and information	4
2.1	Collaborate in the NXP community	4
3	Getting started	4
3.1	Kit contents	5
3.2	Additional hardware	5
3.3	Windows PC workstation	5
3.4	Software	5
4	Getting to know the hardware	5
4.1	RDGD31603PSMKEVM features	5
4.2	Kit featured components	6
4.2.1	Voltage domains, GD3160 pinout, logic	
	header, and IGBT pinout	
4.2.2	GD3160 pinout and MCU interface pinout	6
4.2.3	Test points	9
4.2.4	Indicators	
4.2.5	Connectors, jumpers and potentiometers	
4.2.6	Power supply test points	
4.2.7	Gate drive resistors	
4.2.8	Power module pin connections	
4.2.9	Advanced IGBT/SiC gate driver	
4.2.9.1	General description	
4.2.9.2	GD3160 features	
4.3	Kinetis KL25Z Freedom board	
4.4	3.3 to 5.0 V translator board	16
4.5	Schematic, board layout, and bill of	
	materials	17
5	Installing and configuring software and	
	tools	17
5.1	Installing FlexGUI on your computer	
5.2	Configuring the FRDM-KL25Z microcode	
5.3	Using the FlexGUI	
6	Configuring the hardware	
6.1	Start using the kit	
6.2	Troubleshooting	
7	References	
8	Legal information	34

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