Product Change Notification / SYST-28CLNB029

Date:

29-Sep-2022

Product Category:

8-bit Microcontrollers

PCN Type:

Document Change

Notification Subject:

ERRATA - PIC18(L)F27/47K40 Family Silicon Errata and Data Sheet Clarifications Revision

Affected CPNs:

SYST-28CLNB029_Affected_CPN_09292022.pdf
SYST-28CLNB029_Affected_CPN_09292022.csv

Notification Text:

SYST-28CLNB029

Microchip has released a new Errata for the PIC18(L)F27/47K40 Family Silicon Errata and Data Sheet Clarifications of devices. If you are using one of these devices please read the document located at PIC18(L)F27/47K40 Family Silicon Errata and Data Sheet Clarifications.

Notification Status: Final

Description of Change: Removed 2.1.2. Added silicon errata 2.1.6, 2.1.7, 2.1.8, 2.4.2, 2.5.3, 2.10.1, 2.11.1, 2.12.1. Removed Data Sheet clarification for Operating speed. Modified 3.2.1 (Electrical Specification) ADC Offset Error updated to -+3.0LSb.

Impacts to Data Sheet: None

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 29 Sep 2022

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachments:

PIC18(L)F27/47K40 Family Silicon Errata and Data Sheet Clarifications

Please contact your local Microchip sales office with questions or concerns regarding this notification.

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Affected Catalog Part Numbers (CPN)

PIC18F27K40-E/SP
PIC18LF27K40-E/SP
PIC18F27K40-E/ML
PIC18LF27K40-E/ML
PIC18F27K40-E/SS
PIC18LF27K40-E/SS
PIC18F27K40-E/SO
PIC18LF27K40-E/SO
PIC18F47K40-E/P
PIC18LF47K40-E/P
PIC18F47K40-E/MV
PIC18LF47K40-E/MV
PIC18F47K40-E/ML
PIC18LF47K40-E/ML
PIC18F47K40-E/PT
PIC18LF47K40-E/PT
PIC18F27K40-I/SP
PIC18LF27K40-I/SP
PIC18F27K40-I/ML
PIC18LF27K40-I/ML
PIC18F27K40-I/SS
PIC18LF27K40-I/SS
PIC18F27K40-I/SO
PIC18LF27K40-I/SO
PIC18F47K40-I/P
PIC18LF47K40-I/P
PIC18F47K40-I/MV
PIC18LF47K40-I/MV
PIC18F47K40-I/ML
PIC18LF47K40-I/ML
PIC18F47K40-I/PT
PIC18LF47K40-I/PT
PIC18F27K40T-I/ML
PIC18LF27K40T-I/ML
PIC18F27K40T-I/MLVAO
PIC18F27K40T-I/SS
PIC18LF27K40T-I/SS
PIC18F27K40T-I/SO
PIC18LF27K40T-I/SO
PIC18F47K40T-I/MV
PIC18LF47K40T-I/MV
PIC18F47K40T-I/ML
PIC18LF47K40T-I/ML
PIC18F47K40T-I/PT
PIC18LF47K40T-I/PT
PIC18F47K40T-E/ML

PIC18LF47K40T-E/PTVAO

PIC18(L)F27/47K40 Family Silicon Errata and Data Sheet Clarifications

The PIC18(L)F27/47K40 devices that you have received conform functionally to the current device data sheet (DS40001844E), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in the table below.

The errata described in this document will be addressed in future revisions of the PIC18(L)F27/47K40 silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current.

Table 1. Silicon Device Identification

Part Number	Device ID	Revision ID	
		A2	A3
PIC18F27K40	0x6960	0xA002	0xA003
PIC18LF27K40	0x6A40	0xA002	0xA003
PIC18F47K40	0x6900	0xA002	0xA003
PIC18LF47K40	0x69E0	0xA002	0xA003

1. Silicon Issue Summary

Table 1-1. Silicon Issue Summary

Module	Feature	Item No.	Issue Summary	Affected Revisions	
				A2	A3
Analog-to-Digital Converter (ADC)	ADC Conversion	2.1.1.	Delay of one instruction cycle required prior to setting the ADGO bit when using ADCRC as the ADCC clock source.	X	
	ADCRC Oscillator Operation in Sleep	2.1.2.	The ADCRC oscillator does not stop after conversion is complete in Sleep mode.	X	X
	ADC Conversion with FVR	2.1.3.	Using FVR as the ADC positive voltage reference can cause missing codes.	X	X
	ADC conversion with F_{OSC} as clock	2.1.4.	The ADGO bit remains set when using F_{OSC} as clock source with clock divider.	X	X
	ADC operation in Burst Average mode	2.1.5.	The ADCNT register does not increment past `'0b1'` in Burst Average mode with double sampling enabled.	X	X
	Double Sample Conversions	2.1.6.	An unexpected acquisition time is added between the first and second conversions.	X	X
	ADC Acquisition Time	2.1.7.	Conversion during SLEEP mode when ADACQ=0 affects results on values in the upper half of the 10-bit range. The analog input is disconnected for 3-4 uS and the first bit of the result becomes zero.	X	X
	ADC Short in Precharge State	2.1.8.	ADC shorts briefly in pre-charge state when the corresponding analog pin is selected as an output.	X	X
PIC18 Debug Executive	Data Write Match Breakpoints	2.2.1.	Data write match breakpoints do not work when used on a location GSR space.	X	
	Single Step Function (SSTEP)	2.2.2.	Single Step function does not execute at SW Breakpoint.	X	X
PIC18 Core	TBLRD	2.3.1.	TBLRD requires NVMREG value to point to appropriate memory.	X	
Program Flash Memory (PFM)	Endurance of PFM Cell	2.4.1.	Endurance of the PFM cell is lower than specified.	X	X
	Back to Back Writes	2.4.2.	Repetitive writes may cause write/erase failures.	X	X
MSSP	SMBus 2.0 Voltage Level	2.5.1.	Input low-voltage threshold level is dependent on V_{DD}.	X	X
	SPI	2.5.2.	SSPBUF may become corrupted	X	X
	I2C	2.5.3.	Acknowledge failure on LF devices only	X	

.....continued

Module	Feature	Item No.	Issue Summary	Affected Revisions	
				A2	A3
Electrical Specifications	Min V_{DD} Specification	2.6.1.	V_{DDMIN} specifications are changed for LF devices only for -40°C and 0°C.		X
	FVR Specification	2.6.2.	FVR specifications require use above -20°C.	X	X
	Analog to Digital Converter	2.6.3.	ADC offset error specification is +/- 3.0 LSb	X	X
Timer0	Clock Source	2.7.1.	TMR0 does not function properly in Sync mode	X	X
Windowed Watchdog Timer	WWDT operation in Doze mode	2.8.1.	Erroneous window violation error occurs in Doze mode.	X	X
NVM	NVMERR bit operation	2.9.1.	NVMERR bit is set incorrectly due to specific Reset events.	X	X
Enhanced Universal Synchronous Asynchronous Receiver Transmitter (EUSART)	Transmit mode	2.10.1.	Possible duplicate byte transmitted	X	X
Capture/ Compare/PWM Module (CCP)	PWM mode	2.11.1.	Duty cycle values are incorrect	X	X
In-Circuit Serial Programming™	Low-Voltage Programming	2.12.1.	Low-Voltage Programming is not possible when V_{DD} is below BORV while BOR is enabled	X	X

Note: Only those issues indicated in the last column apply to the current silicon revision.

2. Silicon Errata Issues

CAUTION **Notice:** This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the bold font in the following tables apply to the current silicon revision.

2.1 Module: ADCC - Analog-to-Digital Converter with Computation

2.1.1 ADC Conversion

When using the ADCRC as the clock source for ADCC, there is a delay of one instruction cycle between the user setting the ADGO bit and being able to read it set. This can lead to a false conversion complete scenario (i.e., ADGO being cleared), depending if the user code has a bit clear test `BTFSC` instruction on the ADGO bit, immediately after setting the ADGO bit. See code example below.

```
BSF ADCON0, ADGO                    ;    Start conversion
BTSFC ADCON0, ADGO                  ;    Is conversion done?
GOTO $-1                            ;    No, test again
```

Work around

Add a `NOP` instruction after setting the ADGO bit and before testing the bit for completion of conversion. See code example below.

```
BSF ADCON0, ADGO                    ;    Start conversion
NOP
BTSFC ADCON0, ADGO                  ;    Is conversion done?
GOTO $-1                            ;    No, test again
```

Affected Silicon Revisions

A2	A3
X	

2.1.2 ADCRC Oscillator Operation in Sleep

If the part is in Sleep and the ADCRC oscillator is used as clock source to the ADC, the oscillator continues to run after the conversion is complete. This will increase the current consumption in Sleep mode. The oscillator will stop after the device exits Sleep mode and resumes normal code execution.

Work around

None.

Affected Silicon Revisions

A2	A3
X	X

2.1.3 Missing Codes with FVR Reference

Using the FVR as the positive voltage reference for the ADC can cause an increase in missing codes.

Work around
Method 1:

Increase the bit conversion time, known as T_{AD}, to 8 µs or higher.

Method 2:

Use V_{DD} as the positive voltage reference to the ADC.

Affected Silicon Revisions

A2	A3
X	X

2.1.4 ADC GO Bit May Remain Set When the Clock Source is F_{OSC}

When using F_{OSC} as the clock source (ADCON0.CS = 0) and any clock divider setting other than $F_{OSC}/2$ is selected, the ADGO bit remains set and the conversion does not complete.

Work around
Method 1:

When using F_{OSC} as the clock source (ADCON0.CS = 0), clear the ADCLK register value to zero (ADCLK.CS = 0) and ensure that the F_{OSC} frequency does not violate any timing requirements for the ADC.

Method 2:

Use ADCRC as the clock source (ADCON0.CS = 1).

Affected Silicon Revisions

A2	A3
X	X

2.1.5 ADCC Burst Average Mode

When the ADCC is operated in Burst Average mode (ADMD = 0b011 in the ADCON2 register) while enabling noncontinuous operation and double-sampling (ADCONT = 0 in the ADCON0 register and ADDSEN = 1 in the ADCON1 register), the value in the ADCNT register does not increment beyond '0b1' toward the value in the ADRPT register.

Work around
When operating the ADCC in Burst Average mode with double-sampling, enable continuous operation of the module (ADCONT = 1 in the ADCON0 register) and set the Stop-on-Interrupt bit (the ADSOI bit in the ADCON3 register). After the interrupt occurs, perform appropriate threshold calculations in the software and retrigger ADCC as necessary.

Alternatively, if the CPU is in Low-Power Sleep mode, the ADCC in noncontinuous Burst Average mode can be operated with a single ADC conversion (ADDSEN = 0 in the ADCON1 register). Doing so compromises noise immunity for lower power consumption by preventing the device from waking up to perform threshold calculations in the software.

Affected Silicon Revisions

A2	A3
X	X

2.1.6 Double Sample Conversions

When enabling a Double Sample Conversion (DSEN = 1), with no Precharge time (ADPRE = 0) and no Acquisition time (ADACQ = 0), the maximum number of cycles of acquisition time is inserted prior to the second conversion. The first conversion will be performed as expected with no Precharge time and no Acquisition time. It is only between the first and second conversions where a maximum number of cycles of Acquisition time is performed unexpectedly.

Work around

- Method 1: Disable Double Sample Conversion (DSEN = 0) and perform two single conversions back to back.
- Method 2: If adding acquisition time is acceptable, then select no Precharge time, along with the desired Acquisition time.

Affected Silicon Revisions

A2	A3
X	X

2.1.7 ADC Conversion Acquisition Time in Sleep (ADCC)

Conversion during SLEEP mode when ADACQ=0 affects results on values in the upper half of the 10-bit range. The analog input is disconnected for 3-4 uS and the first bit of the result becomes zero.

Work around

Add 5 counts of ADACQ time.

Affected Silicon Revisions

A2	A3
X	X

2.1.8 ADC Short in Pre-Charge State

During the precharge state, if the analog pin on which the ADC conversion is performed is selected to be an output (such as LATx or ADGRDx), there is a 20 ns short between pullup/down and the external low/high states, resulting in an inaccurate ADC conversion reading.

Work around

None.

Affected Silicon Revisions

A2	A3
X	X

2.2 Module: PIC18 Debug Executive

2.2.1 Data Write Match Breakpoints

If the data in a GPR location is modified using any arithmetic instruction like INCF, ADDWF, SETF, CLRF, etc., the data write match breakpoint does not work. It works with MOVF, which moves the data into the same memory location. See code examples below.

1.

```
MOVLB       0x00
CLRF        0x08
```

```
LOOP
INCF        0x08    ;Doesn't break when data
                    breakpoint set @ 0x08
                    with data match for 0xAA
GOTO LOOP
```

2.

```
MOVLB        0x00
MOVLW        0xAA
MOVF         0x08   ;Breaks when data
                    breakpoint set @ 0x08
                    with data match for 0xAA
GOTO LOOP
```

Work around
Use data write breakpoints without matching wherever possible.

Affected Silicon Revisions

A2	A3
X	

2.2.2 Single Step function does not execute at SW Breakpoint.

The SW breakpoint occurs, but the SSTEP function does not execute at the breakpoint.

Work around
None.

Affected Silicon Revisions

A2	A3
X	X

2.3 Module: PIC18 Core

2.3.1 TBLRD Requires NVMREG Value to Point to Appropriate Memory

The affected silicon revisions of the PIC18(L)F27/47K40 devices improperly require the NVMREG[1:0] bits in the NVMCON register to be set for TBLRD access of the various memory regions. The issue is most apparent in compiled C programs when the user defines a const type and the compiler uses `TBLRD` instructions to retrieve the data from Program Flash Memory (PFM). The issue is also apparent when the user defines an array in RAM for which the compiler creates start-up code, executed before main(), that uses `TBLRD` instructions to initialize RAM from PFM.

Work around
Assembly code:

Set the NVMREG[1:0] bits to select the appropriate memory region before executing `TBLRD` instructions.

C code:

Create an assembly file named powerup.as and include this file with the other files in the project. This file will change the NVMREG[1:0] bits to point to program Flash before any code is executed. Contents of the powerup.as file:

```
#include <xc.inc>
        GLOBAL    powerup, start
```

```
        PSECT     powerup, class=CODE, delta=1, reloc=2
powerup:
        BSF       NVMCON1, 7
        GOTO      start
        end
```

If there is a need to change the NVMREG[1:0] value to anything other than '10' and the Interrupt Service Routine uses constants or literal strings, then interrupts must be disabled before the change and restored to '10' before interrupts are enabled.

Affected Silicon Revisions

A2	A3
X	

2.4 Module: Program Flash Memory (PFM)

2.4.1 Endurance of PFM is Lower than Specified

The Flash memory cell endurance specification (Parameter MEM30) is 1K cycles.

Work around
None.

Affected Silicon Revisions

A2	A3
X	X

2.4.2 PFM Back to Back Writes

When repetitive writes to non-volatile memory (Program Flash Memory) are performed, it could result in write/erase failures at some locations. The issue is due to latent timing in the non-volatile memory controller which can cause the write instruction to fail under certain conditions.

Work around
To avoid the issue, it is recommended to wait an additional 100us after the NVMCON1.WR bit has been set, allowing for the last word to be loaded into the write buffer.

```
        NVMCON2 = 0x55;
        NVMCON2 = 0xAA;
        NVMCON1bits.WR = 1;
        __delay_us(100);

        NVMCON1bits.WREN = 0;
```

Note: The __delay_us() function uses a #define macro definition. For the intrinsic __delay_us() function to work correctly, the value of the _XTAL_FREQ must be clearly defined. This macro is defined in the device_config.h file if the code is generated using MCC. The value of XTAL_FREQ is equal to the system clock frequency.

Affected Silicon Revisions

A2	A3
X	X

2.5 Module: MSSP

2.5.1 SMBus 2.0 Voltage Level

The input low-voltage threshold level (V_{IL}) depends on V_{DD}, as follows:

V_{IL} = 0.7 for V_{DD} < 4V

V_{IL} = 0.8 for V_{DD} > 4V

Work around
None.

Affected Silicon Revisions

A2	A3
X	X

2.5.2 MSSP SPI Client Mode

When operating in SPI Client mode, if the incoming SCK clock signal arrives during any of the conditions below, the SSPBUF Transmit Shift Register (TSR) may become corrupted. The byte transmitted to the client cannot be ensured to be correct, and the state of the WCOL bit may or may not indicate a write collision.

These conditions include:

- A write to an SFR
- A write to RAM following an SFR read
- A write to RAM prior to an SFR read

Work around
Method 1 (Interrupt based using $\overline{SS}$):

1. Connect the $\overline{SS}$ line to both the $\overline{SS}$ input and either an INT or IOC input pin.
2. Enable INT or IOC interrupts (interrupt on falling edge if available, otherwise check that $\overline{SS}$ == 0 when the interrupt occurs).
3. Load SSPBUF with the data to be transmitted.
4. Continue program execution.
5. When the Interrupt Service Routine (ISR) is invoked, do either of the following:
   a. Add a delay that ensures the first SCK clock will be complete, or
   b. Poll SSPSTAT.BF (while(BF == 0)), and wait for the transmission/reception to complete.

Method 2 (Bit polling based using $\overline{SS}$):

1. Load SSPBUF with the data to be transmitted.
2. Poll the $\overline{SS}$ line and wait for the $\overline{SS}$ to go active (while(!PORTx.$\overline{SS}$ == 0)).
3. When $\overline{SS}$ is active ($\overline{SS}$ == 0), do either of the following:
   a. Add a delay that ensures the first SCK clock will be complete, or
   b. Poll SSPSTAT.BF (while(BF == 0)), and wait for the transmission/reception to complete.

Once one of these two methods are complete, it is safe to return to program execution.

Method 3 ($\overline{SS}$ not available):

1. Load SSPBUF with the data to be transmitted.
2. Poll SSPSTAT.BF (while(BF == 0)), and wait for the transmission/reception to complete.

Affected Silicon Revisions

A2	A3

X	X

2.5.3 SMBus 2.0 Voltage Level

When using the MSSP to perform I2C communication and the voltage for V_{DD} is above 3.0 volts, the Acknowledge signal (ACK) does not always occur after the second address byte is received, as expected. This issue exhibits itself when the MSSP is configured either for 7-bit or 10-bit addressing and in either Master or Slave mode.

The issue occurs more frequently when using 10-bit addressing in Slave mode and the lower address bits (A7-A0) are transmitted by the Master on the SDA line.

Work around

Do not exceed 3.0 volts on V_{DD} when using an LF device.

Affected Silicon Revisions

A2	A3
X	

2.6 Module: Electrical Specifications

2.6.1 Min V_{DD} Specification (LF Devies Only)

V_{DDMIN} specifications are changed for LF devices only at -40°C and 0°C as below.

V_{DDMIN} for -40°C to 0°C = 2.3V

V_{DDMIN} for 0°C to 25°C = 2.1V

Work around

None.

Affected Silicon Revisions

A2	A3
	X

2.6.2 FVR - Fixed Voltage Reference

At temperatures below -20°C, the output voltage for the FVR may be greater than the levels specified in the data sheet. This will apply to all three gain amplifier settings, (1X, 2X, 4X). The affected parameter numbers found in the data sheet are: FVR01 (1X gain setting), FVR02 (2X gain setting), and FVR03 (4X gain setting).

Work around

At temperatures above -20°C, the stated tolerances in the data sheet remain in effect. Operate the FVR only at temperatures above -20°C.

Affected Silicon Revisions

A2	A3
X	X

2.6.3 ADC - Analog-to-Digital Converter

The table containing the Offset Error specification (AD04: EOFF) for the Analog-to-Digital Converter is modified. The updated value for Offset Error specification is +/- 3.0 LSb.

Work around
None.

Affected Silicon Revisions

A2	A3
X	X

2.7 Module: Timer0

2.7.1 Synchronous mode

Do not operate Timer0 in Synchronous mode.

Work around
Use TMR0 in Asynchronous Mode by setting the T0ASYNC bit in T0CON1 register. All functions of Timer0 operate properly in Asynchronous mode

Affected Silicon Revisions

A2	A3
X	X

2.8 Module: Windowed Watchdog Timer (WWDT)

2.8.1 Window Operation in Doze Mode

When the Windowed mode of operation is enabled in Doze mode, a window violation error is issued even though the window is open and has been armed. This condition occurs only when the window size is set to a value other than 100% open.

Work around
Method 1:

Use the Windowed mode of operation in any mode other than Doze. If disabling the Doze mode is not an option, use the WWDT module without the window being enabled.

Method 2:

If the device is in Doze mode, perform the arming process for the window in Normal mode and return to the Doze mode.

Method 3:

If there is an Interrupt Service Routine (ISR) in the application code, the arming within the window can be done inside the ISR with the ROI bit of the CPUDOZE register being set.

Affected Silicon Revisions

A2	A3
X	X

2.9 Module: Nonvolatile Memory (NVM)

2.9.1 NVMERR

When a Reset is issued while an NVM high-voltage operation is in progress, the NVMERR bit in the NVMCON0 register is set as expected. After clearing the NVMERR bit, if a Reset reoccurs, the NVMERR bit is set again regardless of whether an NVM operation is in progress or not. A successful write operation will clear the NVMERR condition.

Work around

None.

Affected Silicon Revisions

A2	A3
X	X

2.10 Module: Enhanced Universal Synchronous Asynchronous Receiver Transmitter (EUSART)

2.10.1 Double Byte Transmit

Under certain conditions, a byte written to the TXREG register can be transmitted twice. This happens when a byte is written to TXREG just as the TSR register becomes empty. This new byte is immediately transferred to the TSR register, but also remains in the TXREG register until the completion of the current instruction cycle. If the new byte in the TSR register is transmitted before this instruction cycle has completed, the duplicate in the TXREG register will subsequently be transferred to the TSR register on the following instruction clock cycle and transmitted.

Work around

Method 1: Monitor the Transmit Interrupt Flag (TXIF) bit. Writes to the TXREG register can be performed once the TXIF bit is set, indicating that the TXREG register is empty. If using this method, ensure that the second byte is filled in the TXREG before bit 6 of the first byte is transmitted. If the delay is more than six bit times, there is a possibility of double byte transmission.

Method 2: Monitor the TMRT bit of the TXxSTA register. Writes to the TXREG register can be performed once the TMRT bit is set, indicating that the Transmit Shift Register (TSR) is empty. This work around can be applied if back-to-back transmissions are not necessary.

Affected Silicon Revisions

A2	A3
X	X

2.11 Module: Capture/Compare/PWM Module (CCP)

2.11.1 Wrong Duty Cycle for CCP Module

While in PWM mode and the Timer2 prescaler is configured to 1:1, the duty cycle of the PWM output is as expected. When the Timer2 prescaler is changed to a value other than 1:1, while T2PR = 0 (PWM resolution of two bits), the expected duty cycle is wrong. The corrected duty cycle values are shown in the table below.

Table 2-1. Corrected Duty Cycle Values

Prescaler/CCPR	0	1	2	3	4
1:1	0%	25%	50%	75%	100%
1:2	50%	75%	50%	75%	100%
1:4...1:128	75%	75%	75%	75%	100%

Work around
None.

Affected Silicon Revisions

A2	A3
X	X

2.12 Module: Low-Voltage In-Circuit Serial Programming™ (LVP)

2.12.1 Low-Voltage Programming Not Possible

Low-Voltage Programming is not possible when V_{DD} is below the selected BORV voltage level, while BOR is enabled.

Work around
Method 1: Disable BOR to use Low-Voltage Programming.

Method 2: Raise V_{DD} above the selected BORV level while using Low-Voltage Programming.

Affected Silicon Revisions

A2	A3
X	X

3. Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS40001844E):

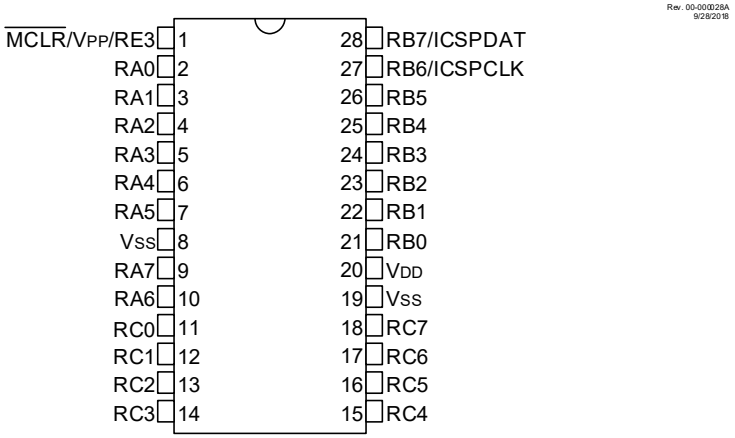
Note:
Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

3.1 Module: Pin Diagrams

3.1.1 28-pin SPDIP/SSOP/SOIC Pin Diagram

The correct marking for pin 26 on the 28-pin SPDIP/SSOP/SOIC package is **RB5.**

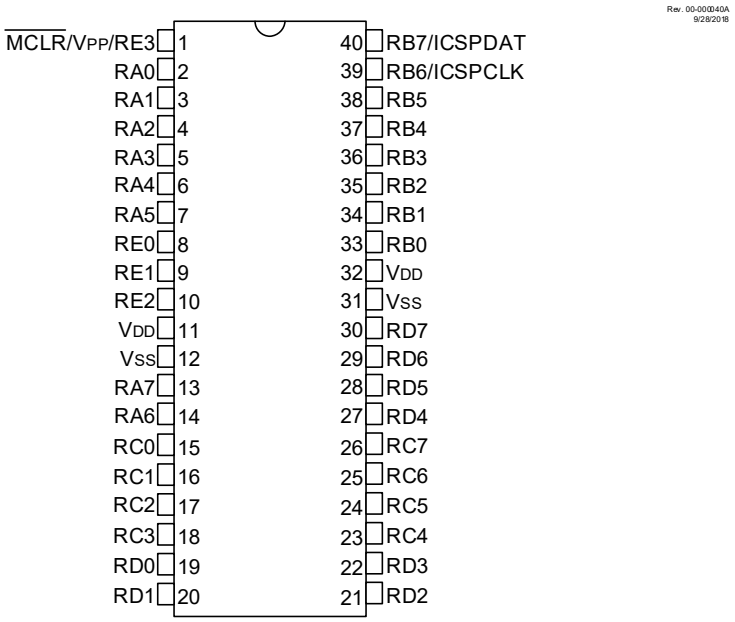
Figure 1. 28-pin SPDIP, SSOP, SOIC



3.1.2 40-pin PDIP Pin Diagram

The correct marking for pin 38 on the 40-pin SPDIP package is **RB5.**

Figure 3. 40-pin PDIP



3.2 Module: Electrical Specifications

3.2.1 ADC Offset Error

Table 38-13 containing the Offset Error Specification (AD04 : E_{OFF}) for the Analog-to-Digital Converter is modified.

The updated value for Offset Error Specification **(AD04) is ±3.0 LSb.**

3.2.2 ADC Conversion Timing Diagram

Refer to the images below for corrections of Figure 38-10 and Figure 38-11. Previously, the parameter numbers were incorrect.

Figure 38-10: ADC Conversion Timing (ADC Clock F_{OSC}-Based)

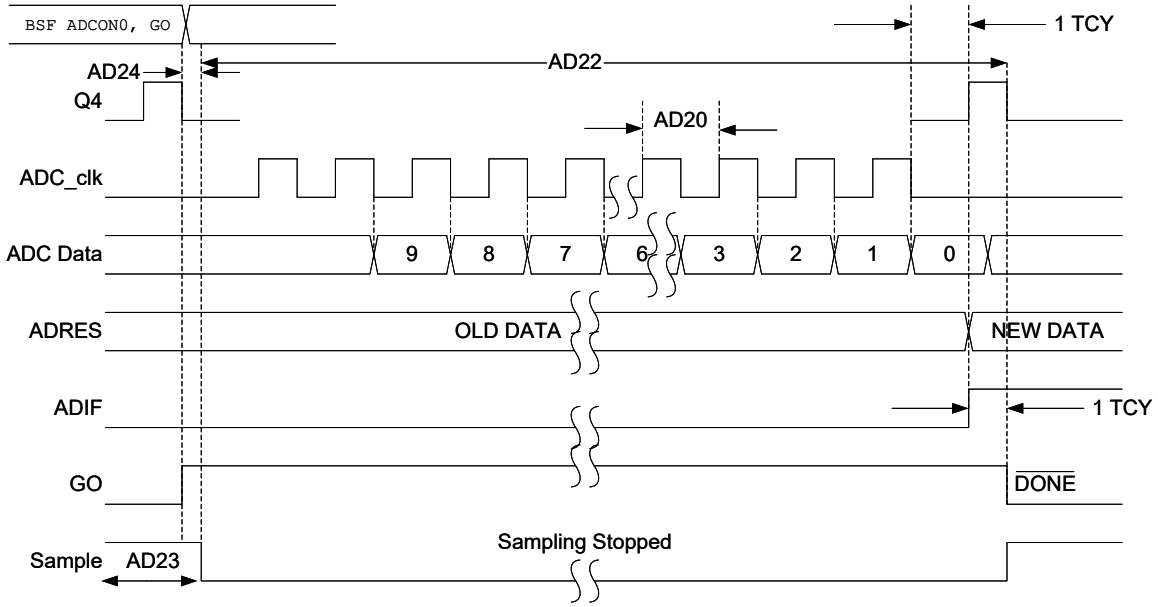
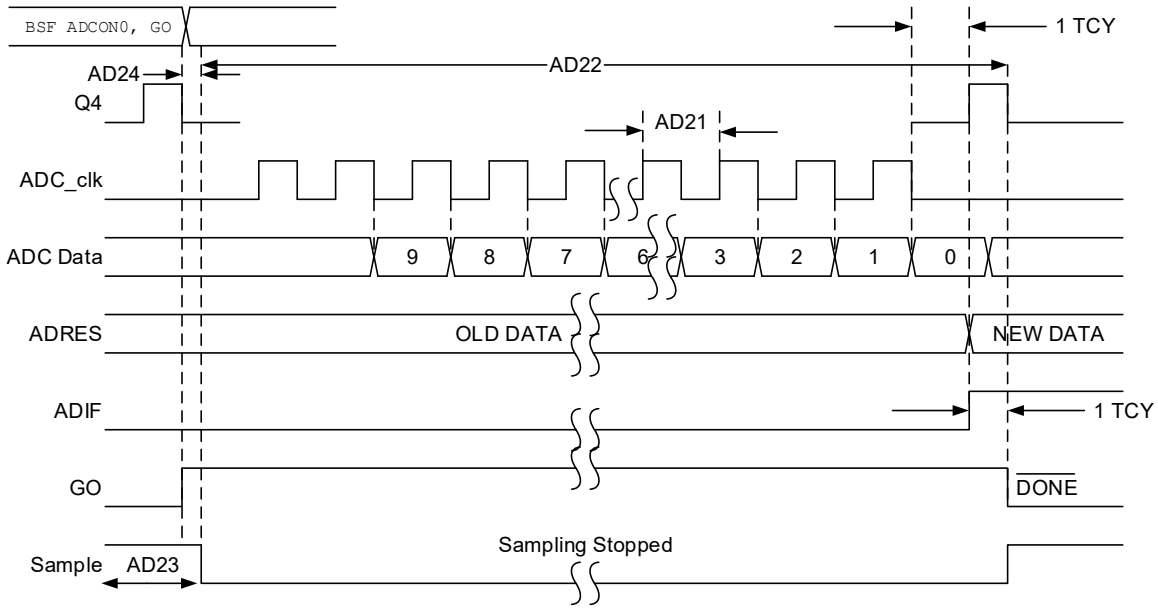


Figure 38-11: ADC Conversion Timing (ADC Clock from ADCRC)



3.2.3 Comparator Offset Error

Table 38-15 containing the Input Offset Voltage Error Specification (CM01 : V_{IOFF}) for the Comparator is modified.

The updated value for Input Offset Voltage Specification **(CM01) is ±60mV.**

3.2.4 I/O Ports - I²C Threshold Values

Table 38-4 containing the Input Low Voltage with I²C levels specification (D303 : V_{IL}) for the I/O ports is modified. Refer to the table below for the updated value.

Param No.	Sym.	Characteristic	Min.	Typ.†	Max.	Units	Conditions
D303	V_{IL}	**Input Low Voltage**					
		I/O PORT:					
		with I²C levels	–	–	0.3 V_{DD}	V	2.0V ≤ V_{DD} ≤ 5.5V
			–	–	0.25 V_{DD}	V	1.8V ≤ V_{DD} < 2.0V

3.3 Module: Analog-to-Digital Converter

3.3.1 ADC Clock Period vs Device Frequency

The ADCLK value for $F_{OSC}/16$ in Table 31-2 is incorrect. The correct value can be found in the table below.

ADC Clock Period (T_{AD})		Device Frequency (F_{OSC})						
ADC Clock Source	ADCLK	64 MHz	32 MHz	20 MHz	16 MHz	8 MHz	4 MHz	1 MHz
$F_{OSC}/2$	000000	31.25 ns(2)	62.5 ns(2)	100 ns(2)	125 ns(2)	250 ns(2)	500 ns(2)	2.0 µs
$F_{OSC}/4$	000001	62.5 ns(2)	125 ns(2)	200 ns(2)	250 ns(2)	500 ns(2)	1.0 µs	4.0 µs
$F_{OSC}/6$	000010	125 ns(2)	187.5 ns(2)	300 ns(2)	375 ns(2)	750 ns(2)	1.5 µs	6.0 µs
$F_{OSC}/8$	000011	187.5 ns(2)	250 ns(2)	400 ns(2)	500 ns(2)	1.0 µs	2.0 µs	8.0 µs(3)
...	...	...	...	...	...	...	...	...
$F_{OSC}/16$	000111	250 ns(2)	500 ns(2)	800 ns(2)	1.0 µs	2.0 µs	4.0 µs	16.0 µs(3)
...	...	...	...	...	...	...	...	...
$F_{OSC}/128$	111111	2.0 µs	4.0 µs	6.4 µs	8.0 µs	16.0 µs(3)	32.0 µs(2)	128.0 µs(2)
FRC	ADCS=1	1.0-6.0 µs	1.0-6.0 µs	1.0-6.0 µs	1.0-6.0 µs	1.0-6.0 µs	1.0-6.0 µs	1.0-6.0 µs

Note:

1. See T_{AD} parameter in the "Electrical Specifications" section for FRC source typical T_{AD} value.
2. These values violate the required T_{AD} time.
3. Outside the recommended T_{AD} time.
4. The ADC clock period (T_{AD}) and total ADC conversion time can be minimized when the ADC clock is derived from the system clock F_{OSC}. However, the FRC oscillator source must be used when conversions are to be performed with the device in Sleep mode.

3.3.2 ADCRS Bits Description in the ADCON2 Register

The description for the ADCRS[2:0] bits in the ADCON2 register is incorrect. The correct description is mentioned below.

3.3.2.1 ADCON2

Name: ADCON2

Bits 6:4 – ADCRS[2:0] ADC Accumulated Calculation Right Shift Select bits

Value	Condition	Description
1 to 6	ADMD = 'b100	Low-pass filter time constant is 2^{ADCRS}, filter gain is 1:1**(2)**
1 to 6	ADMD = 'b011 to 'b001	The accumulated value is right-shifted by ADCRS (divided by 2^{ADCRS})**(1,2)**
x	**ADMD = 'b000**	These bits are ignored

3.3.3 ADC Precharge Time Control Register

Refer to the register below for the modified description of the ADPRE register.

3.3.3.1 ADPRE

Name: ADPRE
Offset: 0xF5E

ADC Precharge Time Control Register

Bit	7	6	5	4	3	2	1	0
	ADPRE[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – ADPRE[7:0] Precharge Time Select bits

Table 3-1.

ADPRE	Precharge Time	
	ADCS != F_{RC}	ADCS = F_{RC}
255	255 clock of F_{OSC}	255 clock of F_{RC}
254	254 clock of F_{OSC}	254 clock of F_{RC}
...	...	
2	2 clock of F_{OSC}	2 clock of F_{RC}
1	1 clock of F_{OSC}	1 clock of F_{RC}
0	Not included in the data conversion cycle	

3.3.4 ADC Acquisition Time Control Register

Refer to the register below for the modified description of the ADACQ register.

3.3.4.1 ADACQ

Name: ADACQ
Offset: 0xF5C

ADC Acquisition Time Control Register

Bit	7	6	5	4	3	2	1	0
	ADACQ[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – ADACQ[7:0] Acquisition (charge share time) Select bits

Table 3-2.

ADACQ	Acquisition Time	
	ADCS != F_{RC}	ADCS = F_{RC}
255	255 clock of F_{OSC}	255 clock of F_{RC}
254	254 clock of F_{OSC}	254 clock of F_{RC}
...	...	
2	2 clock of F_{OSC}	2 clock of F_{RC}
1	1 clock of F_{OSC}	1 clock of F_{RC}
0	Not included in the data conversion cycle(1)	

Note:

1. If ADPRE is not equal to '0', then ADACQ = 0b0000_0000 means Acquisition Time is 256 clocks of F_{OSC} or F_{RC}.

3.4 Module: CCP - Capture/Compare/PWM Module

3.4.1 Module Registers

The description for the CCPTMRS register is missing in the data sheet. The description for this register is mentioned below.

Each CCP/PWM module has an independent timer selection that can be accessed using the CxTSEL or PxTSEL bits. The default timer selection is TMR1 when using Capture/Compare mode and TMR2 when using PWM mode in the CCPx module. The default timer selection for the PWM module is always TMR2.

3.4.1.1 CCPTMRS

Name: CCPTMRS
Offset: 0xFAE

CCP Timers Control Register

Bit	7	6	5	4	3	2	1	0
	P4TSEL[1:0]		P3TSEL[1:0]		C2TSEL[1:0]		C1TSEL[1:0]	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	1	0	1	0	1	0	1

Bits 4:5, 6:7 – PnTSEL PWMn Timer Selection bits

Value	Description
11	PWMn based on Timer6
10	PWMn based on Timer4
01	PWMn based on Timer2
00	Reserved

Bits 0:1, 2:3 – CnTSEL CCPn Timer Selection bits

Value	Description
11	CCPn is based off Timer5 in Capture/Compare mode and Timer6 in PWM mode
10	CCPn is based off Timer3 in Capture/Compare mode and Timer4 in PWM mode
01	CCPn is based off Timer1 in Capture/Compare mode and Timer2 in PWM mode
00	Reserved

4. Appendix A: Revision History

Doc Rev.	Date	Comments
G	09/2022	Remove 2.1.2. Added silicon errata 2.1.6, 2.1.7, 2.1.8, 2.4.2, 2.5.3, 2.10.1, 2.11.1, 2.12.1. Remove Data Sheet clarification for Operating speed. Modified 3.2.1 (Electrical Specification) ADC Offset Error updated to -+3.0LSb.
F	03/2021	Added silicon errata 2.1.2, 2.1.5, 2.1.6, 2.5.2, 2.6.3, 2.8.1 and 2.9.1. Data Sheet Clarifications: Added Module 3.2 (Pin Diagrams), Module 3.3 (Electrical Specifications), Module 3.4 (Analog-to-Digital Convertor) and Module 3.5 (Capture/Compare/PWM (CCP) Module).
E	05/2018	Added Module 7: Electrical Specifications (FVR) and Module 8: Timer0. Data Sheet Clarifications: Added Module 1 (Core Features).
D	04/2017	Data Sheet Clarifications: Removed Module 1 (Peripheral Pin Select). Other minor corrections.
C	03/2017	Added Module 6: Electrical Specifications for LF Devices Only. Other minor corrections.
B	12/2016	Added silicon revisions 1.3, 1.4 and 5.1; Other minor corrections. Data Sheet Clarifications: Added Module 1 (Peripheral Pin Select).
A	09/2012	Initial document release.

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