



PSMN1R0-30YLE

N-channel 30 V, 1.1 mOhm, ASFET for hotswap with enhanced SOA in LFPAK56

17 October 2022

Product data sheet

1. General description

N-channel enhancement mode ASFET for hotswap with enhanced SOA in LFPAK56 package optimized for low R_{DSon} and strong safe operating area, optimized for hot-swap, inrush and linear-mode applications.

2. Features and benefits

- Fully optimized Safe Operating Area (SOA) for superior linear mode operation
- Optimized for low R_{DSon} / low I^2R conduction losses
- LFPAK56 package for applications that demand the highest performance and reliability in a 30 mm² footprint
- Low leakage <1 μ A at 25 °C
- Copper-clip for low parasitic inductance and resistance
- High reliability LFPAK package, qualified to 175 °C

3. Applications

- Hot swap in 12 V - 20 V applications
- e-Fuse
- DC switch
- Load switch
- Battery protection

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	25 °C \leq T_j \leq 175 °C	-	-	30	V
I_D	drain current	$V_{GS} = 10$ V; $T_{mb} = 25$ °C; Fig. 2	[1]	-	275	A
P_{tot}	total power dissipation	$T_{mb} = 25$ °C; Fig. 1	-	-	224	W
T_j	junction temperature		-55	-	175	°C
Static characteristics						
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10$ V; $I_D = 25$ A; $T_j = 25$ °C; Fig. 10	-	0.94	1.11	m Ω
		$V_{GS} = 7$ V; $I_D = 25$ A; $T_j = 25$ °C; Fig. 10	-	1.17	1.55	m Ω
Dynamic characteristics						
Q_{GD}	gate-drain charge	$I_D = 25$ A; $V_{DS} = 15$ V; $V_{GS} = 4.5$ V; $T_j = 25$ °C; Fig. 12 ; Fig. 13	1.8	10	20	nC
$Q_{G(tot)}$	total gate charge		15	33	54	nC

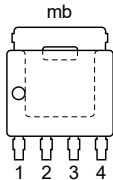
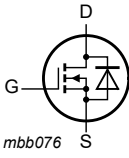
N-channel 30 V, 1.1 mOhm, ASFET for hotswap with enhanced SOA in LFPAK56

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Source-drain diode						
S	softness factor	$I_S = 25\text{ A}$; $di_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$; $V_{DS} = 15\text{ V}$; $T_J = 25\text{ }^\circ\text{C}$; Fig. 16	-	0.95	-	

[1] 275 A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 <p>LFPAK56; Power-SO8 (SOT669)</p>	 <p><i>mbb076</i></p>
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN1R0-30YLE	LFPAK56; Power-SO8	plastic, single-ended surface-mounted package; 4 terminals	SOT669

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN1R0-30YLE	1E0L30Y

8. Limiting values

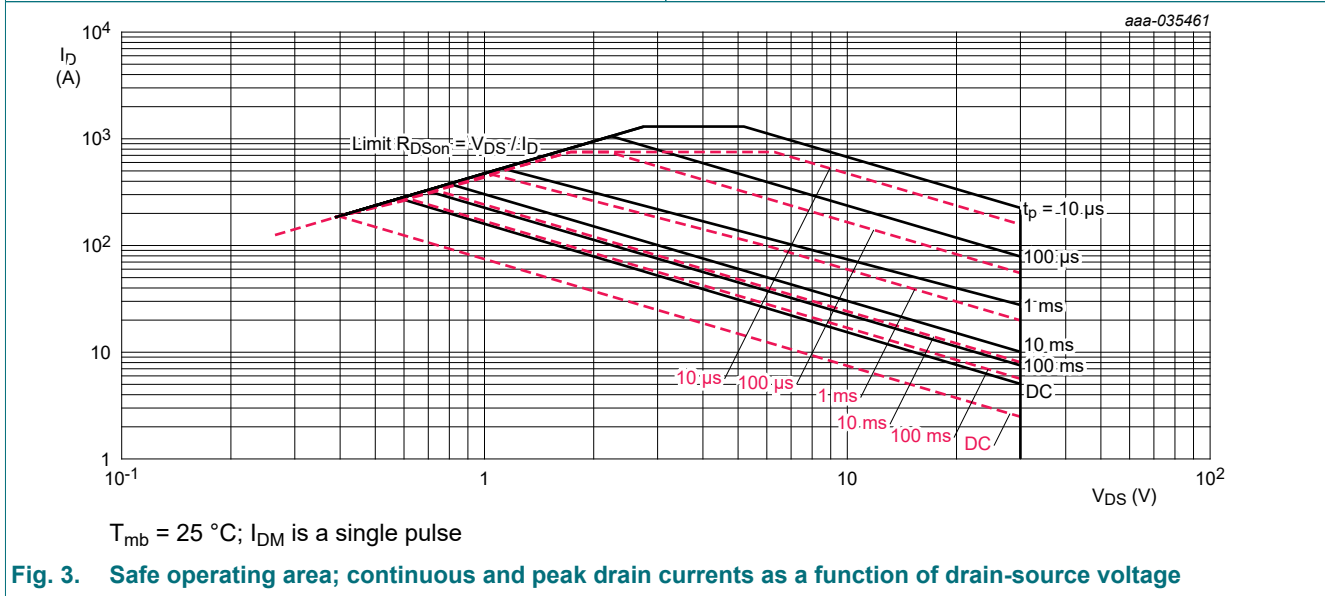
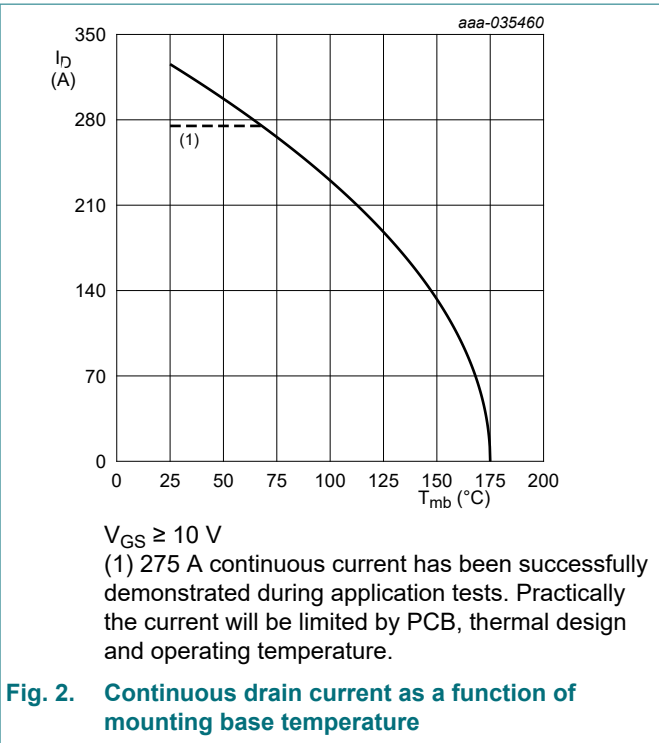
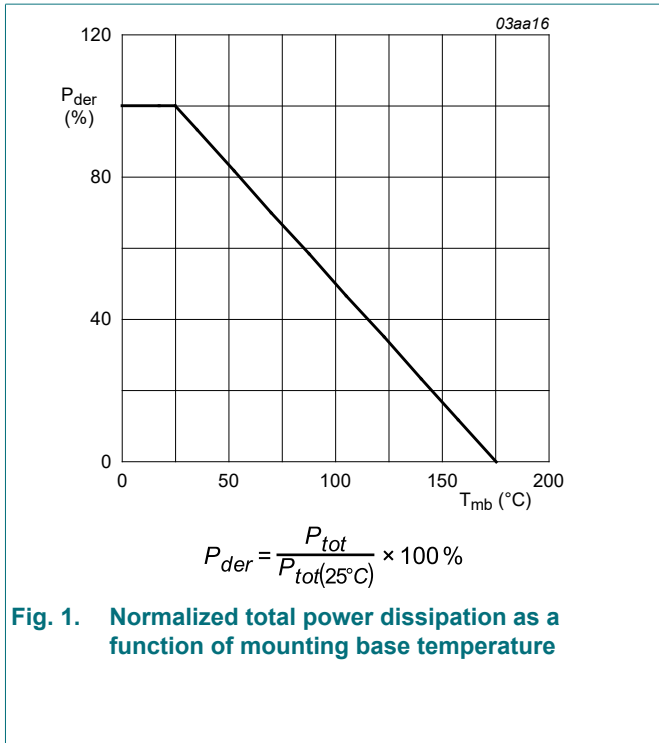
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). $T_j = 25\text{ °C}$ unless otherwise stated.

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$		-	30	V
V_{DGR}	drain-gate voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$		-	30	V
V_{GS}	gate-source voltage			-20	20	V
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1		-	224	W
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2	[1]	-	275	A
		$V_{GS} = 10\text{ V}$; $T_{mb} = 100\text{ °C}$; Fig. 2		-	230	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$; Fig. 3		-	1303	A
T_{stg}	storage temperature			-55	175	°C
T_j	junction temperature			-55	175	°C
$T_{sld(M)}$	peak soldering temperature			-	260	°C
Source-drain diode						
I_S	source current	$T_{mb} = 25\text{ °C}$		-	224	A
I_{SM}	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$		-	1303	A
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 25\text{ A}$; $V_{sup} \leq 30\text{ V}$; $R_{GS} = 50\text{ }\Omega$; $V_{GS} = 10\text{ V}$; $T_{j(\text{init})} = 25\text{ °C}$; unclamped; $t_p = 3\text{ ms}$	[2]	-	1.5	J
I_{AS}	non-repetitive avalanche current	$V_{sup} \leq 30\text{ V}$; $V_{GS} = 10\text{ V}$; $T_{j(\text{init})} = 25\text{ °C}$; $R_{GS} = 50\text{ }\Omega$	[2]	-	128	A

[1] 275 A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

[2] Protected by 100% test.



9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 4	-	0.37	0.67	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Fig. 5	-	42	-	K/W
		Fig. 6	-	85	-	K/W

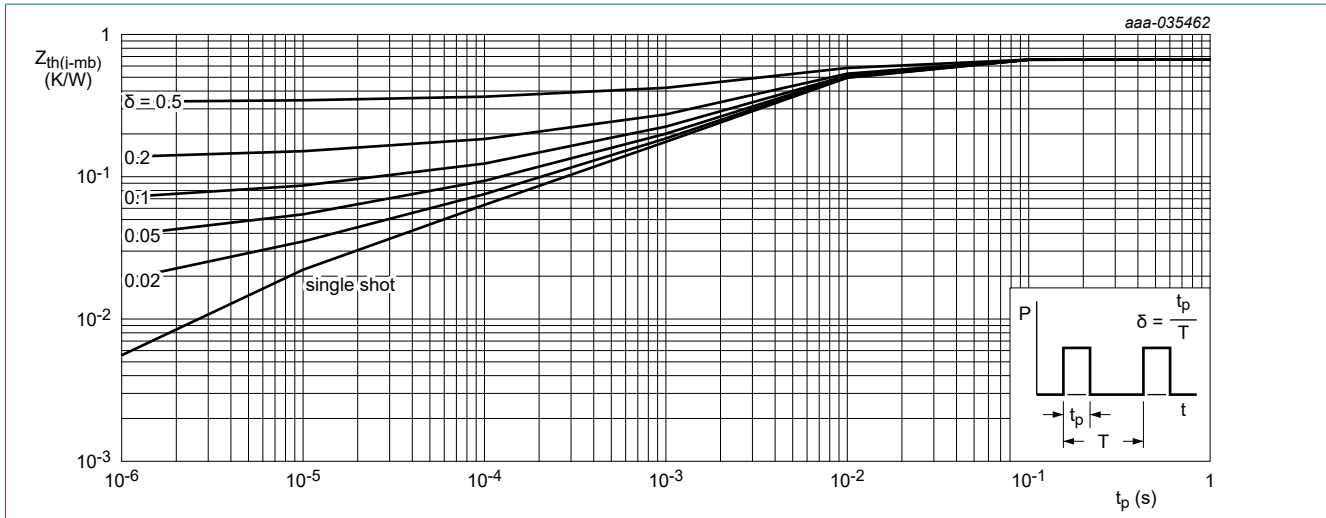
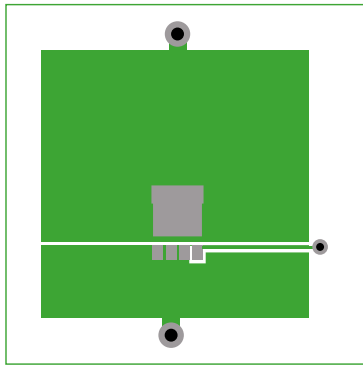


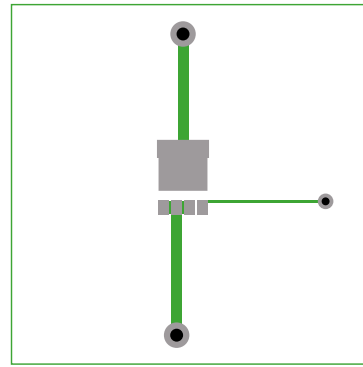
Fig. 4. Transient thermal impedance from junction to mounting base as a function of pulse duration



aaa-027933

Copper area 25.4 mm square; 70 μm thick on FR4 board

Fig. 5. PCB layout for thermal resistance from junction to ambient



aaa-027935

70 μm thick copper on FR4 board

Fig. 6. PCB layout with minimum footprint for thermal resistance from junction to ambient

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	30	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	27	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 2 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C$	1.2	1.86	2.2	V
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature	$25 \text{ }^\circ C \leq T_j \leq 150 \text{ }^\circ C$	-	-3.7	-	mV/K
I_{DSS}	drain leakage current	$V_{DS} = 24 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	-	1	μA
		$V_{DS} = 24 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 125 \text{ }^\circ C$	-	4.2	-	μA
I_{GSS}	gate leakage current	$V_{GS} = 16 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	-	100	nA
		$V_{GS} = -16 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	-	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ C$; Fig. 10	-	0.94	1.11	m Ω
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 150 \text{ }^\circ C$; Fig. 11	-	-	2	m Ω
		$V_{GS} = 7 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ C$; Fig. 10	-	1.17	1.55	m Ω
		$V_{GS} = 7 \text{ V}; I_D = 25 \text{ A}; T_j = 150 \text{ }^\circ C$; Fig. 11	-	-	2.9	m Ω
R_G	gate resistance	$f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ C$	1.3	3.1	7.8	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 25 \text{ A}; V_{DS} = 15 \text{ V}; V_{GS} = 4.5 \text{ V}; T_j = 25 \text{ }^\circ C$; Fig. 12 ; Fig. 13	15	33	54	nC
		$I_D = 25 \text{ A}; V_{DS} = 15 \text{ V}; V_{GS} = 10 \text{ V}; T_j = 25 \text{ }^\circ C$; Fig. 12 ; Fig. 13	32	72	119	nC
		$I_D = 0 \text{ A}; V_{DS} = 0 \text{ V}; V_{GS} = 10 \text{ V}; T_j = 25 \text{ }^\circ C$	-	36	-	nC
Q_{GS}	gate-source charge	$I_D = 25 \text{ A}; V_{DS} = 15 \text{ V}; V_{GS} = 4.5 \text{ V}; T_j = 25 \text{ }^\circ C$; Fig. 12 ; Fig. 13	4	15	29	nC
$Q_{GS(th)}$	pre-threshold gate-source charge	$I_D = 25 \text{ A}; V_{DS} = 15 \text{ V}; V_{GS} = 4.5 \text{ V}; T_j = 25 \text{ }^\circ C$; Fig. 12 ; Fig. 13	2	7.5	14	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		2.1	7.8	15	nC
Q_{GD}	gate-drain charge		1.8	10	20	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 25 \text{ A}; V_{DS} = 15 \text{ V}; T_j = 25 \text{ }^\circ C$; Fig. 12 ; Fig. 13	-	3.4	-	V
C_{iss}	input capacitance	$V_{DS} = 15 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ C$; Fig. 14	2956	4926	7389	pF
C_{oss}	output capacitance		1107	1845	2768	pF
C_{rss}	reverse transfer capacitance		82	305	732	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 15 \text{ V}; R_L = 0.6 \text{ } \Omega; V_{GS} = 4.5 \text{ V}; R_{G(ext)} = 5 \text{ } \Omega; T_j = 25 \text{ }^\circ C$	-	10	-	ns
t_r	rise time		-	20	-	ns
$t_{d(off)}$	turn-off delay time		-	57	-	ns
t_f	fall time		-	38	-	ns
Q_{oss}	output charge	$V_{GS} = 0 \text{ V}; V_{DS} = 15 \text{ V}; f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ C$	-	43	-	nC

N-channel 30 V, 1.1 mOhm, ASFET for hotswap with enhanced SOA in LPAK56

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 25\text{ A}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 15	-	0.78	1	V
t_{rr}	reverse recovery time	$I_S = 25\text{ A}$; $di_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$;	-	34	-	ns
Q_r	recovered charge	$V_{DS} = 15\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 16	[1]	27	-	nC
t_a	reverse recovery rise time		-	17.5	-	ns
t_b	reverse recovery fall time		-	16.7	-	ns
S	softness factor		-	0.95	-	

[1] includes capacitive recovery

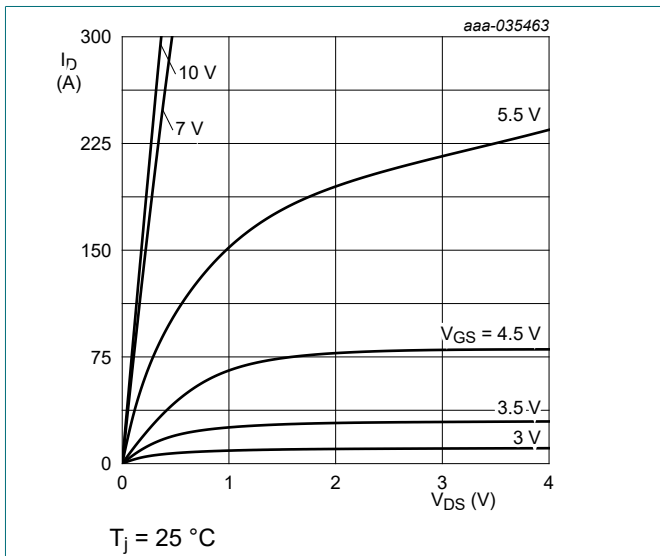


Fig. 7. Output characteristics; drain current as a function of drain-source voltage; typical values

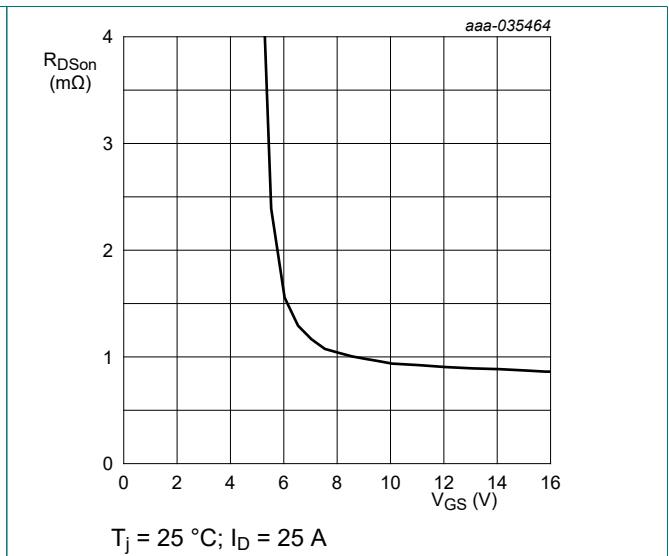


Fig. 8. Drain-source on-state resistance as a function of gate-source voltage; typical values

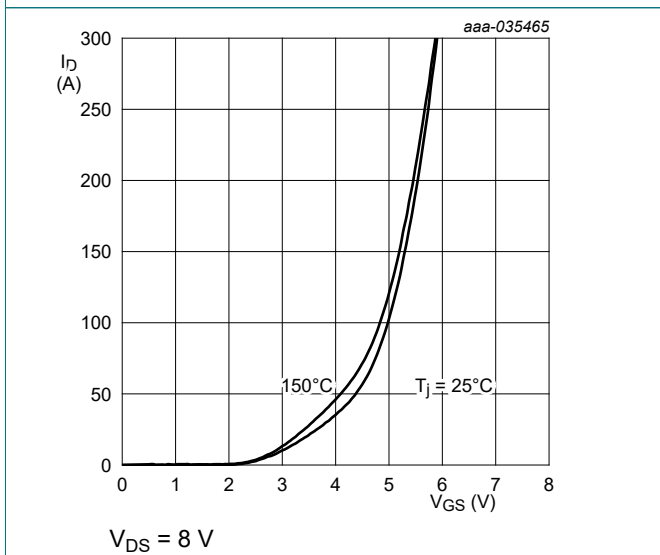


Fig. 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values

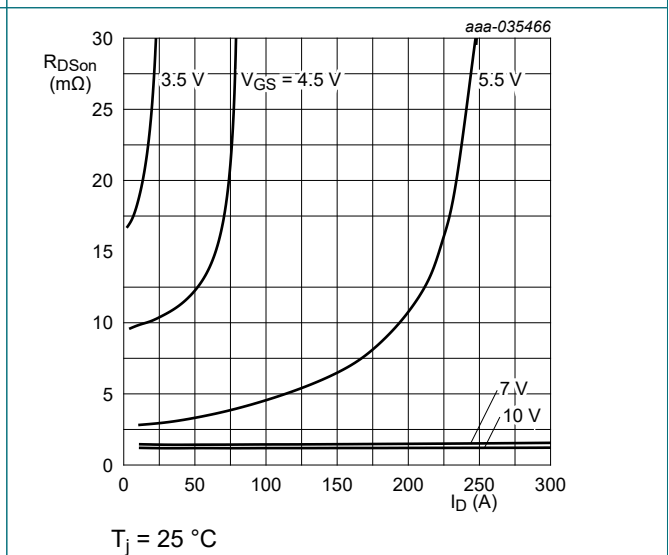
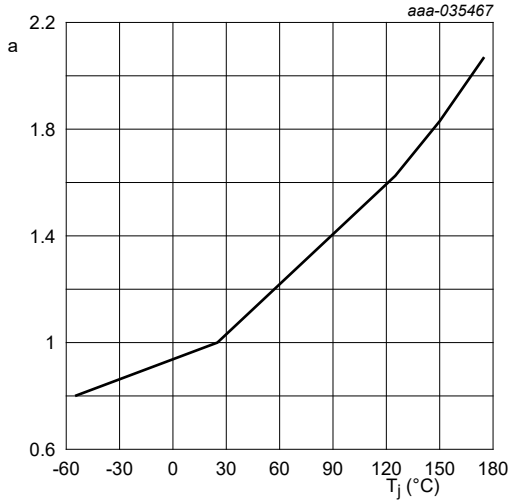
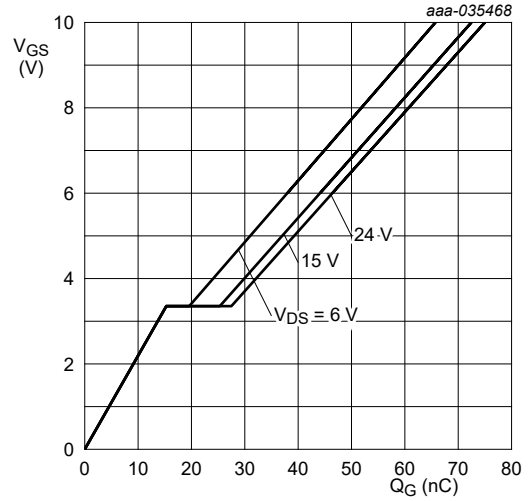


Fig. 10. Drain-source on-state resistance as a function of drain current; typical values



$$a = \frac{R_{DSon}}{R_{DSon}(25^{\circ}C)}$$

Fig. 11. Normalized drain-source on-state resistance factor as a function of junction temperature



$T_j = 25^{\circ}C; I_D = 25 A$

Fig. 12. Gate-source voltage as a function of gate charge; typical values

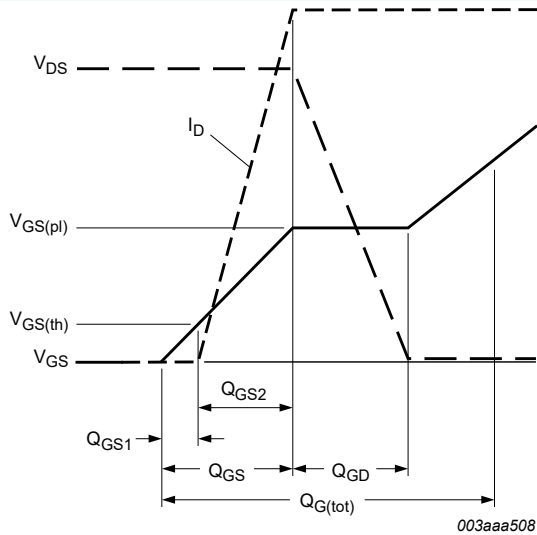
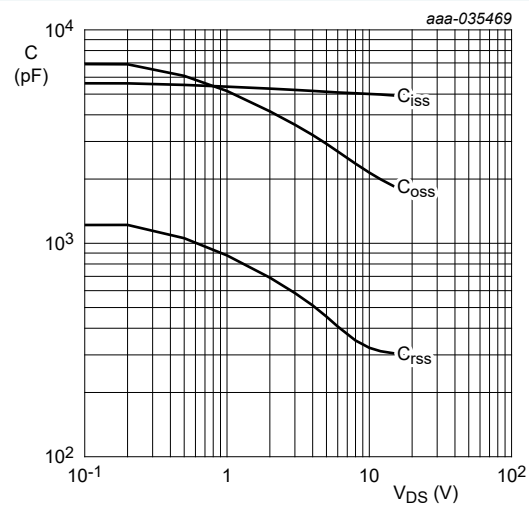
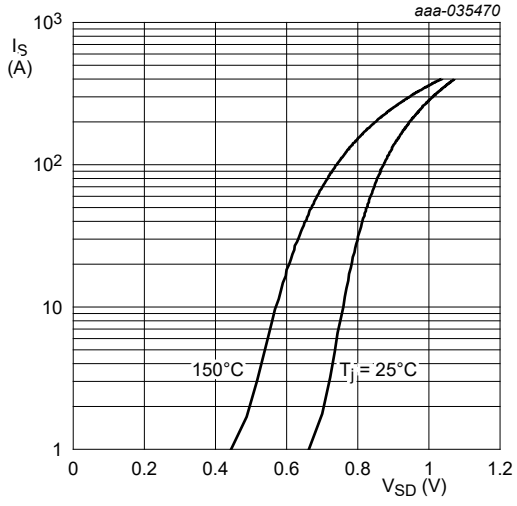


Fig. 13. Gate charge waveform definitions



$V_{GS} = 0 V; f = 1 MHz$

Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$V_{GS} = 0\text{ V}$

Fig. 15. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

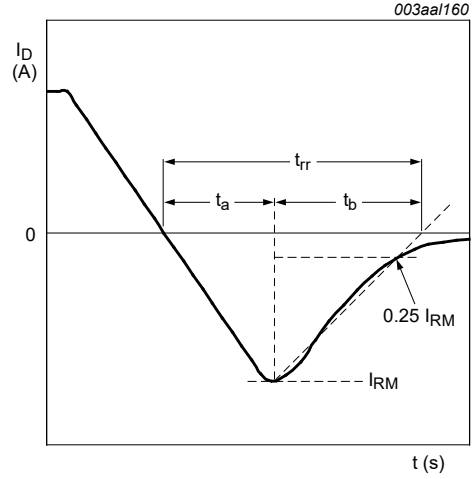


Fig. 16. Reverse recovery timing definition

11. Package outline

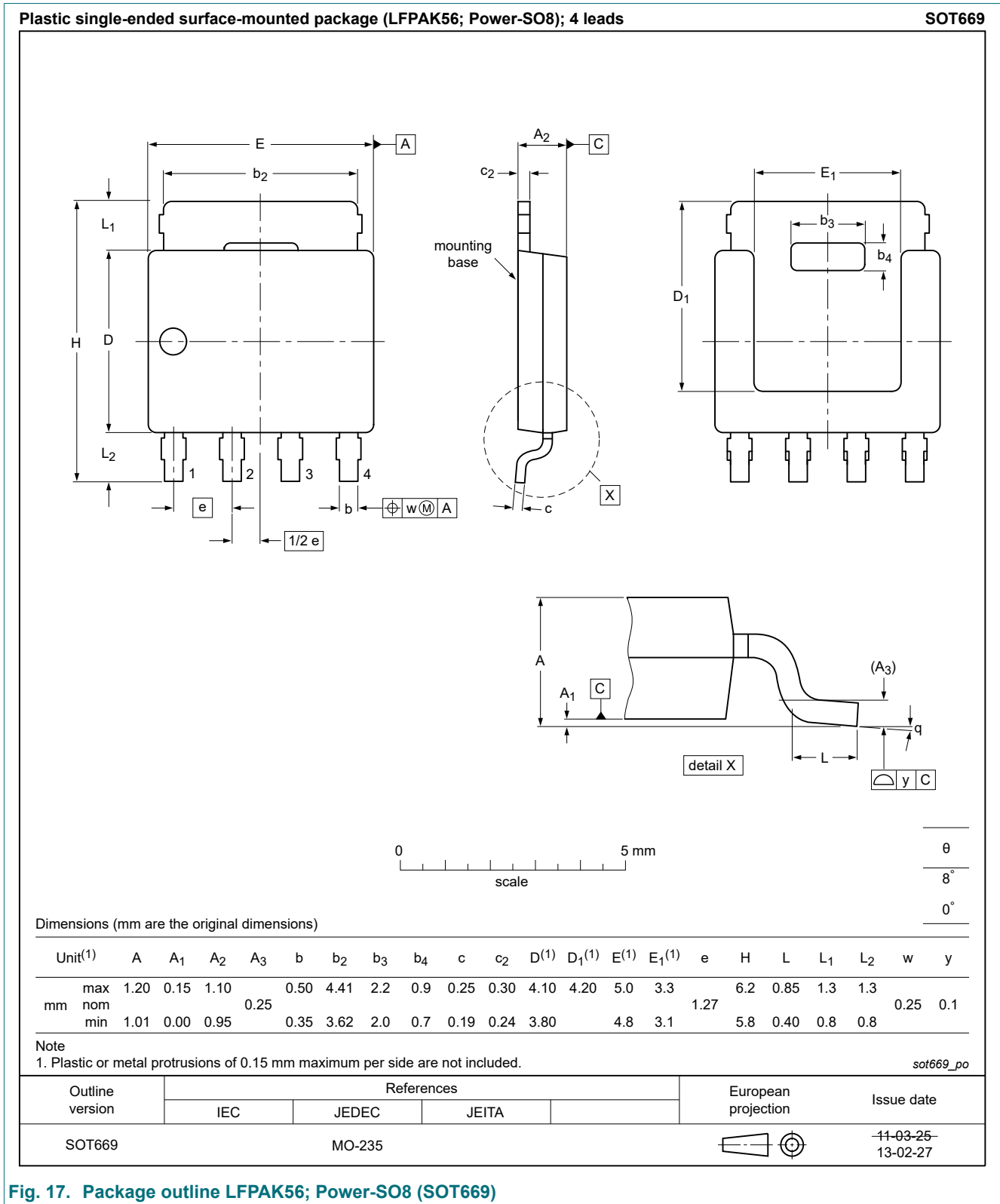


Fig. 17. Package outline LPAK56; Power-SO8 (SOT669)

12. Soldering

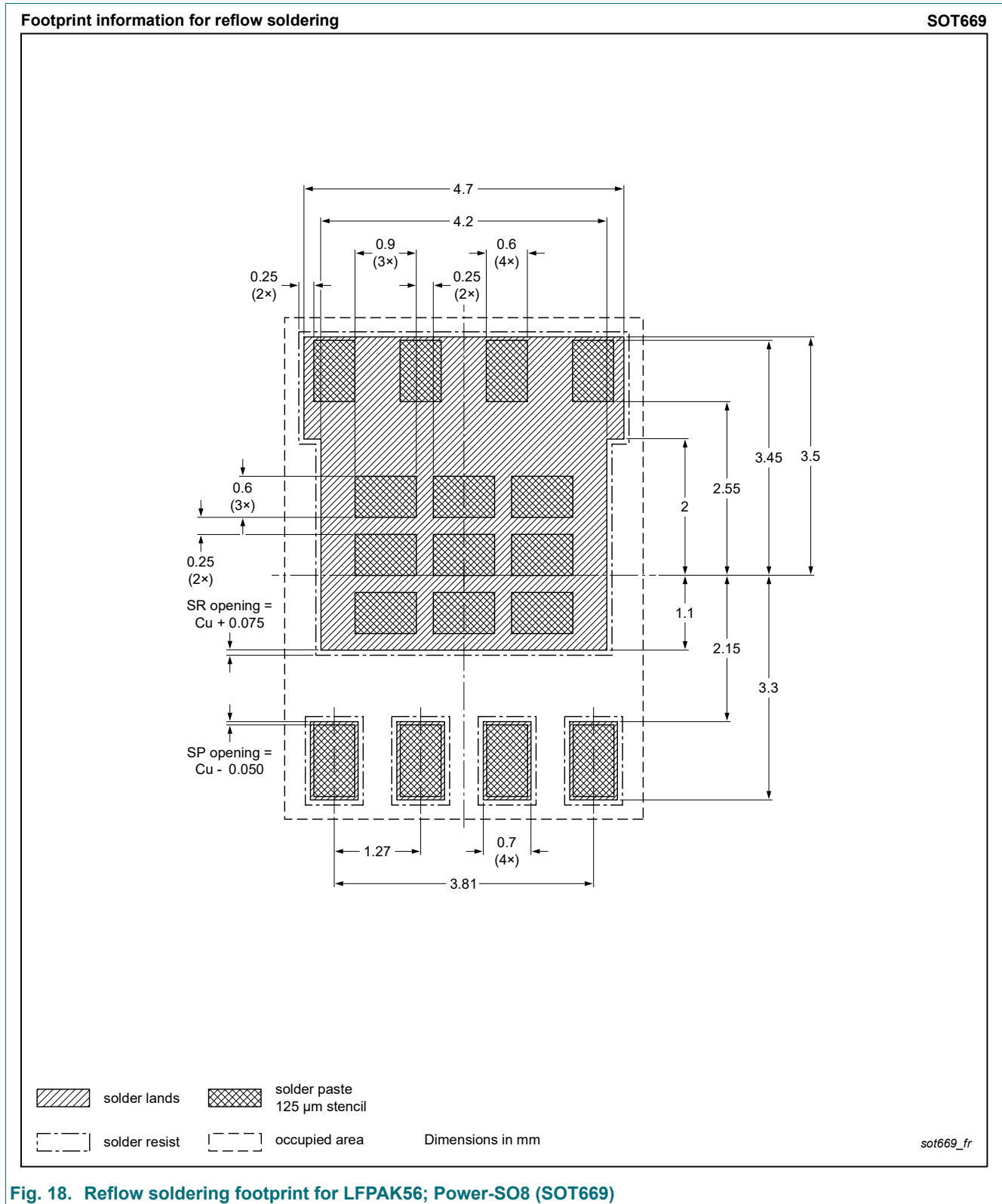
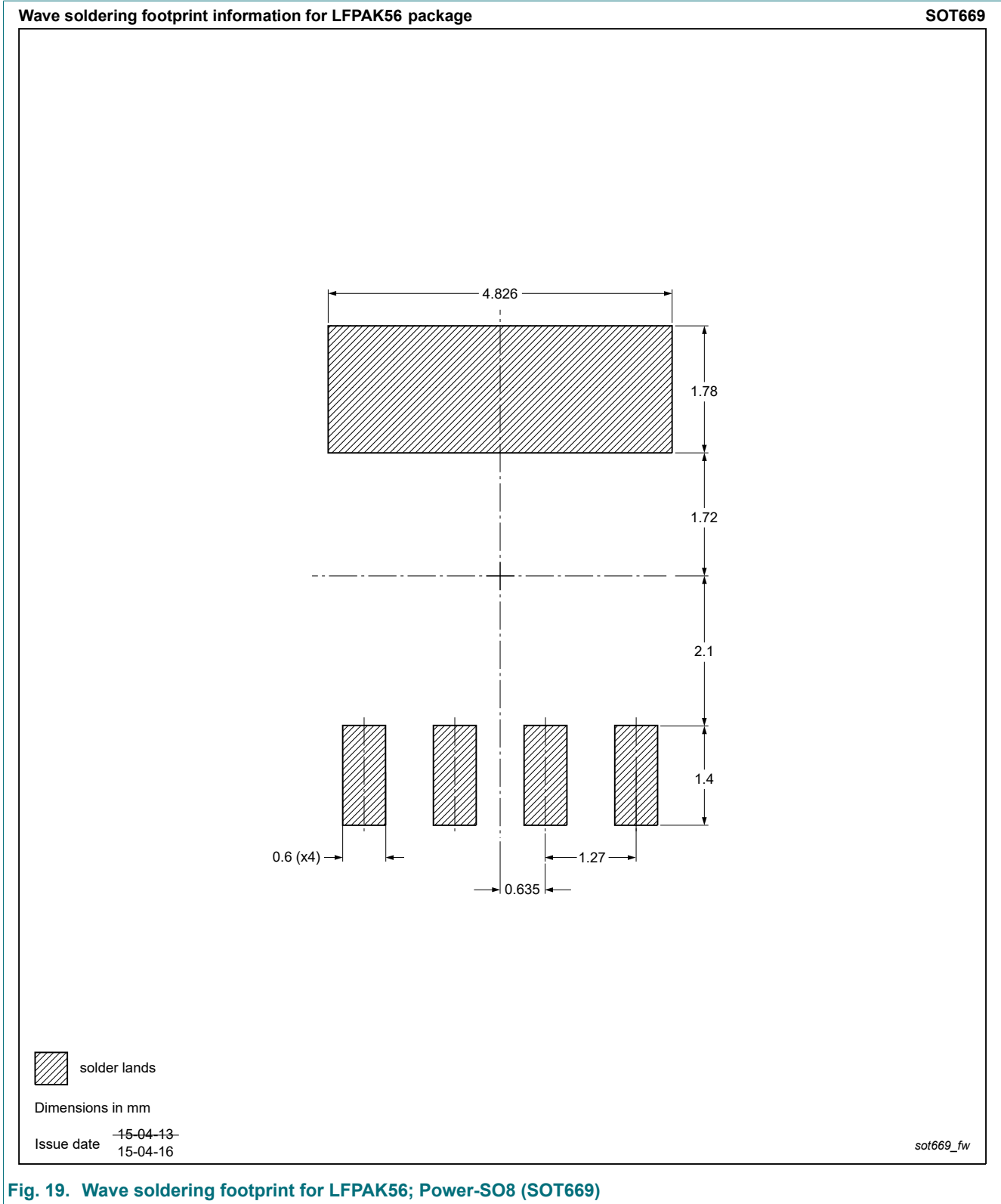


Fig. 18. Reflow soldering footprint for LFPAK56; Power-SO8 (SOT669)



13. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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