

Requirements

- Power supply with 4V and ~800mA rating
- Signal generator (10MHz to 600MHz Input and an amplitude from 0.4V to 0.8V) or crystal
- Signal analyzer
- Two banana plug cables (red and black) to connect the power supply source to the board
- Two SMA cables to connect the signal generator to the CLK/nCLK inputs
- Two SMA cables to connect Q0/nQ0 to the signal analyzer
- 50Ω to ground terminators to terminate the unused outputs
- USB cable to connect the board to a laptop and program the device

DIP Switch Pin

Table 1: DIP Switch Pin Description

| Pin Name | Description |
|-----------------------|---|
| CLK_SEL | Clock select pin. 0: CLK/nCLK; 1: XTAL (Default) |
| OE1 | Output enable. LVCMOS/LVTTL interface levels |
| OE0 | Output enable. LVCMOS/LVTTL interface levels. |
| PLL_BYP | Bypass Selection. Allow PLL references to bypass PLL and appear at Q[0:3]. LVTTL / LVCMOS interface levels. |
| ni ² C/SPI | Serial Interface Mode Selection. LVCMOS Input Levels: 0 = I ² C Mode; 1 = SPI Mode |
| SCAN_MODE | (Factory Use Only) |
| SA1 | I ² C lower address bit A1 / SPI interface serial data input signal. |
| SA0 | I ² C lower address bit A0 / SPI interface chip select signal. |

Legend–Evaluation Board

Inputs

| | |
|-----------|---|
| CLK/nCLK | Clock input lines. Can accept LVPECL, LVDS, LVHSTL, HCSL or LVCMOS input clock. |
| OSCI/OSCO | Crystal input lines. |

Outputs

| | |
|----------|--|
| Q0/nQ0 | Can be a differential pair or two individual single-ended outputs. |
| Q1/nQ1 | Can be a differential pair or two individual single-ended outputs. |
| Q2/nQ2 | Can be a differential pair or two individual single-ended outputs. |
| Q3/nQ3 | Can be a differential pair or two individual single-ended outputs. |
| Q4/nQ4 | Can be a differential pair or two individual single-ended outputs. |
| Q5/nQ5 | Can be a differential pair or two individual single-ended outputs. |
| Q6/nQ6 | Can be a differential pair or two individual single-ended outputs. |
| Q7/nQ7 | Can be a differential pair or two individual single-ended outputs. |
| Q8/nQ8 | Can be a differential pair or two individual single-ended outputs. |
| Q9/nQ9 | Can be a differential pair or two individual single-ended outputs. |
| Q10/nQ10 | Can be a differential pair or two individual single-ended outputs. |
| Q11/nQ11 | Can be a differential pair or two individual single-ended outputs. |

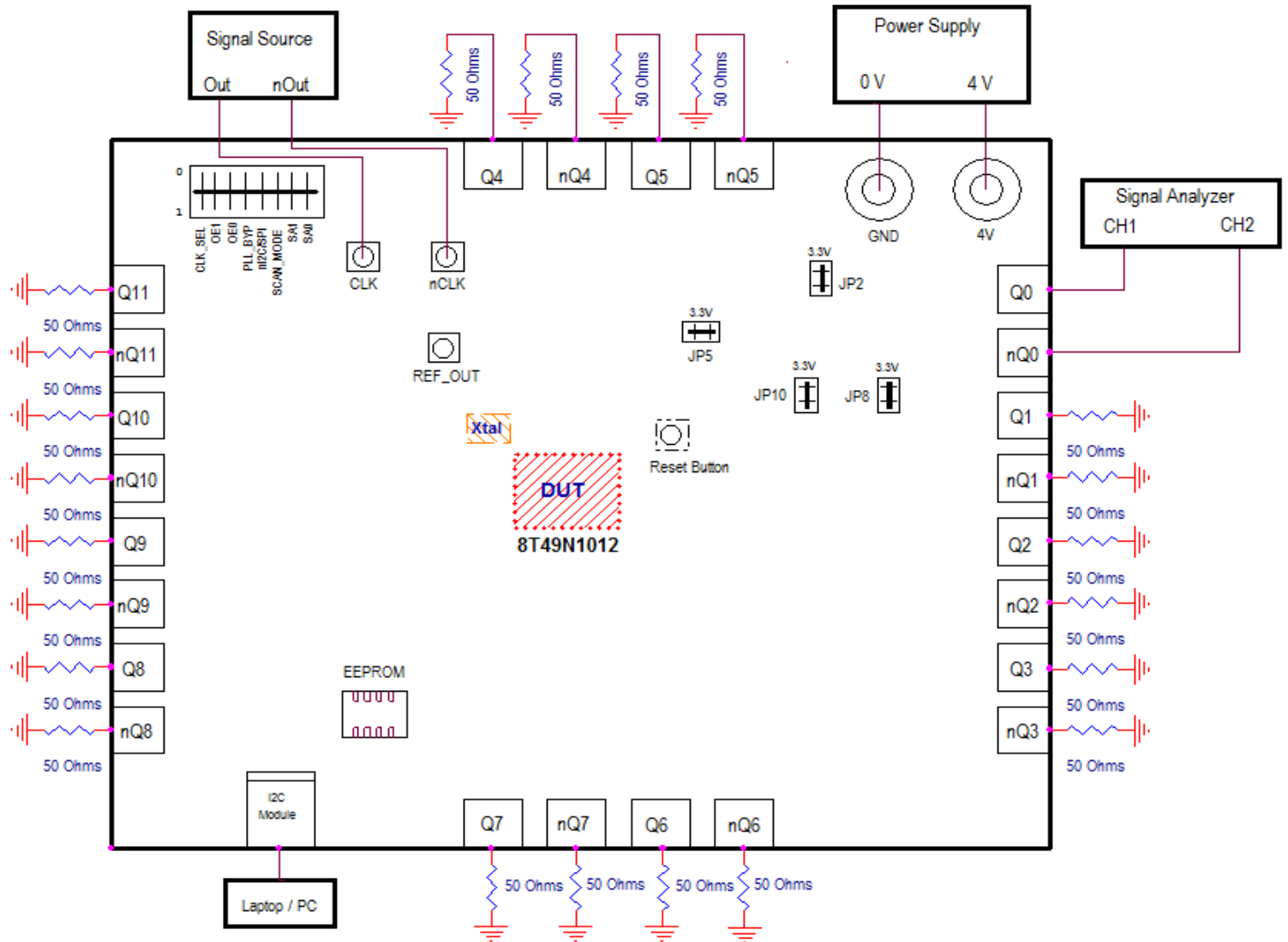
Other

| | |
|---|--|
| A | CLK and nCLK Inputs |
| B | Dip Switch for DC control signals (CLK_SEL, PLL_BYP, etc). |
| C | Device Under Test - 8T49N1012 |
| D | 3.2 x 2.5 mm SMD Fox-603-38.88-4 Crystal. |
| E | EEPROM - AT24CO4C. |
| F | USB connector. |
| G | RESET Button. |
| H | Power Selection Headers and Jumpers. |
| I | REF_OUT. Single-ended 1.8V LVCMOS Output. |
| J | Ground Connection Jack. |
| K | VDD Connection Jack. |

Quick Set-Up 1: Using Clock Generator as Input

- 1) Set power supply to 4V, single supply and set CLK_SEL to "0" on Dip Switch to select Clock as input.
- 2) Place jumpers on JP2, JP5, JP8 and JP10 to set VDD, VDDO and VDDA to 3.3V (if different voltage required, place jumper on the corresponding header).
- 3) Connect the black GND power supply cable to the GND connector of the 8T49N1012 board.
- 4) Connect the red 4 V power supply cable to the 4 V connector of the board.
- 5) Connect the signal generator's SMA cables to CLK/nCLK (*10MHz to 600MHz Input and amplitude from 0.4V to 0.8V*). 50 Ω to GND termination installed on board by default.
- 6) Connect two SMA cables from the Q0/nQ0 outputs of the board to the signal analyzer.
- 7) And finally, connect the USB cable from the laptop to the board's USB connector and program the device using Timing Commander.

Figure 2. Evaluation Board Powered Up and Connectivity Using Clock as Input

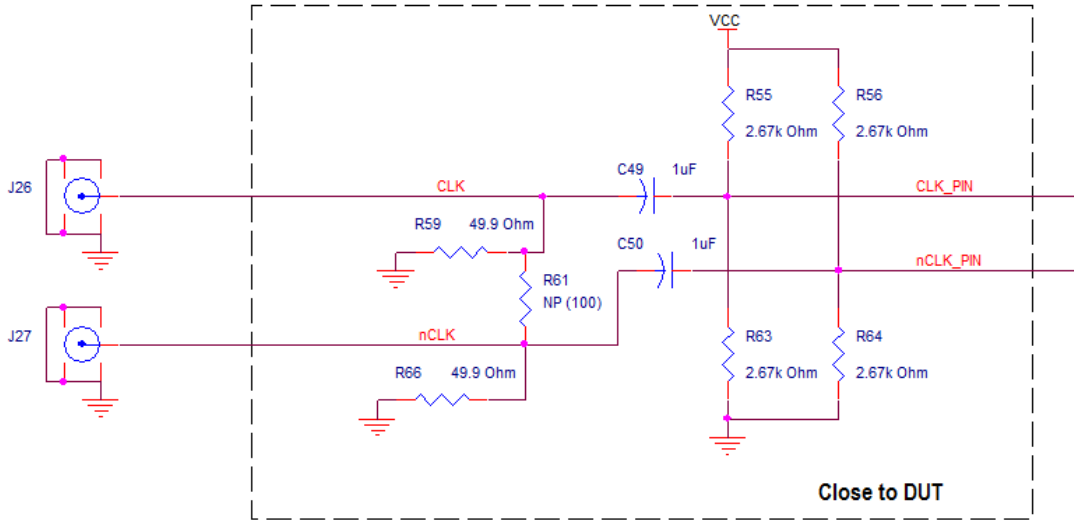


Schematics

The following figures are schematics that are applicable when using a signal generator as input. The complete schematic is available in a separate document. These are the input and output termination schematics.

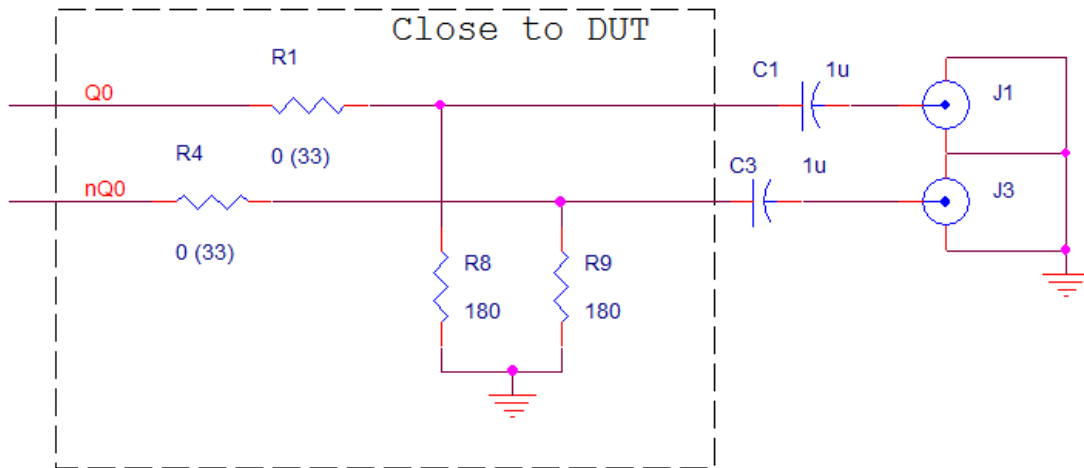
The input schematic is shown in [Figure 3](#).

Figure 3. Input Schematic (Set-up #1)



The output schematic is shown in [Figure 4](#).

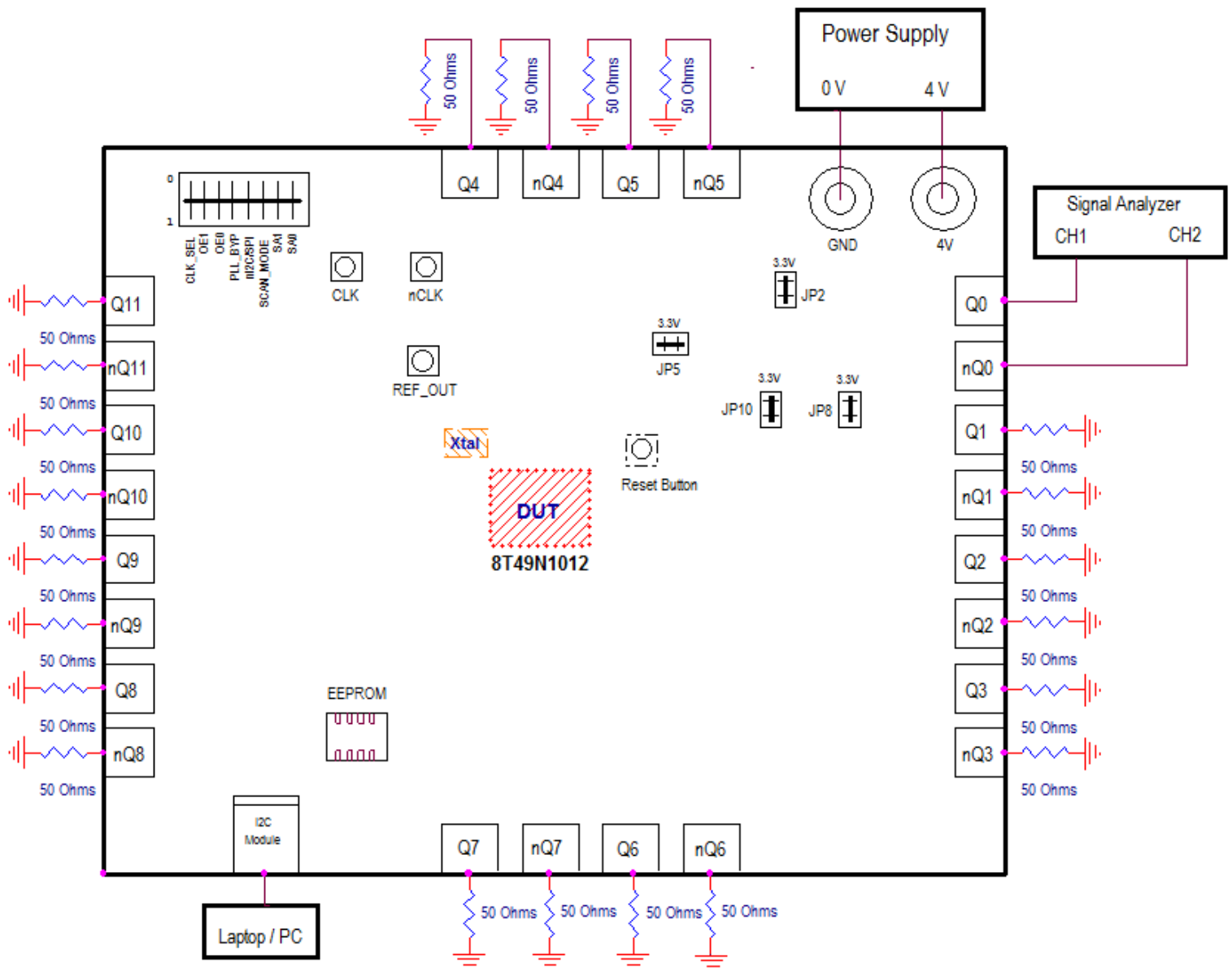
Figure 4. Output Schematic (Set-up #1)



Quick Set-Up 2: Using Crystal as Input

- 1) Set power supply to 4V, single supply and set CLK_SEL to "1" on Dip Switch to select Crystal as input.
- 2) Place jumpers on JP2, JP5, JP8 and JP10 to set VDD, VDDO and VDDA to 3.3V (if different voltage required, place jumper on the corresponding header).
- 3) Connect the black GND power supply cable to the GND connector of the 8T49N1012 board.
- 4) Connect the red 4 V power supply cable to the 4 V connector of the board.
- 5) Connect two SMA cables from the Q0/nQ0 outputs of the board to the signal analyzer.
- 6) Ultimately, connect the USB cable from the laptop to the board's USB connector and program the device using Timing Commander.

Figure 5. Evaluation Board Powered Up and Connectivity Using Crystal as Input

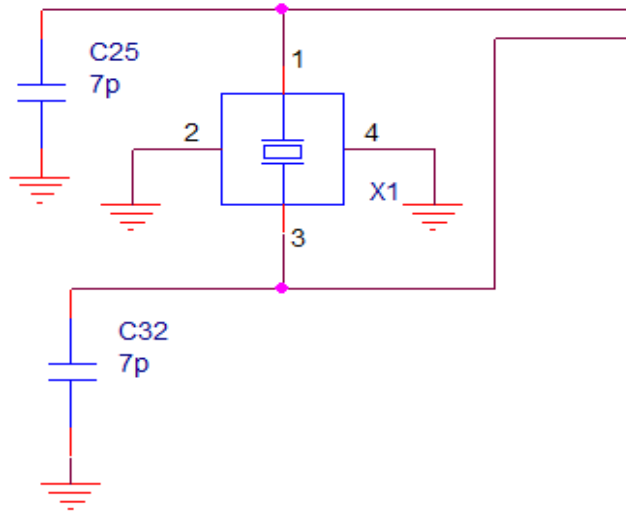


Schematics

The following figures are schematics that are applicable when using the crystal as input. The complete schematic is available in a separate document. These are the input and output termination schematics.

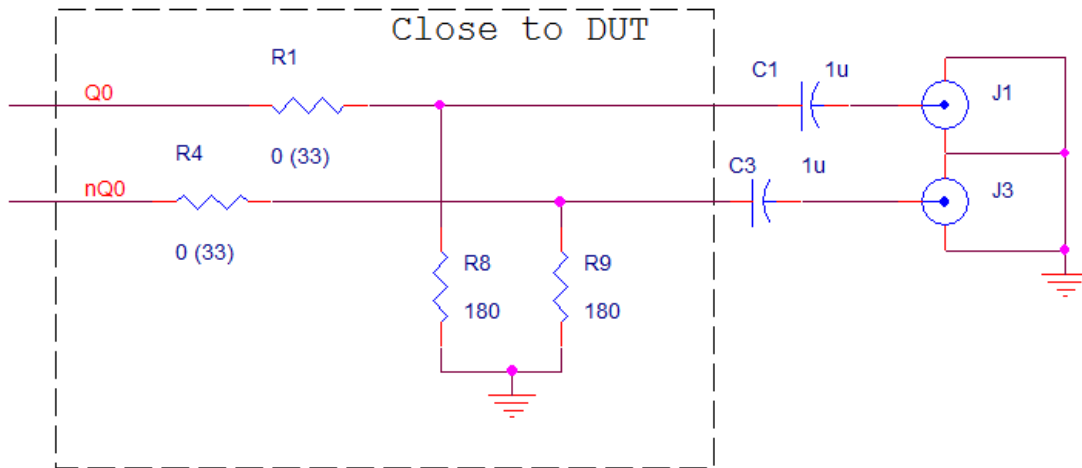
The input schematic is shown in [Figure 6](#).

Figure 6. Input Schematic (Set-Up #2)



The output schematic is shown in [Figure 7](#).

Figure 7. Output Schematic



* If the output frequency is below 50MHz, increase the value of C1 and C3.

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