



## Product Change Notification / SYST-11BSHV285

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### Date:

12-Oct-2022

### Product Category:

Ethernet Switches

### PCN Type:

Document Change

### Notification Subject:

ERRATA - KSZ8567R Silicon Errata and Data Sheet Clarification

### Affected CPNs:

[SYST-11BSHV285\\_Affected\\_CPN\\_10122022.pdf](#)

[SYST-11BSHV285\\_Affected\\_CPN\\_10122022.csv](#)

### Notification Text:

SYST-11BSHV285

Microchip has released a new Errata for the KSZ8567R Silicon Errata and Data Sheet Clarification of devices. If you are using one of these devices please read the document located at [KSZ8567R Silicon Errata and Data Sheet Clarification](#).

**Notification Status:** Final

**Description of Change:** This revision includes the following changes

Silicon Errata Issues	Added note regarding configuration of PHY MMD registers.
Module 1	Added the following text to Work Around description: "Before writing the PHY MMD registers, it is necessary to set the PHY to 100 Mbps speed with auto[negotiation] disabled by writing to register 0xN100- 0xN101. After writing the MMD registers, and after all errata workarounds that involve PHY register settings, write register 0xN100-0xN101 again to enable and restart auto-negotiation. See details in the note above."
Note 1	Updated Module 1's final data address from "0x2001" to "0x2000". Also added note regarding this change.
Module 3	Updated title of section from "Default RGMII ingress timing

	does not comply with the RGMII specification” to “Port 6 Default RGMII ingress timing does not comply with the RGMII specification”
Module 4	Entire Module section rewritten for clarity
Module 6	Added 4 additional addresses to Work Around sec[1]tion: 0xN130 - 0xN133 0xN134 - 0xN137 0xN138 - 0xN13B 0xN13C - 0xN13F
Module 15	Text for Method 2 has been updated from “To detect transmitter lock up, the software should monitor the TxByteCnt (MIB Index 0x81) and the RxByteCnt (MIB Index 0x80). If the RxByteCnt is incrementing but the TxByteCnt remains the same, the software should perform a hard reset of the switch” to “To detect transmitter lockup, see the work around sec[1]tion of Module x: Transmission halt with Half-Duplex and VLAN.”
Module 16	Entire Module section rewritten for updated solution.
Module 18	New Module for I2C usage.
Module 19	New Module for Half-Duplex and VLAN interaction.
Module 20	New Module for Frame Length Check feature.

**Impacts to Data Sheet:** None

**Reason for Change:** To Improve Productivity

**Change Implementation Status:** Complete

**Date Document Changes Effective:** 12 Oct 2022

**NOTE:** Please be advised that this is a change to the document only the product has not been changed.

**Markings to Distinguish Revised from Unrevised Devices:** N/A

## Attachments:

[KSZ8567R Silicon Errata and Data Sheet Clarification](#)

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Affected Catalog Part Numbers (CPN)

KSZ8567RTXI

KSZ8567RTXV-VAO

KSZ8567RTXV-TRV01

KSZ8567RTXV-TRV03

KSZ8567RTXV-TRVAO

KSZ8567RTXI-TR

## KSZ8567R Silicon Errata and Data Sheet Clarification

This document describes known silicon errata for functional revisions A1 of the KSZ8567R. The silicon errata discussed in this document are for silicon revisions as listed in [Table 1](#). The silicon revision can be determined by the device's top marking. A summary of KSZ8567R silicon errata is provided in [Table 2](#).

Some errata work arounds may require modifying register values. If the system design does not include a processor to manage the switch, a small 8-bit PIC or AVR microcontroller can be used to configure the switch via the I<sup>2</sup>C or SPI interface. These low-cost microcontrollers are available in packages as small 8-pins, with integrated oscillator and non-volatile program memory. The microcontroller does not need a MII or RMII connection to the switch. Alternatively, the switch can be configured by a remote computer via the in-band management feature of the switch. The default port for in-band management is port 7.

**TABLE 1: AFFECTED SILICON REVISIONS**

Part Numbers	Silicon Revision	Package Top Mark
KSZ8567RTX	A1	B000

**TABLE 2: SILICON ISSUE SUMMARY**

Item Number	Silicon Issue Summary	Affected Silicon Revisions
1.	<a href="#">Register settings are needed to improve PHY receive performance</a>	A1
2.	<a href="#">Transmit waveform amplitude can be improved (100BASE-TX, 10BASE-T, 10BASE-Te)</a>	A1
3.	<a href="#">Port 6 Default RGMII ingress timing does not comply with the RGMII specification</a>	A1
4.	<a href="#">100BASE-TX Energy Efficient Ethernet (EEE) is subject to link drop</a>	A1
5.	<a href="#">Toggling PHY Powerdown can cause errors or link failures in adjacent PHYs</a>	A1
6.	<a href="#">Certain PHY registers must be written as pairs instead of singly</a>	A1
7.	<a href="#">Register settings are required to meet data sheet supply current specifications</a>	A1
8.	<a href="#">Automatic SPI Data Out Edge Select may cause issues</a>	A1
9.	<a href="#">No Pause frames are generated for ingress rate limiting with an EEE link</a>	A1
10.	<a href="#">Link drop can occur when back pressure is enabled in 100BASE-TX half-duplex mode</a>	A1
11.	<a href="#">Port may hang in half-duplex mode when No Excessive Collision Drop feature is enabled</a>	A1
12.	<a href="#">When tail tag is enabled, frame length field check fails for 802.3 frames</a>	A1
13.	<a href="#">Port based priority remapping is not supported</a>	A1
14.	<a href="#">Occasional high current on AVDDL supply pins during hardware reset</a>	A1
15.	<a href="#">Transmission halt with late collisions</a>	A1
16.	<a href="#">Single-LED Mode Setting Requires Two Register Writes</a>	A1
17.	<a href="#">PTP messages get dropped in PTP 2-Step Mode</a>	A1
18.	<a href="#">IBA Must Be Disabled When Using I<sup>2</sup>C</a>	A1
19.	<a href="#">Transmission halt with Half-Duplex and VLAN</a>	A1
20.	<a href="#">Frame Length Field Check feature does not work well when the actual frame length is less than 64 bytes</a>	A1

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## Silicon Errata Issues

### IMPORTANT NOTE

Multiple errata workarounds in this document call for changing PHY registers for each PHY port. PHY registers 0x0 to 0x1F are in the address range 0xN100 to 0xN13F, while indirect (MMD) PHY registers are accessed via the PHY MMD Setup Register and the PHY MMD Data Register.

Before configuring the PHY MMD registers, it is necessary to set the PHY to 100 Mbps speed with auto-negotiation disabled by writing to register 0xN100-0xN101. After writing the MMD registers, and after all errata workarounds that involve PHY register settings, write register 0xN100-0xN101 again to enable and restart auto-negotiation.

[addr]	[data]	
0xN100-0xN101	0x2100	Disable auto-neg, force 100M full-duplex
[PHY register initialization goes here]		
0xN100-0xN101	0x3300	Enable auto-neg, restart auto-neg

### Module 1: Register settings are needed to improve PHY receive performance

#### DESCRIPTION

The default receiver settings are not optimized. Receive errors may occur, especially at longer cable lengths.

#### END USER IMPLICATIONS

For best receiver performance, users should write the following PHY MMD registers. This is done individually for each port (1-5) using any of the management interfaces: MDC/MDIO, I<sup>2</sup>C, SPI, or in-band.

#### Work Around

Before writing the PHY MMD registers, it is necessary to set the PHY to 100 Mbps speed with auto-negotiation disabled by writing to register 0xN100-0xN101. After writing the MMD registers, and after all errata workarounds that involve PHY register settings, write register 0xN100-0xN101 again to enable and restart auto-negotiation. See details in the important note at the beginning of the Silicon Errata Issues section.

Write to the following MMD registers for each PHY port [1-5]:

[MMD]	[register]	[data]
0x01	0x6F	0xDD0B
0x01	0x8F	0x6032
0x01	0x9D	0x248C
0x01	0x75	0x0060
0x01	0xD3	0x7777
0x1C	0x06	0x3008
0x1C	0x08	0x2000 (Note 1)

**Note 1:** The value of this register may read back as either 0x2000 or 0x2001. Bit 0 is read-only, and is not a fixed value.

#### PLAN

This erratum will not be corrected in a future revision.

## Module 2: Transmit waveform amplitude can be improved (10BASE-TX, 10BASE-T, 10BASE-Te)

### DESCRIPTION

The transmit waveform amplitude can be improved for 10BASE-T, 10BASE-Te and 100BASE-TX.

### END USER IMPLICATIONS

With the default settings, the waveform amplitude may be outside the specifications in some corner case conditions, and the transmitter may not be fully compliant with the IEEE standard. This may degrade performance under some conditions.

#### **Work Around**

If AVDDH = 2.5V (supports 10BASE-Te, not 10BASE-T), write to the following MMD registers for each PHY port [1-5]:

[MMD]	[register]	[data]
0x1C	0x4	0x00D0

If AVDDH = 3.3V (supports 10BASE-T, not 10BASE-Te), write to the following MMD registers for each PHY port [1-5]:

[MMD]	[register]	[data]
0x1C	0x9	0xE214
0x1C	0x4	0x00D0

### PLAN

This erratum will not be corrected in a future revision.

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## Module 3: Port 6 Default RGMII ingress timing does not comply with the RGMII specification

### DESCRIPTION

The RGMII defining document specifies a typical data-to-clock setup time into the receiver (switch signals TXD6\_[3:0], TX\_ER6 and TX\_EN6 to TX\_CLK6) of 1.8ns. However, port 6 requires additional setup time in order to avoid ingress data errors on this interface. Refer to the data sheet for details.

This issue does not occur on port 7, and there are no timing issues with the MII and RMII modes.

### END USER IMPLICATIONS

Careful analysis of the RGMII timing must be performed, considering the timing of both connected devices, and relative signal delay times on the PCB.

#### **Work Around**

Additional PCB trace delay may be needed on the TX\_CLK6 clock signal into port 6 of the switch. Another option is to set the ingress delay bit [4] in register 0x6301. Refer to the data sheet for timing details.

### PLAN

This erratum will not be corrected in a future revision



## Module 4: 100BASE-TX Energy Efficient Ethernet (EEE) is subject to link drop

### DESCRIPTION

Infrequent link drop errors can occur on 100BASE-TX EEE links with long cable length and certain link partners. Separately, data errors may occur at the link partner.

### END USER IMPLICATIONS

By default, EEE is enabled in each switch PHY. If EEE is also enabled in the link partner, then EEE is activated. If the link partner does not support EEE, then EEE will not be activated on the link.

With default settings, the EEE power saving feature can result in occasional data loss or infrequent temporary link down conditions.

#### **Work Around**

1. The suggested workaround is to disable EEE. This is done by writing the following register:

MMD registers:

[MDD]	[register]	[data]
7	0x3C	0x0000

After writing to the MMD register, it is necessary to write to register 0xN100-0xN101 to restart auto-negotiation.

[address]	[data]
0xN100-0xN101	0x3300

2. The 100BASE-TX EEE link problems should be solved by performing the following register writes. Refer to the MMD section of the data sheet for examples of how to access the indirect PHY MMD registers.

Before writing the PHY MMD registers, it is necessary to set the PHY to 100 Mbps speed with auto-negotiation disabled by writing to register 0xN100-0xN101. After writing the MMD registers, and after all errata workarounds that involve PHY register settings, write register 0xN100-0xN101 again to enable and restart auto-negotiation. See details in the note above.

Global register:

[addr]	[data]
0x03C2	0x0080

MMD registers:

[MMD]	[register]	[data]
1	0xCE	0x0900
1	0xCC	0x0FE0
1	0xCA	0x0141
1	0xCB	0x0FD6
1	0xC8	0x0010
1	0xD9	0x0160
0xC7	0x81E0PLAN	1 0xC9 0x0180 1

This erratum will not be corrected in a future revision.

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## Module 5: Toggling PHY Powerdown can cause errors or link failures in adjacent PHYs

### DESCRIPTION

The PHY power down is controlled by bit 11 in registers 0xN100-0xN101. It provides separate power down control for each PHY. When a PHY is brought out of power down by clearing this bit, the resulting power surge can disrupt an adjacent PHY, causing data errors or temporary link down on that port.

### END USER IMPLICATIONS

Data errors or link down can occur in an active PHY when its neighbor is brought out of power down mode.

#### **Work Around**

Avoid dynamically changing the power down state of any PHYs if other PHYs may be linked and active. Only change the power up or power down state of a PHY when no other PHYs on the chip are linked and possibly passing traffic.

### PLAN

This erratum will not be corrected in a future revision.

## Module 6: Certain PHY registers must be written as pairs instead of singly

### DESCRIPTION

When using SPI, I<sup>2</sup>C, or in-band register access, writes to certain PHY registers should be performed as 32-bit writes instead of 16-bit writes.

The PHY control and status registers are 16-bit registers. They occupy the byte address range 0xN100 to 0xN13F, where N is the port number. Registers from 0xN100 to 0xN11F function normally and can be written either 16- or 8-bits at a time.

An error in the register access logic causes all writes from 0xN120 to 0xN13F to be 32-bit writes. For example, a 16-bit write to register 0xN122-0xN123 also results in all zeros being written to register 0xN120-0x121. Also, a 16-bit write to register 0xN120-0xN121 causes all zeros to be written to 0xN122-0xN123.

### END USER IMPLICATIONS

This issue is relevant only to write operations, not to reads. When writing only 16-bits to a register in this address range, all zeros will be written to the adjacent register. This may change the PHY settings and cause the PHY to malfunction.

#### **Work Around**

To avoid writing zero to an adjacent register, always write the registers in this address range in pairs as 32-bits:

0xN120 - 0xN123

0xN124 - 0xN127

0xN128 - 0xN12B

0xN12C - 0xN12F

0xN130 - 0xN133

0xN134 - 0xN137

0xN138 - 0xN13B

0xN13C - 0xN13F

Note that some of these registers are not defined in the data sheet. In order to avoid writing inappropriate data to any undefined register, the register should be read before writing (i.e. read-modify-write). Do not assume that undocumented registers should be all zeros.

### PLAN

This erratum will not be corrected in a future revision.

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## Module 7: Register settings are required to meet data sheet supply current specifications

### DESCRIPTION

The power supply current specifications in the data sheet are based on the following register settings. Without these register changes, the AVDDH current is approximately 21% greater, and total chip power is approximately 7% greater when all PHY ports are linked at 100Mb/s.

### END USER IMPLICATIONS

If the following register settings are not made, the chip can dissipate more power than indicated in the data sheet for the AVDDH power rail. This means that under the worst case conditions (all PHY ports linked at 100 Mb/s), the junction temperature may approach or exceed 125°C when operating at the maximum ambient temperature. Device and system thermal analysis should use the increased AVDDH current value if the following register settings are not made. The voltage regulator supplying AVDDH must also have adequate current capacity.

#### Work Around

Write to the following MMD registers for each PHY port [1-5]:

[MMD]	[register]	[data]
0x1C	0x13	0x6EFF
0x1C	0x14	0xE6FF
0x1C	0x15	0x6EFF
0x1C	0x16	0xE6FF
0x1C	0x17	0x00FF
0x1C	0x18	0x43FF
0x1C	0x19	0xC3FF
0x1C	0x1A	0x6FFF
0x1C	0x1B	0x07FF
0x1C	0x1C	0x0FFF
0x1C	0x1D	0xE7FF
0x1C	0x1E	0xEFFF
0x1C	0x20	0xEEEE

### PLAN

This erratum will not be corrected in a future revision.

## Module 8: Automatic SPI Data Out Edge Select may cause issues

### DESCRIPTION

Automatic SPI Data Out Edge Select is a feature that is normally enabled in register 0x0100. It detects the SPI clock frequency and selects either the rising clock edge or falling clock edge to clock out the SPI data based on that frequency. The behavior is not fully predictable when the SPI clock frequency is near 25MHz, which may cause the SPI interface to stop functioning. Also, it does not adapt to changes in the SPI clock frequency.

### END USER IMPLICATIONS

The SPI interface may stop functioning if the inappropriate clock edge is selected, or if the clock rate changes. Generally there is no problem when operating at lower clock rates, such as below 15 MHz.

#### **Work Around**

When operating the SPI above 15 MHz, it is suggested to disable the automatic feature by clearing register 0x0100 bit 1, and at the same time setting bit 0 to the desired value to manually select the mode of operation.

### PLAN

This erratum will not be corrected in a future revision.

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## Module 9: No Pause frames are generated for ingress rate limiting with an EEE link

### DESCRIPTION

When an Energy Efficient Ethernet (EEE) link is established with another device, and ingress rate limiting is set up, the port may not generate Pause frames in response to ingress traffic exceeding the rate limit. It also assumes that the Ingress Rate Limit Flow Control Enable bit in register 0xN403 has been set.

### END USER IMPLICATIONS

If Pause frames are not generated by the switch, then the link partner will not be able to regulate the rate at which it sends traffic, making ingress rate limiting ineffective. Note that when the flow control function is enabled for ingress rate limiting, the ingress port will not drop packets when the rate limit is exceeded - it relies only on flow control for limiting the ingress rate.

#### **Work Around**

The problem can be resolved by writing to the following three global registers. Note that these registers may not be documented in the data sheet.

Global registers:

[addr]	[data]
0x03C0	0x4090
0x03C2	0x0080
0x03C4	0x2000

### PLAN

This erratum will not be corrected in a future revision.

## Module 10: Link drop can occur when back pressure is enabled in 100BASE-TX half-duplex mode

### DESCRIPTION

When back pressure is enabled for 100BASE-TX half duplex mode, CRS-based back pressure is the default mode. In this mode, if the switch forwards long packets and the link partner is set up to detect and respond to jabber, then the link partner may drop link. The link down condition is temporary.

### END USER IMPLICATIONS

If all of the above conditions are met, then this problem is likely to occur, which will be disruptive, even though it is self-healing. If any of the above conditions are not present, then the problem will not occur. In general, half-duplex is not common. It is also very uncommon for NICs or switches to implement jabber-based link drop since they are normally full-duplex. This function is seen mostly in hubs, which are half duplex.

#### **Work Around**

The workaround is to change the back pressure mode from CRS-based to collision-based by clearing bit 5 in register 0x0331. This completely eliminates the link drop problem. This register can be written using the SPI, I<sup>2</sup>C, or in-band management interface, but not via the MIIM interface.

Global register:

[addr]	[data]
0x0331	0xD0

### PLAN

This erratum will not be corrected in a future revision.

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## Module 11: Port may hang in half-duplex mode when No Excessive Collision Drop feature is enabled

### DESCRIPTION

This issue is seen when two of these switch devices are connected together and are configured in the same way. The two devices use the same back-off algorithm and their back-off can become synchronized, causing lock-up.

### END USER IMPLICATIONS

“No excessive collision drop” is a feature that may be used for half duplex to potentially improve collision performance. It is controlled in register 0x0300, and is disabled by default. If it is enabled and the link partner is a similar device, then lock up can occur on the link. It will persist until the link is broken (either physically or by register) and re-established.

#### **Work Around**

The problem is avoided by enabling the Alternate back-off algorithm when using the No excessive collision drop feature. This is done by setting bit 7 in register 0x0330. This register can be written using the SPI, I<sup>2</sup>C, or in-band management interface, but not via the MIIM interface.

### PLAN

This erratum will not be corrected in a future revision.



## Module 12: When tail tag is enabled, frame length field check fails for 802.3 frames

### DESCRIPTION

The comparison of the length field of the Ethernet frame with the actual length of the data field portion of the frame fails for the ingress packets with tail tag. This issue is not applicable to packets with the type field in the frame.

### END USER IMPLICATIONS

The packets will be dropped when length check fails for the packet.

#### **Work Around**

Do not set the length check in bit 3 of the register 0x0330 (Global Switch MAC Control Register 0). The Microchip provided driver disables the length check.

### PLAN

This erratum will not be corrected in a future revision.

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## Module 13: Port based priority remapping is not supported

### DESCRIPTION

The 802.1Q-2014 Clause 6 (6.9.4 Regenerating priority) describes the Priority Regeneration Table for the reception port, which is required to support an AVB boundary port. The boundary port in the AVB domain needs to remap the priority field of the incoming traffic.

Since the device do not support port based priority remapping, the port cannot be used as a boundary port.

This erratum is not applicable if all the device ports are AVB domain ports.

### END USER IMPLICATIONS

The device port cannot be used as an AVB domain boundary port.

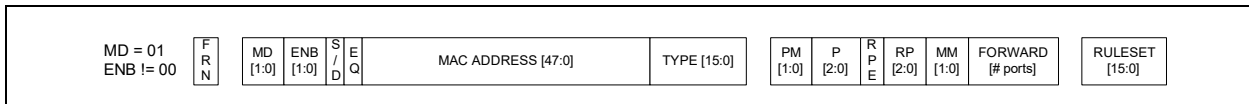
#### Work Around

A software workaround is available to remap the priority of all the incoming traffic to the port. The workaround uses an ACL (Access Control List) mechanism to remap the priority of the incoming traffic to 0. With the workaround, there is no impact on AVB traffic. If the incoming traffic uses QoS, priorities are also remapped to 0. This may have a minor impact on the QoS traffic (i.e., all the QoS traffic uses one egress queue instead of using the two queues available in the device). The workaround is available in Microchip provided driver software.

Software Workaround:

Program the ACL rule to remap all the incoming layer 2 packets to priority 0 (ACL rule format shown in [Figure 1](#)).

**FIGURE 1: ACL RULE FORMAT**



Rule Description:

MD = 01 : Layer 2

ENB = 10 : Comparison on EtherType value

EQ = 0 & TYPE = 0 : I.e., all packets (condition is when EtherType != 0)

PM = 11 : Always change priority to P[2:0]

P = 0 : Priority value to be changed

### PLAN

This erratum will not be corrected in a future revision.

## Module 14: Occasional high current on AVDDL supply pins during hardware reset

### DESCRIPTION

AVDDL is one of the two 1.2V device supply rails. When the in hardware reset (RESET\_N pin is low), AVDDL typically draws less than 15mA. However, the AVDDL current can occasionally be as high as 350mA during hardware reset. Intermediate current levels are also possible. Similarly, AVDDH current is typically less than 40mA during hardware reset, but it can occasionally be as high as 130mA. Increased current always occurs on both rails together. Note that the DVDDL and VDDIO currents never vary during reset. Also note that this high current condition does not occur during any of the software reset modes.

### END USER IMPLICATIONS

The maximum AVDDH reset current is less than the worst case AVDDH operational current, so it presents no issue. However, the AVDDL reset current can exceed the worst case AVDDL operational current by more than a factor of two. Total device power dissipation during reset will always be less than the power consumption during full operation, so there are no issues with power dissipation or temperature. This issue does not cause any concerns relating to the device itself. The only potential concern is if the 1.2V AVDDL voltage regulator cannot supply enough current and maintain the voltage.

#### **Work Around**

There is no method for avoiding this periodic high current condition during hardware reset.

To determine if this is an issue for a particular board design, consider whether AVDDL and DVDDL are powered from the same voltage regulator or from separate regulators. Typical operating current under maximum chip utilization is 350mA and 140mA for DVDDL and AVDDL, respectively. During reset, the currents can be 120mA and 350mA, respectively. Therefore, combined (AVDDL + DVDDL) 1.2V reset current will not exceed the combined 1.2V operational current. If one regulator supplies both AVDDL and DVDDL, there is no issue.

However, if AVDDL has its own voltage regulator separate from DVDDL, then it should be capable of delivering 350mA to ensure the voltage does not droop during reset.

### PLAN

This erratum will not be corrected in a future revision.

# KSZ8567R

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## Module 15: Transmission halt with late collisions

### DESCRIPTION

Section 4 of the IEEE 802.3 Specification details Carrier Sense Multiple Access / Collision Detection (CSMA/CD) parameters when operating in half-duplex mode. The first 512 bit times are designated as the slotTime, which is the maximum amount of time allowed for a collision to occur. If a link partner is configured incorrectly, where the PHY is linking in half-duplex mode but the MAC is configured in full-duplex mode, there is a chance that the link partner will generate a collision after the first 512 bit times, violating the IEEE 802.3 specification. These late collisions, combined with other factors, can cause the switch port transmitter to lock up and stop sending packets. The receiver will still function.

### END USER IMPLICATIONS

If this erratum occurs, the switch will stop transmitting data to the half-duplex port, making it seem the half-duplex link partner has stopped communicating to the network. The more traffic there is, the greater the risk of the violating link partner generating a late collision that will affect the port.

#### **Work Around**

Ideally, the link partner that is violating the specification would need to be updated so the MAC and PHY are correctly configured to the same duplex setting. If the link partner cannot be modified to conform to the IEEE 802.3 specification, the switch can be re-configured to full-duplex when late collisions are detected to avoid a lock up condition. Of note, each switch port functions independently. Therefore, any work around must be implemented separately for each port.

#### **Method 1:**

To avoid transmitter lock up, when a port is linked in half-duplex mode, the software should monitor the TxLateCollision MIB counter (MIB Index 0x16). If the number is ever non-zero, the software should force the link to function in full-duplex mode by disabling auto-negotiation and setting full-duplex and the appropriate speed in the PHY Basic Control Registers (addresses 0xN100 - 0xN101).

#### **Method 2:**

To detect transmitter lockup, see the work around section of [Module 19: Transmission halt with Half-Duplex and VLAN](#).

### PLAN

This erratum will not be corrected in a future revision.

## Module 16: Single-LED Mode Setting Requires Two Register Writes

### DESCRIPTION

The PHY Port LEDx\_0 pin does not go low in the presence of link activity when Single-LED Mode is selected in the MMD LED Mode Register.

### END USER IMPLICATIONS

When Single-LED Mode is selected, an additional bit in a different register must also be written. When this is done, the LED pins will function correctly. When Tri-Color Dual-LED Mode (the default mode) is selected, do not set the additional register bit.

#### **Work Around**

To fully enable Single-LED Mode:

- Single-LED mode is selected by setting bit 4 in the MMD LED Mode Register (PHY MMD address 2, register 0). (Write 0x11 to this register.)
- Implement the workaround by writing 0xfa00 to register 0xN13C-0xN13D (PHY register 0x1E). This sets bit 9, which corrects Single-LED mode operation for the LEDx\_0 pin.

<b>Note:</b> Due to a separate errata module about needing to perform 32-bit writes to certain PHY registers, this needs to be a 32-bit write of data 0xfa00_0300 to registers 0xN13C-0xN13F.
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Each port has its own LED mode setting.

### PLAN

This erratum will not be corrected in a future revision.

# KSZ8567R

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## Module 17: PTP messages get dropped in PTP 2-Step Mode

### DESCRIPTION

When PTP 2-Step Mode is enabled by clearing bit 0 of the Global Message Config 1 Register (bit 0 of 0x0514 - 0x0515), some of the PTP messages (e.g., Sync/Follow-up/Announce) get dropped by the same transmit port. The packet drop will happen when the normal traffic is on the same port as PTP messages. This issue happens only in PTP 2-Step Mode.

### END USER IMPLICATIONS

The gPTP/AVB protocols are required to run in PTP 2-Step Mode. With this erratum, the device cannot achieve time synchronization with the other devices in 2-Step Mode.

#### **Work Around**

To work around this issue, a Software Two-Step Simulation Mode in hardware 1-Step Mode is suggested.

For gPTP operation, the switch hardware needs to be configured in 1-Step Mode by setting bit 0 of Global PTP Message Config 1 Register (Bit 0 of 0x0514 - 0x0515). Because the switch hardware is running in 1-Step Mode, the hardware is still automatically updating the contents of the Sync and Pdelay\_Resp messages.

#### **Sync, Follow-up:**

The Sync transmit interrupt needs to be enabled so that Follow\_Up messages can be updated with the Sync transmit timestamp.

The master sends a Two-Step Sync, which contains the Sync transmit timestamp. The master then sends a Follow\_Up with the same transmit timestamp. The slave still receives the Sync transmit timestamp from the Follow\_Up, so there is no change in application.

#### **Pdelay\_Req, Pdelay\_Resp, Pdelay\_Resp\_Follow\_Up:**

The master sends a Two-Step Pdelay\_Resp with the Pdelay\_Req receive timestamp and the correctionField holding the value turnaround time (Pdelay\_Resp transmit timestamp - Pdelay\_Req receive timestamp). The correction field is updated by hardware, as it is operating in 1-Step Mode.

While preparing the Pdelay\_Resp\_Follow\_Up message, PTP software/stack asks the device driver to return the Pdelay\_Resp transmit timestamp so that it can be put in the Pdelay\_Resp\_Follow\_Up message. In Two-Step Simulation Mode, the device driver returns the Pdelay\_Req receive timestamp instead of the Pdelay\_Resp transmit timestamp. In effect, correctionField of Pdelay\_Resp\_Follow\_Up will be zero because the timestamps in Pdelay\_Resp and Pdelay\_Resp\_Follow\_Up cancel each other, so only the correctionField in Pdelay\_Resp is used in slave peer delay calculation.

Some PTP stacks may take shortcuts and do not implement the timestamp calculation completely. These stacks may assume the correctionField is empty in 2-Step Pdelay\_Resp and do not use it in the calculation.

### PLAN

This erratum will not be corrected in a future revision.

## Module 18: IBA Must Be Disabled When Using I<sup>2</sup>C

### DESCRIPTION

When using I<sup>2</sup>C for device management, it may not function correctly if In-Band Management (IBA) is enabled. In particular, problems can occur when accessing PHY registers.

### END USER IMPLICATIONS

If IBA is enabled while using I<sup>2</sup>C to access PHY registers, reads and writes may not occur correctly, and the I<sup>2</sup>C may become non-functional. If this occurs, the chip may need to be reset. This problem can be avoided by following the work-around. It is possible to alternate between IBA and I<sup>2</sup>C, but IBA must be disabled whenever I<sup>2</sup>C is in use.

### Work Around

There is a pin configuration strap option to enable / disable IBA. Do not strap it high (enabled) unless IBA will actually be used.

IBA can also be enabled / disabled via the In-Band Management (IBA) Control Register (address 0x0104 - 0x0107). This register bit indicates the status of the configuration strap, and is used to override it.

The best advice is to enable IBA only if it is being used. Otherwise leave it disabled. Make sure it is disabled if I<sup>2</sup>C is in use.

### PLAN

This erratum will not be corrected in a future revision.

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## Module 19: Transmission halt with Half-Duplex and VLAN

### DESCRIPTION

A port can stop transmitting if it is operating in half-duplex mode and 802.1Q VLAN is enabled. The half-duplex link can be either 10BASE-T or 100BASE-TX. Note that 1000BASE-T is always full-duplex.

Depending on the traffic at the time of lockup, the problem may only show itself as blocked transmission on that port, or it may cause all packet forwarding through the switch to be blocked. Depending on packet size and traffic rate in each direction, the time for the problem to occur is variable. It may take occur after a few seconds, or it may occur only after hours or days of operation.

The problem has not been observed with full-duplex connections, nor when 802.1Q VLAN is disabled (see Switch Lookup Engine Control 0 Register (address 0x0310)).

Transmission of flow control (Pause) packets is not affected by this issue.

### END USER IMPLICATIONS

When a port stops transmitting due to this issue, it remains stopped until the switch is reset. It causes traffic to back up within the switch, which consumes resources both within the transmit queue for that port, and in the main switch packet memory. If transmit queue resources are exhausted first, then the only impact of the problem is that traffic does not egress the effected port, and packets are forwarded normally to other ports. However, if the switch packet memory resources are exhausted first, then the switch will no longer forward packets between any ports, and all subsequent packets received by the switch will be dropped.

forwarding of packets to other ports may or may not be affected.

There is no direct indication that the issue has occurred. It can only be detected indirectly.

#### Work Around

**Avoidance:** As described above, this problem can be avoided by not using 802.1Q VLAN on a half-duplex port.

**Detection:** There is no interrupt or status bit which will indicate that the problem has occurred. The problem can be detected by monitoring the following MIB Counters which are available for each port:

- RxDropPackets
- TxDropPackets

In normal operation, both counters should always be zero for each port. If the problem occurs and the transmit queue of the blocked port is exhausted before the main packet memory, then the TxDropPackets counter will increase for the blocked port as packets continue to be forwarded to that port but cannot be transmitted. The TxDropPackets counters will remain zero for all other ports. The RxDropPackets counters will remain zero for all ports.

If the problem occurs and the main packet memory is exhausted before the transmit queue of the blocked port, then the RxDropPackets counters will increment for all ports that are receiving traffic. The TxDropPackets counters will remain zero for all ports.

The TxUnicastPkts counter can also be monitored for all ports that may be subject to this issue. The counter will stop incrementing when the problem occurs. However, it will continue to increment if the port is generating flow control (Pause) packets.

The problem may also be detected by monitoring the following resource utilization registers:

- Packet Memory Available Block Count (PMAVBC) in bits [26:16] of global register 0x03AC-0x03Ax
- TX Queue Blocks Used Count (TXQBU) in bits [10:0] of port registers 0xNA10-0xNA13

When the switch is idle, PMAVBC = 0x7e8 and TXQBU = 0.

With normal traffic, these values do not change substantially. PMAVBC will normally be > 0x580, and each TXQBU will be < 0x200. When the problem occurs, these counters will be outside of these limits, and they will remain fixed until the problem is cleared. TXQBU remains within the normal range for ports not directly experiencing lockup.

For example, when the problem occurs and the transmit queue of the blocked port is exhausted before the main packet memory, the following values have occurred: PMAVBC = 0x5e4, TXQBU = 0x204 on the blocked port, and TXQBU = 0 on all other ports.



When the problem occurs and the main packet memory is exhausted before the transmit queue of the blocked port, the following values have occurred: PMAVBC = 0x0060, TXQBU = 0x0788 on the blocked port, and TXQBU = 0 on all other ports.

Clearing the problem: The issue can be cleared either by strobing the RESET\_N pin, or by setting and then clearing the Global Software Reset bit in the Global Chip ID 3 Register (address 0x0003). Note that while the Global Software Reset bit does not clear many registers, it does clear the VLAN Table and the Port Default Tag 0 and 1 registers (addresses 0xN000 and 0xN001).

## PLAN

This erratum will not be corrected in a future revision.

## **Module 20: Frame Length Field Check feature does not work well when the actual frame length is less than 64 bytes**

### DESCRIPTION

The Frame Length Field Check feature will discard any received frame if the actual length does not match the value in the frame length field in the header. Because this test is applied even when the length field value is less than the minimum legal packet length, some legal minimum size packets may get dropped.

### END USER IMPLICATIONS

Some frames, such as Spanning Tree Protocol frames, start out very small - for example 0x26 or 0x27 bytes. This length value is inserted into the frame length field of the header when the frame is created. Before it is transmitted, the network driver or MAC will pad it up to the minimum IEEE frame size. However, the frame length field is typically not updated to match.

Because the Frame Length Field Check does not make an exception for the case of small values in the frame length field, it drops these packets, even though they are valid.

### **Work Around**

Do not enable the Frame Length Field Check feature, found in the Switch MAC Control 0 Register.

## PLAN

This erratum will not be corrected in a future revision.

## APPENDIX A: DOCUMENT REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS80000752D (09-22-22)	<a href="#">Silicon Errata Issues</a>	Added note regarding configuration of PHY MMD registers.
	<a href="#">Module 1</a>	Added the following text to Work Around description: "Before writing the PHY MMD registers, it is necessary to set the PHY to 100 Mbps speed with auto-negotiation disabled by writing to register 0xN100-0xN101. After writing the MMD registers, and after all errata workarounds that involve PHY register settings, write register 0xN100-0xN101 again to enable and restart auto-negotiation. See details in the note above."
	<a href="#">Note 1</a>	Updated Module 1's final data address from "0x2001" to "0x2000". Also added note regarding this change.
	<a href="#">Module 3</a>	Updated title of section from "Default RGMII ingress timing does not comply with the RGMII specification" to "Port 6 Default RGMII ingress timing does not comply with the RGMII specification".
	<a href="#">Module 4</a>	Entire Module section rewritten for clarity.
	<a href="#">Module 6</a>	Added 4 additional addresses to Work Around section: 0xN130 - 0xN133 0xN134 - 0xN137 0xN138 - 0xN13B 0xN13C - 0xN13F
	<a href="#">Module 15</a>	Text for Method 2 has been updated from "To detect transmitter lock up, the software should monitor the TxByteCnt (MIB Index 0x81) and the RxByteCnt (MIB Index 0x80). If the RxByteCnt is incrementing but the TxByteCnt remains the same, the software should perform a hard reset of the switch" to "To detect transmitter lockup, see the work around section of Module x: Transmission halt with Half-Duplex and VLAN."
	<a href="#">Module 16</a>	Entire Module section rewritten for updated solution.
	<a href="#">Module 18</a>	New Module for I2C usage.
	<a href="#">Module 19</a>	New Module for Half-Duplex and VLAN interaction.
	<a href="#">Module 20</a>	New Module for Frame Length Check feature.
DS80000752C (08-23-18)	<a href="#">Module 15.</a> , <a href="#">Module 16.</a> , <a href="#">Module 17.</a>	Added new errata for " <a href="#">Transmission halt with late collisions</a> ", " <a href="#">Single-LED Mode Setting Requires Two Register Writes</a> ", and " <a href="#">PTP messages get dropped in PTP 2-Step Mode</a> "
DS80000752B (04-15-18)	<a href="#">Module 12.</a> , <a href="#">Module 13.</a> , <a href="#">Module 14.</a>	Added new errata for " <a href="#">When tail tag is enabled, frame length field check fails for 802.3 frames</a> ", " <a href="#">Port based priority remapping is not supported</a> " and " <a href="#">Occasional high current on AVDDL supply pins during hardware reset</a> ". Removed "Frame Length Field Check mode is disabled" errata, which is superseded by the <a href="#">Module 12</a> .
DS80000752A (08-10-17)	All	Initial release.

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