PXI-4495 Feature Usage

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Contents

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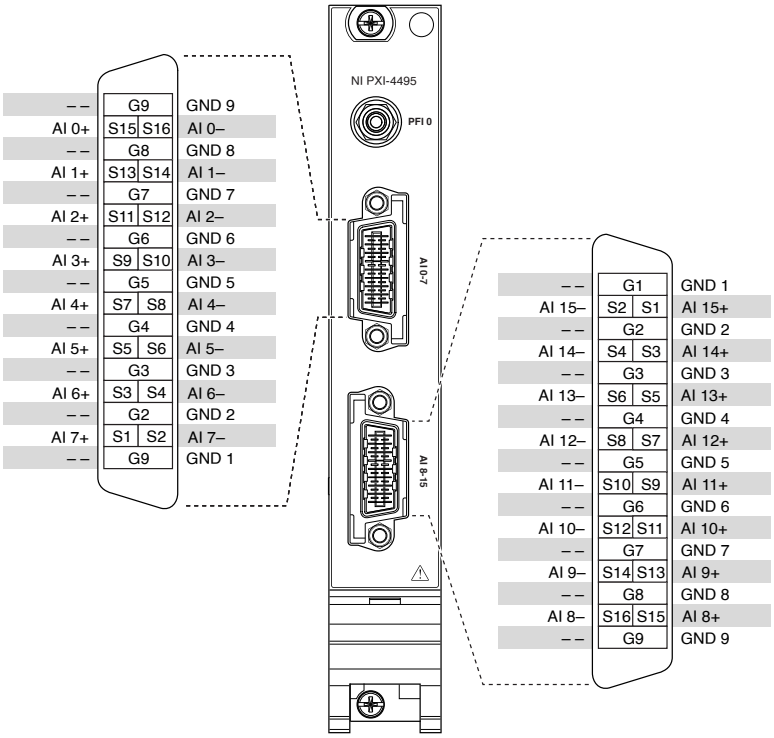
204.8 kS/s, 114 dB, 2 Gains, 0.5 Hz DC-Coupled, 16-Input PXI Sound and Vibration Module

- 2 gain settings up to +20 dB for input ranges from ±1 V to 10 V
- 24-bit resolution for good signal to noise ratio on AI channels
- Software-selectable IEPE signal conditioning (0 or 4 mA)

PXI-4495 Pinout



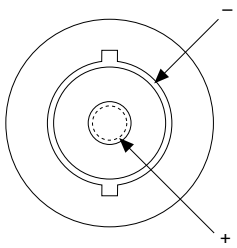
The PXI-4495 features InfiniBand 4x connectors.

Caution Connecting a signal that varies more than ±5 V from the PXI-4495 ground reference to the ground (shield) of any input channel can

result in damage to the device. NI is not responsible for damage caused by such connections.

You can use a BNC-2144 or an Infiniband 4x to 8 BNC cable assembly to create BNC connectors from the PXI-4495. The following figure shows the PFI connector polarity.

Figure 1. BNC Connector Polarity



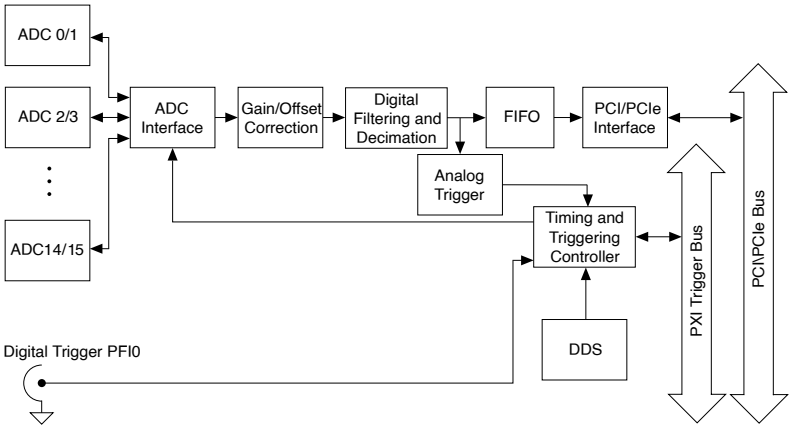
Signal	Reference	Description
AI <0..15>+, AI <0..15>-	—	Analog Input Channel—AI+ and AI- are the positive and negative inputs of the pseudodifferential analog channel.
PFI 0	GND	Programmable Function Interface—A digital trigger input.
GND	—	Ground—Ground terminal.

Table 1. Signal Descriptions

Block Diagram

The following figure shows the PXI-4495 block diagram.

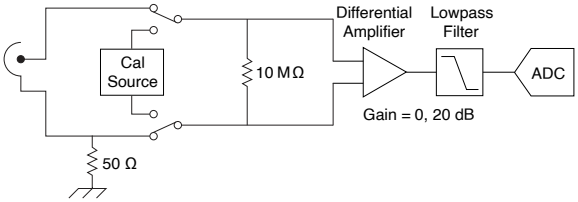
Figure 2. PXI-4495 Block Diagram



Analog Input Features

The following figure shows the PXI-4495 analog input circuitry block diagram.

Figure 3. Analog Input Block Diagram



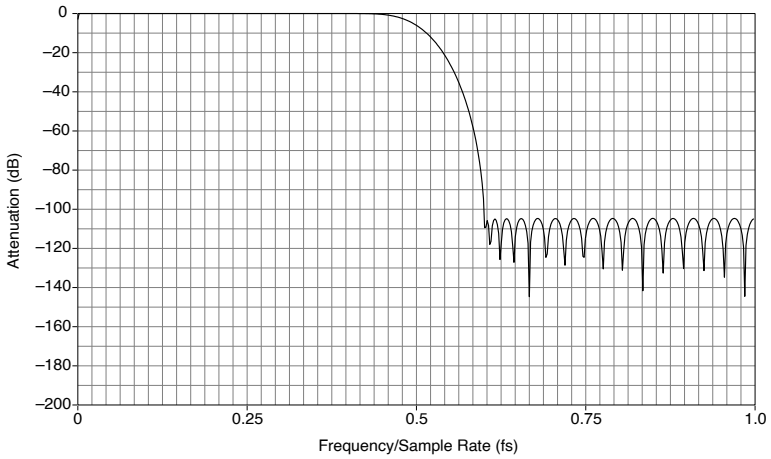
The PXI-4495 analog input channels feature the following:

- Sampling rates up to 204.8 kS/s
- Per channel selection of gain
- Multiple triggering modes, including external digital triggering
- Per channel digital overload detection
- Hardware data packing

Anti-Aliasing Filter Response

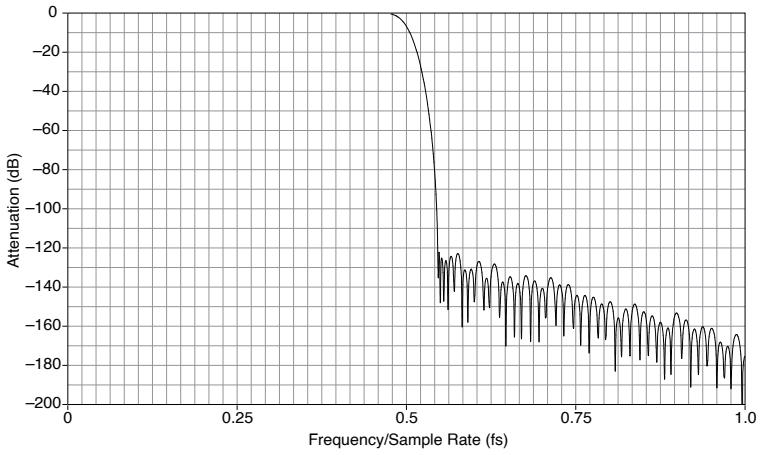
The following figure shows the digital filter input frequency response with low-frequency alias rejection enabled.

Figure 4. Digital Filter Input Frequency Response with Low-Frequency Alias Rejection Enabled



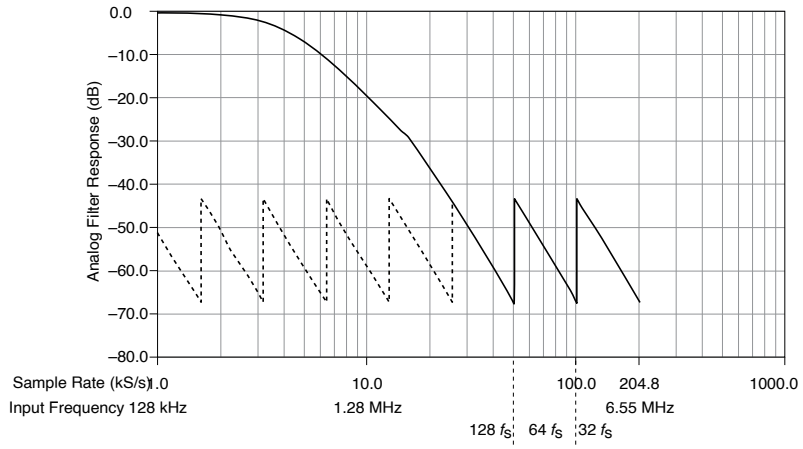
The following figure shows the digital filter input frequency response with low-frequency alias rejection disabled.

Figure 5. Digital Filter Input Frequency Response with Low-Frequency Alias Rejection Disabled



The following figure shows the response of the analog anti-aliasing filter with and without enhanced low-frequency alias rejection enabled. The figure illustrates the alias rejection for a tone that passes the digital filter by falling into one of the $\mathbf{f_S}$-wide bands centered on the oversample rate. The first set of x-axis labels denotes the PXI-4495 sample rate in kS/s. The second set of x-axis labels shows the frequency of an input signal that could pass through the digital filter at the given sampling rate. Refer to the **ADC Modulator Oversample Rate** in the specifications for your device or module for more information.

Figure 6. Analog Filter Input Frequency Response



For example, when sampling at 10 kS/s, the digital filter will remove any out-of-bandwidth tones up to a 10 kHz band centered on 128 $\mathbf{f_S}$, or 1.28 MHz±5 kHz. If noise in the input signal falls into this narrow window, the noise is not rejected by the digital filter. In this limited frequency range, you must consider the analog filter. The following figure illustrates that with a sampling rate of 10 kS/s, the analog filter attenuates an input signal frequency of 1.28 MHz by -20 dB without enhanced low-frequency alias rejection enabled. With enhanced low-frequency alias rejection enabled, the attenuation would be -59 dB.

The sawtooth line in the figure represents the filter response with low-frequency alias rejection enabled. The worst-case alias rejection is approximately -44 dB. This corresponds to the analog filter attenuation at 25.6 kS/s.

This situation represents the worst-case alias rejections for each sampling rate. You would only observe this worst-case scenario with a well-defined tone in a narrow frequency range. In real measurement situations, it is more likely that any energy passing the digital filter consists only of low-amplitude noise. If an unwanted component does appear in the digitized signal, increasing the sampling rate might provide an easy solution by both improving the rejection from the analog filter and by repositioning the digital filter so that it can eliminate the alias.

Reference Clock Synchronization

The PXI-4495 employs onboard PLL circuitry. The PLL circuitry locks the onboard 100 MHz voltage-controlled crystal oscillator (VCXO) to the PXI/PXIe 10 MHz reference clock signal, PXI_CLK10. The VCXO output provides the source for the DDS chip, which generates the sample clock timebase. In this way the PXI-4495 locks the sample clock timebase to PXI_CLK10.