

Video/Audio Interfaces for TV and DVD Recorders

PAL Video I/O Interface BH7624KS2



●Description

BH7624KS2 is a PAL video signal input switch for DVD-Recorder applications. It supports I²C-BUS, 75Ω driver, PAL control functions with fast blinking, I/O BUS port, and the control for BD3825FS audio signal system switch. A built-in scart terminal is incorporated.

●Features

- 1) Vcc 5V Single
- 2) I²C-BUS control (Input switch to high impedance at power-off)
- 3) BD3825FS control function built-in
- 4) Built-in three parallel bus control terminal
- 5) Standby mode
- 6) CVBS/Y 5 inputs, 5 Bottom Clamp circuits, with Mute function
 - 1 output 0/2dB AMP + Buffer
 - 2 outputs 6/8dB AMP + 75Ω driver
 - 1 output 0/6dB AMP + Buffer (for VPS, PDC)
- 7) Chroma 2 inputs, 2 BIAS circuits, with Mute function
 - 2 outputs 6/8dB AMP + 75Ω driver control
 - 3 outputs Buffer + 8 order LPF (Record)
- 8) Each SW independent actuation and all the SW simultaneous actuation are possible for the mute circuit,
- 9) Playback order LPF 6 circuits built-in
- 10) Record 8 order LPF 3 circuits built-in
- 11) Fast blanking circuit built-in
- 12) Function SW Input, 2 circuit built-in
- 13) Crosstalk -60dB Typ.
- 14) DG/DP 0.5%/0.5deg Typ.

●Applications

DVD-Recorder, STB, etc.

●Absolute maximum ratings (Ta=25°C)

Parameter	Symbol	Limits	Unit
Power supply voltage	V	7.0	V
Power dissipation	Pd	1300 *1	mW
Operating temperature range	Topr	-25 ~ +65	°C
Storage temperature range	Tstg	-55 ~ +125	°C

*1 Reduced by 13 mW/°C over 25°C.

●Operating range (Ta=25°C)

Parameter	Symbol	Limits	Unit
Supply voltage	Vcc1, Vcc2, VDD	4.75 ~ 5.25	V

● **Electrical characteristics** (Unless otherwise specified, Vcc1, Vcc2, VDD=5V, Ta=25°C)

Item	Symbol	Limit			Unit	Conditions
		MIN.	TYP.	MAX.		
<Whole>						
VCC Circuit current	I _{CC}	85	130	175	mA	Load 75Ω Resistor
VDD Circuit current	I _{DD}	4.6	7.2	9.8	mA	
VCC Circuit current at standby	I _{CCST}	10	15	20	mA	Load 75Ω Resistor
VDD Circuit current at standby	I _{DDST}	3.5	5.5	7.5	mA	
<SW part>						
L1,AUX CVBS/Y → For VPS,PDC 0dB Voltage gain	G _{VPS0}	-0.7	-0.2	0.3	dB	Vin=1Vpp , f=100kHz
L1,AUX CVBS/Y → For VPS,PDC 6dB Voltage gain	G _{VPS6}	5.7	6.2	6.7	dB	Vin=1Vpp , f=100kHz
ENC CVBS,ENC Y → to INPUT AD 0dB Voltage gain	G _{AD0}	-0.8	-0.3	0.2	dB	Vin=1Vpp , f=100kHz
ENC CVBS,ENC Y → to INPUT AD 2dB Voltage gain	G _{AD2}	1.4	1.9	2.4	dB	Vin=800mVpp , f=100kHz
ENC CVBS,ENC Y → to L1&AUX 6dB Voltage gain	G _{L1AUX6}	5.5	6.0	6.5	dB	Vin=1Vpp , f=100kHz
ENC CVBS,ENC Y → to L1&AUX 8dB Voltage gain	G _{L1AUX8}	7.7	8.2	8.7	dB	Vin=800mVpp , f=100kHz
L1 C →to AUX 6dB Voltage gain	G _{AUX6-1}	5.7	6.2	6.7	dB	Vin=450mVpp , f=100kHz
ENC C →to AUX 6dB Voltage gain	G _{AUX6-2}	5.5	6.0	6.5	dB	Vin=450mVpp , f=100kHz
ENC C →to AUX 8dB Voltage gain	G _{AUX8}	7.7	8.2	8.7	dB	Vin=360mVpp , f=100kHz
ENC C →to L1 6dB Voltage gain	G _{L16-1}	5.5	6.0	6.5	dB	Vin=450mVpp , f=100kHz
ENC C →to L1 8dB Voltage gain	G _{L18-1}	7.7	8.2	8.7	dB	Vin=360mVpp , f=100kHz
ENC R,G,B →to L1 6dB Voltage gain	G _{L16-2}	5.5	6.0	6.5	dB	Vin=450mVpp , f=100kHz
ENC R,G,B →to L1 8dB Voltage gain	G _{L18-2}	7.7	8.2	8.7	dB	Vin=360mVpp , f=100kHz
AUX R,G,B →to L1 Voltage gain	G _{L16-3}	5.7	6.2	6.7	dB	Vin=700mV , f=100kHz
AUX R,G,B →to R,G,B Voltage gain (LPF OFF)	G _{RGB0-1}	-0.6	-0.1	0.4	dB	Vin=560mV , f=100kHz
AUX R,G,B →to R,G,B Voltage gain (LPF ON)	G _{RGB0-2}	-0.8	-0.3	0.2	dB	Vin=560mV , f=100kHz
Difference voltage gain Between the channel	ΔG	-0.5	0.0	0.5	dB	Vin=1.0Vpp,f=100kHz
CVBS/Y OUT to INPUT AD Maximum output level 0dB	V _{AD0}	2.8	3.2	—	Vp-p	Vin: THD=1.0% f=100kHz
CVBS/Y OUT to INPUT AD Maximum output level 2dB	V _{AD2}	2.8	3.2	—	Vp-p	Vin: THD=1.0% f=100kHz
CVBS/Y OUT to L1 Maximum output level 6dB	V _{CV-L6}	2.8	3.2	—	Vp-p	Vin: THD=1.0% f=100kHz
CVBS/Y OUT to L1 Maximum output level 8dB	V _{CV-L8}	2.8	3.2	—	Vp-p	Vin: THD=1.0% f=100kHz
CVBS/Y OUT to AUX Maximum output level 6dB	V _{CV-A6}	2.8	3.2	—	Vp-p	Vin: THD=1.0% f=100kHz
CVBS/Y OUT to AUX Maximum output level 8dB	V _{CV-A8}	2.8	3.2	—	Vp-p	Vin: THD=1.0% f=100kHz
C OUT to AUX Maximum output level 6dB	V _{C-A6}	2.8	3.2	—	Vp-p	Vin: THD=1.0% f=100kHz
C OUT to AUX Maximum output level 8dB	V _{C-A8}	2.8	3.2	—	Vp-p	Vin: THD=1.0% f=100kHz

Item	Symbol	Limit			Unit	Conditions
		MIN.	TYP.	MAX.		
R/C OUT to L1 Maximum output level 6dB	V _{RC-L6}	2.8	3.2	—	Vp-p	Vin: THD=1.0% f=100kHz
R/C OUT to L1 Maximum output level 8dB	V _{RC-L8}	2.8	3.2	—	Vp-p	Vin: THD=1.0% f=100kHz
G OUT to L1 Maximum output level 6dB	V _{G-L6}	2.8	3.2	—	Vp-p	Vin: THD=1.0% f=100kHz
G OUT to L1 Maximum output level 8dB	V _{G-L8}	2.8	3.2	—	Vp-p	Vin: THD=1.0% f=100kHz
B OUT to L1 Maximum output level 6dB	V _{B-L6}	2.8	3.2	—	Vp-p	Vin: THD=1.0% f=100kHz
B OUT to L1 Maximum output level 8dB	V _{B-L8}	2.8	3.2	—	Vp-p	Vin: THD=1.0% f=100kHz
R Maximum output level	V _R	2.8	3.2	—	Vp-p	Vin: THD=1.0% f=100kHz
G Maximum output level	V _G	2.8	3.2	—	V	Vin: THD=1.0% f=100kHz
B Maximum output level	V _B	2.8	3.2	—	V	Vin: THD=1.0% f=100kHz
For VPS, PDC Maximum output level 0dB	V _{VPS0}	2.8	3.2	—	V	Vin: THD=1.0% f=100kHz
For VPS, PDC Maximum output level 6dB	V _{VPS6}	2.8	3.2	—	V	Vin: THD=1.0% f=100kHz
CVBS/Y OUT to INPUT AD Frequency characteristic 0dB	F _{AD0}	-1.0	0	1.0	dB	Vin=1Vpp , f=100k/7MHz
CVBS/Y OUT to INPUT AD Frequency characteristic 2dB	F _{AD2}	-1.0	0	1.0	dB	Vin=800mVpp , f=100k/7MHz
CVBS/Y OUT to L1 Frequency characteristic 6dB	F _{CV-L6}	-1.0	0	1.0	dB	Vin=1Vpp , f=100k/7MHz
CVBS/Y OUT to L1 Frequency characteristic 8dB	F _{CV-L8}	-1.0	0	1.0	dB	Vin=800mVpp , f=100k/7MHz
CVBS/Y OUT to AUX Frequency characteristic 6dB	F _{CV-AU6}	-1.0	0	1.0	dB	Vin=1Vpp , f=100k/7MHz
CVBS/Y OUT to AUX Frequency characteristic 8dB	F _{CV-AU8}	-1.0	0	1.0	dB	Vin=800mVpp , f=100k/7MHz
C OUT to AUX Frequency characteristic 6dB	F _{C-A6}	-1.0	0	1.0	dB	Vin=450mVpp , f=100k/7MHz
C OUT to AUX Frequency characteristic 8dB	F _{C-A8}	-1.0	0	1.0	dB	Vin=360mVpp , f=100k/7MHz
R/C OUT to L1 Frequency characteristic 6dB	F _{RC-L6}	-1.0	0	1.0	dB	Vin=700mVpp , f=100k/7MHz
R/C OUT to L1 Frequency characteristic 8dB	F _{RC-L8}	-1.0	0	1.0	dB	Vin=560mVpp , f=100k/7MHz
G OUT to L1 Frequency characteristic 6dB	F _{G-L6}	-1.0	0	1.0	dB	Vin=700mVpp , f=100k/7MHz
G OUT to L1 Frequency characteristic 8dB	F _{G-L8}	-1.0	0	1.0	dB	Vin=560mVpp , f=100k/7MHz
B OUT to L1 Frequency characteristic 6dB	F _{B-L6}	-1.0	0	1.0	dB	Vin=700mVpp , f=100k/7MHz
B OUT to L1 Frequency characteristic 8dB	F _{B-L8}	-1.0	0	1.0	dB	Vin=560mVpp , f=100k/7MHz
R Frequency characteristic	F _R	-1.0	0	1.0	dB	Vin=700mVpp , f=100k/7MHz
G Frequency characteristic	F _G	-1.0	0	1.0	dB	Vin=700mVpp , f=100k/7MHz
B Frequency characteristic	F _B	-1.0	0	1.0	dB	Vin=700mVpp , f=100k/7MHz
CVBS/Y OUT LPF ON Frequency characteristic 1	F _{CV-LPF1}	-1.5	-0.5	0.5	dB	Vin=1.0Vpp , f=100k/6.75MHz
CVBS/Y OUT LPF ON Frequency characteristic 2	F _{CV-LPF2}	—	-38	-27	dB	Vin=1.0Vpp , f=100kHz/27MHz
C-R/C-G-B OUT LPF ON Frequency characteristic 1	F _{CR-LPF1}	-1.5	-0.5	0.5	dB	Vin=1.0Vpp , f=100k/6.75MHz
C-R/C-G-B OUT LPF ON Frequency characteristic 2	F _{CR-LPF2}	—	-38	-27	dB	Vin=1.0Vpp , f=100kHz/27MHz

Item	Symbol	Limit			Unit	Conditions
		MIN.	TYP.	MAX.		
R-G-B LPF ON Frequency characteristic 1	F _{RGB1}	-3	0	1	dB	V _{in} =700mVpp , f=100kHz/6MHz
R-G-B LPF ON Frequency characteristic 2	F _{RGB2}	—	-15	-1.5	dB	V _{in} =700mVpp , (f=100kHz/14.3MHz)
CVBS/Y OUT to INPUT AD MUTE attenuation	M _{AD}	—	-60	-55	dB	V _{in} =1.0Vpp , f=4.43MHz
CVBS/Y OUT to L1 MUTE attenuation	M _{L1}	—	-60	-55	dB	V _{in} =1.0Vpp , f=4.43MHz
CVBS/Y OUT to AUX MUTE attenuation	M _{AUX}	—	-60	-55	dB	V _{in} =1.0Vpp , f=4.43MHz
C OUT to AUX MUTE attenuation	M _C	—	-60	-55	dB	V _{in} =1.0Vpp , f=4.43MHz
R/C OUT to L1 MUTE attenuation	M _{RC}	—	-60	-55	dB	V _{in} =1.0Vpp , f=4.43MHz
G OUT to L1 MUTE attenuation	M _G	—	-60	-55	dB	V _{in} =1.0Vpp , f=4.43MHz
B OUT to L1 MUTE attenuation	M _B	—	-60	-55	dB	V _{in} =1.0Vpp , f=4.43MHz
SW1 Switch crosstalk	C _{SW1}	—	-60	-55	dB	V _{in} =1.0Vpp , f=4.43MHz AMP0dB
SW2 Switch crosstalk	C _{SW2}	—	-60	-55	dB	V _{in} =1.0Vpp , f=4.43MHz AMP6dB
SW3 Switch crosstalk	C _{SW3}	—	-60	-55	dB	V _{in} =1.0Vpp , f=4.43MHz AMP6dB
SW4 Switch crosstalk	C _{SW4}	—	-60	-55	dB	V _{in} =1.0Vpp , f=4.43MHz AMP6dB
SW5 Switch crosstalk	C _{SW5}	—	-60	-55	dB	V _{in} =1.0Vpp , f=4.43MHz AMP6dB
SW7 Switch crosstalk	C _{SW7}	—	-60	-55	dB	V _{in} =1.0Vpp , f=4.43MHz AMP6dB
SW8 Switch crosstalk	C _{SW8}	—	-60	-55	dB	V _{in} =1.0Vpp , f=4.43MHz AMP6dB
SW10 Switch crosstalk	C _{SW10}	—	-60	-55	dB	V _{in} =1.0Vpp , f=4.43MHz AMP6dB
CVBS/Y OUT Between the channel crosstalk	C _{CVBS}	—	-60	-55	dB	V _{in} =1.0Vpp , f=4.43MHz AMP0,6dB
C-R/C-G-B OUT Between the channel crosstalk	C _{CR/CGB}	—	-60	-55	dB	V _{in} =1.0Vpp , f=4.43MHz AMP6dB
R-G-B Between the channel crosstalk	C _{RGB}	—	-60	-55	dB	V _{in} =1.0Vpp , f=4.43MHz
BIAS input impedance	R _{BIAS}	14	20	26	kΩ	
BIAS input impedance AUX R/C terminal	R _{RC}	100	150	200	kΩ	
<Scart connector part>						
FB threshold	V _{FB}	0.4	0.7	0.9	V	
L1 FB OUT Output voltage H	V _{FB-HI}	3.6	4	4.4	V	R _L =150Ω
L1 FB OUT Output voltage L	V _{FB-LO}	0	—	0.7	V	R _L =150Ω
FSW Output voltage H	V _{FSW-HI}	VCC -0.5	VCC -0.1	VCC	V	No load
FSW Output voltage L	V _{FSW-LOW}	0	—	0.7	V	No load
<ADR>						
Input voltage H	V _{ADR-HI}	2.0	—	VCC	V	
Input voltage L	V _{ADR-LOW}	0	—	1.0	V	
Input impedance	R _{ADR}	65	100	135	kΩ	Pull down resistor

Item	Symbol	Limit			Unit	Conditions
		MIN.	TYP.	MAX.		
<SCL, SDA>						
Input voltage H	$V_{II\text{-}C\text{-}HI}$	2.0	—	VCC	V	
Input voltage L	$V_{II\text{-}C\text{-}LOW}$	0	—	1.0	V	
Input bias current	$V_{II\text{-}C\text{-}BIAS}$	0	-1	-10	μA	
INT Output voltage H	$V_{INT\text{-}HI}$	V_{CC} -0.5	V_{CC} -0.1	V_{CC}	V	Pull up 100k Ω
INT Output voltage L	$V_{INT\text{-}LOW}$	0	0.3	0.5	V	$I_{load}=1\text{mA}$
ALL MUTE threshold	V_{MUTE}	1.0	1.5	2.0	V	The span that input is possible. 0~VCC
FS1, FS2 Input threshold H	$V_{FS\text{-}H}$	2.5	2.75	3	V	Maximum input voltage VCC (VCC \pm 5%)
FS1, FS2 Input threshold L	$V_{FS\text{-}L}$	0.83	1.08	1.33	V	Minimum input voltage 0V (VCC \pm 5%)
PARALLEL 1~4 Output voltage H	V_{OPH}	V_{CC} -0.5	V_{CC} -0.1	V_{CC}	V	Pull up 100k Ω
PARALLEL 1~4 Output voltage L	V_{OPL}	0	0.3	0.5	V	$I_{load}=1\text{mA}$
ASW1~4 Output voltage H	V_{OSH}	3.5	V_{CC} - 0.1	VCC	V	No load
ASW1~4 Output voltage L	V_{OSL}	0	0.1	1.0	V	No load
FSL1, FSAUX Output voltage H	V_{OFSH}	4.0	0.95 $\times V_{CC}$	VCC	V	$R_L=200\text{k}\Omega$
FSL1, FSAUX Output voltage M	V_{OFSM}	2.0	2.5	3.0	V	$R_L=200\text{k}\Omega$
FSL1, FSAUX Output voltage L	V_{OFSL}	0	0.1	0.75	V	$R_L=200\text{k}\Omega$
<Guaranteed design parameters>						
<SW part>						
L1,AUX CVBS/Y → For VPS,PDC 0dB Differential Gain	D_{GVPS0}	-	0.1	-	%	75 Ω terminating. 1Vpp output
L1,AUX CVBS/Y → For VPS,PDC 6dB Differential Gain	D_{GVPS6}	-	0.1	-	%	75 Ω terminating. 1Vpp output
ENC CVBS,ENC Y → to INPUT AD 0dB Differential Gain	D_{GAD0}	-	0.1	-	%	75 Ω terminating. 1Vpp output
ENC CVBS,ENC Y → to INPUT AD 2dB Differential Gain	D_{GAD2}	-	0.1	-	%	75 Ω terminating. 1Vpp output
ENC CVBS,ENC Y → to L1&AUX 6dB Differential Gain	D_{GL1AU6}	-	0.5	-	%	75 Ω terminating. 1Vpp output
ENC CVBS,ENC Y → to L1&AUX 8dB Differential Gain	D_{GL1AU8}	-	0.5	-	%	75 Ω terminating. 1Vpp output
L1C→to AUX 6dB Differential Gain	D_{GLCAUX}	-	1.0	-	%	75 Ω terminating. 1Vpp output
ENC C→to AUX 6dB Differential Gain	$D_{GC\text{-}A6}$	-	1.0	-	%	75 Ω terminating. 1Vpp output
ENC C →to AUX 8dB Differential Gain	$D_{GC\text{-}A8}$	-	1.0	-	%	75 Ω terminating. 1Vpp output
ENC C →to L1 6dB Differential Gain	$D_{GC\text{-}L6}$	-	1.0	-	%	75 Ω terminating. 1Vpp output
ENC C →to L1 8dB Differential Gain	$D_{GC\text{-}L8}$	-	1.0	-	%	75 Ω terminating. 1Vpp output
ENC R,G,B →to L1 6dB Differential Gain	D_{GRGBL6}	-	0.8	-	%	75 Ω terminating. 1Vpp output
ENC R,G,B →to L1 8dB Differential Gain	D_{GRGBL8}	-	0.8	-	%	75 Ω terminating. 1Vpp output
AUX R,G,B →to L1 Differential Gain	$D_{GAUX\text{-}L}$	-	0.2	-	%	75 Ω terminating. 1Vpp output

Item	Symbol	Limit			Unit	Conditions
		MIN.	TYP.	MAX.		
AUX R,G,B → R,G,B Differential Gain	D _{GAURB}	-	0.2	-	%	75Ω terminating. 1Vpp output
L1,AUX CVBS/Y →For VPS,PDC 0dB Differential Phase	D _{PVPS0}	-	0.2	-	deg	75Ω terminating. 1Vpp output
L1,AUX CVBS/Y →For VPS,PDC 6dB Differential Phase	D _{PVPS6}	-	0.2	-	deg	75Ω terminating. 1Vpp output
ENC CVBS,ENC Y →to INPUT AD 6dB Differential Phase	D _{PAD6}	-	0.2	-	deg	75Ω terminating. 1Vpp output
ENC CVBS,ENC Y →to INPUT AD 8dB Differential Phase	D _{PAD8}	-	0.2	-	deg	75Ω terminating. 1Vpp output
ENC CVBS,ENC Y →to L1&AUX 6dB Differential Phase	D _{PL1AU6}	-	0.2	-	deg	75Ω terminating. 1Vpp output
ENC CVBS,ENC Y →to L1&AUX 8dB Differential Phase	D _{PL1AU8}	-	0.2	-	deg	75Ω terminating. 1Vpp output
L1 C →to AUX 6dB Differential Phase	D _{PLCAU6}	-	0.2	-	deg	75Ω terminating. 1Vpp output
ENC C to AUX 6dB Differential Phase	D _{PC-A6}	-	0.4	-	deg	75Ω terminating. 1Vpp output
ENC C →to AUX 8dB Differential Phase	D _{PC-A8}	-	0.4	-	deg	75Ω terminating. 1Vpp output
ENC C →to L1 6dB Differential Phase	D _{PC-L6}	-	0.4	-	deg	75Ω terminating. 1Vpp output
ENC C →to L1 8dB Differential Phase	D _{PC-L8}	-	0.4	-	deg	75Ω terminating. 1Vpp output
ENC R,G,B →to L1 6dB Differential Phase	D _{PRGBL6}	-	0.2	-	deg	75Ω terminating. 1Vpp output
ENC R,G,B →to L1 8dB Differential Phase	D _{PRGBL8}	-	0.2	-	deg	75Ω terminating. 1Vpp output
AUX R,G,B →to L1 Differential Phase	D _{PAUX-L}	-	0.2	-	deg	75Ω terminating. 1Vpp output
AUX R,G,B →to R,G,B Differential Phase	D _{PAURB}	-	0.2	-	deg	75Ω terminating. 1Vpp output
L1,AUX CVBS/Y → For VPS,PDC 0dB S/N ratio	SN _{VPS0}	-	-70	-	dB	Standard 100% white signal
L1,AUX CVBS/Y → For VPS,PDC 6dB S/N ratio	SN _{VPS6}	-	-70	-	dB	Standard 100% white signal
ENC CVBS,ENC Y → to INPUT AD 0dB S/N ratio	SN _{AD0}	-	-70	-	dB	Standard 100% white signal
ENC CVBS,ENC Y → to INPUT AD 2dB S/N ratio	SN _{AD2}	-	-70	-	dB	Standard 100% white signal
ENC CVBS,ENC Y → to L1&AUX 6dB S/N ratio	SN _{L1AU6}	-	-70	-	dB	Standard 100% white signal
ENC CVBS,ENC Y → to L1&AUX 8dB S/N ratio	SN _{L1AU8}	-	-70	-	dB	Standard 100% white signal
L1 C →to AUX 6dB S/N ratio	SN _{LCAU6}	-	-70	-	dB	Standard 100% white signal
ENC C →to AUX 6dB S/N ratio	SN _{C-A6}	-	-70	-	dB	Standard 100% white signal
ENC C →to AUX 8dB S/N ratio	SN _{C-A8}	-	-70	-	dB	Standard 100% white signal
ENC C →to L1 6dB S/N ratio	SN _{C-L6}	-	-70	-	dB	Standard 100% white signal
ENC C →to L1 8dB S/N ratio	SN _{C-L8}	-	-70	-	dB	Standard 100% white signal
ENC R,G,B →to L1 6dB S/N ratio	SN _{RGBL6}	-	-70	-	dB	Standard 100% white signal
ENC R,G,B →to L1 8dB S/N ratio	SN _{RGBL8}	-	-70	-	dB	Standard 100% white signal
AUX R,G,B →to L1 S/N ratio	SN _{AUX-L}	-	-70	-	dB	Standard 100% white signal
AUX R,G,B →to R,G,B S/N ratio	SN _{AURB}	-	-70	-	dB	Standard 100% white signal

● Block diagram

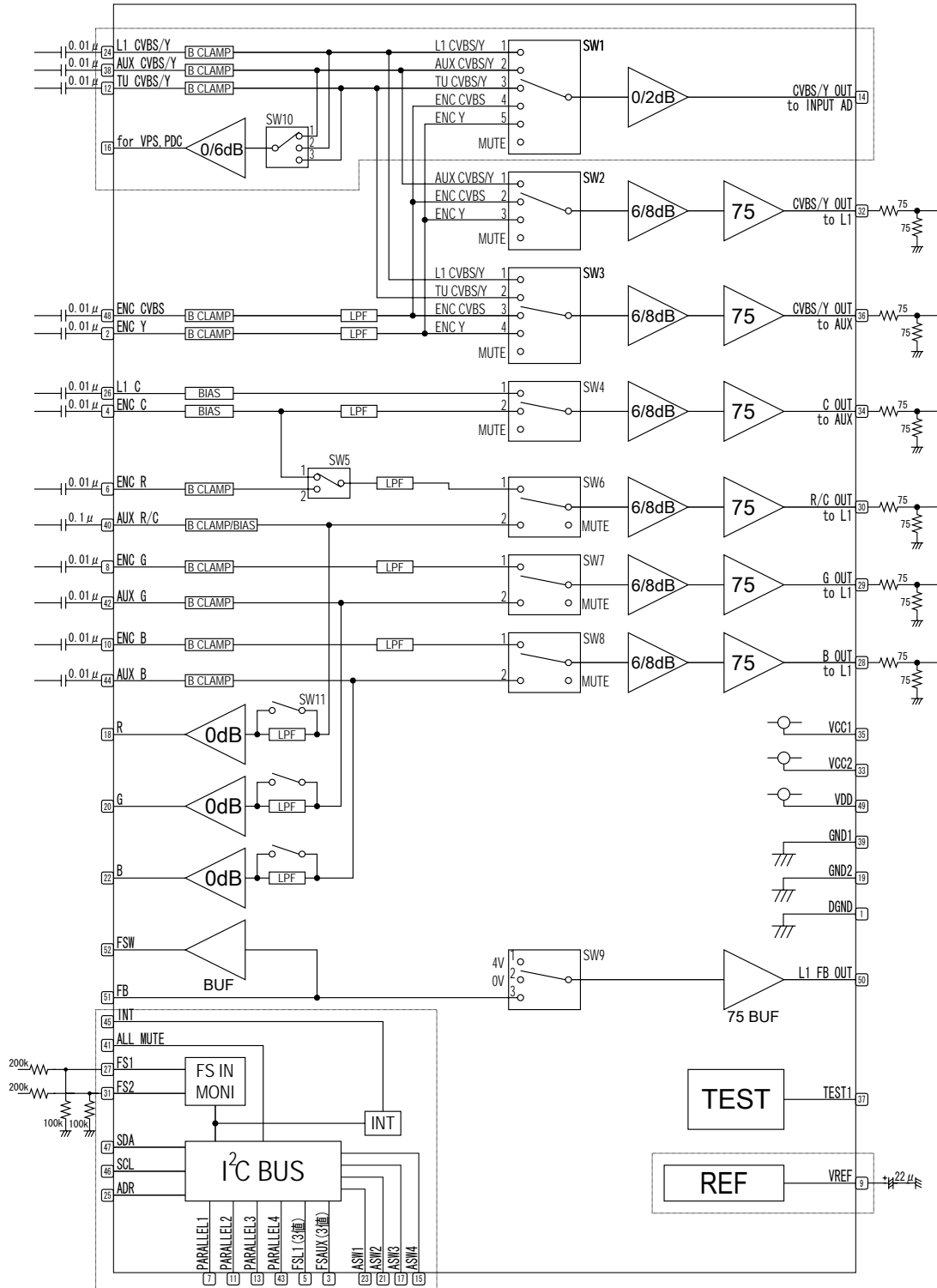
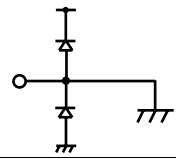
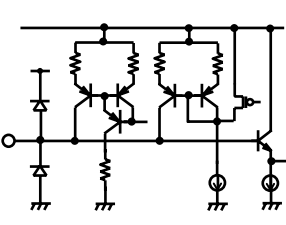
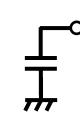
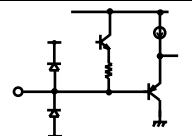
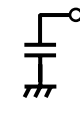
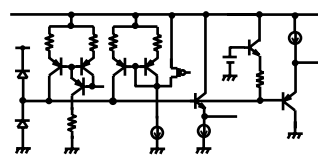
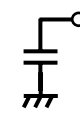
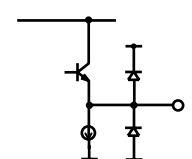
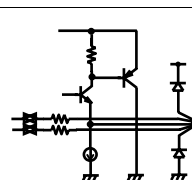
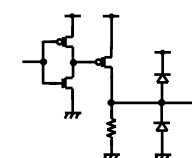
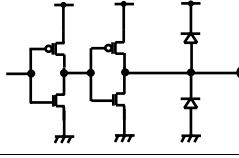
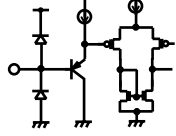

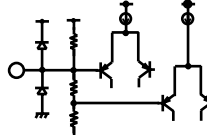

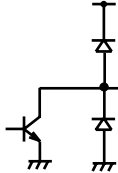

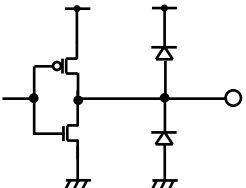
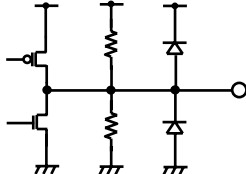
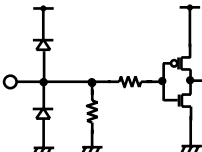

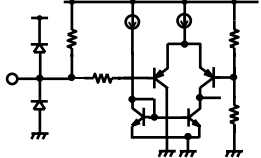

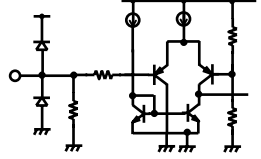

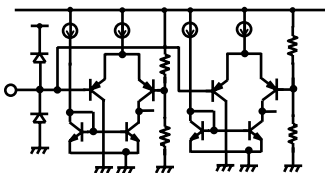

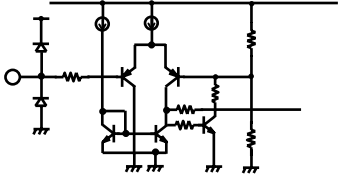

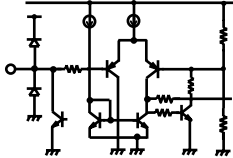

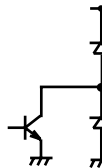



Fig.1
Blocks inside the dotted line operate at a standby mode.

●Equivalent circuit

Pin No. Pin name (Input/Output)	Function	Equivalent circuit	No used	INPUT range (V)
				Terminal voltage (V)
1. DGND 19. GND2 39. GND1	GND terminal		—	0
2. ENCY 6. ENCR 8. ENCG 10. ENCB 12. TV CVBS/Y 24. L1 CVBS/Y 38. AUX CVBS/Y 42. AUX G 44. AUX B 48. L1 C	Signal input terminal The video signal input pins is a bottom clamp.			1.4
4. ENC C 26. L1 C	Signal input terminal The video signal input pins is a resistance bias.			2.9
40. AUX R/C	Signal input terminal AUX R input can be a bottom clamp or resistance bias.			1.4
14. CVBS/Y OUT to INPUT AD for VPS PDC 16. R 18. G 20. G 22. B	S-Video signal input distinction terminal The state of each pin can be read by I ² C-BUS.		—	0.7
28. B OUT to L1 29. G OUT to L1 30. R/C OUT to L1 32. CVBS/Y OUT to AUX 34. C OUT to AUX	Signal output terminal 75Ω driver output pin gain can be selected 6/8dB by I ² C-BUS.		—	0.7 2.1
50. L1 FB OUT	Signal output terminal This pin is an output terminal for scart connector. The drive of 75Ω is possible.		—	—
52. FSW	Signal output terminal The input from FB is outputted as is.		—	—
51. FB	Signal input terminal The signal from scart connector input.			—
9. VREF	Reference voltage terminal A capacitor is connected to opposite GND.			2.8

<p>7. PARALLEL1 11. PARALLEL2 13. PARALLEL3 43. PARALLEL4</p>	<p>Open collector output terminal It can be set up by I²C-BUS.</p>			<p>0</p>
<p>15. ASW4 17. ASW3 21. ASW2 23. ASW1</p>	<p>BD3825FS control terminal The signal which switches SW of BD3825FS is output. It can be set by I²C-BUS.</p>		<p>—</p>	<p>LOW 0 HI 5</p>
<p>3. FS AUX 5. FS L1</p>	<p>FS output terminal Controls the FS output of BD3825FS. It can be set up by I²C-BUS.</p>		<p>—</p>	<p>0</p>
<p>37. TEST1</p>	<p>TEST control terminal Short to GND.</p>			<p>0</p>
<p>41. ALL MUTE</p>	<p>ALL MUTE control terminal It can set all 75Ω driver outputs to mute mode.</p>			<p>5</p>
<p>5. ADR</p>	<p>ADR control terminal Pin to set slave address which is 90H(91H) or 92H(93H).</p>			<p>0</p>
<p>27. FS1 31. FS2</p>	<p>FS monitor terminal It acts as the monitor for the FS change.</p>			<p>—</p>
<p>46. SCL</p>	<p>I²C-BUS Clock input terminal The pin is an input clock of I²C-BUS. It uses a resistor to pull up.</p>			<p>—</p>
<p>47. SDA</p>	<p>I²C-BUS Data input terminal The pin is data of the I²C-BUS. It uses a resistor to pull up.</p>			<p>—</p>
<p>45. INT</p>	<p>INT terminal When INT terminal changes FS pin, it outputs HiZ.</p>			<p>0</p>

●Description of operations

■I²C-BUS Control input specifications

· I²C -BUS Format (WRITE MODE)

S	SLAVE ADDRESS	A	DATA1	A	DATA2	A	DATA3	A	DATA4	A	DATA5	A	DATA6	A	P
---	---------------	---	-------	---	-------	---	-------	---	-------	---	-------	---	-------	---	---

S : Start Condition A : Acknowledge P: Stop Condition

	b7	b6	b5	b4	b3	b2	b1	b0
Slave address	1	0	0	1	0	0	ADR	R/W
DATA1	ADSW			L1SW		YAUXSW		
DATA2	CAUVSW		RSW		GBSW		LASW	
DATA3	CRSW	FBSW		AMP0/6	AMP6/8	FILTERSW	CL/BI SEL	#
DATA4	INT_EN	OUTCTL1	OUTCTL2	Standby	#	#	#	#
DATA5	PARALLEL1	PARALLEL2	PARALLEL3	PARALLEL4	ASW1	ASW2	ASW3	ASW4
DATA6	FSL		FSA		#	#	#	#

(Don't Care) When the power is turned on, the condition is as marked *.

	Explanation		Explanation
ADR	The slave address configured with the ADR terminal (write mode). 0 : When ADR terminal input is L. Address becomes "90H". 1 : When ADR terminal input is H. Address becomes "92H".	YAUXSW	SW3 input select. A signal to output in "CVBS/Y to AUX", select. 000 :L1 CVBS/Y * 001 :TU CVBS/Y 010 : ENC CVBS 011 : ENC Y 1XX : MUTE
R/W	READ/WRITE mode setting 0 : WRITE 1 : READ	CAUXSW	SW4 input select. A signal to output in "C OUT to AUX", select. 00 : L1 C * 01 : ENC C 1X : MUTE
ADSW	SW1 input select. A signal to output in "CVBS/Y to INPUT AD", select. 000 : L1 CVBS/Y 001 : AUX CVBS/Y * 010 : TU CYBS/Y 011 : ENC CVBS 100 : ENC Y 101 : MUTE 110 : MUTE 111 : MUTE	L1SW	SW2 input select. A signal to output in "CVBS/Y to L1", select. 00 : AUX CVBS/Y * 01 : ENC CVBS 10 : ENC Y 11 : MUTE
RSW	SW6 input select. A signal to output in "R/C OUT to L1", select. 00 : ENC C or ENC R 01 : AUX R/C * 1X : MUTE	GBSW	SW7, SW8 input selects. Signals to output in "G OUT to L1" and "B OUT to L1", select. 00 : ENC G、ENC B 01 : AUX G、AUX B * 1X : MUTE
CRSW	A signal to input in RSW (SW5), select. 0 : ENC C * 1 : ENC	FBSW	The output of L1 FB OUT, select. 0X : FB (Through)* 10 : 0V 11 : 4V
AMP0/6	for VPS、PDC terminal AMP gain configuration. 0 : 0dB * 1 : 6dB	CL/BI SEL	The configuration of AUX R/C input mode. 0 : B CLAMP * 1 : BIAS
PARALLEL 1~4	The output configuration of the PARALLEL terminal. 0 : Low * 1 : Hi		

LASW	SW10 input select. A signal to output in “for VPS, PDC”, select. 00 : AUX CVBS/Y * 01 : L1 CVBS/Y 1X : TU CVBS/Y	INT_EN	INT signal output control. 0 : Enable * 1 : Disable Caution: When Enable→Disable change, INT signal is cleared.
AMP6/8	When encoder input is chosen, the gain of AMP is configured. (Encoder input terminal :ENC CVBS, ENC Y, ENC C, ENC R, ENC G, ENC B) 0: 6dB (0dB) * 1: 8dB (2dB) Caution : As for “CVBS/Y OUT to INPUT AD”, it is 0/2 dB switchover.	FILTERSW	SW11 input select. Select the R, G and B each output signal are outputted through the filter, or not outputted through the filter. 0: There is no filter. * 1: There is a filter.
OUTCTL1	“C OUT to AUX” output control. 0 : Normal * 1 : HI Z	OUTCTL2	“B OUT to L1” output control. 0 : Normal * 1 : HI Z
Standby	normal/standby mode configuration. 0 : Normal * 1 : Standby Caution : Block diagram is referred for the actuation block at the time of Standby.	ASW 1~4	The output configuration of the ASW terminal. 0 : Low 1 : Hi (Initial condition) ASW1:H ASW 2:L ASW 3:L ASW 4:H *
FSL	The output configuration of the FSL1. 00 : input mode * 01 : Low 10 : MID 11 : HI Caution : When input mode, the output of BD3825FS becomes HiZ(Low).	FSA	The output configuration of the FSAUX. 00 : input mode * 01 : Low 10 : MID 11 : HI Caution : When input mode, the output of BD3825FS becomes HiZ(Low).

• I²C-BUS format (READ MODE)

S	SLAVE ADDRESS	A	DATA1	A/N	DATA2	A/N	DATA3	A/N	DATA4	A/N	DATA5	A/N	DATA6	A/N	P
---	---------------	---	-------	-----	-------	-----	-------	-----	-------	-----	-------	-----	-------	-----	---

S : Start Condition A/N : NO acknowledge P: Stop Condition

	b7	b6	b5	b4	b3	b2	b1	b0
Slave address	1	0	0	1	0	0	ADR	R/W
DATA1	ADSW			L1SW		YAUXSW		
DATA2	CAUVSW		RSW		GBSW		LASW	
DATA3	CRSW	FBSW		AMP0/6	AMP6/8	FILTERSW	CL/BI SEL	HI
DATA4	INT_EN	OUTCTL1	OUTCTL2	Standby	HI	HI	HI	HI
DATA5	PARALLEL1	PARALLEL2	PARALLEL3	PARALLEL4	ASW1	ASW2	ASW3	ASW4
DATA6	FSL		FSA		FS1		FS2	

(Don't Care)

In the read mode, 00h is output from DATA4 after power-on is reset to 09h. If a write movement occurs once, it is set to normal mode.

	Explanation		Explanation
ADR	The slave address configured with the ADR terminal. (read mode) 0 : When ADR terminal input is L. Address becomes "91H". 1 : When ADR terminal input is H. Address becomes "93H".	R/W	READ/WRITE mode setting 0 : WRITE 1 : READ
FS1	The state of FS1 is outputted. 00 : Low 10 : MID 11 : HI	FS2	The state of FS2 is outputted. 00 : Low 10 : MID 11 : HI

■ INT signal (45pin)

- An INT signal outputs HI (high impedance) when the state of FS1, FS2 is monitored by I²C-BUS for transition stage, during input mode configuration.

Mode		Monitor
FS1	FS2	
Input mode	Input mode	Both
Input mode	Others	Only FS1
Others	Input mode	Only FS2
Others	Others	No monitoring

- INT signal clearance occurs every time the read (read mode) of the data with I²C-BUS when slave address is sent.

○ INT signal output control

It can be controlled with I²C-BUS. INT signal is cleared at switching by Enable→Disable.

■ Standby mode

- Standby mode can be configured by I²C-BUS. Only the section marked in the dotted line, in the Figure 3, Block Diagram, is active during standby state. All others are off.

■ ALL MUTE

- CVBS/Y, C, R/C, G, B output (14pin, 29pin, 30pin, 31pin, 32pin, 34pin, 36pin) are all muted. Mute controls each output separately by I²C-BUS.

ALL MUTE	Mode
H	Normal
L	Mute

■ The bias of an AUX R/C

As for CLAMP/BIAS change of AUX R/C (40pin), the output bias of R/C OUT to L1 (30pin) is synchronized. Setup "CL/BI SEL" by the I²C-BUS control, in accordance with the bias method of the input chosen when input from ENC C (4pin) and ENC R (6pin) is output.

● Reference data

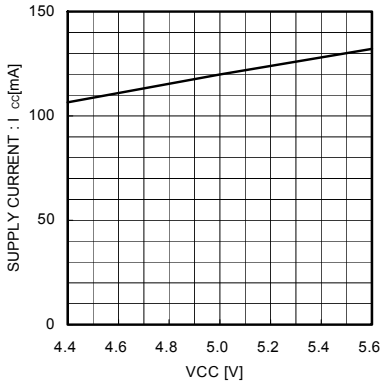


Fig.2 VCC Circuit Current (Supply voltage dependence)

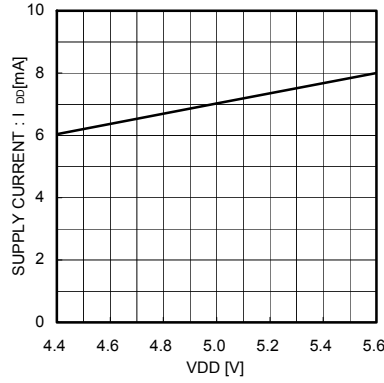


Fig.3 VDD Circuit Current (Supply voltage dependence)

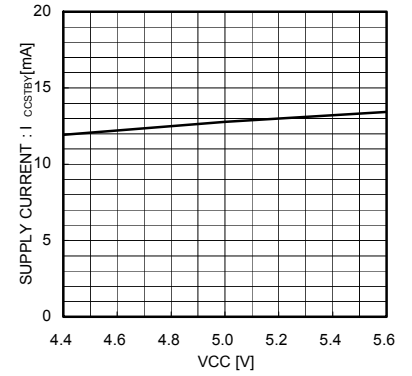


Fig.4 VCC Circuit Current (Standby) (Supply voltage dependence)

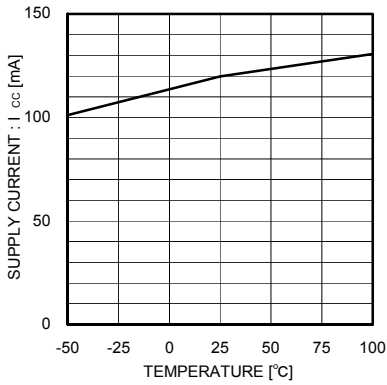


Fig.5 VCC Circuit Current (Temperature dependence)

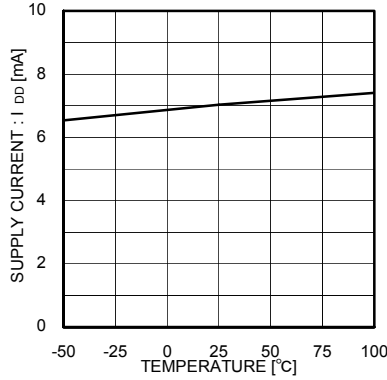


Fig.6 VDD Circuit Current (Temperature dependence)

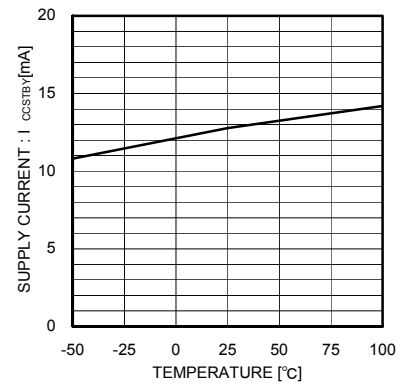


Fig.7 VCC Circuit Current (Standby) (Temperature dependence)

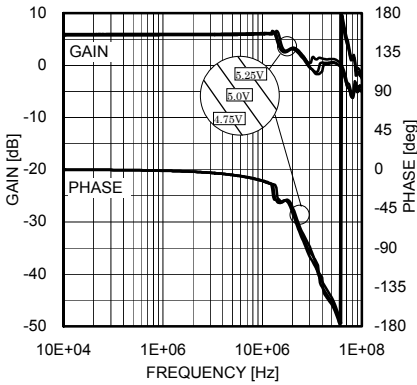


Fig.8 Frequency Characteristics CVBS/Y OUT to L1

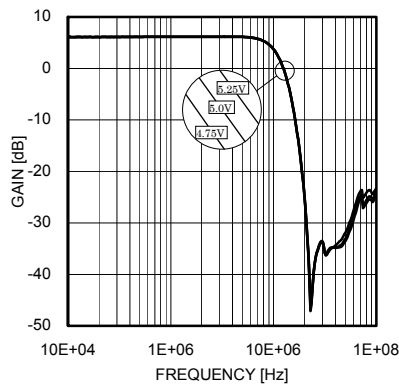


Fig.9 Frequency Characteristics CVBS/Y OUT to L1 (with LPF)

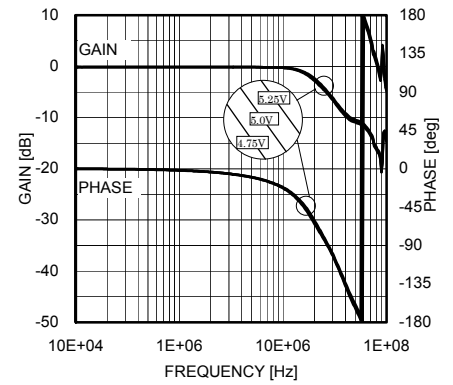


Fig.10 Frequency Characteristics G

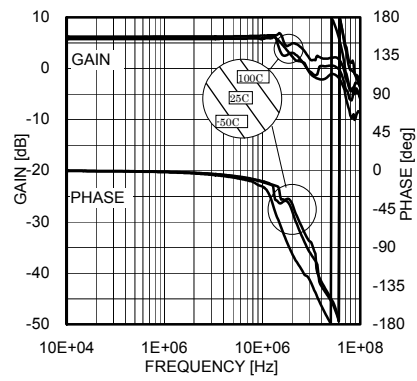


Fig.11 Frequency Characteristics CVBS/Y OUT to L1

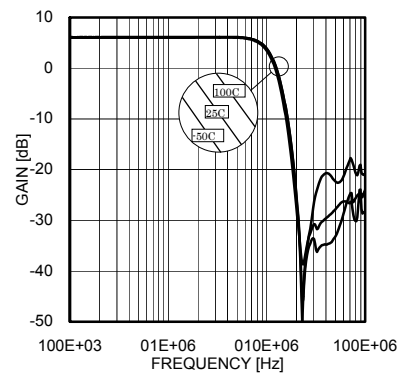


Fig.12 Frequency Characteristics CVBS/Y OUT to L1 (with LPF)

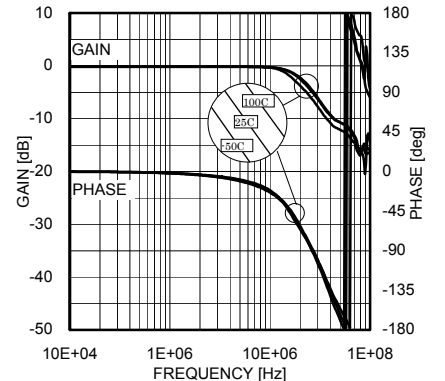


Fig.13 Frequency Characteristics G

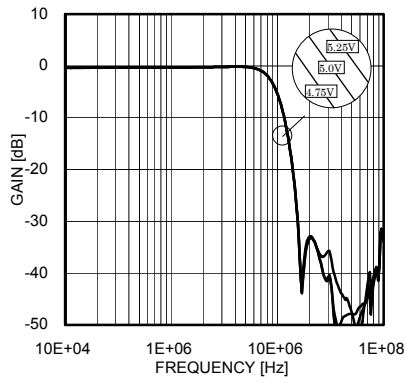


Fig.14 Frequency Characteristics G (with LPF)

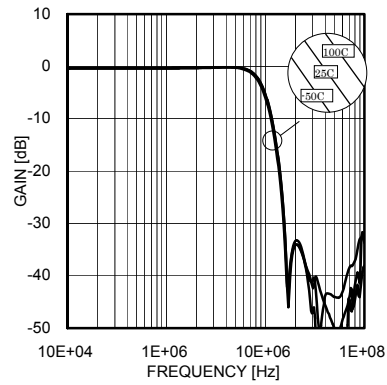


Fig.15 Frequency Characteristics G (with LPF)

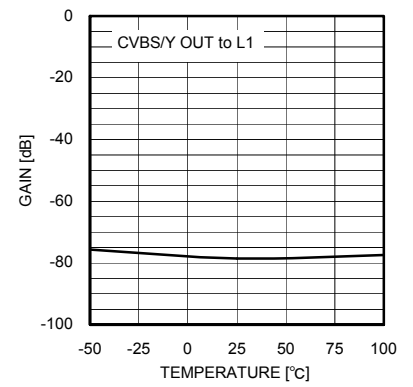


Fig.16 MUTE Attenuation (Temperature dependence)

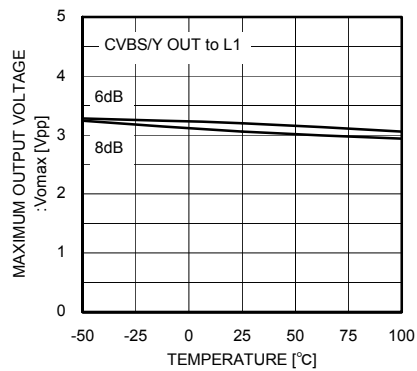


Fig.17 Maximum Output Level CVBS/Y OUT to L1

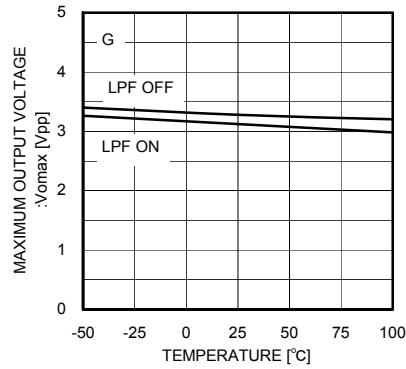


Fig.18 Maximum Output Level G

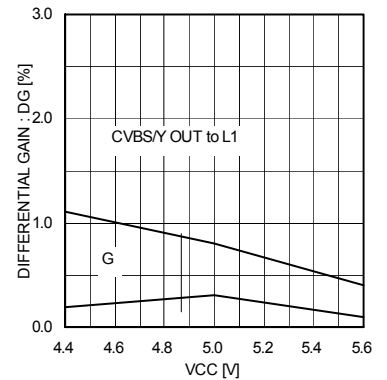


Fig.19 Differential Gain (Supply voltage dependence)

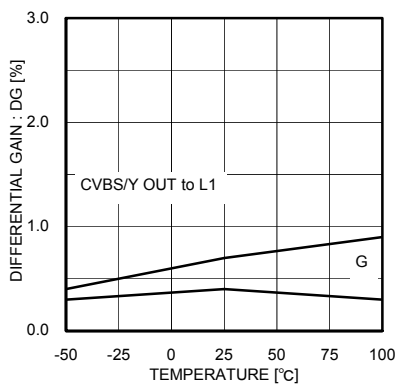


Fig.20 Differential Gain (Temperature dependence)

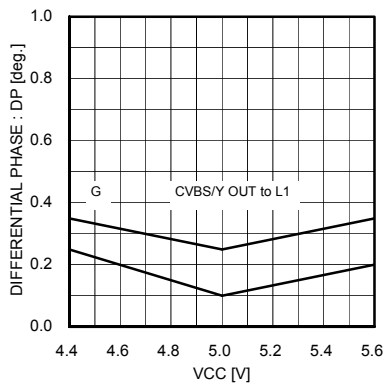


Fig.21 Differential Phase (Supply voltage dependence)

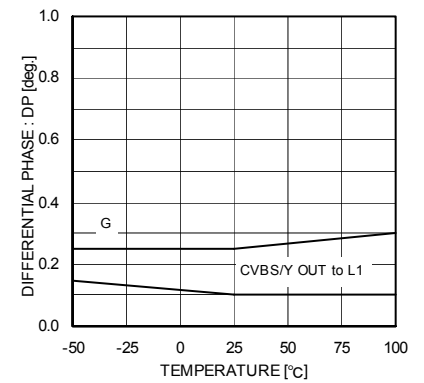


Fig.22 Differential Phase (Temperature dependence)

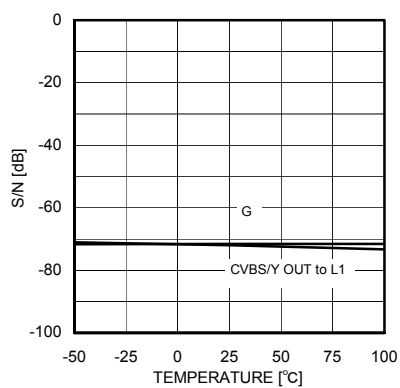


Fig.23 S/N ratio (Temperature dependence)

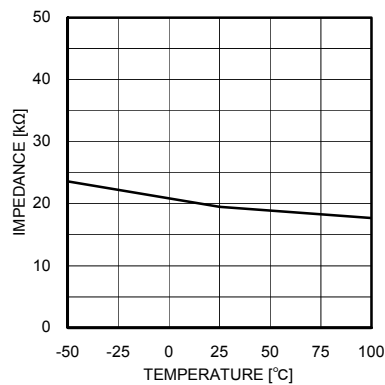


Fig.24 BIAS input impedance (Temperature dependence)

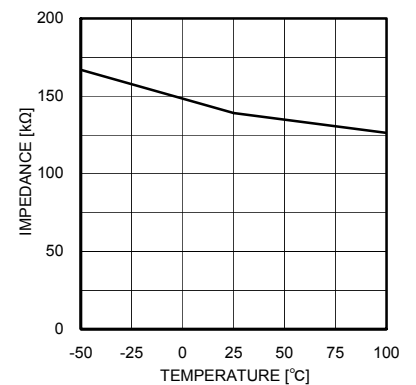


Fig.25 AUX R BIAS input impedance (Temperature dependence)

●Cautions on use

1. Numbers and data in entries are representative design values and are not guaranteed values of the items.
2. Although ROHM is confident that the example application circuit reflects the best possible recommendations, be sure to verify circuit characteristics for your particular application. Modification of constants for other externally connected circuits may cause variations in both static and transient characteristics for external components as well as this Rohm IC. Allow for sufficient margins when determining circuit constants.
3. Absolute maximum ratings
Use of the IC in excess of absolute maximum ratings, such as the applied voltage or operating temperature range (Topr), may result in IC damage. Assumptions should not be made regarding the state of the IC (short mode or open mode) when such damage is suffered. A physical safety measure, such as a fuse, should be implemented when using the IC at times where the absolute maximum ratings may be exceeded.
4. GND potential
Ensure a minimum GND pin potential in all operating conditions. Make sure that no pins are at a voltage below the GND at any time, regardless of whether it is a transient signal or not.
5. Thermal design
Perform thermal design, in which there are adequate margins, by taking into account the permissible dissipation (Pd) in actual states of use.
6. Short circuit between terminals and erroneous mounting
Pay attention to the assembly direction of the ICs. Wrong mounting direction or shorts between terminals, GND, or other components on the circuits, can damage the IC.
7. Operation in strong electromagnetic field
Using the ICs in a strong electromagnetic field can cause operation malfunction.
8. Operating Voltage Range and Operating Temperature Range
The circuit functional operations and electrical characteristics are guaranteed within the Operating Voltage Range and Operating Temperature Range. However, careful consideration must be taken in designing the circuit.
9. Supply voltage of operation
Although basic circuit function is guaranteed under normal voltage operation (4.75V~5.25V), ensure each parameter complies with appropriate electrical characteristics, when using this device.
10. The first resistor of 75Ω driver output must be layout nearest to the IC.
11. The coupling capacitor must be layout nearest to the IC and each pin.
12. I²C BUS is compatible with fast mode of Version 2.0 but not compatible with Hs mode.

●Thermal derating characteristics

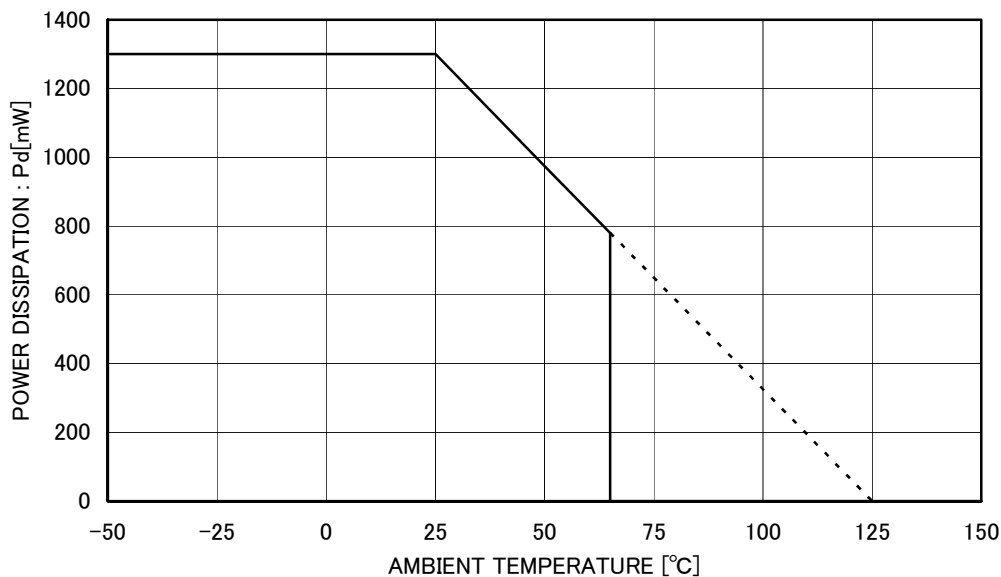


Fig.26

● Selection of order type

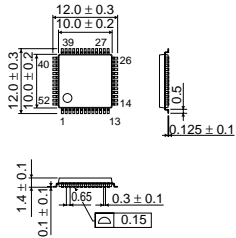
B H 7 6 2 4 K S 2

TYPE

BH7624KS2

SQFP-T52

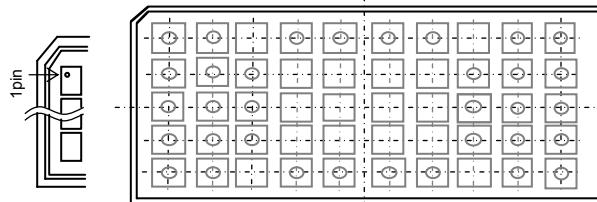
<Dimension>



(Unit:mm)

<Packing information>

Container	Tray(with dry pack)
Quantity	1000pcs
Direction of feed	Direction of product is fixed in a tray.



※Orders are available in complete units only.

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