

HDMI Switch ICs

3 for input 1 output switch with Termination sense correspondence (Sync with HPD_SINK)

BU16028KV**●Description**

BU16028KV is 3 for input 1 output HDMI/DVI switch LSI. Each port supports 2.25Gbps. (HDMI 1.3a)

This device control is simple. It requires only 3.3V source and a few GPIO controls.

Terminated resistors(50Ω) are integrated at input port. When channel is not selected, termination resistors are turned off. TMDS inputs are high impedance.

This device is integrated equalization function and DDC buffer function, so it can adapt long cable.

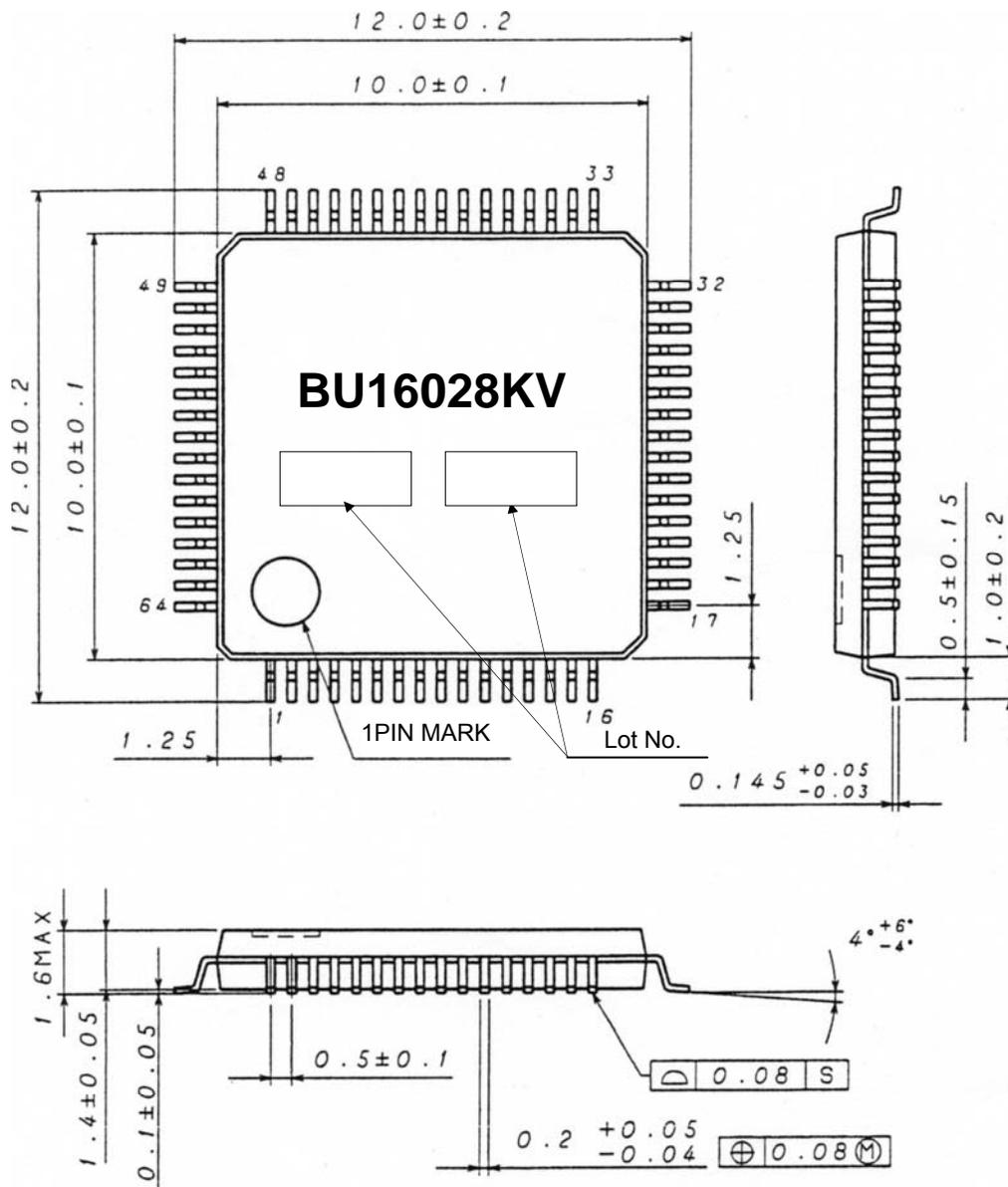
●Features

- Supports 2.25 Gbps signaling rate for 480i/p, 720i/p, and 1080i/p resolution to 12-bit color depth
- Compatible with HDMI 1.3a
- 5V tolerance to all DDC and HPD_SINK inputs
- Integrated DDC buffer
- Integrated switchable 50Ω receiver termination
- Integrated equalizer circuit to adapt long cable
- HBM ESD protection exceeds 10kV
- 3.3V fixed supply to TMDS I/Os
- 64Pin VQFP package
- ROHS compatible

●Applications

- Digital TV
- DVD Player
- Set-Top-Box
- Audio Video Receiver
- Digital Projector
- DVI or HDMI Switch Box

●OUTSIDE DIMENSION CHART



(UNIT : mm)

Fig. 1-1 . Outside dimension chart

● BLOCK DIAGRAM

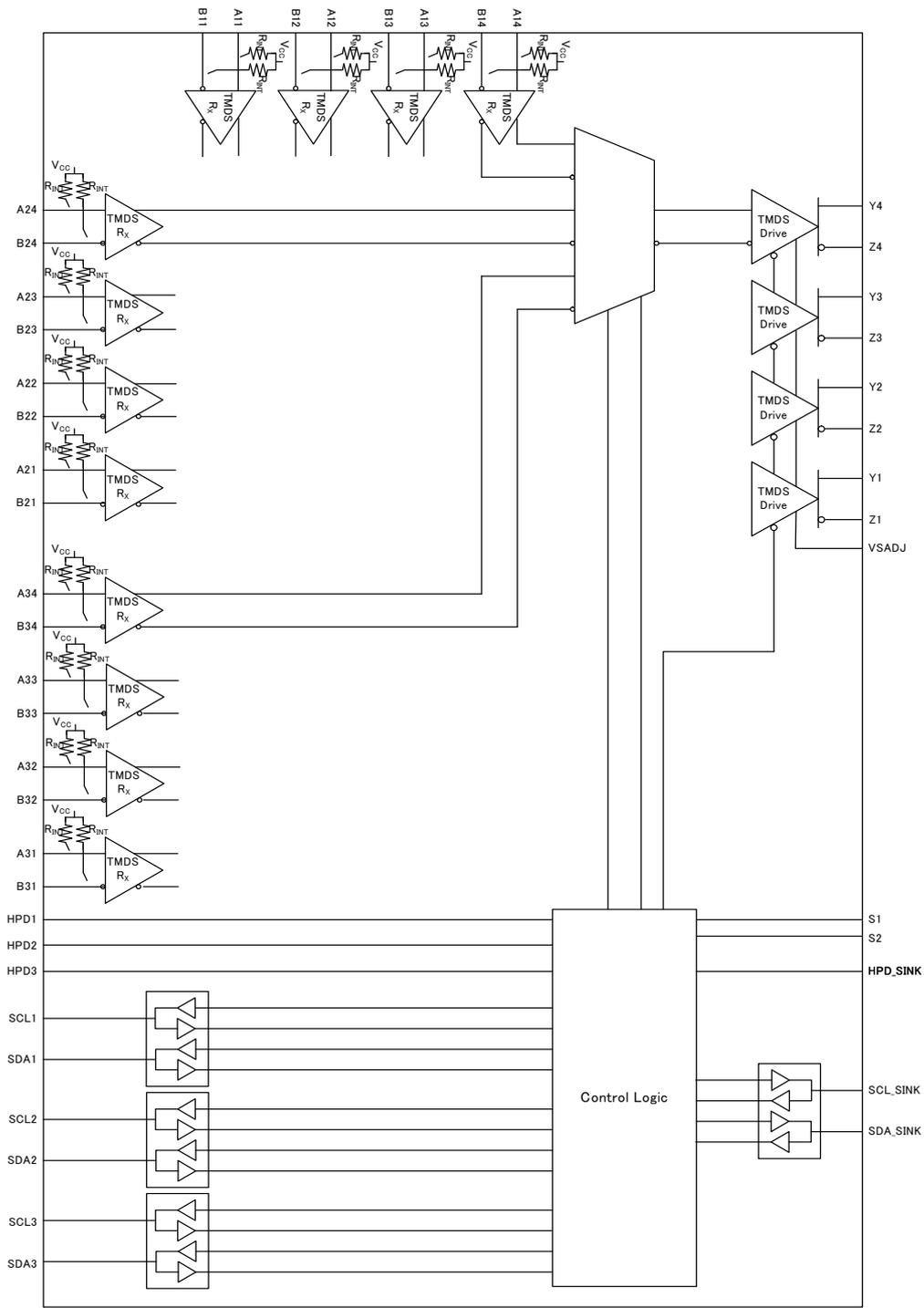


Fig. 2-1. Block Diagram

● PIN EXPLANATION

1). PIN ASSIGNMENT

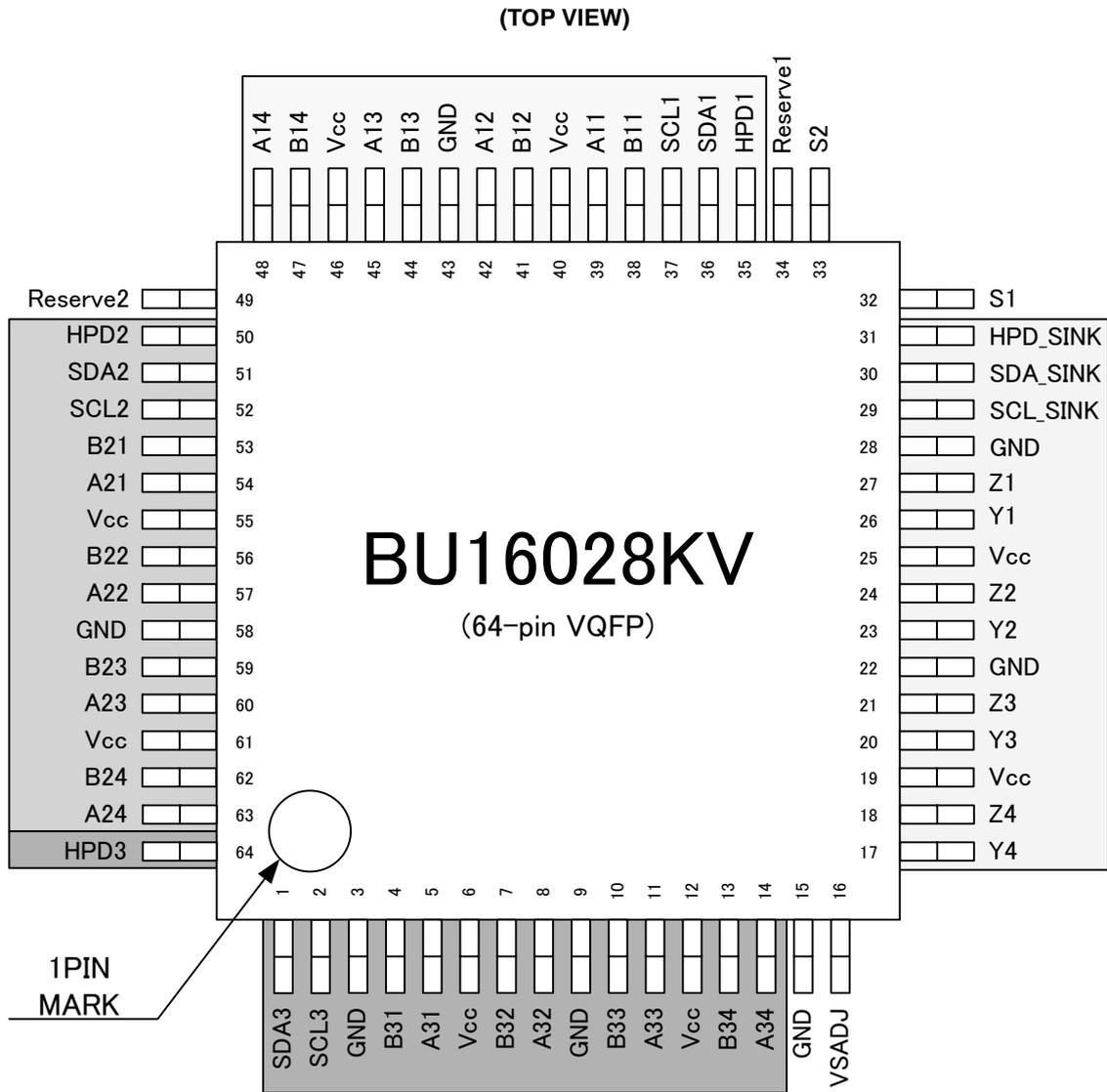


Fig3-1. Pin Location

2). PIN LIST

TERMINAL		I/O	DESCRIPTION
NAME	No.		
A11, A12, A13, A14	39, 42, 45, 48	I	Source port 1 TMDS positive inputs
A21, A22, A23, A24	54, 57, 60, 63	I	Source port 2 TMDS positive inputs
A31, A32, A33, A34	5, 8, 11, 14	I	Source port 3 TMDS positive inputs
B11, B12, B13, B14	38, 41, 44, 47	I	Source port 1 TMDS negative inputs
B21, B22, B23, B24	53, 56, 59, 62	I	Source port 2 TMDS negative inputs
B31, B32, B33, B34	4, 7, 10, 13	I	Source port 3 TMDS negative inputs
GND	3, 9, 15, 22, 28, 43, 58	-	Ground
HPD1	35	O	Source port 1 hot plug detector output (status pin)
HPD2	50	O	Source port 2 hot plug detector output (status pin)
HPD3	64	O	Source port 3 hot plug detector output (status pin)
HPD_SINK	31	I	Sink port hot plug detector input (status pin)
Reserve1	34	I/O	Set to HIGH/LOW/OPEN
Reserve2	49	I/O	Non Connect Pin
SCL1	37	I/O	Source port 1 DDC I ² C clock line
SCL2	52	I/O	Source port 2 DDC I ² C clock line
SCL3	2	I/O	Source port 3 DDC I ² C clock line
SCL_SINK	29	I/O	Sink port DDC I ² C clock line
SDA1	36	I/O	Source port 1 DDC I ² C data line
SDA2	51	I/O	Source port 2 DDC I ² C data line
SDA3	1	I/O	Source port 3 DDC I ² C data line
SDA_SINK	30	I/O	Sink port DDC I ² C data line
S1, S2	32, 33	I	Source selector
VCC	6, 12, 19, 25, 40, 46, 55, 61	-	Power supply
VSADJ	16	I	TMDS compliant voltage swing control (via 4.64k Ω to GND)
Y1, Y2, Y3, Y4	26, 23, 20, 17	O	Sink port TMDS positive outputs
Z1, Z2, Z3, Z4	27, 24, 21, 18	O	Sink port TMDS negative outputs

●EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS

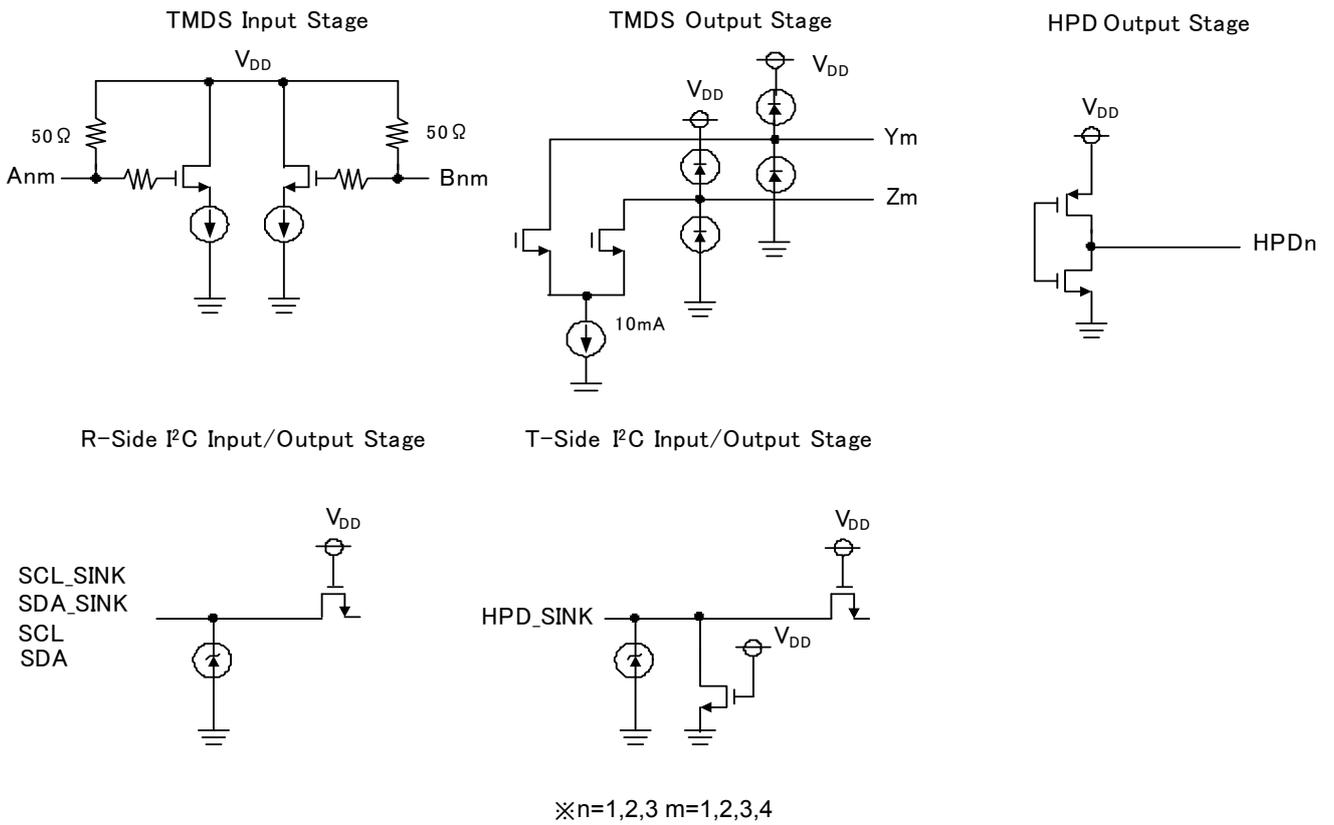


Fig. 4-1 . I/O pin schematic diagram

●SOURCE SELECTION LOOKUP TABLE

CONTROL PINS			I/O SELECTED	HOT PLUG DETECT STATUS			
HPD_SINK	S1	S2	Y/Z	SCL_SINK SDA_SINK	HPD1	HPD2	HPD3
H	H	H	A1/B1 Terminations of A2/B2 and A3/B3 are disconnected	SCL1 SDA1	H	L	L
H	L	H	A2/B2 Terminations of A1/B1 and A3/B3 are disconnected	SCL2 SDA2	L	H	L
H	L	L	A3/B3 Terminations of A1/B1 and A2/B2 are disconnected	SCL3 SDA3	L	L	H
H	H	L	None (Z) All terminations are disconnected	None (Z) Are pulled HIGH by external pull-up termination	H	H	H
L	H	H	Disallowed (indeterminate)State All terminations are disconnected	SCL1 SDA1	L	L	L
L	L	H	Disallowed (indeterminate)State All terminations are disconnected	SCL2 SDA2	L	L	L
L	L	L	Disallowed (indeterminate)State All terminations are disconnected	SCL3 SDA3	L	L	L
L	H	L	None (Z) All terminations are disconnected	None (Z) Are pulled HIGH by external pull-up termination	L	L	L

(1)H: Logic high; L: Logic low; X: Don't care; Z: High impedance

● ELECTRICAL SPECIFICATIONS

1.) ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range (unless otherwise noted)⁽¹⁾

ITEM	MIN.	TYP.	MAX.	UNIT
Power supply voltage (V _{CC})	-0.3	-	4.0	V
DDC, HPD_SINK input voltage	-0.3	-	6.0	V
Differential input voltage	2.5	-	4.0	V
S1, S2 input voltage	-0.3	-	4.0	V
Power dissipation	-	-	1250	mW
Storage temperature range	-55	-	125	°C

※70mm×70mm×1.6mm glass epoxy board mount. (Reverse Cu occupation rate: 15mm×15mm)

When it's used by than Ta=25°C, it's reduced by 12.5mW/°C.

2.) RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V _{CC}	Supply voltage	3	3.3	3.6	V
T _A	Operating free-air temperature	0	-	70	°C
TMDS DIFFERENTIAL PINS					
V _{IC}	Input common mode voltage	V _{CC} -0.6	-	V _{CC} +0.01	V
V _{ID}	Receiver peak-to-peak differential input voltage	150	-	1560	mVp-p
R _{VSADJ}	Resistor for TMDS compliant voltage swing range	4.60	4.64	4.68	kΩ
AV _{CC}	TMDS Output termination voltage, see Figure 5-1.	3	3.3	3.6	V
R _T	Termination resistance, see Figure 5-1.	45	50	55	Ω
Signaling rate		0	-	2.25	Gbps
CONTROL PINS (S1,S2)					
V _{IH}	LVTTL High-level input voltage	2	-	V _{CC}	V
V _{IL}	LVTTL Low-level input voltage	GND	-	0.8	V
STATUS(HPD_SINK)					
V _{IH}	LVTTL High-level input voltage	2.4	-	5.5	V
V _{IL}	LVTTL Low-level input voltage	GND	-	0.8	V
DDC I/O PINS Tx (SCL_SINK, SDA_SINK)					
V _{IH}	High-level input voltage	2.1	-	5.5	V
V _{IL}	Low-level input voltage	-0.3	-	0.35	V
DDC I/O PINS Rx (SCLn, SDAn) n = 1, 2, 3					
V _{IH}	High-level input voltage	2.4	-	5.5	V
V _{IL}	Low-level input voltage	-0.3	-	0.8	V

3.) ELECTRICAL CHARACTERISTICS

Over recommended operating conditions (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	TYP. ⁽¹⁾	MAX.	
I _{CC}	Supply current	V _{IH} = V _{CC} , V _{IL} = V _{CC} -0.4V, R _{VSADJ} = 4.64kΩ R _T = 50Ω, AV _{CC} = 3.3V Am/Bm = 2.25 Gbps HDMI data pattern, m = 2,3,4 A1/B1 = 225 MHz clock	-	120	150	mA
P _D	Power dissipation	V _{IH} = V _{CC} , V _{IL} = V _{CC} -0.4V, R _{VSADJ} = 4.64kΩ R _T = 50Ω, AV _{CC} = 3.3V Am/Bm = 2.25Gbps HDMI data pattern, m = 2,3,4 A1/B1 = 255 MHz clock	-	450	600	mW
TMD5 DIFFERENTIAL PINS (A/B;Y/Z)						
V _{OH}	Single-ended high-level output voltage	See Figure 5-2, AV _{CC} = 3.3V, R _T = 50Ω	AV _{CC} -200	-	Av _{CC} -50	mV
V _{OL}	Single-ended low-level output voltage		AV _{CC} -600	-	Av _{CC} -400	mV
V _{SWING}	Single-ended low-level swing voltage		300	-	460	mV
V _{od(O)}	Overshoot of output differential voltage		-	6%	15%	2xV _{swing}
V _{od(U)}	Undershoot of output differential voltage		-	12%	25%	2xV _{swing}
V _{OD(pp)}	Steady state output differential voltage	See Figure 5-2, Am/Bm = 250 Mbps HDMI data pattern , m = 2,3,4 A1/B1 = 25 MHz clock	600	-	920	mVp-p
R _{INT}	Input termination resistance	V _{IN} = 2.9V	45	50	55	Ω
ΔV _{OC(SS)}	Change in steady-state common-mode output voltage between logic states		-	5	-	mV

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	TYP. ⁽¹⁾	MAX.	
DDC Input and output						
Tx						
V _{IH}	High-level input voltage		2.1	-	5.5	V
V _{IL}	Low-level input voltage		-0.3	-	0.35	V
I _{IKT①}	Input leak current,	V _I =5.5V	-10	-	10	μA
I _{IKT②}	Input leak current,	V _I =V _{CC}	-10	-	10	μA
I _{OHT}	High-level output current	V _O =3.6V	-10	-	10	μA
I _{ILT}	Low-level input current	V _{IL} =GND	-10	-	10	μA
V _{OLT}	Low-level output voltage	R _L =4.7kΩ	0.43	0.5	0.57	V
V _{OLT} -V _{IL}	Low-level input voltage below output low-level voltage		20	100	190	mV
Rx						
V _{IH}	High-level input voltage		2.4	-	5.5	V
V _{IL}	Low-level input voltage		-0.3	-	0.8	V
I _{IKR①}	Input leak current	V _I =5.5V	-10	-	10	μA
I _{IKR②}	Input leak current	V _I =V _{CC}	-10	-	10	μA
I _{OHR}	High-level output current	V _O =3.6V	-10	-	10	μA
I _{ILR}	Low-level input current	V _{IL} =GND	-10	-	10	μA
V _{OLR}	Low-level output voltage	I _{out} = 4mA	-	-	0.2	V
DDC Input and output						
STATUS PINS (HPD 1, HPD 2, HPD 3)						
V _{OH(TTL)}	TTL High –level output voltage	I _{OH} = -8mA	2.4	-	V _{CC}	V
V _{OL(TTL)}	TTL Low –level output voltage	I _{OL} = 8mA	0	-	0.4	V
CONTROL PINS (S1, S2)						
I _{IH}	High –level digital input current	V _{IH} = V _{CC}	-10	-	10	μA
I _{IL}	Low –level digital input current	V _{IL} = GND	-10	-	10	μA
STATUS PINS (HPD_SINK)						
I _{IH}	High –level digital input current	V _{IH} = 5.5V	10	50	100	μA
		V _{IH} = V _{CC}	5	30	80	μA
I _{IL}	Low –level digital input current	V _{IL} = GND	-10	-	10	μA

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	TYP. ⁽¹⁾	MAX.	
TMDS DIFFERENTIAL PINS (Y/Z)						
t _{PLH}	Propagation delay time low-high-level output	See Figure 5-2, AV _{CC} = 3.3V, R _T = 50Ω	-	480	-	ps
t _{PHL}	Propagation delay time low-high-level output		-	500	-	ps
t _r	Differential output signal rise time (20%-80%)		-	150	-	ps
t _f	Differential output signal fall time (20%-80%)		-	150	-	ps
t _{sk(p)}	Pulse skew (t _{PHL} - t _{PLH})		-	20	-	ps
t _{sk(D)}	Intra-pair differential skew, see Figure 5-3.		-	50	-	ps
t _{sk(o)}	Inter-pair channel-to-channel output skew		-	50	-	ps
t _{sk(pp)}	Part to part skew		-	400	-	ps
DDC I/O PINS (SCL, SCL_SINK, SDA, SDA_SINK)						
t _{pdLHTR} (DDC)	Propagation delay time, low-to-high-level output Tx to Rx	R _L = 4.7kΩ C _L = 100pF	-	650	-	ns
t _{pdHLTR} (DDC)	Propagation delay time, high-to-low-level output Tx to Rx		-	200	-	ns
t _{pdLHRT} (DDC)	Propagation delay time, low-to-high-level output Rx to Tx	R _L = 1.67kΩ C _L = 400pF	-	500	-	ns
t _{pdHLRT} (DDC)	Propagation delay time, high-to-low-level output Rx to Tx		-	350	-	ns
t _r TX _(DDC)	Tx output Rise time	R _L = 4.7kΩ C _L = 100pF	-	800	-	ns
t _f TX _(DDC)	Tx output Fall time		-	150	-	ns
t _r RX _(DDC)	Rx output Rise time	R _L = 1.67kΩ C _L = 400pF	-	950	-	ns
t _f RX _(DDC)	Rx output Fall time		-	50	-	ns
t _{sx}	Select to switch output		-	8	-	ns
t _{dis}	Disable time		-	5	-	ns
t _{en}	Enable time		-	7	-	ns
t _{sx(DDC)}	Switch time from SCLn to SCL_SINK	C _L =10pF	-	800	-	Ns
STATUS PINS (HPD1,HPD2,HPD3)						
t _{pdLH(HPD)}	Propagation delay time, low-to-high-level output from HPD_SINK to HPDn(n=1,2,3)	C _L =10pF	-	5	-	ns
t _{pdHL(HPD)}	Propagation delay time, high-to-low-level output from HPD_SINK to HPDn(n=1,2,3)	C _L =10pF	-	5	-	ns
t _{sx(HPD)}	Switch time from port select to the latest valid status of HPD	C _L =10pF	-	8	-	ns

Note:

1. All typical values are at 25°C and with a 3.3V supply.

● MEASUREMENT SYMBOL AND CIRCUIT

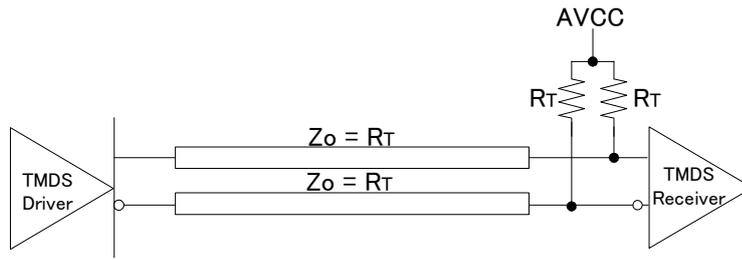


Figure 5-1. Termination for TMDS Output Driver

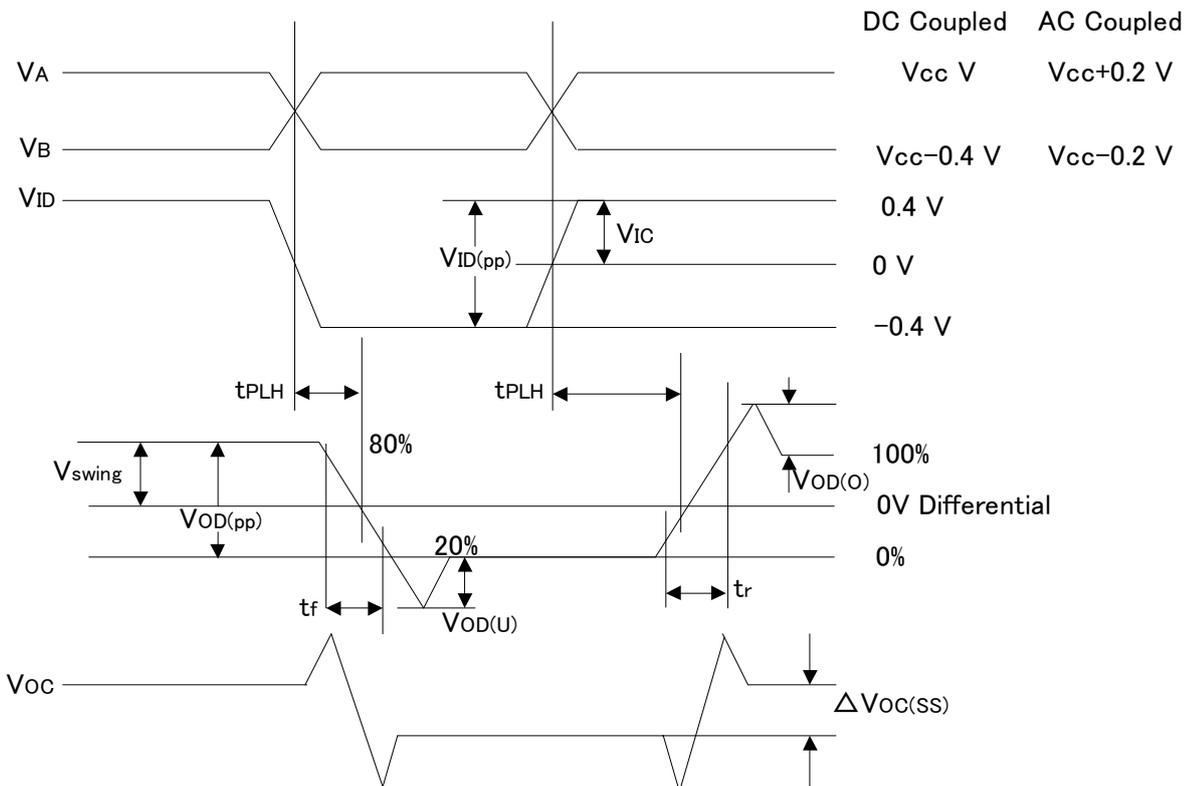
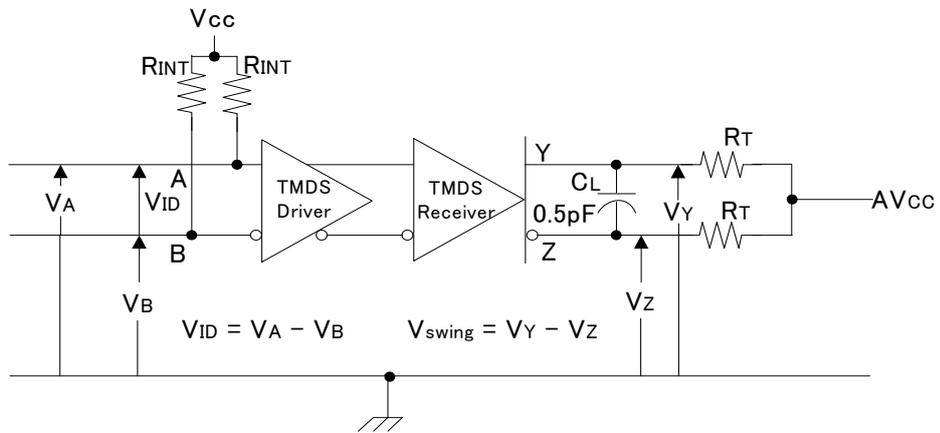


Figure 5-2. Timing Test Circuit and Definitions

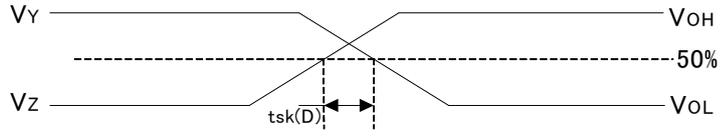


Figure 5-3. Definition of Intra-Pair Differential Skew

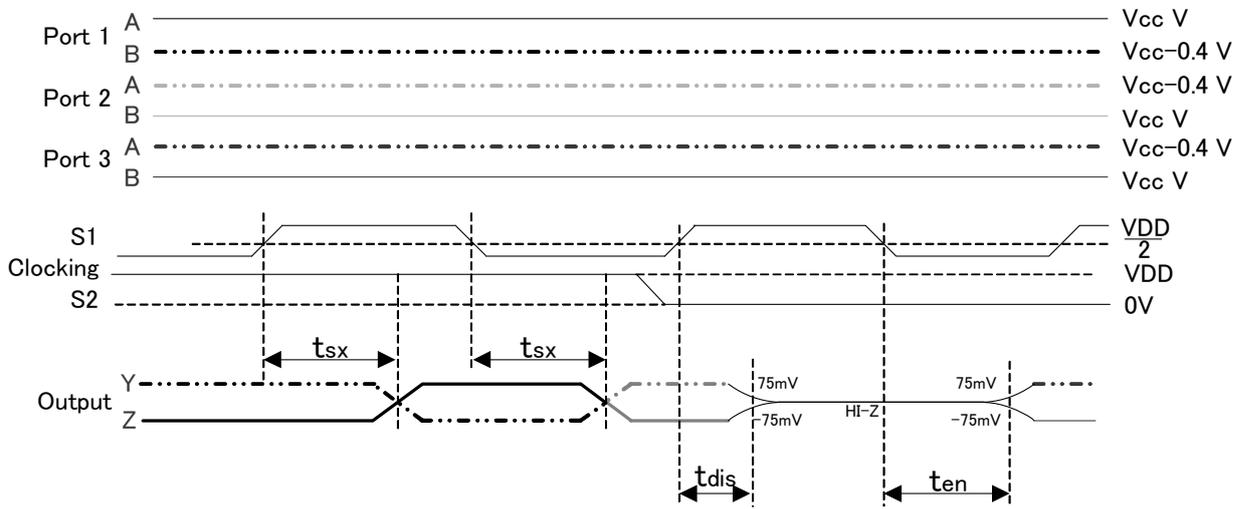


Figure 5-4. TMDs Outputs Control Timing Definitions

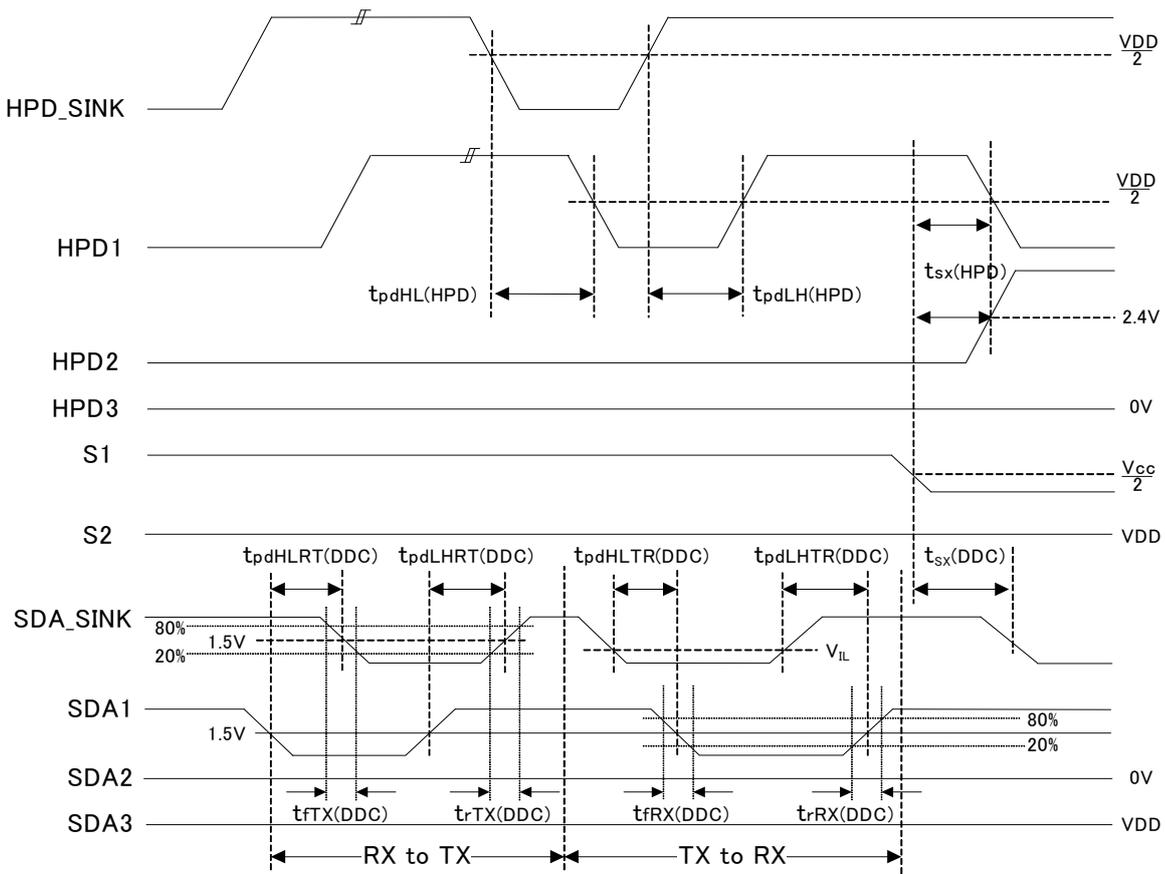


Figure 5-5. DDC and HPD Timing Definitions

1). Y and Z terminal ESD Diode notice.

Y and Z terminals are connected ESD diode.
 When $VCC + 0.4 < AVCC$.
 BU16028KV flow leak current from AVCC to VCC.
 In order to minimize leak current.
 Please use following application.
 If you use "Repeater" or "output Buffer"

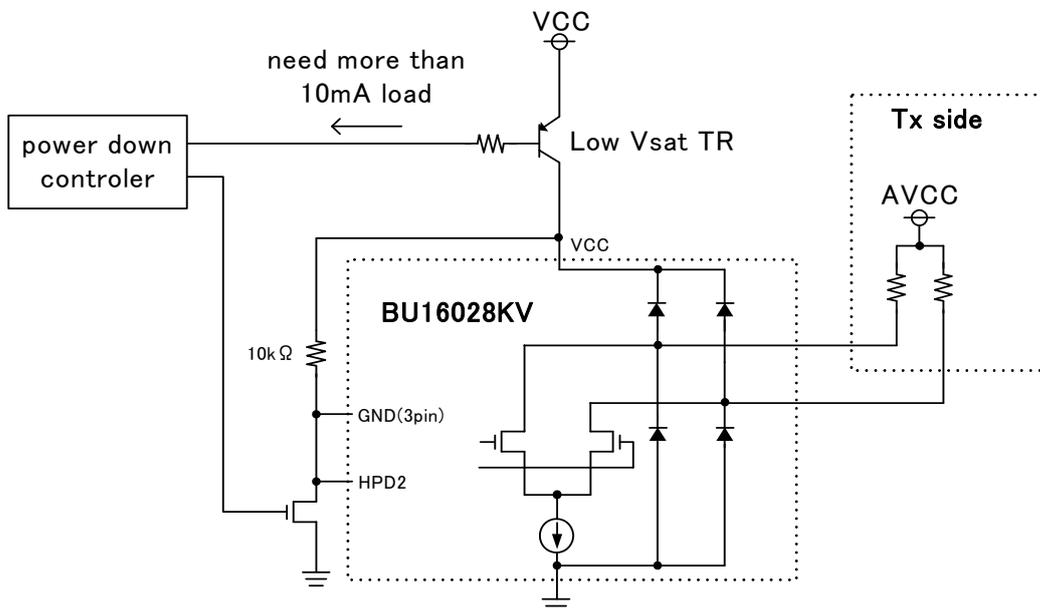


Figure 6-1. Ist mode application

2). HPD_SINK Pull down resistance.

HPD_SINK is a 5V tolerant structure shown in Fig6-2.
 It needs some drive current to pull down HPD_SINK "H" to "L"(max10uA@HPD_SINK=2V).
 So to pull down HPD_SINK, please use 10kΩ (or under 10kΩ) resistor.

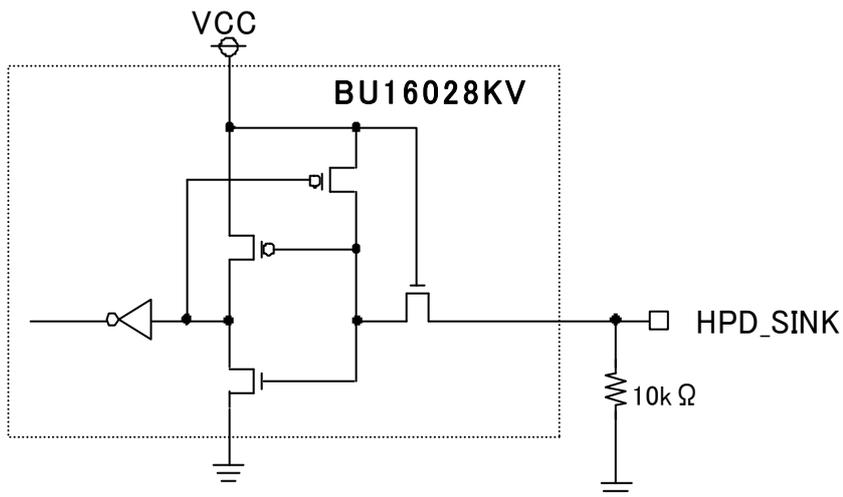


Figure 6-2. HPD_SINK I/O schematic

3). About don't use terminal.

Unused TMD5 input channel can be opened.

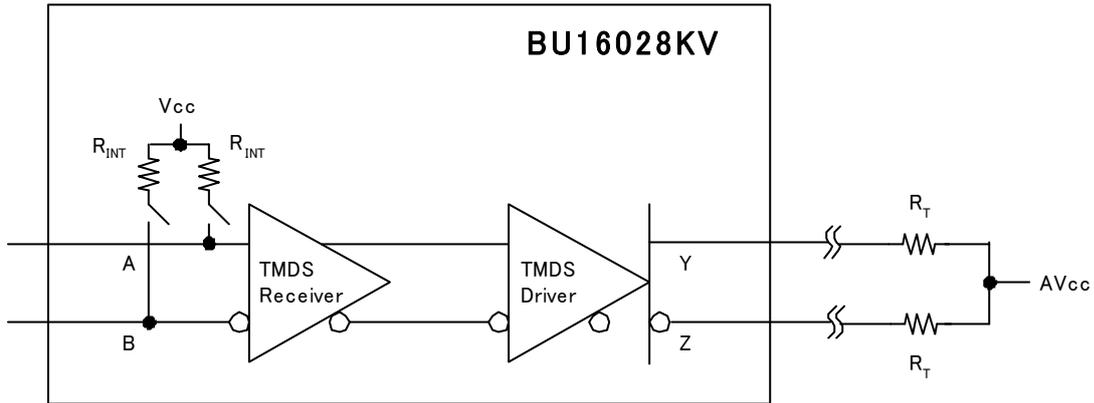


Figure 6-3. TMD5 Input Fail-Safe Recommendation

Unused DDC Buffers of R side pull up to Vdd .

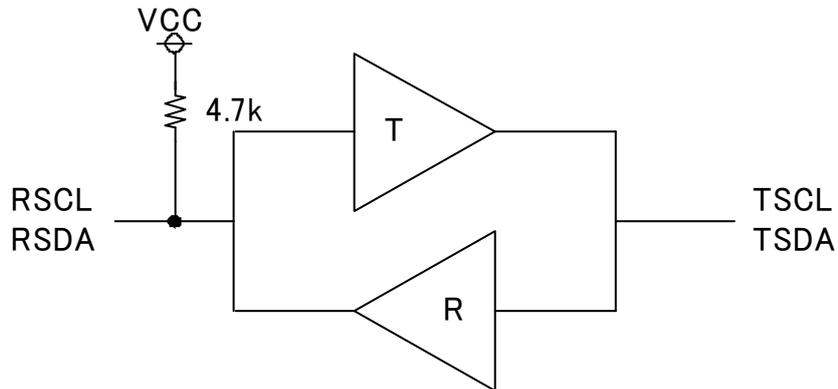


Figure 6-4. DDC Buffers in BU16028KV

4). About serial connect notice.

When HDMI sw output connect to other HDMI sw input like following application.

There is possibility that. 1080p(12bit) image isn't displayed. It 's depend on receiver IC characteristic.

When system is required 1080p (12bit), Rohm doesn't recommend serial connect application.

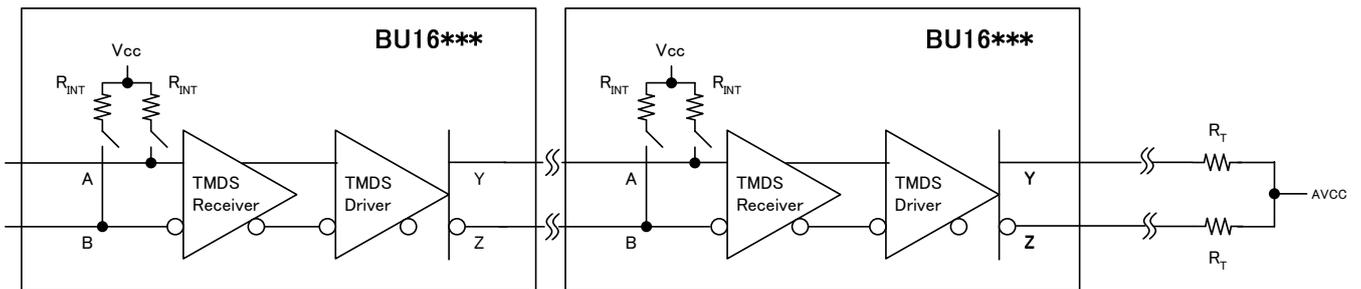


Fig6-5 serial connect notice

Notes

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