

MC56F80000-EVKUM

MC56F80000-EVK Board User Manual

Rev. 1 — 14 December 2022

User manual

Document information

Information	Content
Keywords	MC56F80000-EVK, MC56F80748, MC56F80xxx
Abstract	The NXP MC56F80000 Evaluation Kit board (MC56F80000-EVK) is a simple, yet sophisticated design featuring the MC56F80748 digital signal controller (DSC), a device that combines the processing power of a digital signal processor (DSP) and the functionality of a microcontroller (MCU).



1 Overview

The NXP MC56F80000 Evaluation Kit board (MC56F80000-EVK) is a simple, yet sophisticated design featuring the MC56F80748 digital signal controller (DSC), a device that combines the processing power of a digital signal processor (DSP) and the functionality of a microcontroller (MCU).

The MC56F80xxx device family is based on a 32-bit 56800EF core with:

- Up to 100 MIPS at 100 MHz core frequency
- DSP and MCU functionality in a unified C-efficient architecture
- Enhanced single-precision floating-point unit (eFPU)
- Coordinate rotation digital computer (CORDIC) engine

MC56F80748 has 64 kB on-chip Flash memory and 8 kB on-chip RAM.

The MC56F80000-EVK board features OpenSDA, which provides an onboard debugger (consider it as an on-chip Multilink debugger) and a virtual serial port for rapid prototyping and product development. On MC56F80000-EVK, the OpenSDA MCU is a Kinetis K Series K26 family device, MK26FN2M0VMI18.

The MC56F80000-EVK hardware is form-factor compatible with the Arduino™ R3 pin layout, providing a broad range of expansion board options. The onboard interface includes a 3-axis MEMS accelerometer, PWM and user LEDs, buttons, ADC test circuits, OPAMP test circuits, and external serial flash memory.

This document provides detailed information about the MC56F80000-EVK board interfaces, power supplies, clocks, LEDs, and other interfaces.

1.1 Acronyms

The table below lists and explains the acronyms and abbreviations used in this document.

Table 1. Acronyms and abbreviations

Term	Description
ADC	Analog-to-digital converter
CLK	Clock
CMP	Comparator
DIO	Data input/output
DNP	Do not populate
DSC	Digital signal controller
DSP	Digital signal processor
GPIO	General-purpose input/output
JTAG	Joint test access group
LDO	Low dropout
LPI2C	Low-power inter-integrated circuit (LPI2C)
MCU	Microcontroller unit
MEMS	Microelectromechanical system
NTC	Negative temperature coefficient

Table 1. Acronyms and abbreviations...continued

Term	Description
OPAMP	Operational amplifier
OpenSDA	Open-standard serial and debug adapter
PGA	Programmable gain amplifier
PWM	Pulse width modulation
QSPI	Quadruple serial peripheral interface
SDK	Software development kit
SPI	Serial peripheral interface
SWD	Serial wire debug
UART	Universal asynchronous receiver transmitter
USB	Universal serial bus

1.2 Related documentation

The table below lists and explains the additional documents and resources that you can refer to for more information on MC56F8000-EVK. Some of the documents listed below may be available only under a non-disclosure agreement (NDA). To request access to these documents, contact your local field applications engineer (FAE) or sales representative.

Table 2. Related documentation

Document	Description	Link/how to access
MC56F80xxx Reference Manual	Intended for system software and hardware developers and applications programmers who want to develop products with this device.	MC56F80XXXRM
MC56F80xxx Data Sheet	Provides information about electrical characteristics, hardware design considerations, and ordering information	MC56F80XXX
MCUXpresso Software Development Kit (SDK) documentation	The MCUXpresso SDK is a comprehensive software enablement package designed to simplify and accelerate application development with NXP MCUs	mcuxpresso.nxp.com
K26 Sub-Family Reference Manual	Intended for system software and hardware developers and applications programmers who want to develop products with this device.	K26P169M180SF5RM

1.3 Board kit contents

The table below lists the items included in the MC56F8000-EVK kit.

Table 3. Hardware kit contents

Item	Quantity
MC56F80000-EVK board hardware assembly	1
USB Type A to micro USB Type B cable, 1 m	1
MC56F80000-EVK Quick Start Guide	1

1.4 Block diagram

The figure below shows the MC56F80000-EVK block diagram.

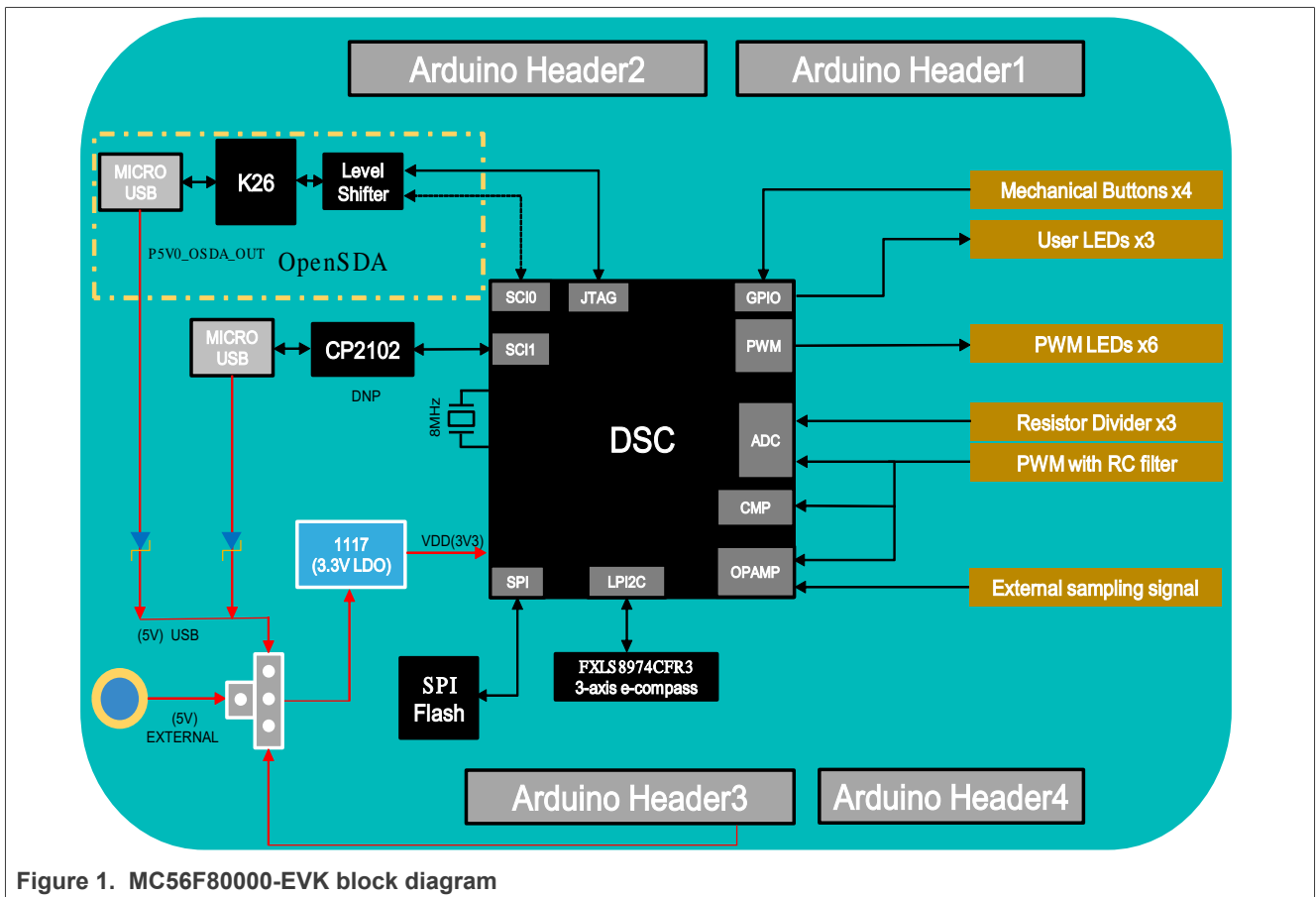


Figure 1. MC56F80000-EVK block diagram

1.5 Board pictures

The following figure shows the top-side view of MC56F80000-EVK.

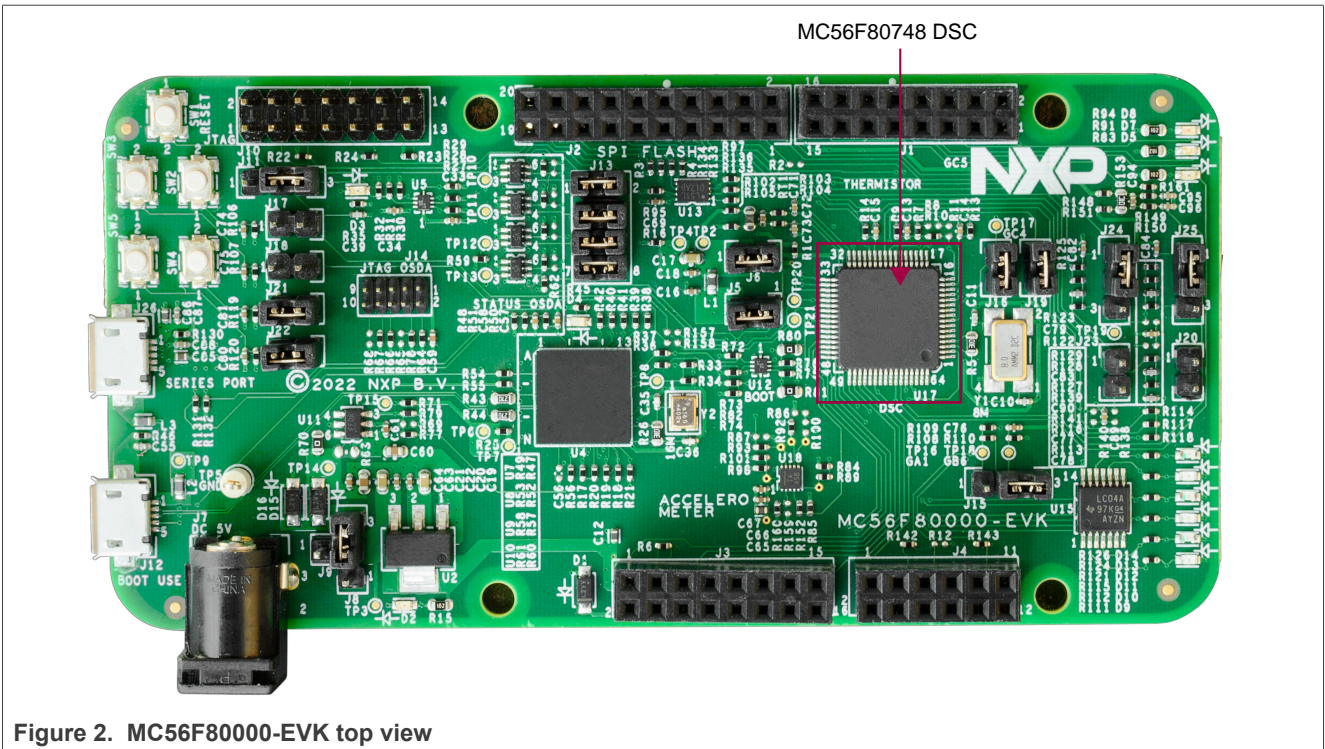
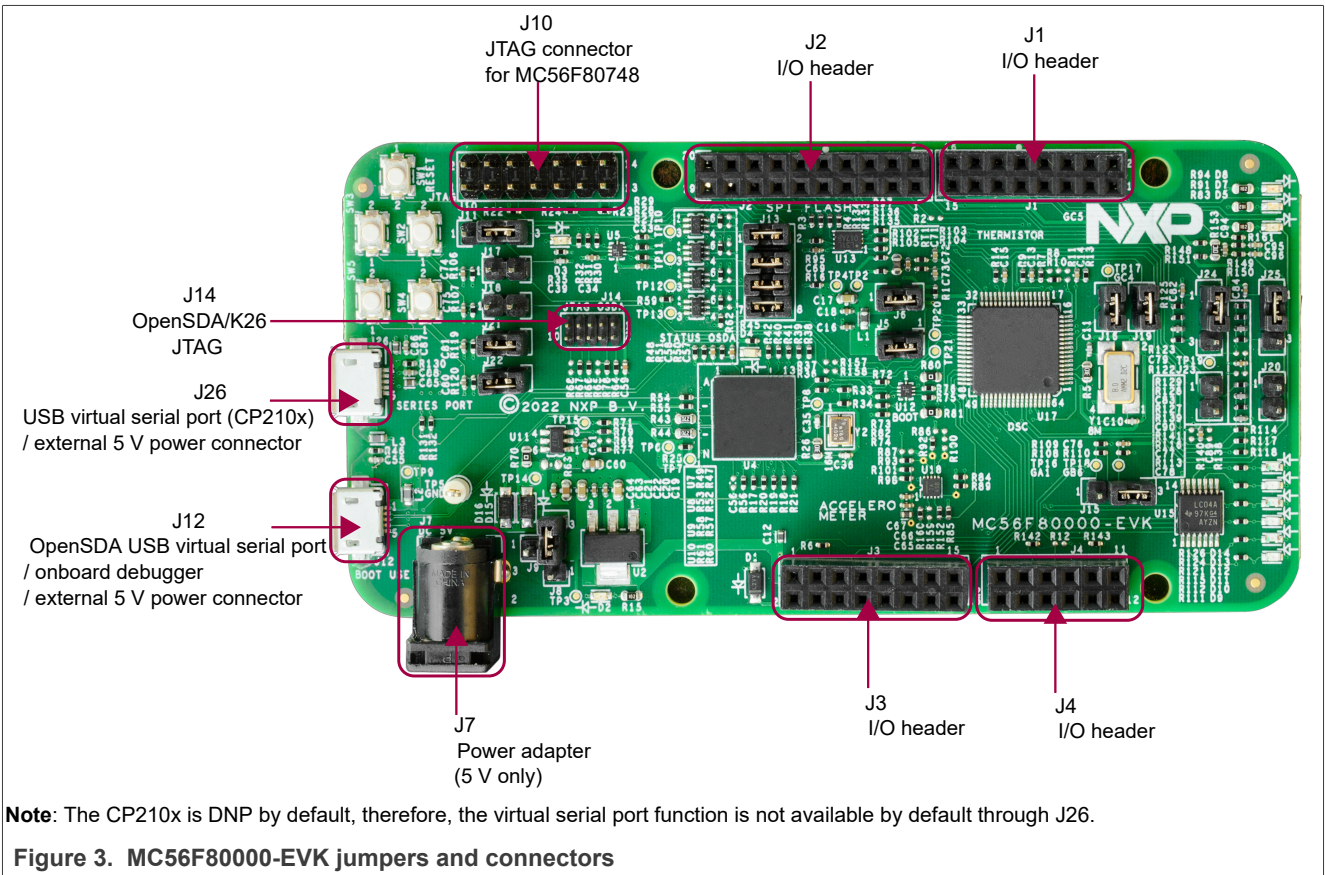


Figure 2. MC56F8000-EVK top view

The following figure shows the onboard connectors on MC56F8000-EVK.



Note: The CP210x is DNP by default, therefore, the virtual serial port function is not available by default through J26.

Figure 3. MC56F8000-EVK jumpers and connectors

The following figure shows the Jumpers, LEDs, and push buttons on MC56F80000-EVK.

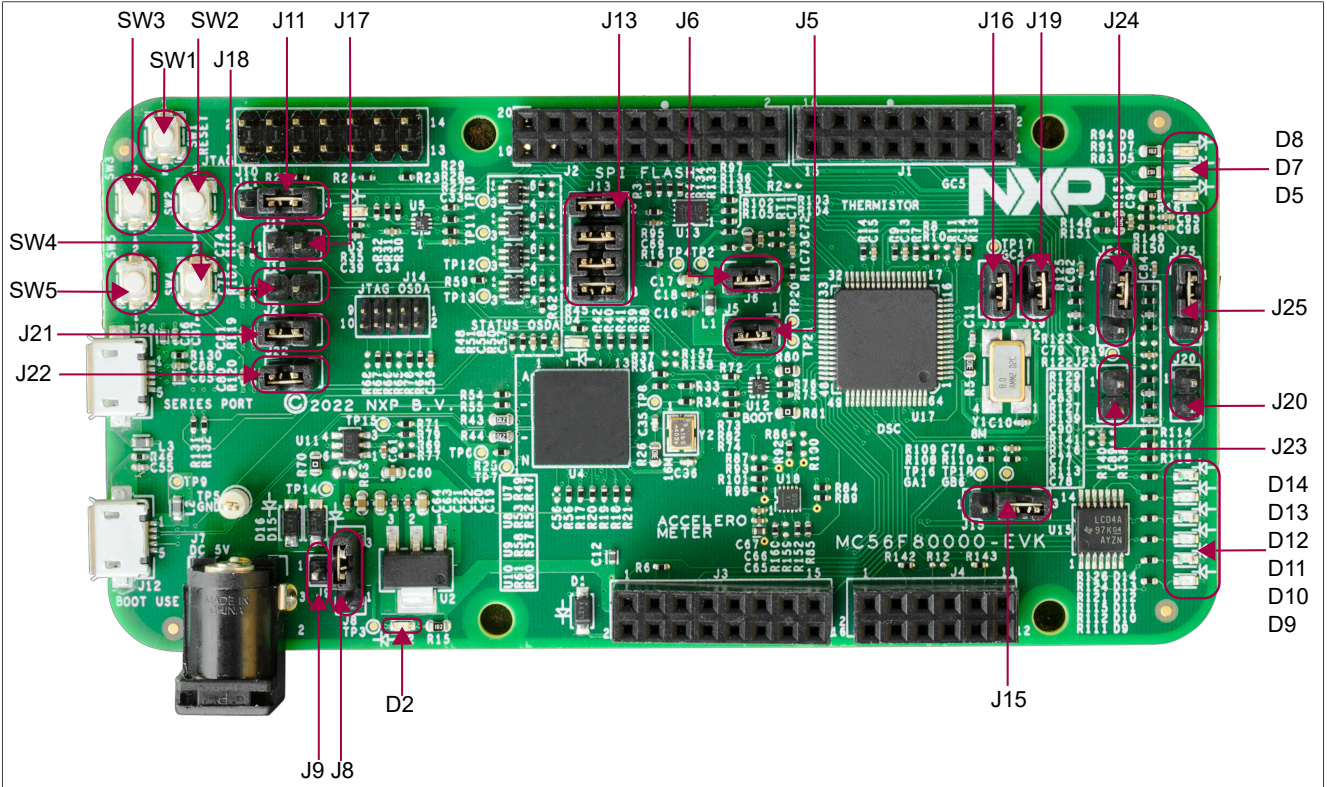


Figure 4. MC56F80000-EVK jumpers, LEDs, and push buttons

1.6 Board features

The following table lists the features of MC56F80000-EVK. [Figure 2](#) shows different components of MC56F80000-EVK.

Table 4. MC56F80000-EVK features

MC56F80000-EVK feature	Processor feature used	Description
MC56F80748 DSC		The processor is based on 32-bit 56800EF core of up to 100 MIPS at 100 MHz core frequency Note: For details on the MC56F80748 DSC, refer to MC56F80XXX Reference Manual.
Power supply		<ul style="list-style-type: none"> 5 V input power supply from any of the following: <ul style="list-style-type: none"> External DC power supply connector (J7) I/O header (J3) OpenSDA USB micro-AB connector (J12) USB micro-AB connector (J26) Jumpers J8 and J9 are used for 5 V power source selection LD1117 LDO for 3.3 V VDD supply
Clock		<ul style="list-style-type: none"> 8 MHz crystal clock for MC56F80748 16 MHz crystal clock for MK26FN2M0VMI18

Table 4. MC56F80000-EVK features...continued

MC56F80000-EVK feature	Processor feature used	Description
3-axis low-g accelerometer	Low-power inter-integrated circuit (LPI2C) module	<ul style="list-style-type: none"> Supports NXP FXLS8974CF accelerometer for motion sensing Device supports both high-performance and low-power operating modes
x3 resistor divider	High-speed analog-to-digital converter (ADC)	<ul style="list-style-type: none"> Three resistor dividers circuits are used on the MC56F80000-EVK board to test the ADC block functions One negative temperature coefficients (NTC) thermistor (NCP18XH103F03RB) supporting temperature from 90 °C to -20 °C
Debug		<ul style="list-style-type: none"> Onboard serial and debug adapter (OpenSDA) circuit <ul style="list-style-type: none"> Provides a debug circuit for MC56F80748 through USB connector J12 when all the four jumpers in J13 are connected Supports a JTAG/SWD connector (J14) to program and debug OpenSDA MCU MK26FN2M0VMI18 Provides a virtual serial port through USB connector (J12), which uses QSCI0 in MC56F80748 USB-to-UART device (CP2102N) (Not populated by default) <ul style="list-style-type: none"> Provides a virtual serial port through USB connector (J26), which uses QSCI1 in MC56F80748 JTAG connector (J10) to program and debug MC56F80748, when all the four jumpers in J13 are disconnected
Mechanical buttons	GPIO	Five Tactile switches (SW[1:5]) as push buttons. SW1 is the reset button. (See Section 1.7)
I/O headers		Headers compatible with: <ul style="list-style-type: none"> Arduino shields
LED		<ul style="list-style-type: none"> Supports six LEDs controlled by 6 PWM channels Supports three user-defined LEDs
PCB		MC56F80000-EVK: 107.6 mm X 53.4 mm, 4 layer
Orderable part number		MC56F80000-EVK

1.7 Push-button switches

Five push buttons are supported on the MC56F80000-EVK using the Tactile switches (TL1015AF160QG).

The following table explains the onboard push buttons. [Figure 4](#) shows the push buttons locations on the MC56F80000-EVK board.

Table 5. Push buttons

Part identifier	Switch type	Description
SW1	Push button	When pressed, resets the MC56F80748 MCU. Note: The MCU can also be reset using the JTAG connector (J10) or by the reset signal from OpenSDA circuitry.
SW2	Push button	SW2 connects to GPIOE6 when jumper J17 is shorted. Pressing SW2 gives a low level on GPIOE6, otherwise, it is a high level on GPIOE6.

Table 5. Push buttons...continued

Part identifier	Switch type	Description
SW3	Push button	SW3 connects to GPIOE7 when jumper J18 is shorted. Pressing SW3 gives a low level on GPIOE7, otherwise, it is a high level on GPIOE7.
SW4	Push button	SW4 connects to GPIOF8 when jumper J21 is shorted. Pressing SW4 gives a low level on GPIOF8, otherwise, it is a high level on GPIOF8.
SW5	Push button	SW5 connects to GPIOC13 when jumper J22 is shorted. Pressing SW4 gives a low level on GPIOC13, otherwise, it is a high level on GPIOC13.

1.8 Connectors

Connectors are onboard devices that allow to connect external devices to the board. [Figure 3](#) shows the MC56F80000-EVK connectors. The table below describes the connectors.

Table 6. MC56F80000-EVK connectors

Part identifier	Connector type	Description	Reference section
J1	2x8 connector	I/O headers compatible with the Arduino shields	Section 2.9
J2	2x10 connector		
J3	2x8 connector		
J4	2x6 connector		
J7	DC power jack	For 5 V input power supply to the board; connects to 5 V power adapter.	Section 2.1.1
J10	2x7 connector	JTAG connector to program and debug the MC56F80748. Note: Remove four jumpers on J13 when this JTAG connector is used. This is to avoid the impact of onboard OpenSDA circuit.	Section 2.12.1
J12	USB 2.0 micro-AB connector	OpenSDA USB port, and external 5 V power connector. Used for virtual serial communication and to debug/program MC56F80748.	Section 2.8
J14	2x5 connector	K26 (OpenSDA) JTAG/SWD connector. Provides debug interface to program and debug MK26FN2M0VMI18.	See board schematic
J26	USB 2.0 micro-AB connector	USB connector for USB-to-UART CP210x device, which provides a virtual serial port. Also, used as an external 5 V power connector. Note: CP210x USB-to-UART bridge VCP drivers are needed. CP210x is not populated by default on the board.	Section 2.11

1.9 Jumpers

Jumpers (or shorting headers) are small connectors that allow to choose from two or more options available. [Figure 3](#) highlights the MC56F80000-EVK jumpers available for use. The following table describes the jumpers available on MC56F80000-EVK.

Table 7. MC56F80000-EVK jumpers

Part identifier	Jumper type	Description	Jumper settings
J5	1x2-pin header	VDD	Shorted pin 1-2 (default setting): Connect VDD to DSC digital power supply VDD_MCU
J6	1x2-pin header	VDDA	Shorted pin 1-2 (default setting): Connect VDDA to DSC analog power supply VDDA_MCU
J8, J9	1x3-pin header 1x1-pin header	5 V power source selection	<ul style="list-style-type: none"> Shorted J8 (pin 1-2): P5V_DC_IN (5 V) input power supply is from I/O header (J3, pin 16) Shorted J8 (pin 2-3) (default setting): 5 V input power source is either P5V0_OSDA_OUT power supply from OpenSDA USB connector (J12) or P5V_USB2 power supply from USB connector (J26) Shorted J8 (pin2) and J9 (pin1): 5 V input power source is DC jack J7
J11	1x3-pin header	Reset selection	<ul style="list-style-type: none"> Shorted pin 1-2: Manual reset signal after pressing switch SW1 is controlled through the OpenSDA microcontroller MK26FN2M0VMI18 using the NTSX2102GU8H dual-supply translating transceiver. Use this setting only when OpenSDA MCU MK26FN2M0VMI18 is powered and has been programmed with a correct OpenSDA firmware Shorted pin 2-3 (default setting): Manual reset signal after pressing switch SW1 is routed to MC56F80748 directly.
J13	2x4-pin header	DSC JTAG signal connectors between MC56F80748 and OpenSDA circuit	<ul style="list-style-type: none"> Shorted pin 1-2 (default setting): Connect OpenSDA circuit with MC56F80748 GPIOD2 (TCK signal) Shorted pin 3-4 (default setting): Connect OpenSDA circuit with MC56F80748 GPIOD3 (TMS signal) Shorted pin 5-6 (default setting): Connect OpenSDA circuit with MC56F80748 GPIOD0 (TDI signal) Shorted pin 7-8 (default setting): Connect OpenSDA circuit with MC56F80748 GPIOD1 (TDO signal)
J15	1x3-pin header	OPAMP test	<ul style="list-style-type: none"> Shorted pin 1-2: Configure the internal OPAMP to work at PGA mode Shorted pin 2-3 (default setting): Configure the internal OPAMP to work at OPAMP mode
J16	1x2-pin header	OPAMP test	<ul style="list-style-type: none"> Open: Configure the internal OPAMP to work at PGA mode Shorted (default setting): Configure the internal OPAMP to work at OPAMP mode
J17	1x2-pin header	SW2	<ul style="list-style-type: none"> Open (default setting): Disconnect SW2 button from MC56F80748 GPIOE6 Shorted: Connect SW2 button to MC56F80748 GPIOE6
J18	1x2-pin header	SW3	<ul style="list-style-type: none"> Open (default setting): Disconnect SW3 button from MC56F80748 GPIOE7 Shorted: Connect SW3 button to MC56F80748 GPIOE7
J19	1x2-pin header	OPAMP/ADC/CMP test with filtered PWM output	<ul style="list-style-type: none"> Open: Disconnect the GPIOE6 (PWMA_3B) from the RC filter Shorted (default setting): Connect the GPIOE6 (PWMA_3B) with the RC filter
J20	1x2-pin header	Current sensing	<ul style="list-style-type: none"> Open (default setting): Use external OPAMP from FRDM-MC-LVPMSM board for motor phase A current sensing Shorted: Use DSC internal OPAMP for motor phase A current sensing

Table 7. MC56F80000-EVK jumpers...continued

Part identifier	Jumper type	Description	Jumper settings
J21	1x2-pin header	SW4	<ul style="list-style-type: none"> Open: Disconnect SW4 button from MC56F80748 GPIOF8 Shorted (default setting): Connect SW4 button to MC56F80748 GPIOF8
J22	1x2-pin header	SW5	<ul style="list-style-type: none"> Open: Disconnect SW5 button from MC56F80748 GPIOC13 Shorted (default setting): Connect SW5 button to MC56F80748 GPIOC13
J23	1x2-pin header	Current sensing	<ul style="list-style-type: none"> Open (default setting): Use external OPAMP from FRDM-MC-LVPMSM board for motor phase A current sensing Shorted: Use DSC internal OPAMP for motor phase A current sensing
J24	1x3-pin header	Current sensing	<ul style="list-style-type: none"> Shorted pin 1-2 (default setting): Use external OPAMP from FRDM-MC-LVPMSM board for motor phase A current sensing Shorted pin 2-3: Use DSC internal OPAMP for motor phase A current sensing
J25	1x3-pin header	Current sensing	<ul style="list-style-type: none"> Shorted pin 1-2 (default setting): Use external OPAMP from FRDM-MC-LVPMSM board for motor phase B current sensing Shorted pin 2-3: Use DSC internal OPAMP for motor phase B current sensing

1.10 LEDs

MC56F80000-EVK has light-emitting diodes (LEDs) to monitor system functions, such as power-on, reset, board faults, and so on. The information collected from LEDs can be used for debugging purposes.

LEDs are highlighted in [Figure 4](#). The table below describes the MC56F80000-EVK LEDs.

Table 8. MC56F80000-EVK LEDs

Part identifier	LED color	LED name	Description (When LED in ON)
D2	Green	Power	Indicates that VDD (3.3 V) supply is available and the MC56F80000-EVK board is powered up.
D3	Red	Reset	Indicates that the MC56F80748 device is under reset.
D4	Orange	OpenSDA power	Indicates that the OpenSDA microcontroller MK26FN2M0 VMI18 is powered up and has been programmed with an OpenSDA firmware.
D5	Red	User LED1	User-programmable LED connected with GPIOF6. A low level turns on the LED.
D7	Blue	User LED2	User-programmable LED connected with GPIOF4. A low level turns on the LED.
D8	Yellow	User LED3	User-programmable LED connected with GPIOF5. A low level turns on the LED.
D9	Yellow/Green	PWM LED0	Indicates that GPIOE0/PWMA_0B function is enabled and PWM signal is outputted
D10	Yellow	PWM LED1	Indicates that GPIOE1/PWMA_0A function is enabled and PWM signal is outputted. A high level turns on the LED.

Table 8. MC56F80000-EVK LEDs...continued

Part identifier	LED color	LED name	Description (When LED in ON)
D11	Yellow/Green	PWM LED2	Indicates that GPIOE2/PWMA_1B function is enabled and PWM signal is outputted. A high level turns on the LED.
D12	Yellow	PWM LED3	Indicates that GPIOE3/PWMA_1A function is enabled and PWM signal is outputted. A high level turns on the LED.
D13	Yellow/Green	PWM LED4	Indicates that GPIOE4/PWMA_2B function is enabled and PWM signal is outputted. A high level turns on the LED.
D14	Yellow	PWM LED5	Indicates that GPIOE5/PWMA_2A function is enabled and PWM signal is outputted. A high level turns on the LED.

2 MC56F80000-EVK functional description

This chapter describes the features and functions of MC56F80000-EVK. For details of the MC56F80748 MCU features, see *MC56F80xxx Reference Manual*.

2.1 Power supplies

The MC56F80000-EVK board can be powered with 5 V power supply using one of the following source options:

- External DC power supply adapter (J7)
- OpenSDA USB micro-AB connector (J12)
- I/O header (J3, pin 6)
- CP2102 USB micro-AB connector (J26)

The following figure shows the 5 V power source selection circuit diagram.

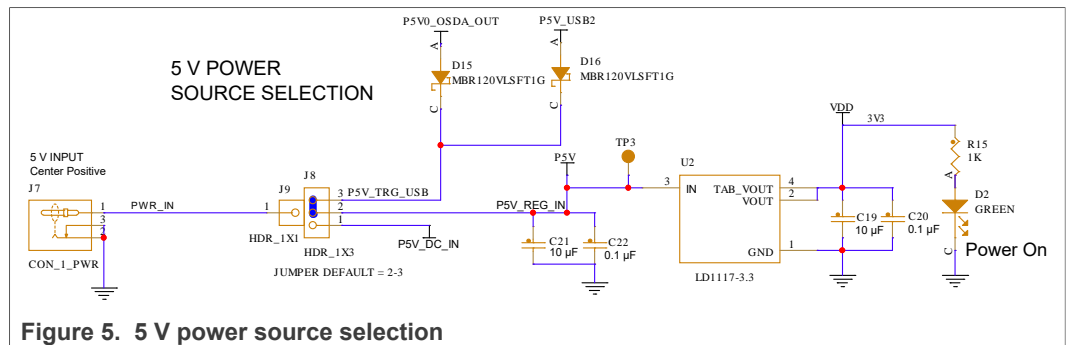


Figure 5. 5 V power source selection

Jumpers J8 and J9 are used for 5 V input power source (P5V) selection purpose. For J8 and J9 detail, see [Section 1.9](#).

P5V is then converted into 3.3 V (VDD) for DSC, SPI Flash, 3-axis low-g accelerometer, and Arduino header. Especially, P5V0_OSDA is converted into 3.3 V (P3V3_VREG_OUT) with a regulator inside MK26FN2M0VMI18 to power OpenSDA circuits.

2.1.1 5 V power sources

The following table describes the 5 V input power sources and their output power supplies.

Table 9. 5 V power sources

Part identifier	Device/Power source	Output power supply	Description
J7	5 V DC power jack	PWR_IN	
J12	OpenSDA micro-AB USB connector providing 5 V power supply	P5V0_OSDA	<ul style="list-style-type: none"> Source of P5V0_OSDA_OUT Supplies power to the power switch, MIC2005-0.8YM6 (U11) USB regulator input power supply for OpenSDA microcontroller (MK26FN2M0VM18)
U11	MIC2005-0.8YM6 (Microchip Technology)	P5V0_OSDA_OUT ^[1]	<p>See Figure 6</p> <ul style="list-style-type: none"> Power supply for P5V_REG_IN supply
J3	2x8-pin Arduino power header provides 5 V input power supply through pin 16	P5V_DC_IN	One of the sources for P5V_REG_IN
J26	CP2102 Micro-AB USB connector providing 5 V power supply	P5V_USB2	One of the sources for P5V_REG_IN
-	From P5V_REG_IN	P5V	<ul style="list-style-type: none"> Power supply for voltage regulator, LD1117 (U2) 5 V power supply for pin 12 of 2x8-pin Arduino power header (J3)

[1] P5V0_OSDA_OUT is only available from P5V0_OSDA when USB cable is connected to J12, and a correct OpenSDA firmware has been programmed into MK26FN2M0VM18 (A correct OpenSDA firmware is programmed into MK26FN2M0VM18 during MC56F80000-EVK manufacturing).

The following figure shows the power switch circuit diagram.

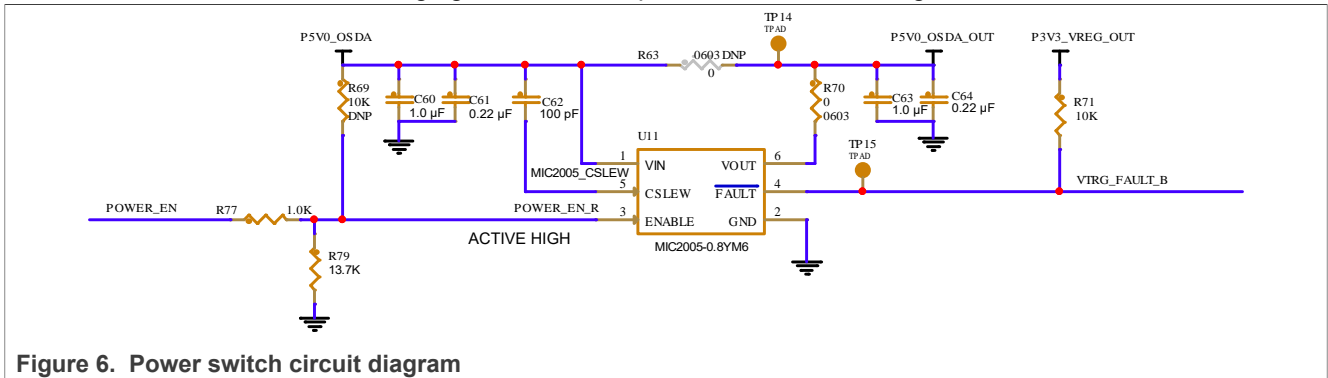


Figure 6. Power switch circuit diagram

2.1.2 3.3 V power distribution

The table below describes the 3.3 V power nodes on MC56F80000-EVK board.

Table 10. 3.3 V power nodes on MC56F80000-EVK

Part identifier	Device	Power supply voltage	Description
U2	LD1117	VDD (3.3 V)	<ul style="list-style-type: none"> Source of VDD_MCU and VDDA Power supply for voltage level translators, NTSX2102GU8H (U5), 74LVC1T45GW (U7, U8, U9, U10), and NTSX2102GU8H (U12) Power supply for FXLS8974CF accelerometer Power supply for MX25L512E SPI Flash Power supply for buttons and user-defined and PWM LEDs Power supply for pins 6 and 10 of Arduino power header (J3) and pull-up resistors on pins 20 and 18 of Arduino header (J2)
J5	2-pin header	VDD_MCU	<ul style="list-style-type: none"> Power supply for digital circuits of MC56F80748
L1	Magnetic bead	VDDA	<ul style="list-style-type: none"> Source of VDDA_MCU Power supply for Resistor Divider circuit
J6	2-pin header	VDDA_MCU	<ul style="list-style-type: none"> Power supply for analog circuits of MC56F80748 Power supply for AREF (reference voltage for Arduino header J2)
U4	MK26FN2M0VMI18	P3V3_VREG_OUT	<ul style="list-style-type: none"> Regulator output voltage of MK26FN2M0VMI18 Power supply for OpenSDA circuit Power supply for OpenSDA JTAG/SWD connector (J14) Power supply for voltage level translators, NTSX2102GU8H (U5), 74LVC1T45GW (U7, U8, U9, U10), NTSX2102GU8H (U12)

The following figure shows the VDD circuit diagram.

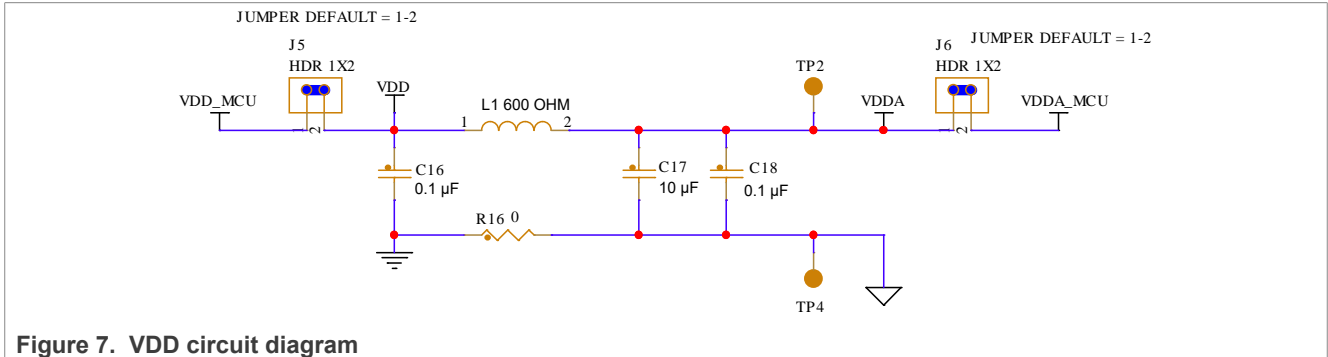


Figure 7. VDD circuit diagram

2.2 Clocking

The table below provides details of different clocks of the MC56F80000-EVK board.

Table 11. MC56F80000-EVK clocks

Clock generator	Clock specifications	Destination
Crystal oscillator, Y1	Frequency: 8 MHz	MC56F80748 MCU: <ul style="list-style-type: none"> EXTAL on MC56F80748 pin 3 (GPIOC0/EXTAL/CLKIN0) XTAL on MC56F80748 pin 4 (GPIOC1/XTAL)
Crystal oscillator, Y2	Frequency: 16 MHz	OpenSDA MCU MK26FN2M0VMI18: <ul style="list-style-type: none"> EXTAL0 on MK26FN2M0VMI18 pin N13 (PTA18/EXTAL0/FTM0_FLT2/FTM_CLKIN0/TPM_CLKIN0) XTAL0 on MK26FN2M0VMI18 pin M13 (PTA19/XTAL0/FTM1_FLT0/FTM_CLKIN1/LPTMR0_ALT1/TPM_CLKIN1)

2.3 3-axis digital sensor

The MC56F80000-EVK board supports motion sensing using NXP FXLS8974CFR3 accelerometer. FXLS8974CFR3 is a compact 3-axis MEMS accelerometer designed for use in applications that require ultra-low-power wake-up on motion.

FXLS8974CFR3 is connected to MC56F80748 through I2C interface, LPI2C. The INTF_SEL pin of FXLS8974CFR3 has been connected to GND, so that I2C interface mode is selected for this device.

The SA0 pin of the FXLS8974CFR3 device selects the least significant bit of its I2C secondary address (device address). SA0 is set to 0 by default, remove R101 to set SA0 to 1.

- When SA0 = 0, the I2C address (7-bit format) of the FXLS8974CFR3 device is set to 18h (default)
- When SA0 = 1, the I2C address (7-bit format) of the FXLS8974CFR3 device is set to 19h

Since the BT_MODE pin of the device is connected to GND, default operation mode is enabled. For more information, refer to FXLS8974CF data sheet.

The following figure shows the accelerometer circuit diagram.

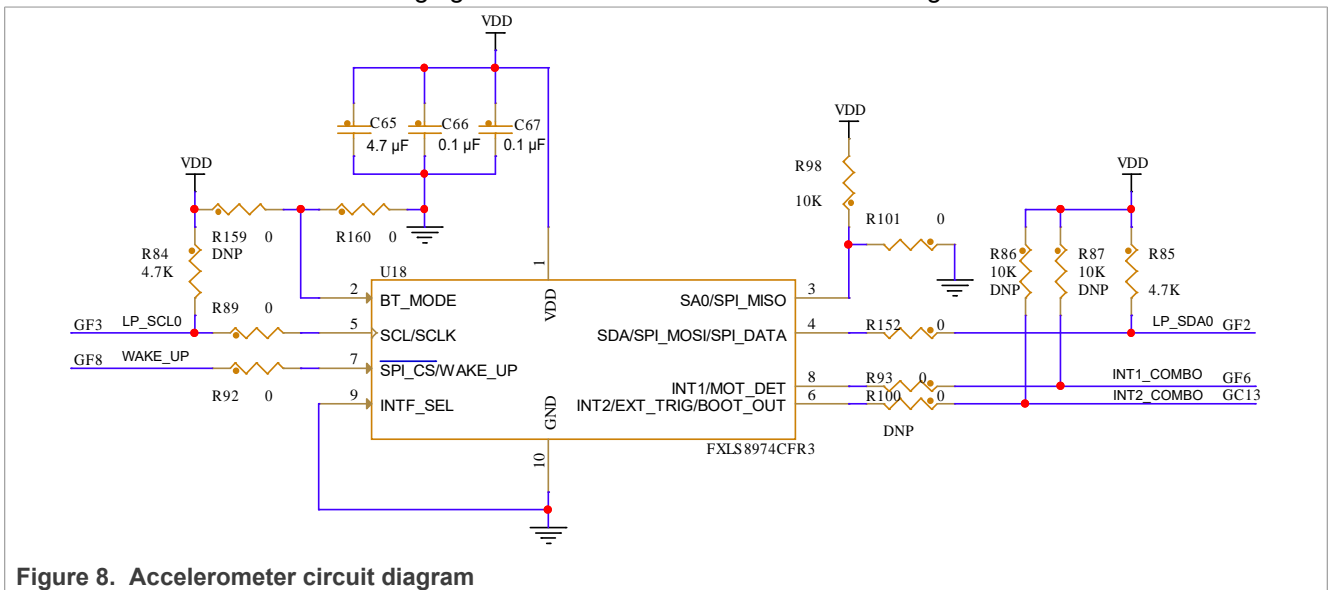


Figure 8. Accelerometer circuit diagram

Table 12. FXLS8974CFR3 pin connections

FXLS8974CFR3 pin/signal	MC56F80748 pin	Description
SCL/SCLK	GPIOF3 (LP_SCL0)	I2C serial clock
SDA	GPIOF2 (LP_SDA0)	I2C serial data
INT1/MOT_DET	GPIOF6 (INT1_COMBO)	Mode-dependent multifunction I/O pin 1. For more detail, refer to FXLS8974CF data sheet .
INT2/EXT_TRIG/BOOT_OUT	GPIOC13 (INT2_COMBO) (disconnected from GPIOC13 by default)	Mode-dependent multifunction I/O pin 2. For more detail, refer to FXLS8974CF data sheet .

2.4 SPI Flash interface

The MC56F80748 supports one queued serial peripheral interface (QSPI) controller that provides:

- Maximum of 25 Mbit/s baud rate
- Full-duplex operation
- Master and slave modes

The QSPI controller signals are multiplexed with the GPIO (Group C) pin signals.

On the MC56F80000-EVK board, QSPI controller connects to the 512 kbit Macromix MX25L512E Flash memory. The MX25L512E memory features a serial peripheral interface and the protocol that uses three bus signals: clock input (SCLK), serial data input (SI), and serial data output (SO). Serial access to the device is enabled by CS input.

The following figure shows the SPI Flash interface circuit diagram.

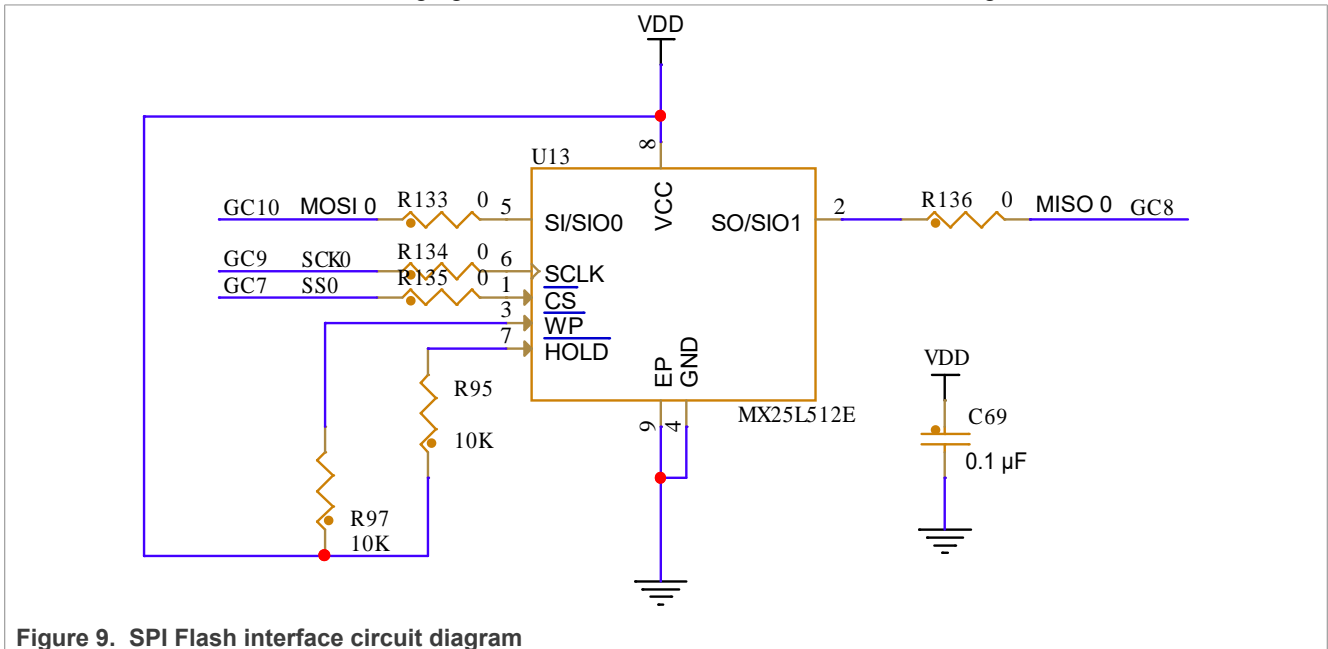


Figure 9. SPI Flash interface circuit diagram

The following table describes the MX25L512E SPI Flash pin connection with the QSPI controller of the MC56F80748.

Table 13. MX25L512E SPI Flash pin connection

MX25L512E pin/signal	MC56F80748 pin	Description
SI/SIO0	GPIOC10 (MOSI0)	Master-out Slave-in
SO/SIO1	GPIOC8 (MISO0)	Master-in slave-out
SCLK	GPIOC9 (SCK0)	Serial clock
CS	GPIOC7 (SS0)	Chip select

2.5 Resistor dividers

The three resistor dividers circuits are used on the MC56F80000-EVK board to test the ADC block functions.

- Resistor divider circuit 1
 - Thermistor RT1 is between THER_A and THER_B
 - Supports temperature from 90 °C to -20 °C
 - THER_A is connected to the GPIOA6 (ANA6) pin of MC56F80748
 - THER_B is connected to the GPIOA7 (ANA7) pin of MC56F80748
 - Voltage between THER_A and THER_B can vary from 0.372 V to 2.879 V depending on the temperature
- Resistor divider circuit 2
 - Is used to test the ANA4/ANB4 Expansion Mux of ADC control block of MC56F80748
 - Is connected to the GPIOC5 (ANB4d) pin of MC56F80748
 - Is connected to the GPIOF7 (ANA4f) pin of MC56F80748
- Resistor divider circuit 3
 - Is used to test the ANA4/ANB4 Expansion Mux of ADC control block of MC56F80748
 - Is connected to the GPIOC14 (ANB4c) pin of MC56F80748
 - Is connected to the GPIOC15 (ANA4c) pin of MC56F80748

2.6 PWM interface

The filtered PWM circuit on the MC56F80000-EVK is provided to test the function of the OPAMP, CMP, and ADC blocks of the processor.

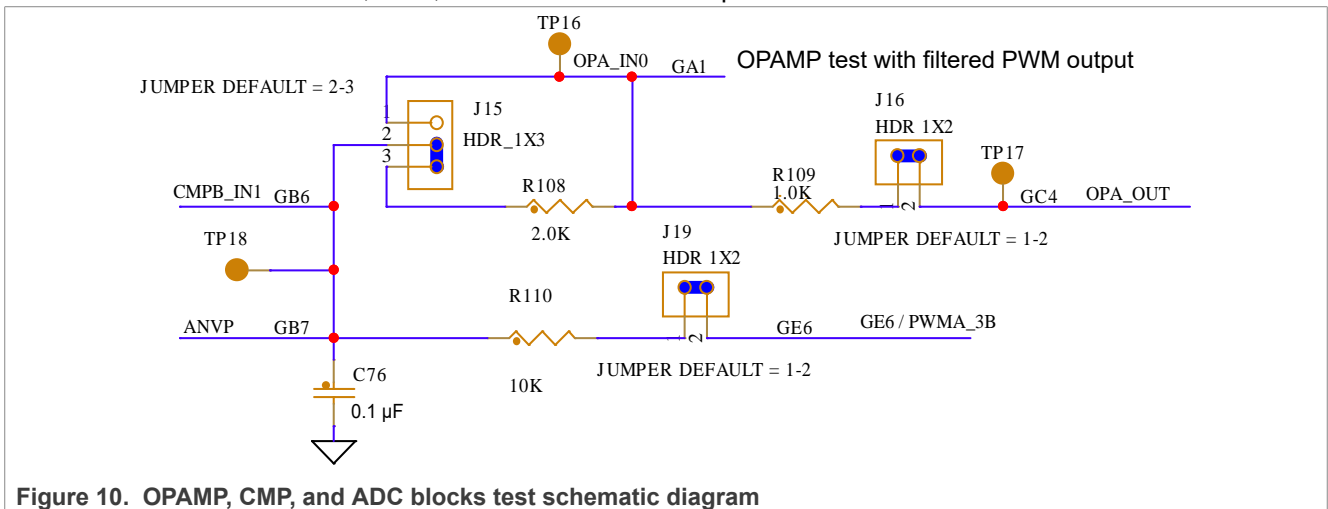


Figure 10. OPAMP, CMP, and ADC blocks test schematic diagram

The GPIOE6 (PWMA_3B) output is connected with GPIOB7 and GPIOB6 through RC filter circuit. The filtered PWM signal can be connected with GPIOA1 (OPAMPA_IN0) directly or through resistor R108 depending on jumper J15. The resistor R109, which is in between GPIOA1 (OPAMPA_IN0) and GPIOC4 (OPAMPA_OUT), can be used as OPAMP feedback resistor, if GPIOA1 is configured as OPAMP inverting input.

The following configurations can be used to test the function of the ADC, CMP, and OPAMP on this circuit.

- **CMP/ADC test configuration**
 - The GPIOE6 (PWMA_3B) can be configured to output a PWM signal. The cut-off frequency of the low-pass RC filter is 160 Hz. When the frequency of the PWM signal is much higher than the cut-off frequency, the output signal of the RC filter

is a DC signal, which can be used as ADC/CMP input signal through GPIOB6 (ANB6+CMPB_IN1) and GPIOB7 (ANB7+CMPB_IN2).

• **OPAMP test configuration**

– **PGA mode test**

When the pin 1 and pin 2 of J15 are connected, J16 is unconnected and J19 is connected, the PGA mode for OPAMP can be tested. The circuit is shown in [Figure 11](#). The low frequency PWM signal from GPIOE6 is filtered as DC signal through the RC filter, the voltage of the DC signal is $D*V_{dd}$, where D is the duty cycle of the PWM signal and V_{dd} is the voltage of the DSC power supply. The OPAMP must be configured to work at PGA mode, so the output of the OPAMP should be $Gain*D*V_{dd}$. You can select the gain through OPAMP register configuration. GPIOA1 must be configured as OPAMP non-inverting input in this case.

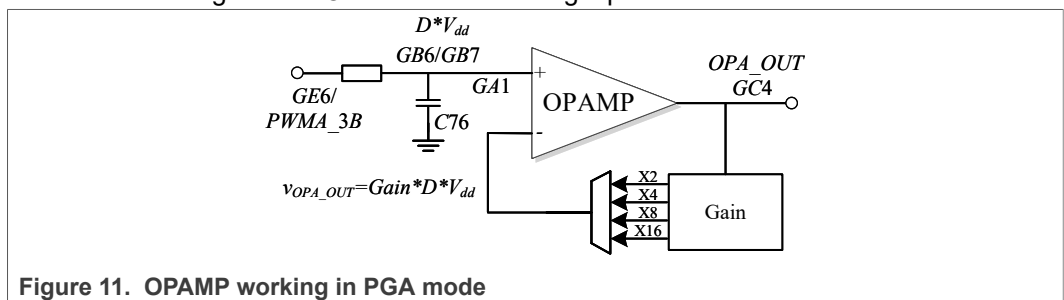


Figure 11. OPAMP working in PGA mode

– **OPAMP mode test**

When the pin 2 and pin 3 of J15 are connected, J16 and J19 are both connected, and GPIOA1 is configured as inverting input, the OPAMP mode for OPAMP can be tested. You can modify the gain of the OPAMP circuit by changing the value of the external resistors.

The equivalent circuit is shown in [Figure 12](#).

Note: The VR which is connected with the non-inverting input of the OPAMP is a DSC internal 1.2 V voltage reference, which is selected through OPAMP configuration registers.

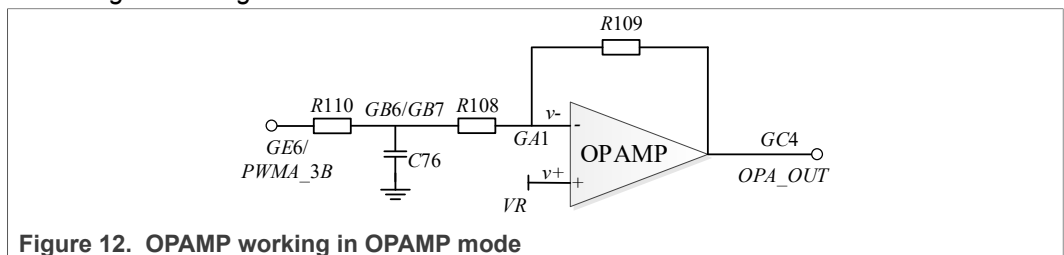


Figure 12. OPAMP working in OPAMP mode

Since the capacitor C76 filters all the AC component of the PWM signal and has no impact on the DC component, the equivalent circuit can be obtained as shown in [Figure 13](#). The capacitor is removed and the PWM input signal is seen as its DC component. And the OPAMP works at OPAMP mode, you can calculate the output of the OPAMP based on the formula in the following figure.

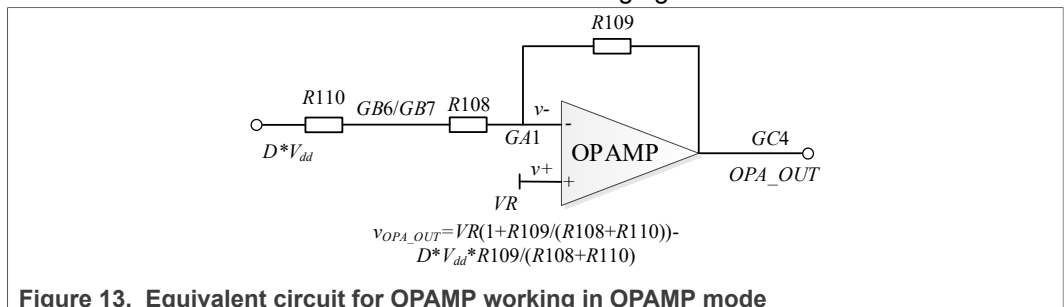


Figure 13. Equivalent circuit for OPAMP working in OPAMP mode

2.7 OPAMP test circuit

The OPAMP test circuit is designed to use the DSC internal OPAMPs together with the phase current sensing circuit of motor power stage board (FRDM-MC-LVPMSM). The FRDM-MC-LVPMSM board is connected with the EVK board through Arduino interface. You can select to use the external OPAMPs on FRDM-MC-LVPMSM or DSC internal OPAMPs for current sensing by configuring the jumpers.

The following figure shows the schematic diagram of the OPAMP test circuit.

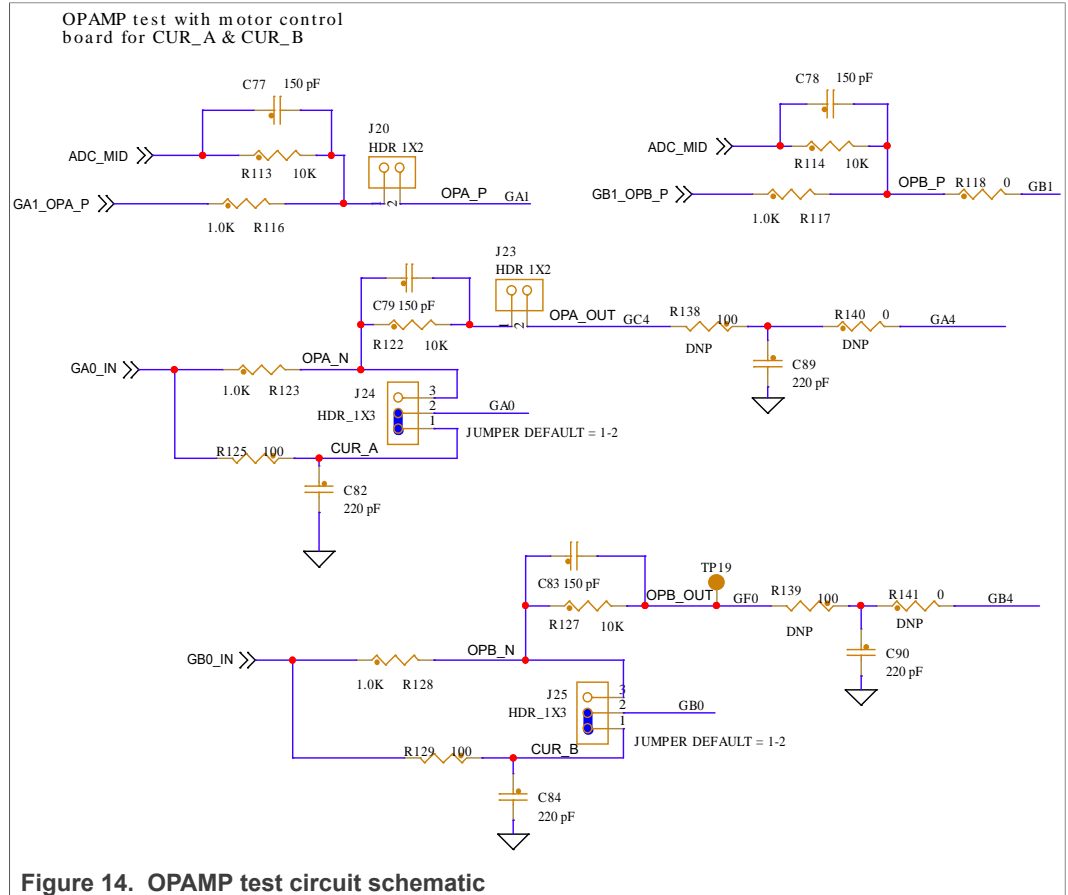


Figure 14. OPAMP test circuit schematic

• With external OPAMP (default)

In phase A current sensing circuit, when the external OPAMP on FRDM-MC-LVPMSM is used for current sensing, the jumpers configuration is described as follows. The pin 1 and pin 2 of J24 are connected, and J20 and J23 are both unconnected. The sensing signal from the output of the external OPAMP is connected with GPIOA0 (ANA0) through an RC filter. The following figure shows the equivalent circuit.

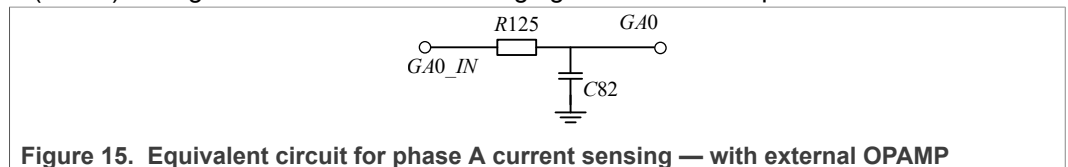


Figure 15. Equivalent circuit for phase A current sensing — with external OPAMP

For phase B current sensing, connect pin 1 and pin 2 of J25. Sensed phase B current signal is connected to GPIOB0 (ANB0) through an RC filter. Figure 16 shows the equivalent circuit.

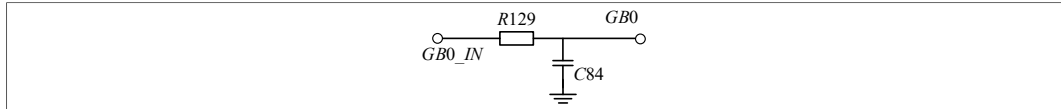


Figure 16. Equivalent circuit for phase B current sensing — with external OPAMP

• **With DSC internal OPAMP**

In phase A current sensing circuit, when the DSC internal OPAMP is used for current sensing, the jumpers configuration is described as follows.

The pin 2 and pin 3 of J24 are connected, and J20 and J23 are both connected. The equivalent circuit is shown in Figure 17. In this condition, GA0_IN and GA1_OPA_P are signals at both sides of the shunt resistor, and ADC_MID is a bias voltage, which makes sure the output of the OPAMP is a positive value and the typical value is 1.65 V. GA0_IN is connected with GPIOA0 (OPAMPA_IN3) through R123, GPIOA0 (OPAMPA_IN3) is configured as inverting input of the OPAMPA. GA1_OPA_P and ADC_MID are connected with GPIOA1 (OPAMPA_IN0) through R116 and R113, respectively. GPIOA1 (OPAMPA_IN0) is configured as non-inverting input of the OPAMPA. The R122 is between GPIOA0 (OPAMPA_IN3) and GPIOC4 (OPAMPA_OUT), and GPIOC4 (OPAMPA_OUT) is used as output of the OPAMPA. Therefore, R122 is a negative feedback resistor. The signal of the GPIOC4 (OPAMPA_OUT) is the phase A current sensing signal.

The OPAMPA output signal OPA_OUT on GPIOC4 can be connected with ANA7 directly within DSC though ADC register configuration. RC filter can also be added between the OPAMP and the ADC input when R138 and R140 are soldered, which is not populated by default. In this case, the filtered OPAMP output signal is connected with GPIOA4 (ANA4). If a 0 Ω resistor is soldered at the R138 position, and R140 is DNP, C89 is connected with the OPAMPA output directly, which can reduce the noise too.

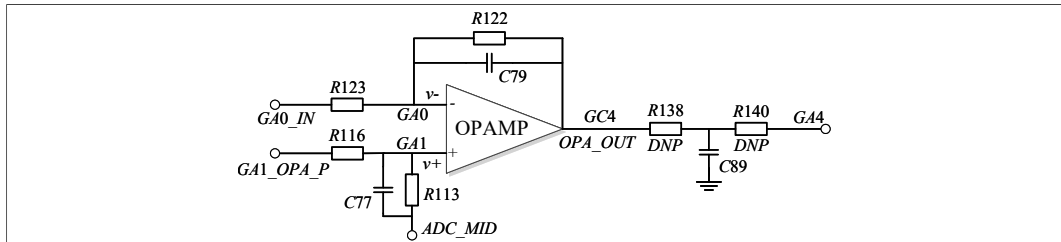


Figure 17. Equivalent circuit for phase A current sensing — with DSC internal OPAMP

The circuit designed for phase B current sensing is similar as phase A current sensing circuit, connect pin 2 and pin 3 of J25, and the equivalent circuit is shown in Figure 18.

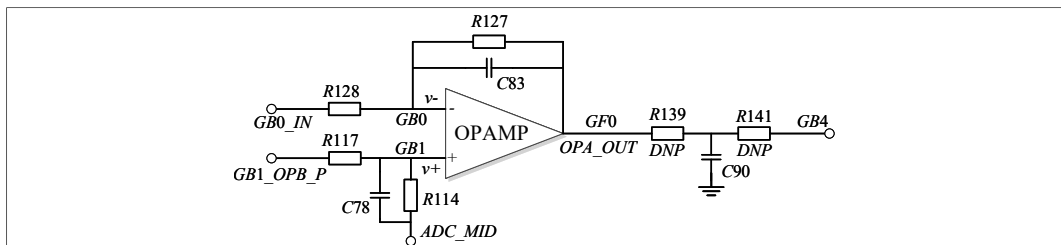


Figure 18. Equivalent circuit for phase B current sensing — with DSC internal OPAMP

2.8 OpenSDA

OpenSDA is a serial and debug adapter circuit. It bridges serial and debug communications between the USB host and the target processor MC56F80748.

The OpenSDA circuit is based on the NXP Kinetis K26 family microcontroller (MK26FN2M0VMI18) with 2 MB of embedded flash and an integrated USB controller. OpenSDA comes preloaded with the firmware, which provides a debug protocol interface and a virtual serial port interface.

The OpenSDA circuit provides a JTAG debug interface to MC56F80748. A standard USB A male to micro B male cable is used for debugging via the USB connector (J12).

USB drivers for this onboard OpenSDA circuit are available in the host PC once the latest CodeWarrior IDE or any P&E tools that support DSC have been installed.

For details about the JTAG connector, see [Section 1.8](#).

The following table describes the OpenSDA signals connected to the target MCU (MC56F80748).

Table 14. OpenSDA interface signals

OpenSDA signals	MC56F80748 pin	Description
SDA_RST_TGTMCU	GPIOD4 (RESET_MCU)	Reset to target MCU
OPENSDA_UART_RX	GPIOC2 (Boot_TXD0)	Function = TXD0; Peripheral = SCI0; Direction = IO
OPENSDA_UART_TX	GPIOC3 (Boot_RXD0)	Function = RXD0; Peripheral = SCI0; Direction = I
SDA_SWD_SWO	GPIOD1 (TGTMCU_TDO)	Test data out
SDA_SWD_SCK	GPIOD2 (TGTMCU_TCK)	Test clock
SDA_SWD_DOUT	GPIOD3 (TGTMCU_TMS)	Test mode select
SDA_SWD_DOUT_TDI	GPIOD0 (TGTMCU_TDI)	Test data in

2.9 Input/output headers

The MC56F80748 microcontroller is packaged in a 64-pin QFP package. Some pins are utilized in onboard circuitry, however, many are directly connected to one of four I/O headers (J1, J2, J3, and J4), which are also compatible with Arduino R3 pin layout.

The following tables describe the MC56F80000-EVK Arduino connectors pinout.

Table 15. J2 (2x10-pin) connector pinout

Pin	Signal	Pin	Signal
2	GPIOF6	1	GA0_IN (CUR_A/CS_A_H)
4	GPIOE6 (GE6/PWMA_3B)	3	GB0_IN (CUR_B/CS_B_H)
6	GPIOE7 (GE7/PWMA_3A)	5	GA3/GB3_RC (CUR_C)
8	GPIOC10 (MOSI0/XB_OUT9)	7	GA2_RC (VOLT_DCB)
10	GPIOC8 (MISO0)	9	GB2_RC (CUR_DCB)
12	GPIOC9 (SCK0)	11	GA1_OPA_P (CS_A_L)
14	GND	13	GB1_OPB_P (CS_B_L)
16	AREF	15	ADC_MID
18	GPIOF2 (LP_SDA0)	17	Not connected
20	GPIOF3 (LP_SCL0)	19	Not connected

Table 16. J1 (2x8-pin) connector pinout

Pin	Signal	Pin	Signal
2	GPIOC12 (RXD1)	1	Not connected
4	GPIOC11 (TXD1)	3	GPIOC6 (ENC_I/XB_IN3)
6	GPIOF5 (GF5/XB_OUT9)	5	Not connected
8	GPIOF4 (GF4/XB_OUT8)	7	Not connected
10	GPIOC4/OPA_OUT	9	Not connected
12	GPIOC15 (ANA4c)	11	Not connected
14	GPIOC7 (SS0/XB_OUT6)	13	Not connected
16	GPIOC5 (ANB4d)	15	Not connected

Table 17. J3 (2x8-pin) connector pinout

Pin	Signal	Pin	Signal
2	Not connected	1	GPIOF1 (ENC_B/XB_IN7)
4	VDD	3	GPIOE7 (ENC_A/XB_IN5)
6	GD4 (RESET)	5	GPIOE4/PWMA_2B
8	VDD	7	GPIOE5/PWMA_2A
10	P5V	9	GPIOE2/PWMA_1B
12	GND	11	GPIOE3/PWMA_1A
14	GND	13	GPIOE0/PWMA_0B
16	P5V_DC_IN	15	GPIOE1/PWMA_0A

Table 18. J4 (2x6-pin) connector pinout

Pin	Signal	Pin	Signal
2	ANA3/B3	1	Not connected
4	GPIOA4 (ANA4)	3	Not connected
6	GPIOA5 (ANA5)	5	Not connected
8	GPIOB1 (ANB1)	7	Not connected
10	GPIOB4 (ANB4)	9	Not connected
12	GPIOB5 (ANB5)	11	Not connected

2.10 Arduino compatibility

The Input/Output headers (J1, J2, J3, J4) on the MC56F80000-EVK board are arranged to enable compatibility with peripheral boards (known as shields) that connect to Arduino and Arduino-compatible microcontroller boards. The outer rows of pins (even-numbered pins) on the headers share the same mechanical spacing and placement with the I/O headers on the Arduino Revision 3 (R3) standard.

2.11 USB-to-UART interface

The MC56F80000-EVK board supports the USB-to-UART function through OpenSDA circuit and CP2102N device.

- **OpenSDA circuit** — The OpenSDA microcontroller MK26FN2M0VMI18 provides a virtual COM between the host computer and MC56F80748 through USB port (J12) by using SCI0 on MC56F80748.

The MC56F80748 features two high-speed queued serial communication interface (QSCI) modules (SCI0 and SCI1) with LIN slave functionality. The SCI allows asynchronous serial communications with peripheral devices.

On MC56F80000-EVK, the signals used in asynchronous serial communication between the OpenSDA processor and MC56F80748 are voltage translated from P3V3_VREG_OUT to VDD and vice versa using the NTSX2102GU8H (U12) voltage translator.

The following table describes the signal mapping between OpenSDA and target MCU (MC56F80748) connected through SCI0 interface.

Table 19. Signal mapping between OpenSDA and DSC using SCI0 interface

OpenSDA	MC56F80748	Description
Signal	Signal	
OPENSDA_UART_TX	GPIOC3	GPIOC3 is configured as RXD function of SCI0.
OPENSDA_UART_RX	GPIOC2	GPIOC2 is configured as TXD function of SCI0.

- **CP2102N USB-to-UART bridge controller** — Not populated by default. The device provides a virtual COM interface between the host computer and MC56F80748 through USB port (J26) by using SCI1 on MC56F80748. The CP2102N device includes a USB 2.0 full-speed function controller, USB transceiver, oscillator, and universal asynchronous receiver/transmitter (UART) in a small package.

Note:

The CP2102N device requires installing the virtual COM port (VCP) device drivers that can be downloaded from <https://www.silabs.com/developers/usb-to-uart-bridge-vcp-drivers?tab=downloads>. After the driver for CP2102N is installed, the host computer will enumerate COM ports when the USB cable is plugged into the J26 USB port. This makes the device appear as a VCP. You can use these ports to communicate with the processor with USB interface via a standard PC serial emulation port (for example, Putty and Tera Term).

The following figure shows the circuit diagram of CP2102N USB-to-UART device using SCI1 interface.

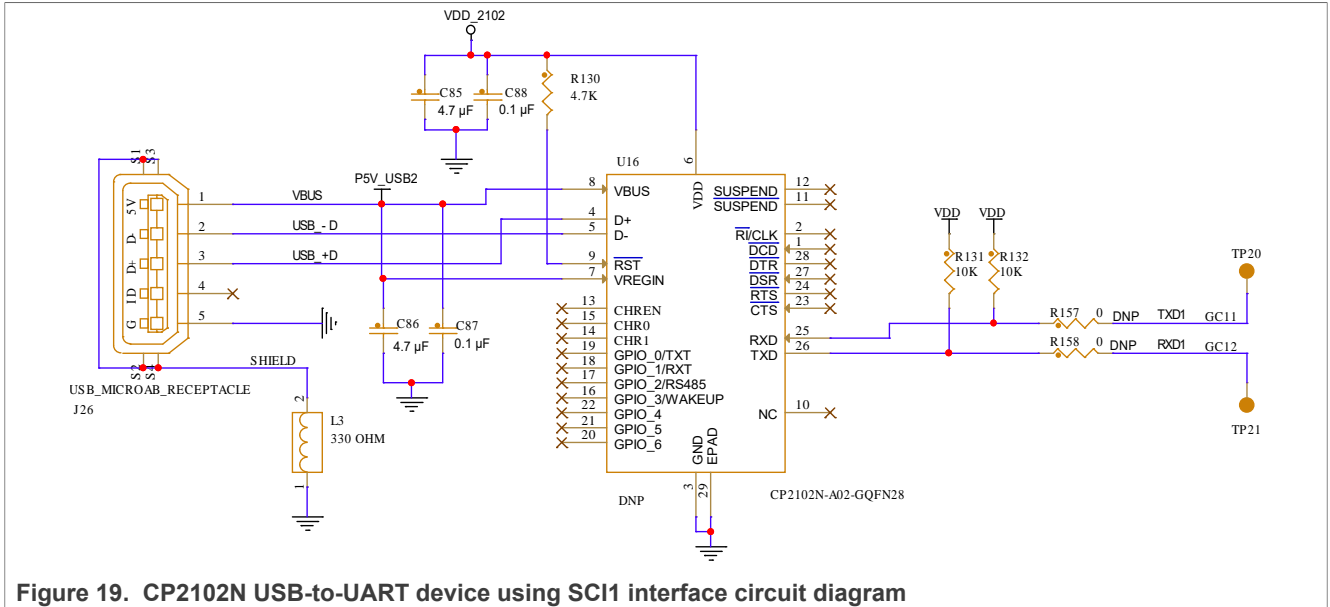


Figure 19. CP2102N USB-to-UART device using SCI1 interface circuit diagram

Table 20. CP2102N pin connections

CP2102N pin	MC56F80748 pin	Description
RXD	GPIOC11 (TXD1)	QSCI1 transmit data output on DSC
TXD	GPIOC12 (RXD1)	QSCI1 receive data input on DSC

2.12 Debug

2.12.1 JTAG interface

The MC56F80748 processor has five GPIO pins multiplexed with the four JTAG signals and one reset signal. The reset signal and JTAG signals used by the processor are:

- RESETB input (default signal on GPIOD4 pin)
- TMS input (default signal on GPIOD3 pin)
- TCK input (default signal on GPIOD2 pin)
- TDO output (default signal on GPIOD1 pin)
- TDI input (default signal on GPIOD0 pin)

The GPIOD[4:0] signals are connected on the MC56F8000-EVK board to the 14-pin JTAG connector (J10).

The following table describes the JTAG header pinout.

Table 21. JTAG header (J10) pinout

Pin number	Signal name	Description
1	GPIOD0/TDI	TAP data In
2	GND	Ground
3	GPIOD1/TDO	TAP data out
4	GND	Ground
5	GPIOD2/TCK	TAP clock

Table 21. JTAG header (J10) pinout...continued

Pin number	Signal name	Description
6	GND	Ground
7	-	Not connected
8	-	Not connected
9	GPIOD4/RESET	Reset signal
10	GPIOD3/TMS	TAP machine state
11	VDD	Power supply
12	-	Not connected
13	VDD	Power supply
14	-	Not connected

2.12.2 OpenSDA debug interface

The MC56F80000-EVK board supports onboard OpenSDA debugging.

The below table describes the signals and peripherals used for OpenSDA JTAG interface.

Table 22. OpenSDA JTAG interface

OpenSDA processor			Voltage translator, 74 LVC1T45GW, part identifier	Jumper configuration	Target processor		Description
JTAG signal	Direction control / Enable signal	Voltage			Signal	Voltage	
SDA_SWD_SCK	SDA_SWD_EN	P3V3_VREG_OUT	U7	J13: short pin 1-2	GPIOD2/TCK	VDD	TAP clock
SDA_SWD_DOUT	SDA_SWD_OE	P3V3_VREG_OUT	U8	J13: short pin 3-4	GPIOD3/TMS	VDD	TAP machine state
SDA_SWD_DOUT_TDI	SDA_SWD_EN	P3V3_VREG_OUT	U9	J13: short pin 5-6	GPIOD0/TDI	VDD	TAP data in
SDA_SWD_SWO	GND	P3V3_VREG_OUT	U10	J13: short pin 7-8	GPIOD1/TDO	VDD	TAP data out
SDA_RST_TGTMCU	SDA_LVLRST_EN	P3V3_VREG_OUT	U5	J11: short pin 1-2	GPIOD4/RESET	VDD	For Jumper 11 setting detail, see Section 1.9

3 Revision history

The table below summarizes the revisions to this document.

Table 23. Revision history

Revision	Date	Topic cross-reference	Change description
1	14 December 2022	-	Initial public release

4 Legal information

4.1 Definitions

Draft — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

4.2 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Suitability for use in non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

Translations — A non-English (translated) version of a document, including the legal information in that document, is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Security — Customer understands that all NXP products may be subject to unidentified vulnerabilities or may support established security standards or specifications with known limitations. Customer is responsible for the design and operation of its applications and products throughout their lifecycles to reduce the effect of these vulnerabilities on customer's applications and products. Customer's responsibility also extends to other open and/or proprietary technologies supported by NXP products for use in customer's applications. NXP accepts no liability for any vulnerability. Customer should regularly check security updates from NXP and follow up appropriately. Customer shall select products with security features that best meet rules, regulations, and standards of the intended application and make the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP.

NXP has a Product Security Incident Response Team (PSIRT) (reachable at PSIRT@nxp.com) that manages the investigation, reporting, and solution release to security vulnerabilities of NXP products.

4.3 Trademarks

Notice: All referenced brands, product names, service names, and trademarks are the property of their respective owners.

NXP — wordmark and logo are trademarks of NXP B.V.

CodeWarrior — is a trademark of NXP B.V.

Kinetis — is a trademark of NXP B.V.

Contents

1	Overview	2
1.1	Acronyms	2
1.2	Related documentation	3
1.3	Board kit contents	3
1.4	Block diagram	4
1.5	Board pictures	4
1.6	Board features	6
1.7	Push-button switches	7
1.8	Connectors	8
1.9	Jumpers	8
1.10	LEDs	10
2	MC56F80000-EVK functional description	11
2.1	Power supplies	11
2.1.1	5 V power sources	11
2.1.2	3.3 V power distribution	12
2.2	Clocking	13
2.3	3-axis digital sensor	14
2.4	SPI Flash interface	15
2.5	Resistor dividers	15
2.6	PWM interface	16
2.7	OPAMP test circuit	18
2.8	OpenSDA	19
2.9	Input/output headers	20
2.10	Arduino compatibility	21
2.11	USB-to-UART interface	21
2.12	Debug	23
2.12.1	JTAG interface	23
2.12.2	OpenSDA debug interface	24
3	Revision history	24
4	Legal information	25

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.
