Product Change Notification / SYST-30JOVN709

Date:

31-Jan-2023

Product Category:

Ethernet PHYs

PCN Type:

Document Change

Notification Subject:

ERRATA - LAN8670/1/2 10BASE-T1S Ethernet PHY Transceiver Silicon Errata and Data Sheet Clarifications

Affected CPNs:

SYST-30JOVN709_Affected_CPN_01312023.pdf
SYST-30JOVN709_Affected_CPN_01312023.csv

Notification Text:

SYST-30JOVN709

Microchip has released a new Errata for the LAN8670/1/2 10BASE-T1S Ethernet PHY Transceiver Silicon Errata and Data Sheet Clarifications of devices. If you are using one of these devices please read the document located at LAN8670/1/2 10BASE-T1S Ethernet PHY Transceiver Silicon Errata and Data Sheet Clarifications.

Notification Status: Final

Description of Change: Added Data Sheet Clarification section

Impacts to Data Sheet: None

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 31 January 2023

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachments:

LAN8670/1/2 10BASE-T1S Ethernet PHY Transceiver Silicon Errata and Data Sheet Clarifications

Please contact your local Microchip sales office with questions or concerns regarding this notification.

Terms and Conditions:

If you wish to receive Microchip PCNs via email please register for our PCN email service at our PCN home page select register then fill in the required fields. You will find instructions about registering for Microchips PCN email service in the PCN FAQ section.

If you wish to change your PCN profile, including opt out, please go to the PCN home page select login and sign into your myMicrochip account. Select a profile option from the left navigation bar and make the applicable selections.

Affected Catalog Part Numbers (CPN)

LAN8670B1-E/LMX
LAN8672B1-E/LNX
LAN8671B1-E/U3B
LAN8670B1T-E/LMX
LAN8672B1T-E/LNX
LAN8671B1T-E/U3B

LAN8670/1/2

Silicon Errata and Data Sheet Clarifications

The LAN8670/1/2 devices that you have received conform functionally to the Device Data Sheet (DS60001573C), except for the anomalies described in this document.

The issues discussed in the following pages are for hardware revisions listed in Table 1. The silicon issues are summarized in Table 2. Items relating to data sheet changes are summarized in Table 3 of the Data Sheet Clarifications section.

TABLE 1: SILICON PART ID AND HARDWARE REVISION VALUES

Part Number	Part ID [1]	Hardware Revision [1]	Package Marking
LAN8670	010110	0010	B1
LAN8671	010110	0010	B1
LAN8672	010110	0010	B1

Note 1: The Part ID and Hardware Revision are located in the PHY_ID1 register Model Number and Revision Number fields, respectively.

FIGURE 1: TOP MARKING FOR LAN8670 DEVICE

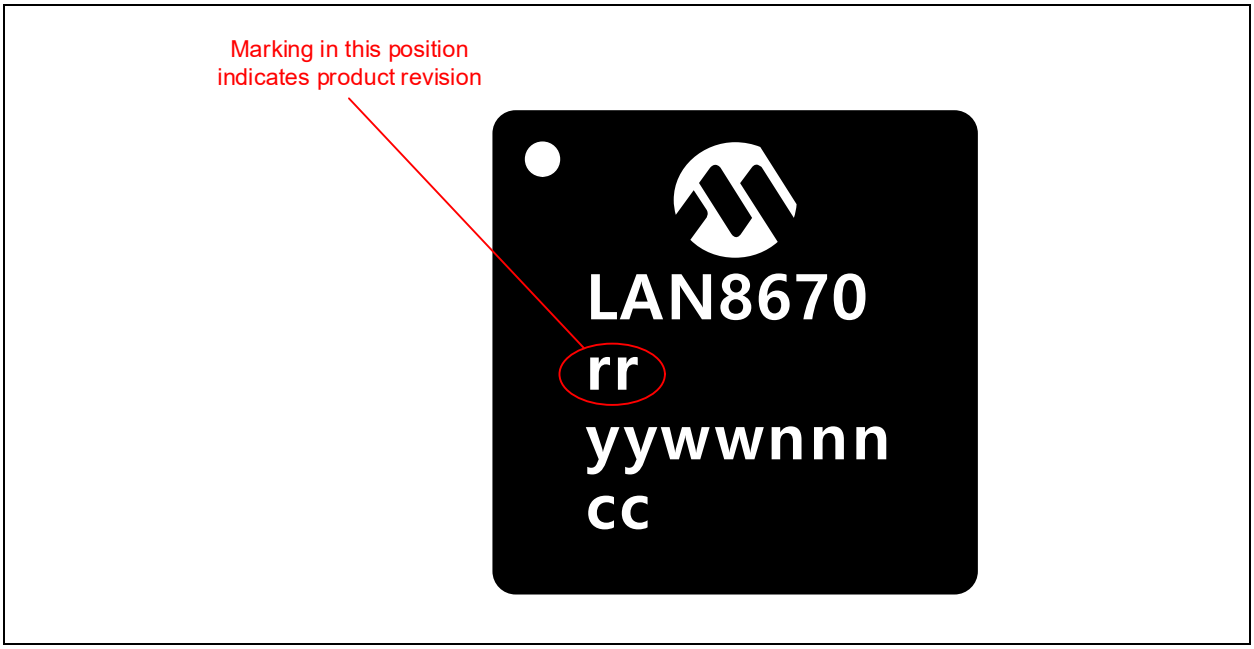


FIGURE 2: TOP MARKING FOR LAN8671 DEVICE

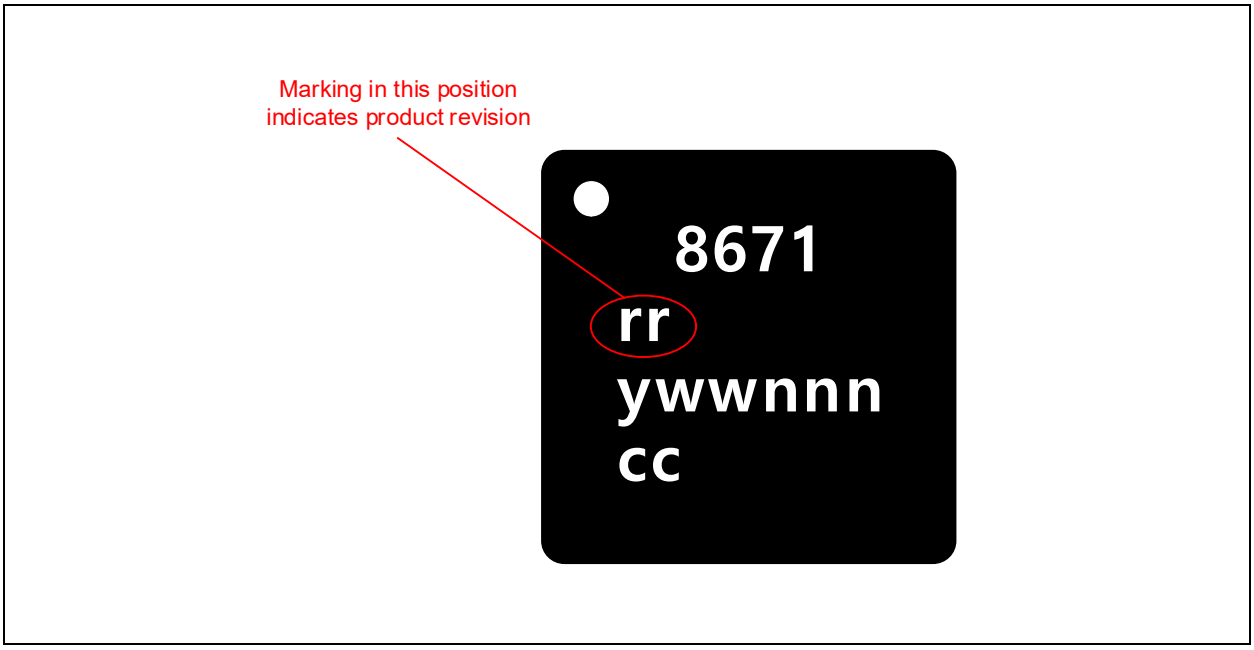


FIGURE 3: TOP MARKING FOR LAN8672 DEVICE

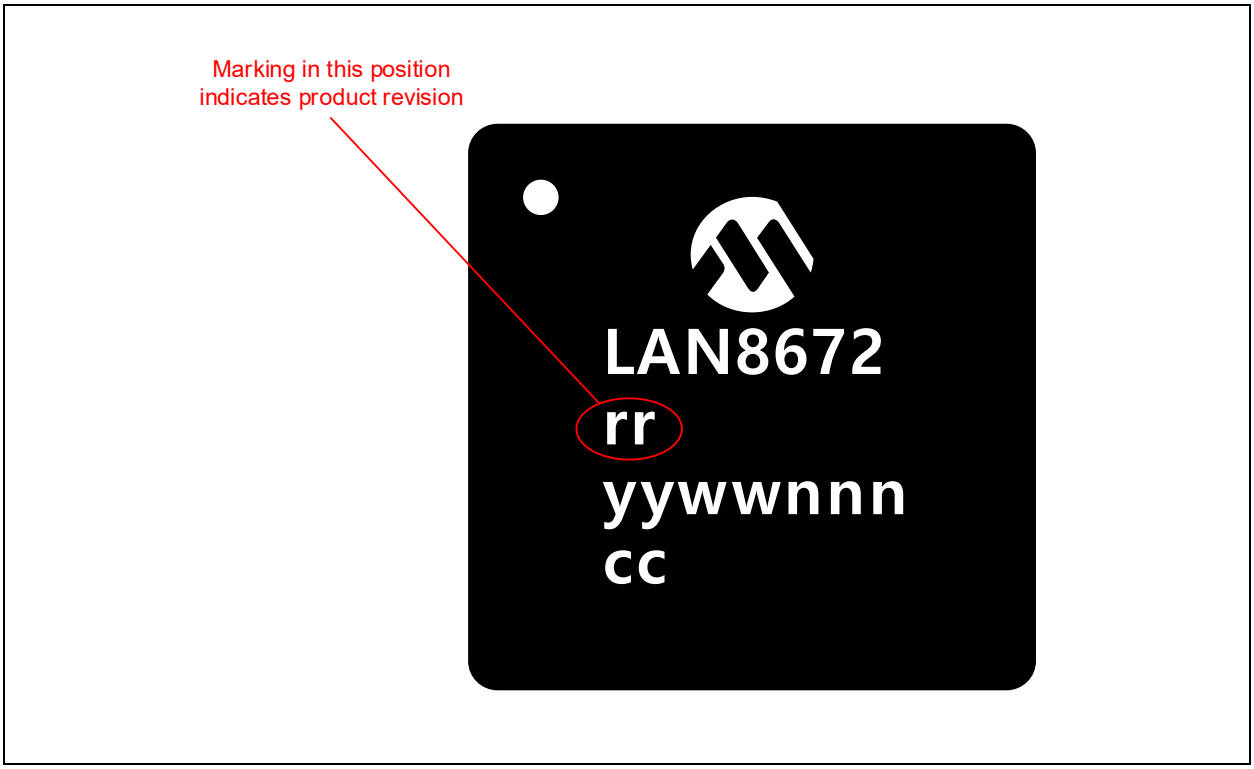


TABLE 2: SILICON ISSUE SUMMARY

Item Number	Issue Summary	Affected Devices		
		LAN8670	LAN8671	LAN8672
		Rev B1	Rev B1	Rev B1
s1.	Media interface mode (RMII) identification	-	X	-
s2.	Package Type identification	-	X	-
s3.	RMII CSMA/CD operation in mixed PLCA segments	X	X	-
s4.	Incorrect reset indication on IRQ_N	X	X	X
s5.	Multi-coordinator PLCA action	X	X	X
s6.	Transmission of collision fragments with PLCA and RMII	X	X	-
s7.	Detection of late collisions with PLCA and RMII	X	X	-
s8.	Revert to CSMA/CD when PLCA Beacons are missing	X	X	X

Legend

- \- Erratum is not applicable.
- X Erratum is applicable.

Silicon Errata Issues:

s1. Module: Media interface mode (RMII) identification

DESCRIPTION

The Media Interface Type (MITYP) field of the Strap Control 0 (STRAP_CTRL0) register does not properly indicate that RMII is active on the LAN8671. When reading the Media Interface Type field, the LAN8671 will return a random value.

END USER IMPLICATIONS

The station management entity cannot read the Media Interface Type field of the LAN8671 to determine the operating mode of the media interface.

Work Around

The LAN8671 only supports RMII operation. The station management entity should read the Package Type (PKGTYP) field of the Strap Control 0 register to determine the specific device that is used and assume RMII operation for the LAN8671.

PLAN

This erratum will be corrected in a future revision.

s2. Module: Package Type identification

DESCRIPTION

The Package Type (PKGTYP) field of the Strap Control 0 (STRAP_CTRL0) register does not always return the correct value for the LAN8671. When reading the Package Type field, the LAN8671 will return a value of 00b or 10b.

END USER IMPLICATIONS

The station management entity cannot reliably read the Package Type field to determine the device.

Work Around

The station management entity should interpret Package Type values of 00b or 10b as the LAN8671.

PLAN

This erratum will be corrected in a future revision.

s3. Module: RMII CSMA/CD operation in mixed PLCA segments

DESCRIPTION

The LAN8670/1 RMII cannot be operated with PLCA disabled on a network with other PLCA-enabled nodes. When the device is configured for CSMA/CD operation (i.e., PLCA is disabled), then the reception of PLCA BEACON and COMMIT symbols from the network will be improperly transferred via the RMII to the MAC resulting in undefined behavior including dropped packets.

The LAN8672 does not support RMII operation.

END USER IMPLICATIONS

The RMII may only be used with PLCA disabled when all other nodes on the mixing segment are also configured for pure CSMA/CD operation.

Work Around

None.

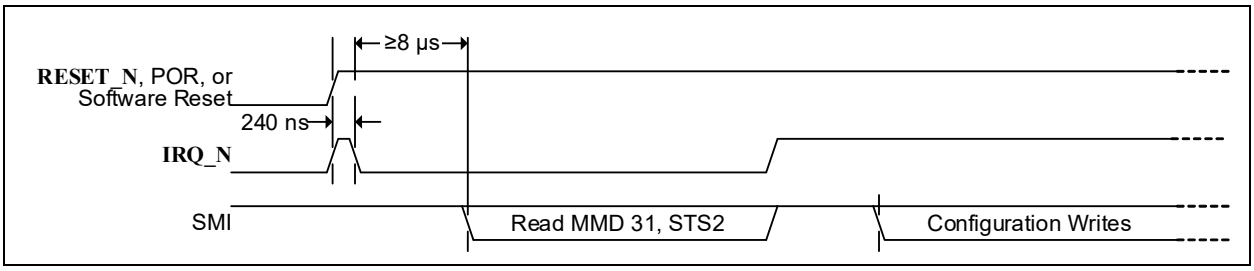
PLAN

This erratum will be corrected in a future revision.

s4. Module: Incorrect reset indication on IRQ_N

DESCRIPTION

The device does not properly assert the IRQ_N pin to interrupt the station management entity once it has been reset. The device should allow the IRQ_N pin to be pulled high when it is in reset and only assert IRQ_N low once it is ready for initialization by the station management entity. However, the device will assert IRQ_N low during reset. Once the device reset is deasserted, the IRQ_N pin will become deasserted for about 240 ns. The station management entity can only attempt communication with the device 8 µs following reset.



END USER IMPLICATIONS

When the device has been reset, the station management entity cannot immediately communicate with the device.

The station management entity will receive a false interrupt indication on IRQ_N when the device is reset. This may result in a failure to communicate with the device.

Work Around

The station management entity must wait at least 8 µs following reset to communicate with the device.

PLAN

This erratum will be corrected in a future revision.

s5. Module: Multi-coordinator PLCA action

DESCRIPTION

When operating as a PLCA Coordinator, if the PHY receives an unexpected BEACON from an additional coordinator on the segment, it will set the Unexpected BEACON Received (UNEXPB) bit in the Status 1 (STS1) register. The PHY will then enter a recovery state in which it can receive packets but will transmit neither packets nor BEACONs for the next two PLCA bus cycles. Should the duplicate Coordinator continue sending periodic BEACONs, then the PHY will remain in the recovery state unable to transmit to avoid collisions with the duplicate Coordinator in Transmit Opportunity 0.

Clause 148 of the IEEE 802.3cg-2019™ specification describes that when this condition occurs, the PHY should avoid transmitting in its transmit opportunity until the end of the current bus cycle when the PHY will again transmit its BEACON to the segment.

END USER IMPLICATIONS

The PHY will halt transmitting packets and BEACONs to the network when configured as a PLCA Coordinator and an unexpected BEACON is detected. This results in the node becoming an inactive Coordinator.

Work Around

The station management entity should monitor the Unexpected BEACON Received bit and configure the PHY as a PLCA Follower.

PLAN

This erratum will be corrected in a future revision.

s6. Module: Transmission of collision fragments with PLCA and RMII

DESCRIPTION

Clause 4 of the IEEE Std 802.3-2018™ specifies the MAC shall implement an Inter-Packet Gap (IPG) delay of 96 bit times (BT) between packets. This IPG is split into two parts. The first part, IPG part 1, requires that no carrier be sensed. If carrier is sensed during IPG part 1, then the timer is restarted. Once IPG part 1 is complete, the MAC may transmit following IPG part 2. The IPG part 1 is nominally 64 BT, but may be less, including zero. The IPG part 2 timing is nominally 32 BT, but is always equal to the full IPG duration minus the IPG part 1.

Some MACs implement an IPG part 1 of very small duration. If the IPG part 1 time is too small, then the MAC may attempt to transmit after the PHY has asserted carrier indication with CRSDV. The result is that the MAC will quickly detect a collision and send a collision fragment to the PHY. When PLCA is enabled, the PHY, not expecting the MAC to transmit after carrier was indicated, will not detect the collision and end up transmitting the collision fragment to the network.

END USER IMPLICATIONS

Use of a MAC with an IPG part 1 time of less than 18 bits will result in the transmission of short 10.4 µs packets onto the network.

Work Around

While the transmission of the collision fragments to the network are benign, they may be eliminated by reducing the size of the PLCA delay line buffer with the register configuration provided below. This will cause the PHY detecting a normal logical collision preventing the transmission of the collision fragment. Additionally, the PHY will capture the next transmit opportunity guaranteeing the MAC the ability to transmit according to the PLCA algorithm.

Access	MMD	Address	Data	Mask
RMW	0x1F	0x008F	0x00D0	0x07F0

Legend:
R - Read
W - Write
RMW - Read-Modified Write

PLAN

This erratum will be corrected in a future revision.

s7. Module: Detection of late collisions with PLCA and RMII

DESCRIPTION

Clause 4 of the IEEE Std 802.3-2018 specifies the MAC shall implement an Inter-Packet Gap (IPG) delay of 96 bit times (BT) between packets. This IPG is split into two parts. The first part, IPG part 1, requires that no carrier be sensed. If carrier is sensed during IPG part 1, then the timer is restarted. Once IPG part 1 is complete, the MAC may transmit following IPG part 2. The IPG part 1 is nominally 64 BT, but may be less, including zero. The IPG part 2 timing is nominally 32 BT, but is always equal to the full IPG duration minus the IPG part 1.

Some MACs implement an IPG part 2 duration of longer than 32BT. In this case the MAC may attempt to transmit longer after carrier indication than the PHY has expected. This results in an incorrect carrier sense indication to the MAC which, if the MAC attempts to transmit again, may lead to a late collision.

END USER IMPLICATIONS

Use of a MAC with an IPG part 2 time of greater than 32 bits may result in the PHY asserting a late collision to the MAC.

Work Around

Please contact your Microchip support with details of the MAC being used and its Inter-Packet Gap timing for details on resolving this issue.

PLAN

This erratum will be corrected in a future revision.

s8. Module: Revert to CSMA/CD when PLCA Beacons are missing

DESCRIPTION

Clause 148 of IEEE 802.3cg-2019 specifies the behavior of PLCA Follower nodes when the BEACONs from the Coordinator are no longer regularly received. If BEACONs are not received by the device it will continue incrementing its transmit opportunity counter. When the transmit opportunity counter reaches the maximum count of 255, it will then stop incrementing and a 13 ms timer started. If no BEACON is received after the timer expires, the PLCA Status bit will be cleared. When the PLCA Status bit is zero, the device will revert to CSMA/CD operation with PLCA deactivated.

The device does not properly revert to CSMA/CD operation in this condition. It will indicate the lack of received BEACONs by asserting the PLCA Status (PST) bit in the PLCA Status (PLCA_STS) register, however, it will not deactivate PLCA and revert to CSMA/CD operation.

END USER IMPLICATIONS

When BEACONs from the PLCA coordinator are no longer regularly received, the PHY will not properly revert to CSMA/CD operation, as specified, and will no longer transmit packets to the network.

Work Around

The station management entity (STA) should monitor the PLCA Status (PST) bit in the PLCA Status (PLCA_STS) register. When the PST bit is set, the STA should disable PLCA to manually revert to CSMA/CD operation. While in CSMA/CD operation, the STA should monitor the PLCA Symbols Detected (PLCASYM) bit in the Status 1 (STS1) register. When PLCASYM is set, it indicates the detection of PLCA BEACON symbols received when PLCA is disabled. The STA may then re-enable PLCA.

PLAN

This erratum will be corrected in a future revision.

TABLE 3: DATA SHEET CLARIFICATION SUMMARY

Item Number	Port/Function	Issue Summary	Resolved with Data Sheet Revision
d1.	Table 3-7. Miscellaneous Pins	The table incorrectly states that clock oscillators may be used in MII mode.	TBD
d2.	Section 4.1 Media Independent Interface (MII)	Text does not clearly state that a crystal must be used in MII mode.	TBD
d3.	Section 4.8.1 Crystal Pins (XTI/XTO)	Text incorrectly states that clock oscillators may be used in MII mode.	TBD
d4.	Figure 4-4. Crystal Oscillator Input	Figure incorrectly states that clock oscillators may be used in MII mode.	TBD
d5.	Table 7-7. DC Electrical Characteristics (other than 10BASE-T1S PMA)	Note 3 incorrectly states that the MII crystal input XTI may be driven by a clock oscillator.	TBD

Data Sheet Clarifications:

The following typographic corrections and clarifications are to be noted for the data sheet (DS60001573C):

Note: Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

d1. Module: Table 3-7. Miscellaneous Pins

The following shows corrections in bold to be made to the first two rows in Table 3-7:

Table 3-7. Miscellaneous Pins

Name	Symbol	Buffer Type	Description
External 25 MHz Crystal Input **(MII Mode)**	XTI	ICLK	External 25 MHz Crystal Input **– required in MII mode.**
External **50 MHz** Clock Input **(RMII Mode)**	REFCLKIN	ICLK	Single-ended 50 MHz clock oscillator input **– required in RMII mode.** Note: When using a single-ended clock oscillator, XTO must be left unconnected with <10 pF stray capacitance.

d2. Module: Section 4.1 Media Independent Interface (MII)

After paragraph

> "For timing information, refer to the MII Timing section. Refer to Clause 22 of the IEEE Std 802.3-2018 IEEE Standard for Ethernet specification for additional MII information."

Add

> **When operating in MII mode, the LAN8670/2 XTI and XTO pins must be connected to a 25 MHz crystal.**

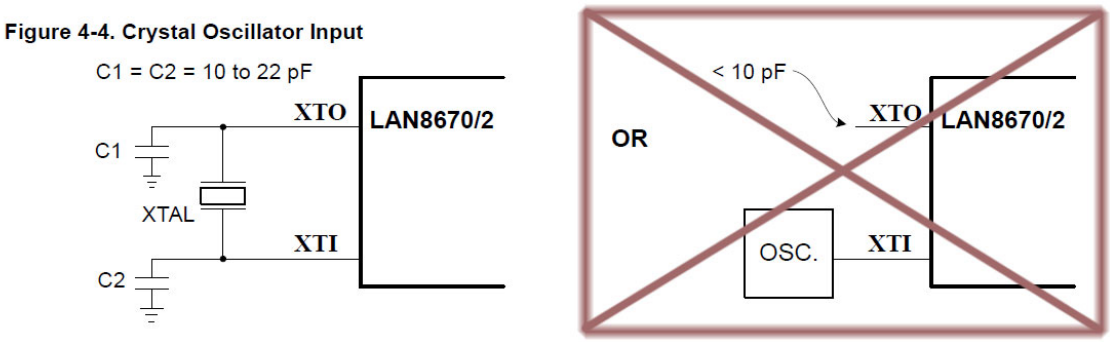
d3. Module: Section 4.8.1 Crystal Pins (XTI/XTO)

Remove entire paragraph:

> "**If an external clock oscillator is used in lieu of a crystal oscillator, it must be connected to the XTI pin. The clock must be stable prior to the negation of reset and remain stable for proper operation. In addition, the XTO pin should float and have minimal capacitance (see Figure 4-4).**"

d4. Module: Figure 4-4. Crystal Oscillator Input

Updates to drawing as shown below:



d5. Module: Table 7-7. DC Electrical Characteristics (other than 10BASE-T1S PMA)

Update to notes at end of table, change note 3 from:

3. REFCLKIN**, and optionally XTI,** can be driven from a single-ended clock oscillator to which these specifications apply.

to:

3. REFCLKIN is driven from a single-ended clock oscillator to which these specifications apply.

APPENDIX A: DOCUMENT REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS80000962B, 1/2023		Added Data Sheet Clarification section
DS80000962A, 7/2021	All	Initial Release of Errata

Note the following details of the code protection feature on Microchip products:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner, within operating specifications, and under normal conditions.
- Microchip values and aggressively protects its intellectual property rights. Attempts to breach the code protection features of Microchip product is strictly prohibited and may violate the Digital Millennium Copyright Act.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not mean that we are guaranteeing the product is "unbreakable" Code protection is constantly evolving. Microchip is committed to continuously improving the code protection features of our products.

For information regarding Microchip's Quality Management Systems, please visit www.microchip.com/quality.

ISBN: 978-1-6683-1864-5

Worldwide Sales and Service

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
http://www.microchip.com/support
Web Address:
www.microchip.com

Atlanta
Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Austin, TX
Tel: 512-257-3370

Boston
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Novi, MI
Tel: 248-848-4000

Houston, TX
Tel: 281-894-5983

Indianapolis
Noblesville, IN
Tel: 317-773-8323
Fax: 317-773-5453
Tel: 317-536-2380

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608
Tel: 951-273-7800

Raleigh, NC
Tel: 919-844-7510

New York, NY
Tel: 631-435-6000

San Jose, CA
Tel: 408-735-9110
Tel: 408-436-4270

Canada - Toronto
Tel: 905-695-1980
Fax: 905-695-2078

ASIA/PACIFIC

Australia - Sydney
Tel: 61-2-9868-6733

China - Beijing
Tel: 86-10-8569-7000

China - Chengdu
Tel: 86-28-8665-5511

China - Chongqing
Tel: 86-23-8980-9588

China - Dongguan
Tel: 86-769-8702-9880

China - Guangzhou
Tel: 86-20-8755-8029

China - Hangzhou
Tel: 86-571-8792-8115

China - Hong Kong SAR
Tel: 852-2943-5100

China - Nanjing
Tel: 86-25-8473-2460

China - Qingdao
Tel: 86-532-8502-7355

China - Shanghai
Tel: 86-21-3326-8000

China - Shenyang
Tel: 86-24-2334-2829

China - Shenzhen
Tel: 86-755-8864-2200

China - Suzhou
Tel: 86-186-6233-1526

China - Wuhan
Tel: 86-27-5980-5300

China - Xian
Tel: 86-29-8833-7252

China - Xiamen
Tel: 86-592-2388138

China - Zhuhai
Tel: 86-756-3210040

ASIA/PACIFIC

India - Bangalore
Tel: 91-80-3090-4444

India - New Delhi
Tel: 91-11-4160-8631

India - Pune
Tel: 91-20-4121-0141

Japan - Osaka
Tel: 81-6-6152-7160

Japan - Tokyo
Tel: 81-3-6880- 3770

Korea - Daegu
Tel: 82-53-744-4301

Korea - Seoul
Tel: 82-2-554-7200

Malaysia - Kuala Lumpur
Tel: 60-3-7651-7906

Malaysia - Penang
Tel: 60-4-227-8870

Philippines - Manila
Tel: 63-2-634-9065

Singapore
Tel: 65-6334-8870

Taiwan - Hsin Chu
Tel: 886-3-577-8366

Taiwan - Kaohsiung
Tel: 886-7-213-7830

Taiwan - Taipei
Tel: 886-2-2508-8600

Thailand - Bangkok
Tel: 66-2-694-1351

Vietnam - Ho Chi Minh
Tel: 84-28-5448-2100

EUROPE

Austria - Wels
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4485-5910
Fax: 45-4485-2829

Finland - Espoo
Tel: 358-9-4520-820

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Garching
Tel: 49-8931-9700

Germany - Haan
Tel: 49-2129-3766400

Germany - Heilbronn
Tel: 49-7131-72400

Germany - Karlsruhe
Tel: 49-721-625370

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Germany - Rosenheim
Tel: 49-8031-354-560

Israel - Ra'anana
Tel: 972-9-744-7705

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Italy - Padova
Tel: 39-049-7625286

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Norway - Trondheim
Tel: 47-7288-4388

Poland - Warsaw
Tel: 48-22-3325737

Romania - Bucharest
Tel: 40-21-407-87-50

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

Sweden - Gothenberg
Tel: 46-31-704-60-40

Sweden - Stockholm
Tel: 46-8-5090-4654

UK - Wokingham
Tel: 44-118-921-5800
Fax: 44-118-921-5820

1/24/23
091421B