TAOGLAS

Datasheet

Multiband GNSS Front End

Part No:
TFM.110A

Description:

Surface Mount GNSS Front End Active Electronics

Covering the full Multiband GNSS Spectrum excluding the L-Bands

Features:

Two-stage LNA providing >25 dB Gain across all bands
Low Noise Figure: <3.5 dB in low bands and <4.0 dB in high bands
Vin = +1.8 to +5.5 VDC
Easy to integrate surface-mount
Dimensions: 15 x 15 x 2.7 mm

RoHS & Reach Compliant

1. Introduction

The Taoglas TFM.110A is a surface-mount active electronics GNSS front end which covers L1/L2/L5 for multiband multi-constellation high-precision applications. The TFM.110A features a SAW/LNA/SAW/LNA topology in the signal path to prevent unwanted out-of-band interference from overdriving the GNSS LNAs or receiver. The SAW filters have been carefully selected and placed to provide excellent out-of-band rejection while also maintaining low noise figure.

Many currently available dual-band GNSS receivers require additional RF circuits between the antenna and the receiver to properly set the overall system noise figure. This requires additional development time for an otherwise simple integration. Many organizations don't have the RF expertise to effectively design such a solution. The TFM.110 captures the required additional RF circuits in modular form, allowing the designer to simply place the TFM.110 between their GNSS antenna and GNSS receiver.

The TFM.110 offers > 25 dB gain across all applicable bands while maintaining a high Input P1dB of -25 dBm or better. Noise Figure is < 3.5 dB in the low bands and < 4.0 dB in the high bands. A wide input voltage of +1.8 to +5.5 VDC allows for easy integration in most GNSS systems.

TFM.110A Features & Benefits:

- **Ease-of-integration** – Single-package solution combines impedance matching, filter efficiency and low noise design for easy, drop-in use with any antenna or GNSS receiver
- **Low-noise System Design** – Integrated pre-filters deliver exceptional out-of-band rejection across multiple band configurations and neighboring interference to properly set noise figure
- **Dual-gain Stage Architecture** – Cascaded LNAs, pre-filters and optimized impedance matching deliver sufficient gain to the GNSS receiver without signal-to-noise overload
- **Low-profile Form Factor** – Small footprint and low-profile design saves valuable real estate without the need for external components and routing
- **Accelerated Development Cycles** – 2+ years of development by antenna and RF design experts, delivering the highest levels of integration, manufacturability and robustness in a single package

For further information, please contact your regional Taoglas customer support team.

2. Specifications

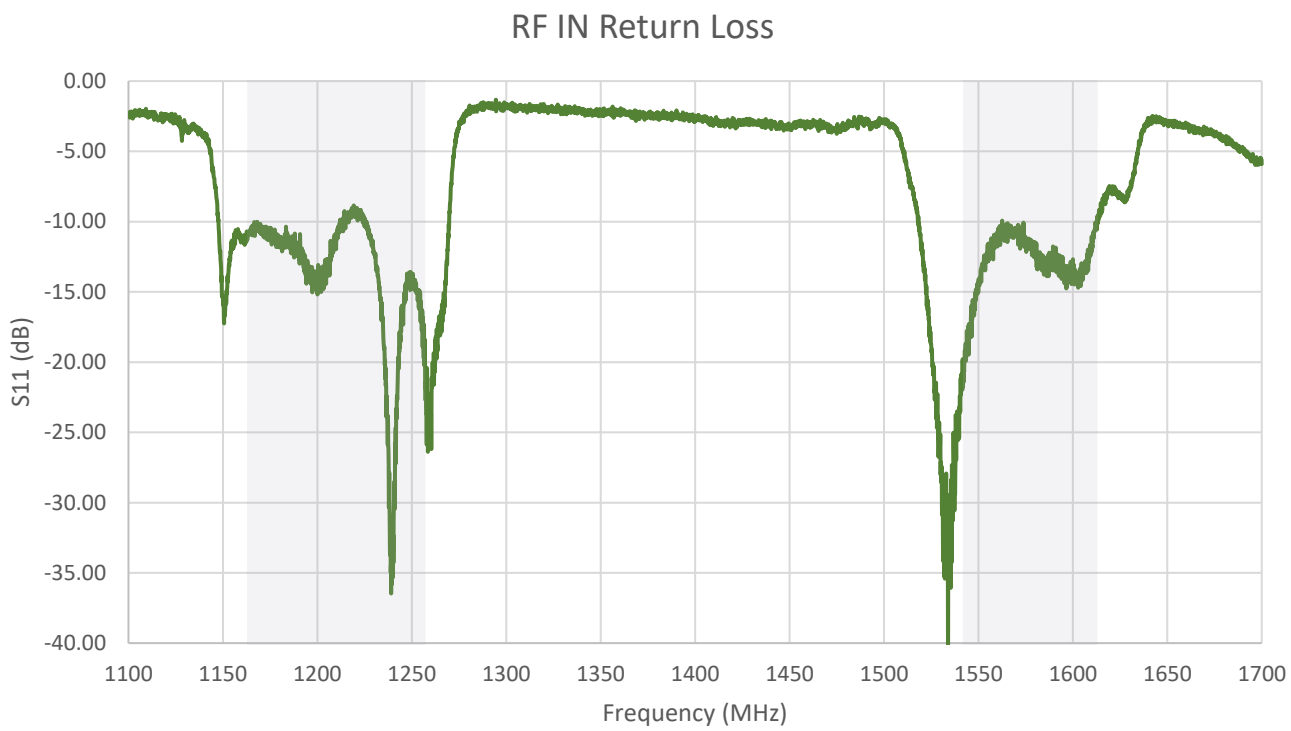
Electrical									
Frequency (MHz)	**1166**	**1176**	**1186**	**1197**	**1227**	**1249**	**1559**	**1575.42**	**1606**
Noise Figure (dB)*	2.9	2.7	2.6	2.5	3.1	3.1	3.3	3.1	3.6
Gain (dB)	29	30	30	31	30	31	27	26	25
Group Delay (ns)	22	20	18	19	17	23	16	16	23
Input P1dB (dBm)	-23	-24	-24	-24	-22	-23	-18	-18	-17
Input Return Loss (dB)	-10	-11	-12	-13	-11	-14	-11	-11	-13
Output Return Loss	-9	-9	-10	-14	-14	-17	-24	-31	-25
Vin	+1.8 to +5.5 VDC								

***Note: Tested on evaluation board. Board losses removed.**

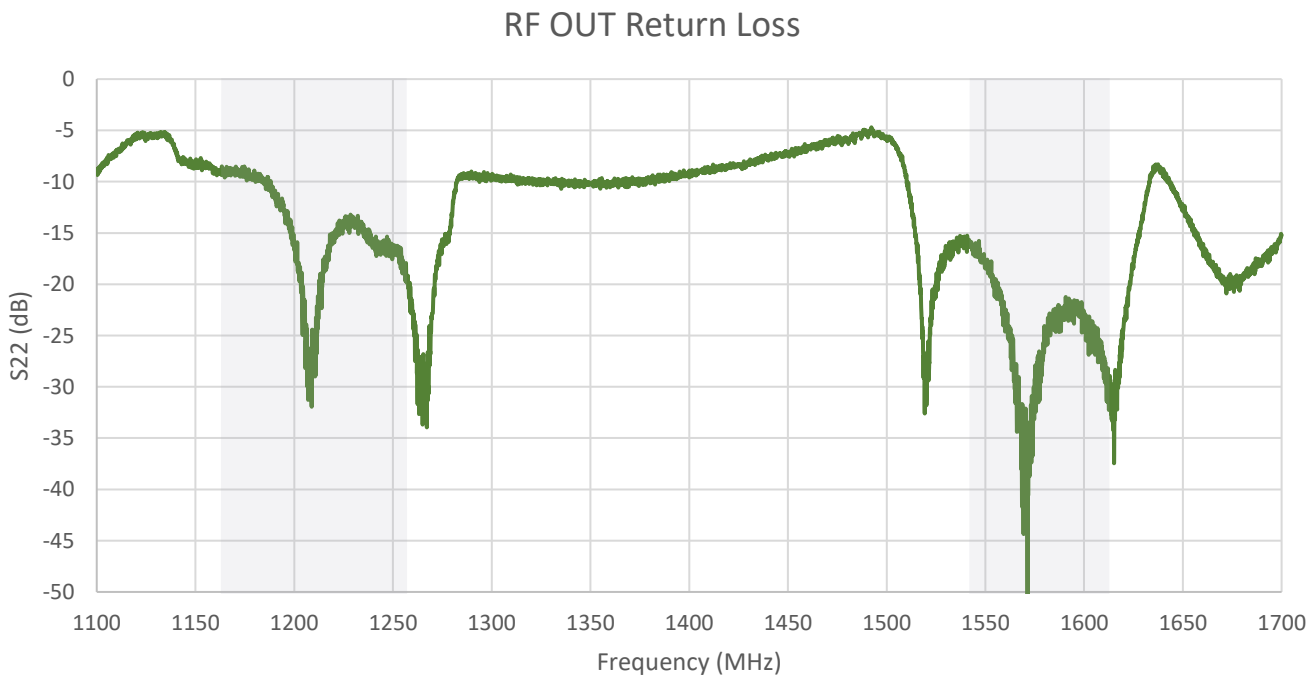
Mechanical	
Height	2.76mm
Planar Dimension	15.50 x 15.50mm
Weight	--
Environmental	
Temperature Range	-40°C to 85°C
RoHS Compliant	Yes
REACH Compliant	Yes

3. FEM Characteristics

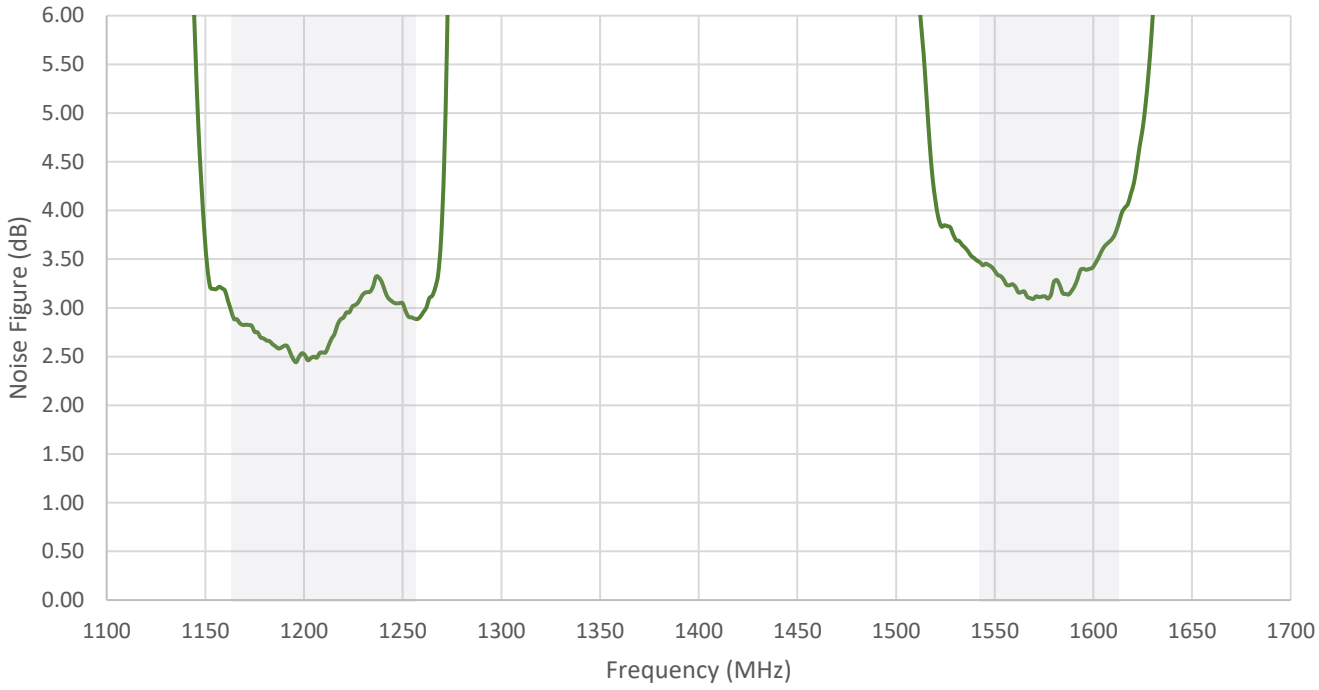
3.1 Input Return Loss



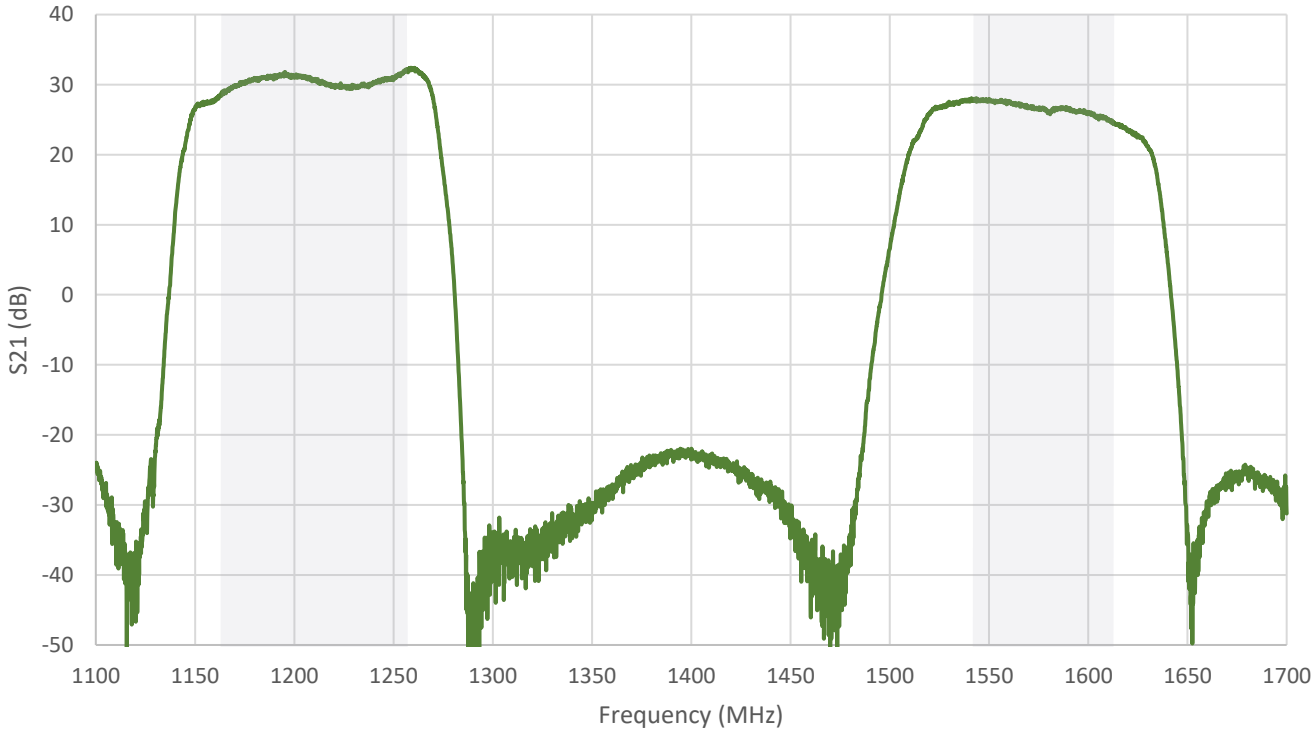
3.2 Output Return Loss



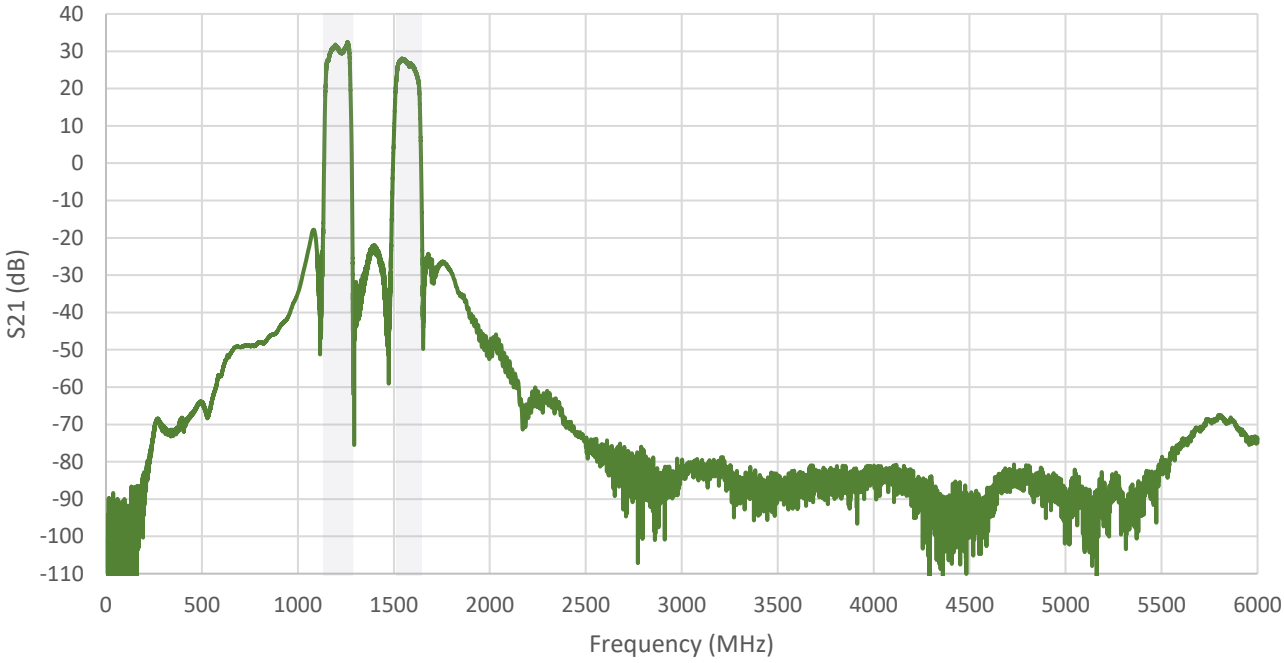
3.3 Noise Figure



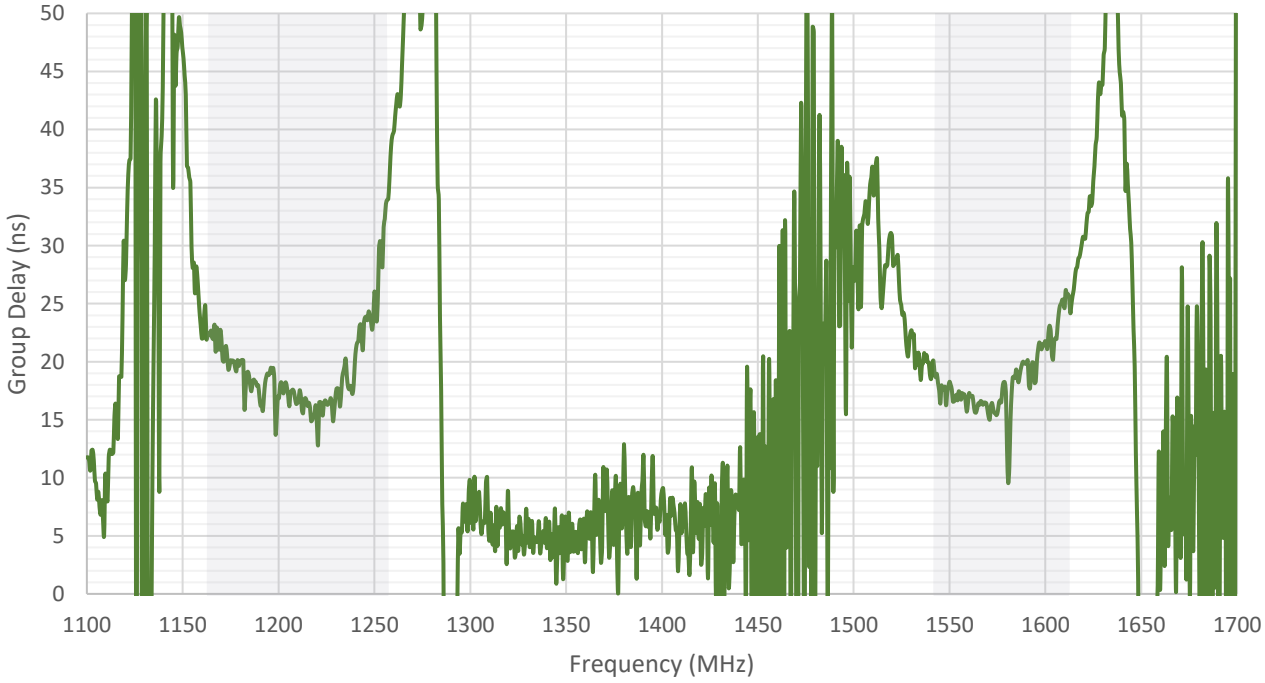
3.4 In-Band Gain



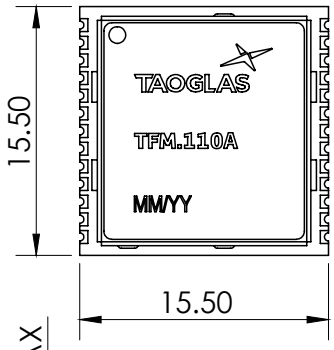
3.5 Wideband Gain



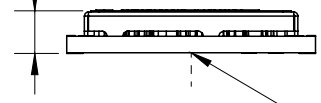
3.6 Low Band Group Delay



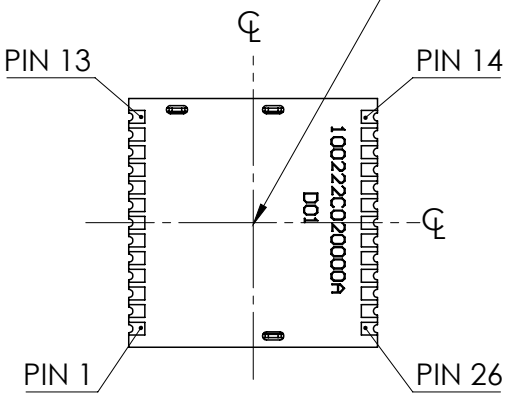
4. Mechanical Drawing



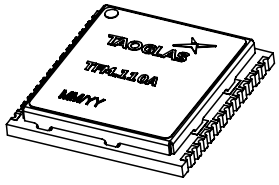
TOP VIEW



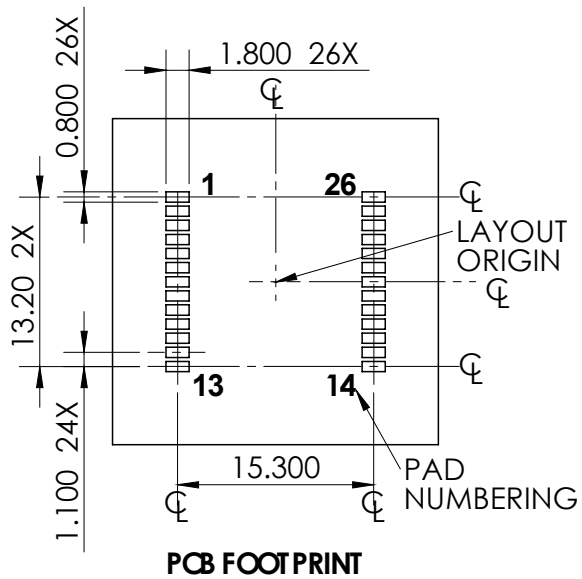
SIDE VIEW



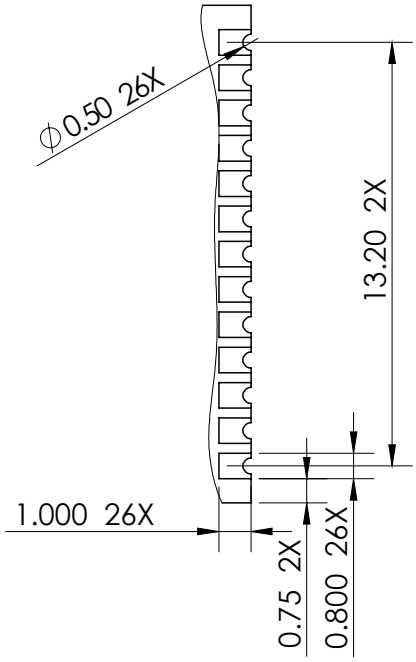
BOTTOM VIEW



ISO VIEW

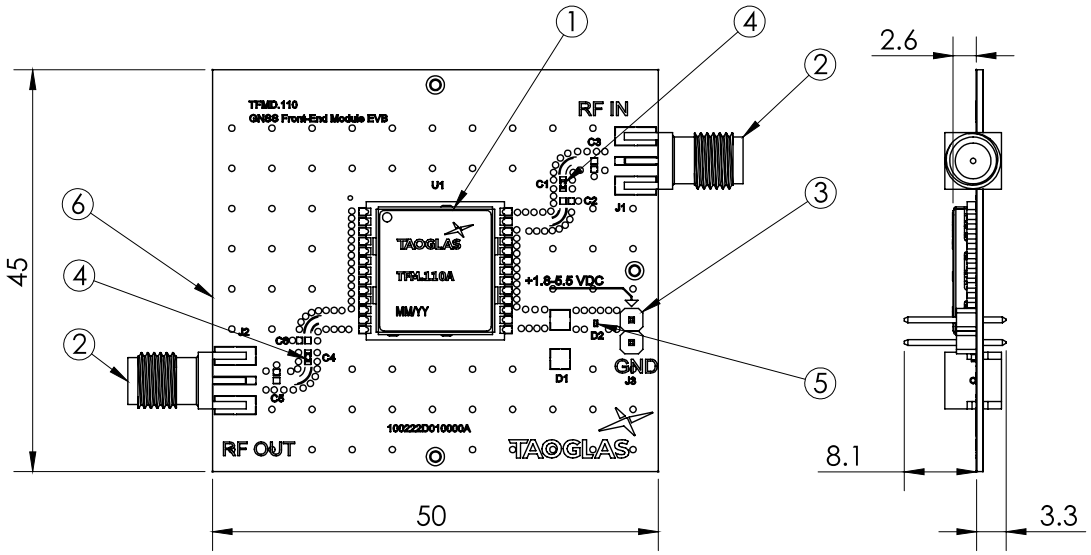


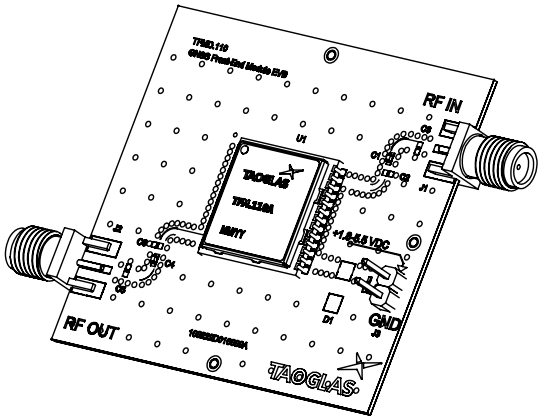
PCB FOOTPRINT



BOTTOM VIEW
SOLDER PAD DETAIL

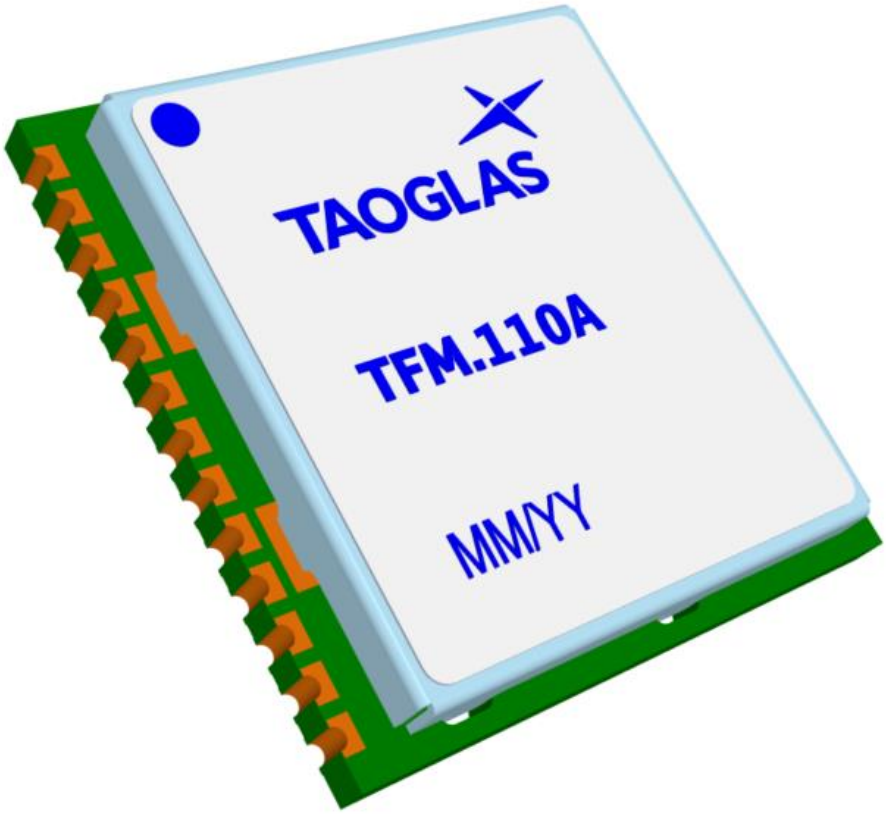
5. Eval Board Drawing





	Name	Material	Designator	QTY
1	TFM.110A GNSS Front End	NA	U1	1
2	Conn SMA Jack STR 50 Ohm Edge Mtg	Brass	J1, J2	2
3	Conn Header Vert 2 POS 2.54 mm	Brass/Plastic	J3	1
4	Cap, Cer 1000 PF 50V COG/NPO 0402	Ceramic	C1, C4	2
5	TVS Diaode 5.5VWM 7.5VC WLL-2-3	NA	D2	1
6	Eval Board PCB	FR4	NA	1

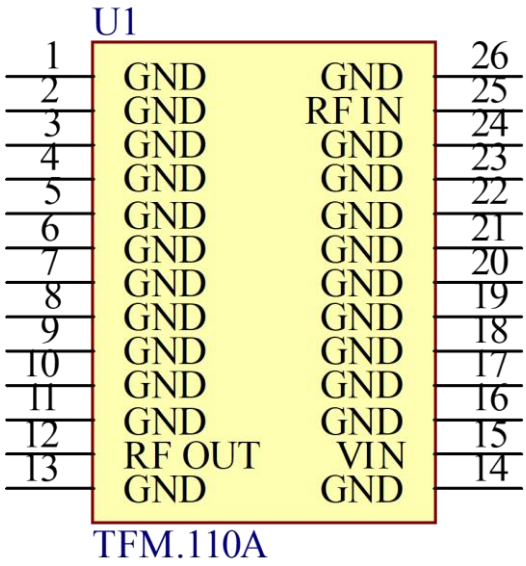
6. Antenna Integration Guide



6.1 Schematic Symbol and Pin Definitions

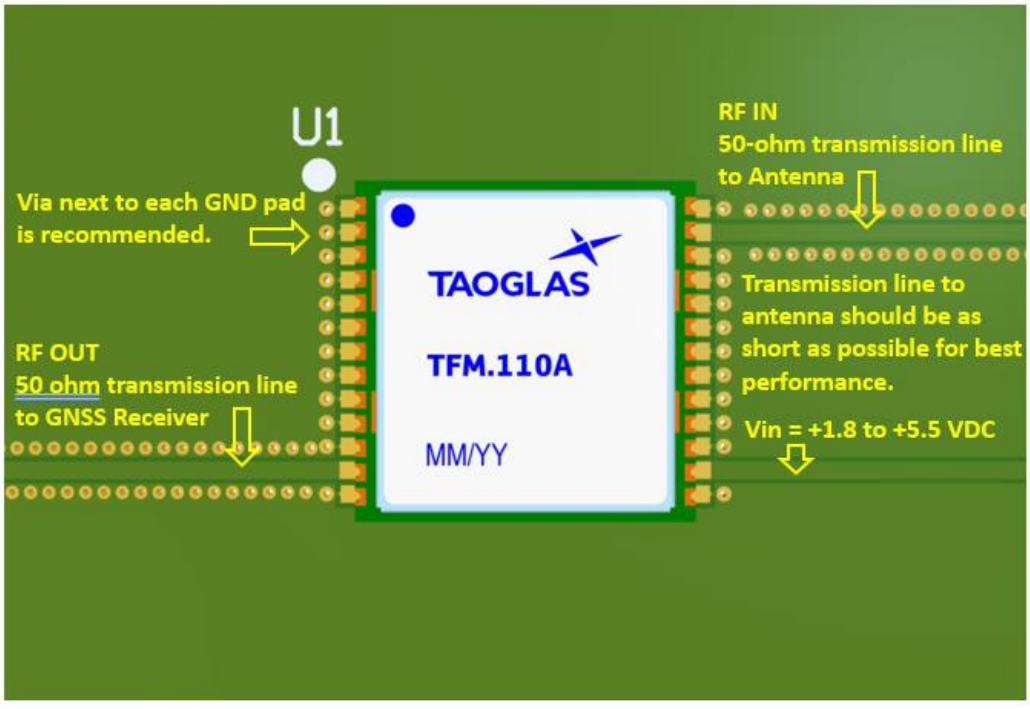
The circuit symbol for the TFM.110A is shown below. The front-end module has 26 pins as indicated below.

Pin	Description
1-11, 13-14, 16-24, 26	Ground
12	Signal Output
15	Voltage Input
25	Signal Input



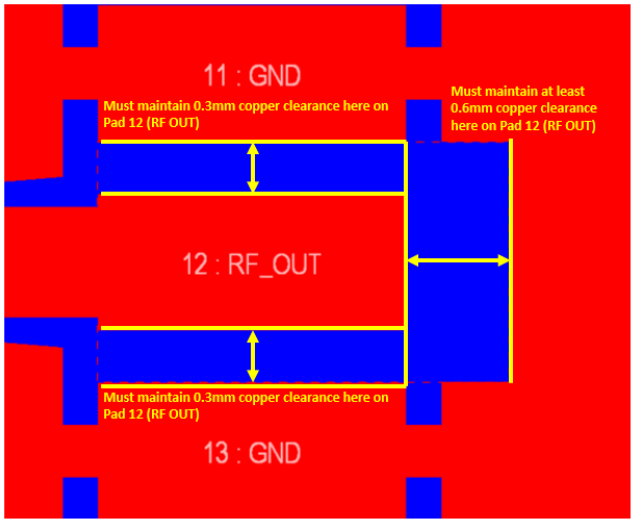
6.2 Antenna Integration Gudie

The TFM.110A should be placed as close to the signal input and output as possible to shorten the length of the transmission lines. The RF IN/OUT traces must maintain a 50 Ohm transmission line. A Pi Matching Network is recommended for the RF IN transmission line, the values and components for the matching circuit will depend on the tuning needed. Ground vias should be placed beside each ground pad and the DC Voltage input should be between +1.8 & +5.5 VDC. It's recommended that the DC Voltage input should be coupled with a 100pF Capacitor.

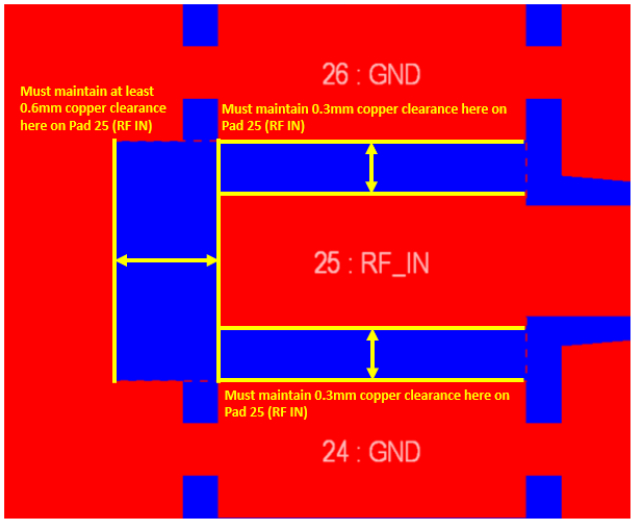


6.3 PCB Clearance

The footprint and clearance on the PCB must comply with the front-end module's specification. The PCB layout shown in the diagram below demonstrates the TFM.110A clearance area for Pin 12 (RF OUT Pad) & Pin 25 (RF IN Pad). The copper keep out area only applies to the same layer the TFM110.A was placed.



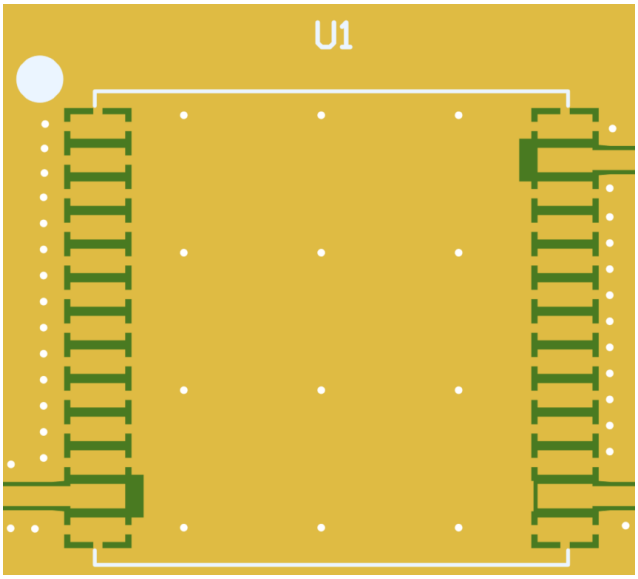
Pin 12 (RF OUT PAD)



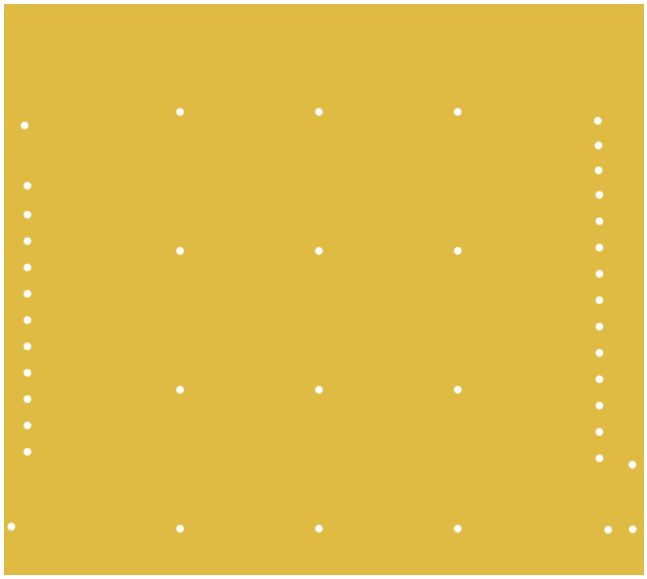
Pin 25 (RF IN PAD)

6.4 PCB Layout

The footprint and clearance on the PCB must comply with the front-end module's specification. The PCB layout shown in the diagram below demonstrates the TFM.110A footprint.

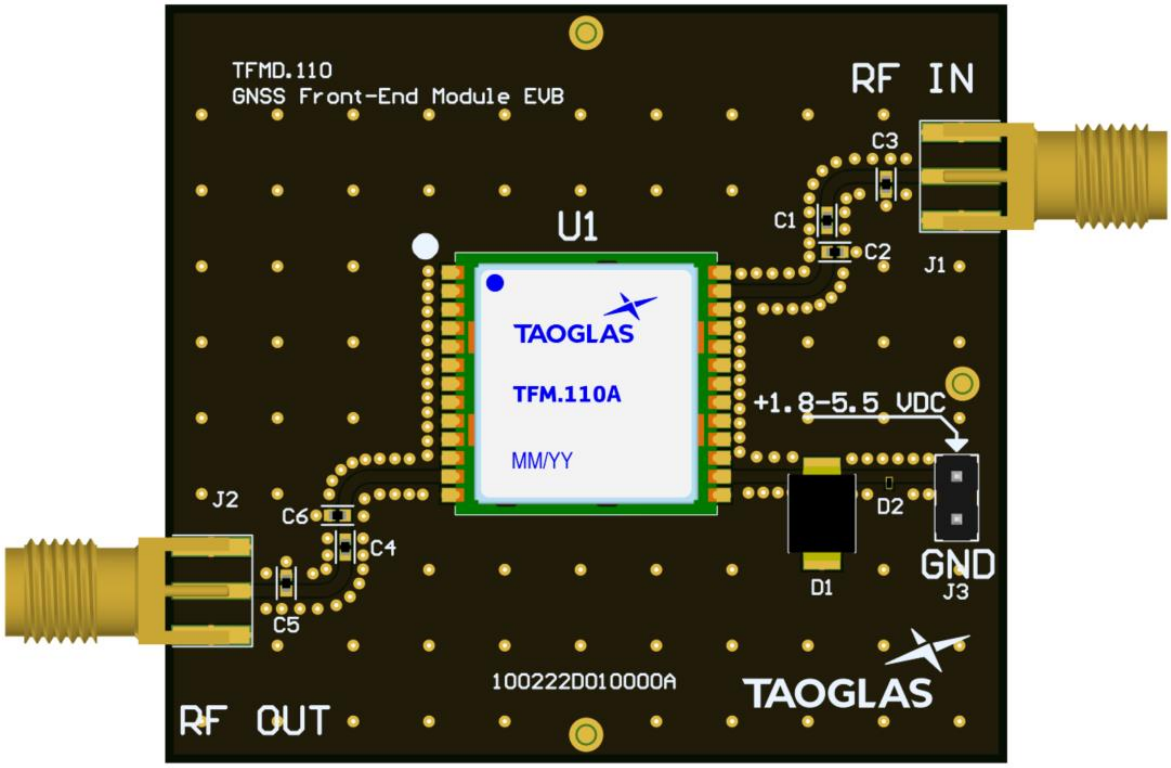


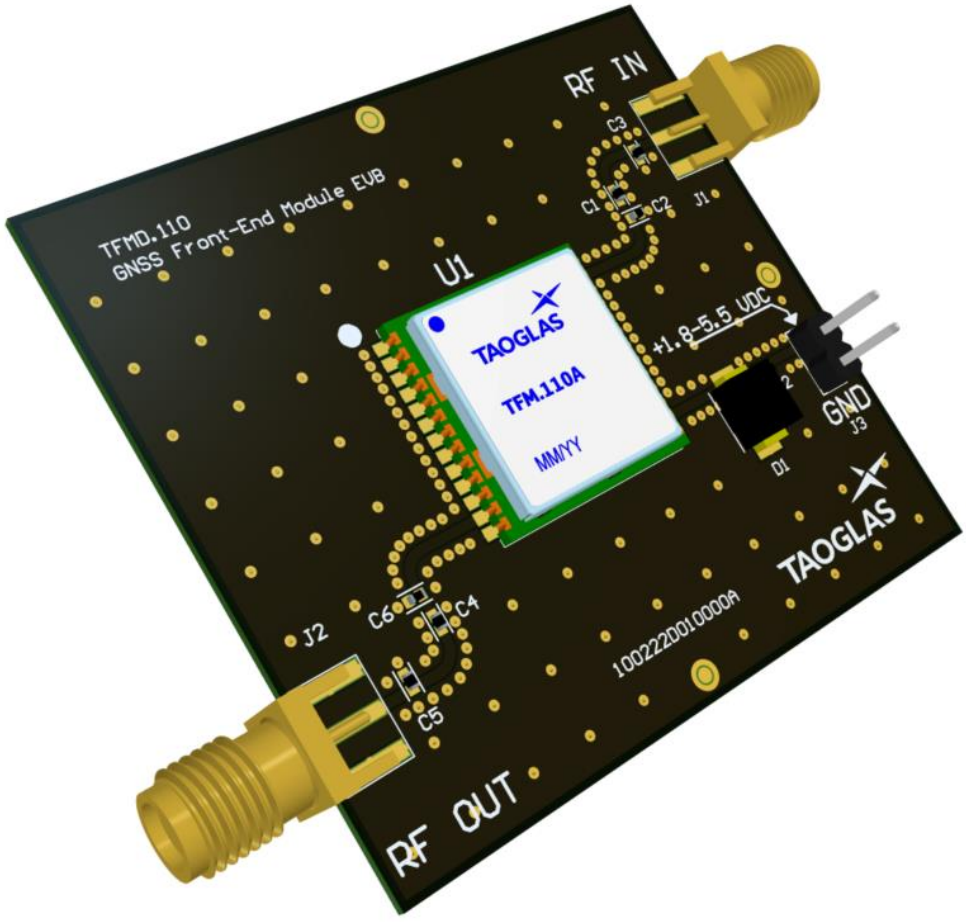
Topside



Bottom side

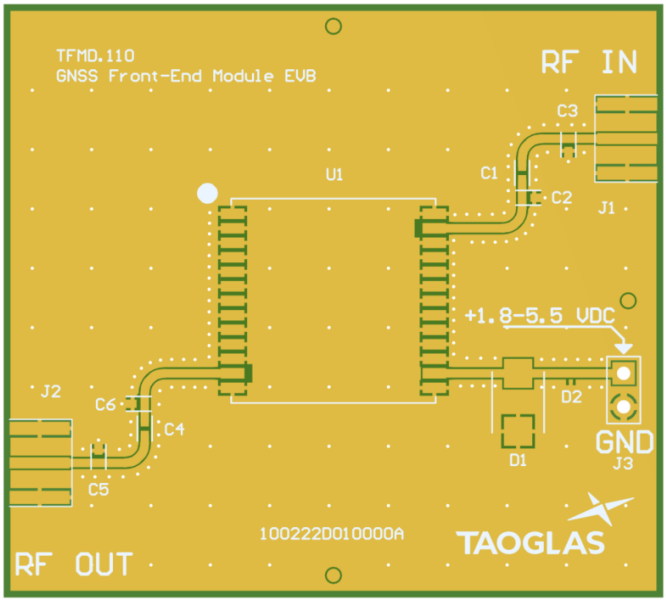
6.5 Evaluation Board



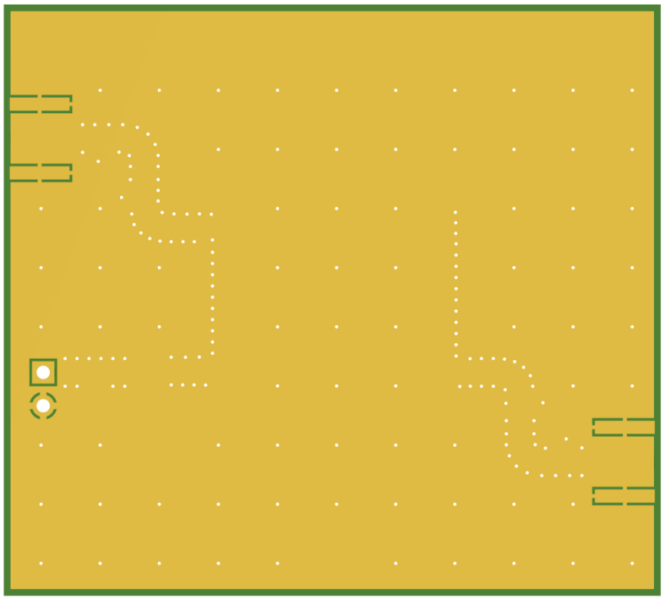


6.6 Evaluation Board Layout

The footprint and clearance on the PCB must comply with the front-end module's specification. The PCB layout shown in the diagram below demonstrates the TFM.110A footprint.

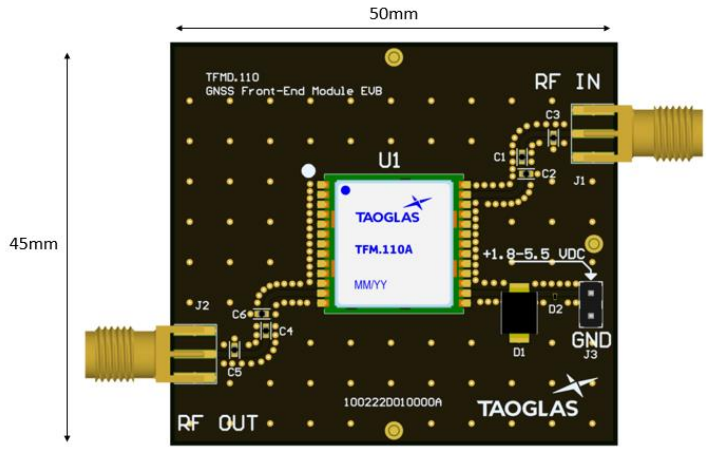


Topside

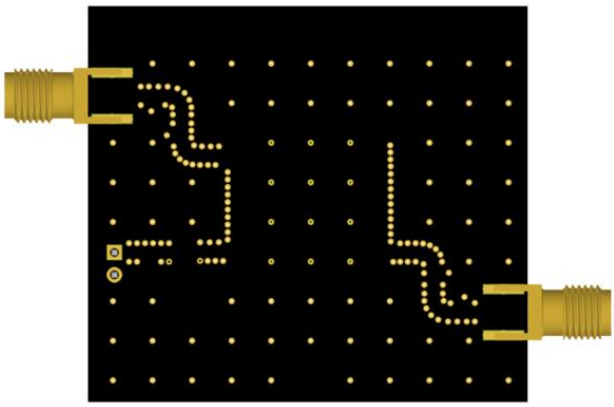


Bottom side

6.7 Evaluation Board

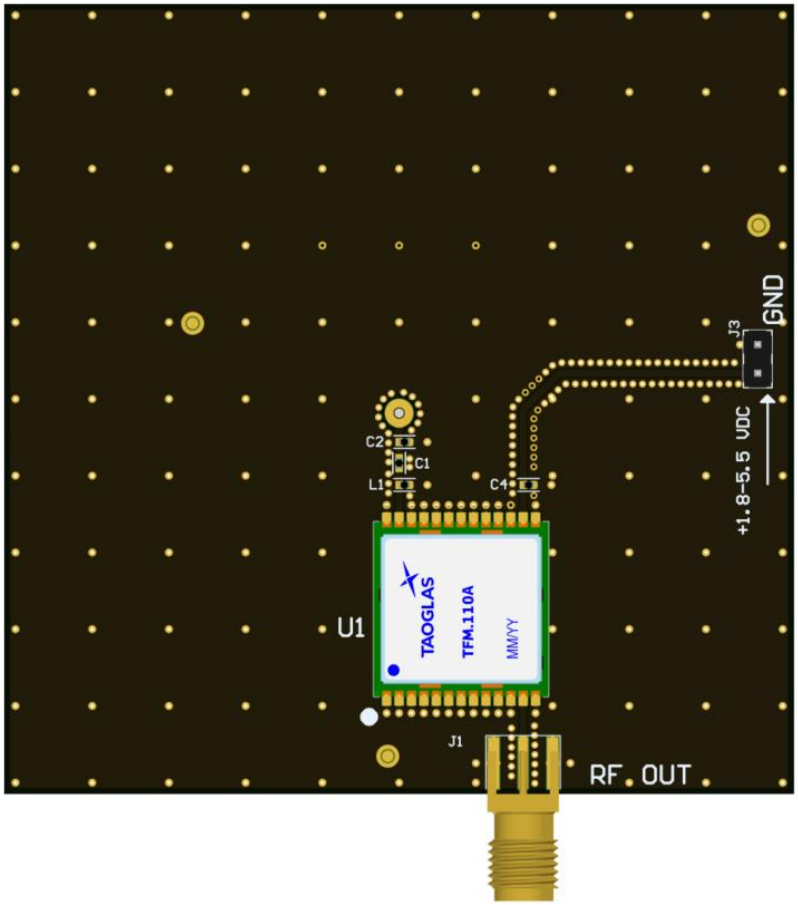


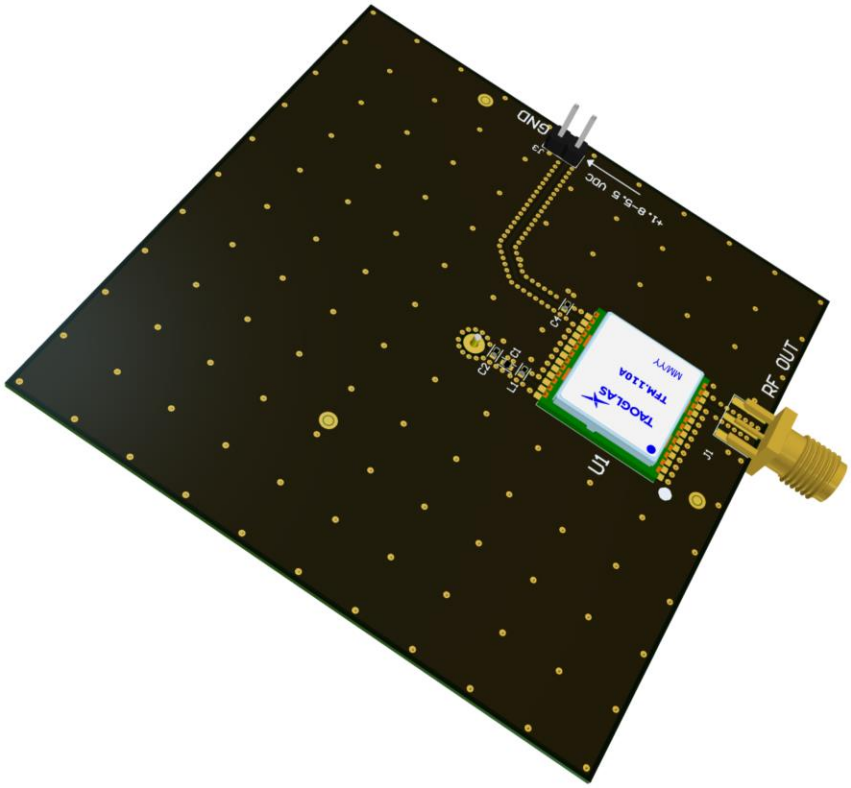
Topside



Bottom side

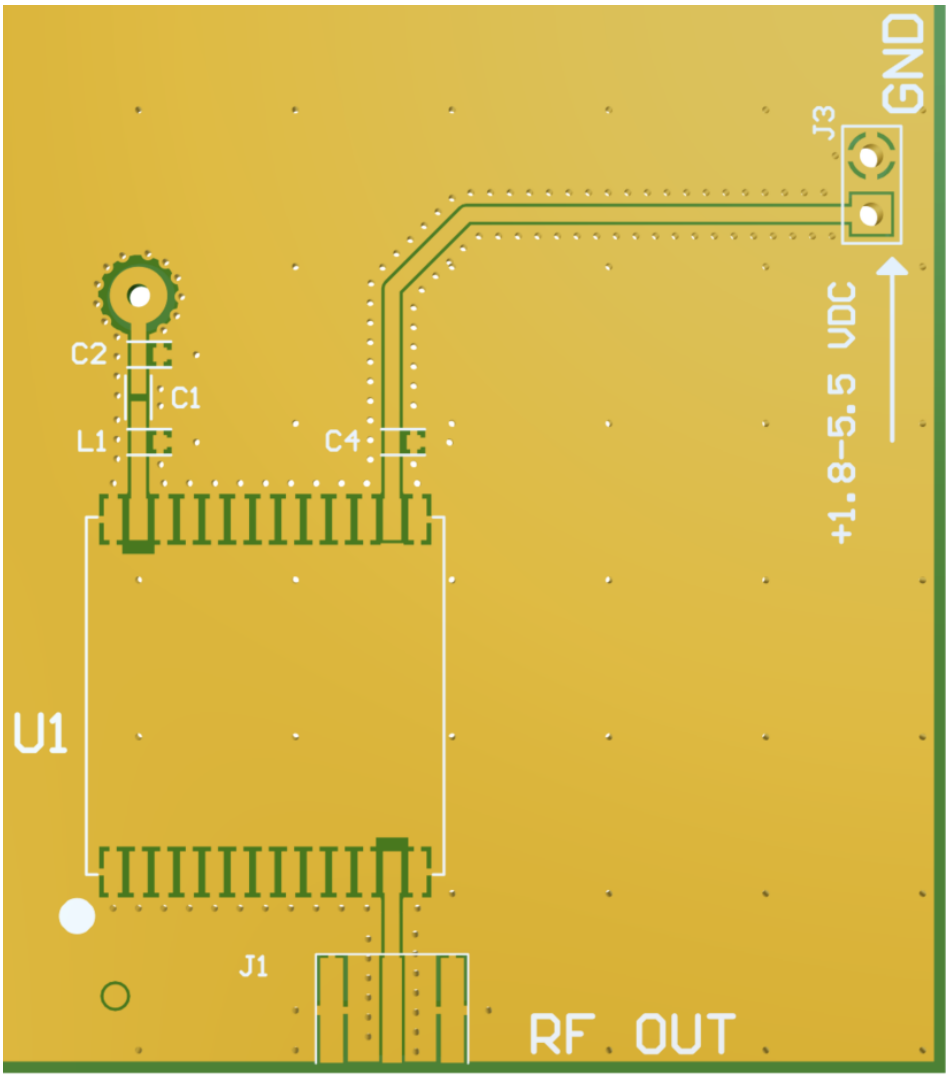
6.8 Demonstration Board





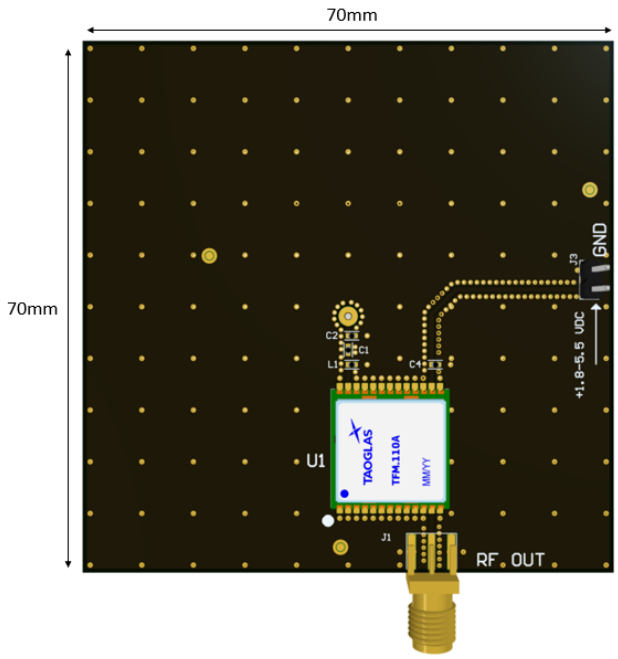
6.9 Demonstration Board Layout

The footprint and clearance on the PCB must comply with the front-end module's specification. The PCB layout shown in the diagram below demonstrates the TFM.110A footprint. This is a typical implementation.

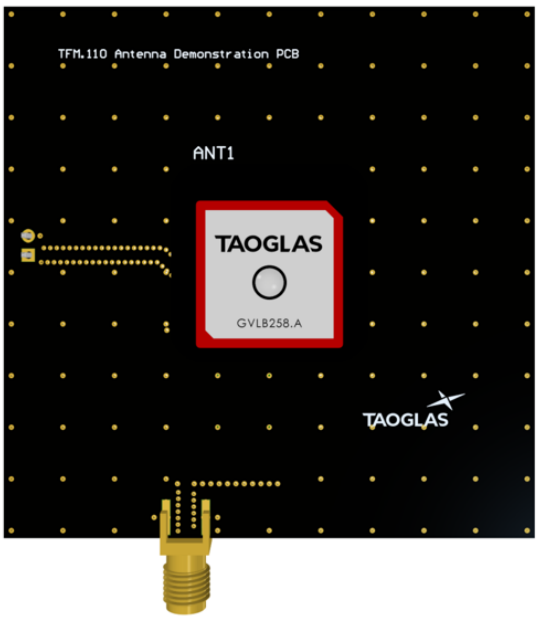


Topside

6.10 Demonstration Board



Topside



Bottom side

Changelog for the datasheet

SPE-22-8-149 – TFM.110.A

Revision: B (Current Version)	
Date:	2022-10-28
Notes:	Added antenna integration guide
Author:	Gary West

Previous Revisions

Revision: A (Original First Release)	
Date:	2022-09-26
Notes:	Initial Release
Author:	David Connolly

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