Product Change Notification / LIAL-04DQNT801

Date:

10-May-2023

Product Category:

General Purpose FPGAs, Radiation Tolerant FPGAs, System On Chip FPGAs

PCN Type:

Manufacturing Change

Notification Subject:

eSign# E000173629 Final notice: Released of updated Libero SoC v2022.3 for selected products in the PolarFire FPGA device family, including MPFxxx and RTPF device families.

Affected CPNs:

LIAL-04DQNT801_Affected_CPN_05102023.pdf
LIAL-04DQNT801_Affected_CPN_05102023.csv

Notification Text:

PCN Status: Final Notification

PCN Type: Manufacturing Change

Microchip Parts Affected: Please open one of the files found in the Affected CPNs section.
Note: For your convenience Microchip includes identical files in two formats (.pdf and .xls)

Description of Change: Released of updated Libero SoC v2022.3 for selected products in the PolarFire FPGA device family, including MPFxxx and RTPF device families as described in the attached customer notice details.

Notes:

Libero SoC v2022.3 released on Dec 16th, 2022 and is available for download on the webpage below:
https://www.microchip.com/en-us/products/fpgas-and-plds/fpga-and-soc-design-tools/fpga/lib

ero-software-later-versions#Download%20Software

Pre and Post Change Summary:

	Pre Change	Post Change
Software / Tool	PolarFire, RT PolarFire, and PolarFire SoC programming bitstreams created with Libero SoC v2022.2 or earlier.	PolarFire, RT PolarFire, and PolarFire SoC programming bitstreams created with Libero SoC v2022.3 or later.

Impacts to Data Sheet: None

Change Impact None

Reason for Change: Release updated Libero SoC v2022.3 to prevent usage of device programming bitstreams that could result in false Power-On Reset digest check failures and tamper flag assertion, for scenarios where the user has enabled POR digest check settings for device components not included in the programming bitstream.

Change Implementation Status:
Complete

Estimated First Ship Date: December 16, 2022 (date code: 2251)

Note: Please be advised that after the estimated first ship date customers may receive pre and post change parts.

Time Table Summary:

	December 2022					>	May 2023				
Workweek	49	50	51	52	53		18	19	20	21	22
Final PCN Issue Date								x			
Estimated Implementation Date			x								

Method to Identify Change: Not applicable. New software release is available as defined above.

Qualification Report: Not applicable

Revision History: May 10, 2023: Issued final notification.

The change described in this PCN does not alter Microchip's current regulatory compliance regarding the material content of the applicable products.

Attachments:

CN_PolarFire_FPGA_Tamper_PORDIGEST_Update_Libero_v2022p3.pdf

Please contact your local Microchip sales office with questions or concerns regarding this notification.

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If you wish to change your PCN profile, including opt out, please go to the PCN home page select login and sign into your myMicrochip account. Select a profile option from the left navigation bar and make the applicable selections.

Affected Catalog Part Numbers (CPN)

MPF300T-1FCVG484T2
MPF300T-FCVG484T2
MPF300T-1FCSG536T2
MPF300T-FCSG536T2
MPF300TS-FC484M
MPF300T-FCG484X547
MPF300TS-FCV484M
MPF300TS-FC784M
MPF300TS-FCS536M
MPF300TS-WAFER
MPF300T-1FCG484E
MPF300T-1FCG484I
MPF300T-FCG484EX52
MPF300T-FCG484E
MPF300T-FCG484I
MPF300TL-FCG484E
MPF300TL-FCG484I
MPF300TLS-FCG484I
MPF300TS-1FCG484I
MPF300TS-FCG484I
MPF300T-1FCG484IX548
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MPF300TS-FCVG484I
MPF300T-FCVG484EX548
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MPF300T-1FCG784I
MPF300T-FCG784E
MPF300T-FCG784I
MPF300TL-FCG784E
MPF300TL-FCG784I
MPF300TLS-FCG784I
MPF300TS-1FCG784I
MPF300TS-FCG784I
MPF300T-FCG784ES0317
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MPF300T-FCG784NE

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MPF300TS-FCG784NI
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MPF300T-1FCG1152I
MPF300T-FCG1152E
MPF300T-FCG1152I
MPF300TL-FCG1152E
MPF300TL-FCG1152I
MPF300TLS-FCG1152I
MPF300TS-1FCG1152I
MPF300TS-FCG1152I
MPF300T-1FCG1152IX45
MPF300T-FCG1152ES0311
MPF300T-FCG1152ES0324
MPF300T-1FCSG536E
MPF300T-1FCSG536I
MPF300T-FCSG536E
MPF300T-FCSG536I
MPF300TL-FCSG536E
MPF300TL-FCSG536I
MPF300TLS-FCSG536I
MPF300TS-1FCSG536I
MPF300TS-FCSG536I
MPF500TS-FC784M
MPF500TS-FC1152MX167
MPF500TS-FC1152M
MPF500TS-FC1152MX3
MPF500TS-WAFER
MPF500T-1FCG784E
MPF500T-1FCG784I
MPF500T-FCG784E
MPF500T-FCG784I
MPF500TL-FCG784E
MPF500TL-FCG784I
MPF500TLS-FCG784I
MPF500TS-1FCG784I
MPF500TS-FCG784I
MPF500T-1FCG1152E
MPF500T-1FCG1152I
MPF500T-FCG1152E
MPF500T-FCG1152I
MPF500TL-FCG1152E
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MPF100T-FCVG484T2
MPF100T-1FCSG325T2
MPF100T-FCSG325T2
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MPF100T-FCG484T2
MPF100TS-WAFER
MPF100TS-WAFER-PROCESSED
MPF100T-1FCG484E
MPF100T-1FCG484I
MPF100T-FCG484E
MPF100T-FCG484I
MPF100TL-FCG484E
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MPF100TL-FCVG484I
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MPF050TLS-FCSG325I
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MPFS160T-1FCVG484I
MPFS160T-FCVG484E
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MPFS160TL-FCSG536I
MPFS160TLS-FCSG536I
MPFS160TS-1FCSG536I
MPFS160TS-FCSG536I
RTPF500T-1CB1509MS
RTPF500T-1CB1509PROTO
RTPF500T-1CG1509EX259
RTPF500T-1CG1509EX3
RTPF500T-1CG1509MS
RTPF500T-1CG1509PROTO
RTPF500T-1LG1509MS
RTPF500T-1LG1509PROTO
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RTPF500T-CG1509PROTO
RTPF500T-LG1509PROTO
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RTPF500TL-CB1509PROTO
RTPF500TL-CG1509E
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RTPF500TL-LG1509ES
RTPF500TL-LG1509PROTO
RTPF500TLS-CB1509ES

RTPF500TLS-CB1509PROTO
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RTPFS460TS-1CG1509PROTO
RTPFS460TS-1LG1509PROTO
RTPFS460TS-CB1509PROTO
RTPFS460TS-CG1509PROTO
RTPFS460TS-LG1509PROTO

Customer Notification (CN)

Subject: PolarFire® FPGA and SoC PORDIGEST and Tamper IP Update

March 2023

Description:

This customer notification applies to PolarFire, RT PolarFire, and PolarFire SoC programming files generated by Libero SoC versions v2022.2 and earlier, that enable the device Power-On Reset Digest check (PORDIGEST). When using Libero 2022.2 or earlier releases, the Power-On Reset digest check settings programmed into the device didn't distinguish which device components, amongst FPGA Fabric, sNVM/eNVM or security settings, were selected for export into the programming bitstream file. This behavior could lead to scenarios where the Power-On Reset digest check was enabled for a component that was not programmed by the user design. This issue has been fixed in Libero SoC v2022.3 and later.

Reason for Change:

In Libero SoC versions v2022.2 and earlier, if a Power-On Reset digest check is enabled, and the corresponding device component not selected for export into the programming file, the Power-On Reset digest check setting for that unselected component is programmed. This causes the Power-On Reset digest check to fail and asserts a tamper flag from the user instantiated Tamper IP core. Depending on the user design reaction to the incorrectly triggered tamper flag, the user design might initiate a non-recoverable device zeroization, thereby losing the device permanently.

In Libero SoC v2022.3 or later, the behavior is changed. If a device component is not selected for bitstream export, then the Power-On Reset digest check setting for that component is not programmed, even if it is selected in the Tamper IP core. This means Libero Soc v2022.3 or later will only program Power-On Reset digest check settings for those device components that are included in programming bitstream or job file.

Application Impact:

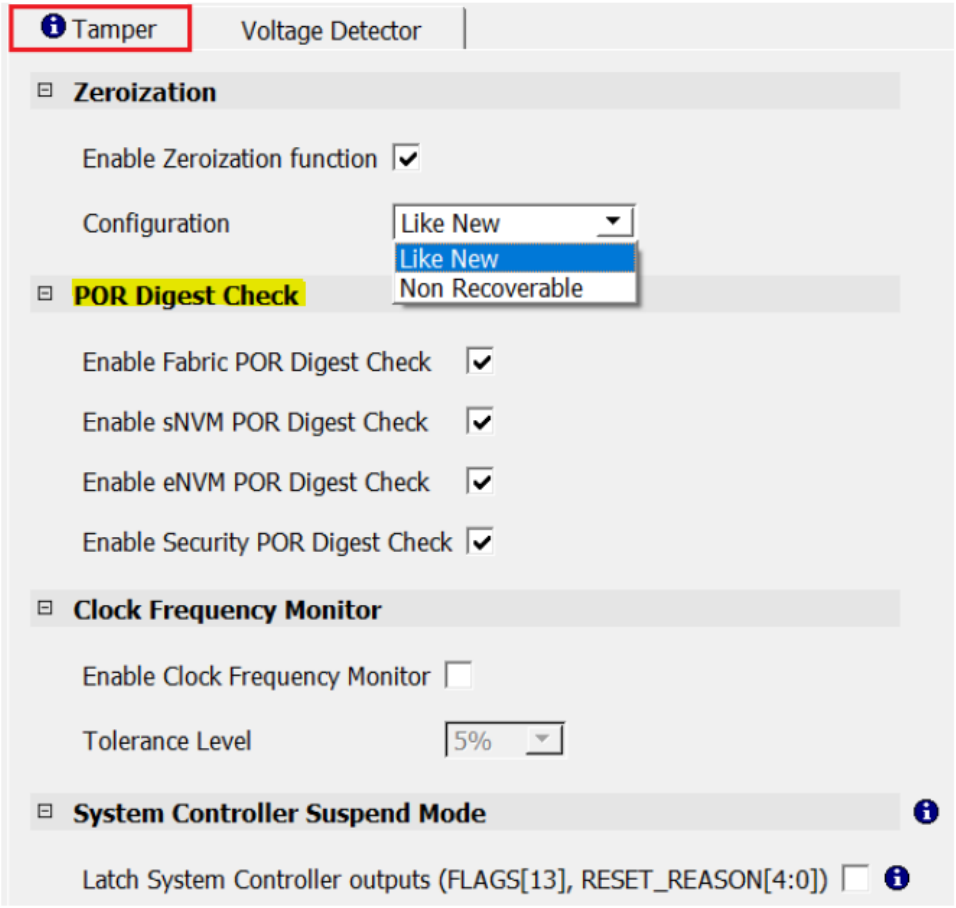
The following design configurations are NOT impacted:

- Designs that don't contain the Tamper IP core in the fabric design, PF_TAMPER or PFSOC_TAMPER
- Designs that don't enable Power-On Reset digest checks in the Tamper IP core
- Designs that program all device components selected for Power-On Reset digest checks in the configured Tamper IP core

Designs using bitstreams generated prior to Libero SoC v2022.3, where the Tamper IP core is instantiated and configured to enable Power-On Reset digest checks on device components that were ***not*** included in the

programming bitstream, will see the Power-On Reset digest check fail. The Power-On Reset digest check failure causes the assertion of the corresponding Tamper IP core flag output. Although this Power-On Reset digest check failure is a false failure, the user design response to the tamper flag assertion determines the impact to the application.

The figure below shows the Tamper IP core configured with the Power-On Reset Digest Check enabled for all device components:



Important: Enable eNVM POR Digest Check is only applicable for the PolarFire SoC FPGA.

For more information about the Tamper IP core responses and Power-On Reset Digest (POR Digest) checks, refer to the PolarFire FPGA and SoC Security User Guide.

Required Action:

New and ongoing designs using Power-On Reset Digest Checks:
Upgrade to Libero SoC v2022.3, or later. Upgrade to the latest PF_TAMPER (v1.0.212 or later) or PFSOC_TAMPER (v2.0.100 or later) IP core, if used in the design. Then re-run the design flow, including the programming file generation and exports steps: Generate Bitstream, Export Bitstream, Export FlashPro Express Job and Export Job Manager Data.

Designs completed using Libero SoC versions prior to v2022.3:
No further actions are listed if the affected design conditions described above don't apply to the design.

Completed designs observing false PORDIGEST check failures due to the issue above:
Open the pre-2022.3 design in Libero SoC v2022.3. Notice that the following design flow steps will be invalidated: Generate Bitstream, Export Bitstream, Export Flashpro Express Job and Export Job Manager Data. Re-run the invalidated programming bitstream generation and export steps, then reprogram the device using the updated programming file. Updating the Tamper IP core version is not required if the core configuration is unchanged. If updates to the Tamper IP core configuration are desired, a Tamper core version update will be required as listed in section 2 of the Libero SoC v2022.3 Software Release Notes.

Contact Information:

For any questions about this subject, contact Microchip FPGA-BU Technical Support at the web portal below:
http://www.microchip.com/support

Regards,

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