EV2650-V-01A

5A, Buck or Boost Charger with NVDC Power Path Management and USB OTG for 2S to 4S Battery Pack Applicatons Evaluation Board

DESCRIPTION

The EV2650-V-01A is an evaluation board designed for the MP2650, a highly integrated buck or boost charger IC with narrow-voltage DC (NVDC) power path management and USB On-the-Go (OTG) for battery packs with 2 cells, 3 cells, and 4 cells in series. The integrated power MOSFETs provide a compact system solution size that is easy to use.

The device can accept a wide input voltage (V_{IN}) range (up to 21V) for charge mode. This device has two operating modes while charging: boost charging mode and buck charging mode. The mode is determined by the input voltage and cell count. The MP2650 can also provide a constant voltage (5V/3A) at input in USB OTG mode.

With the I²C interface, the MP2650 can be flexibly configured to set the parameters in both charge mode and OTG mode. It can also provide the operation status through status and fault registers.

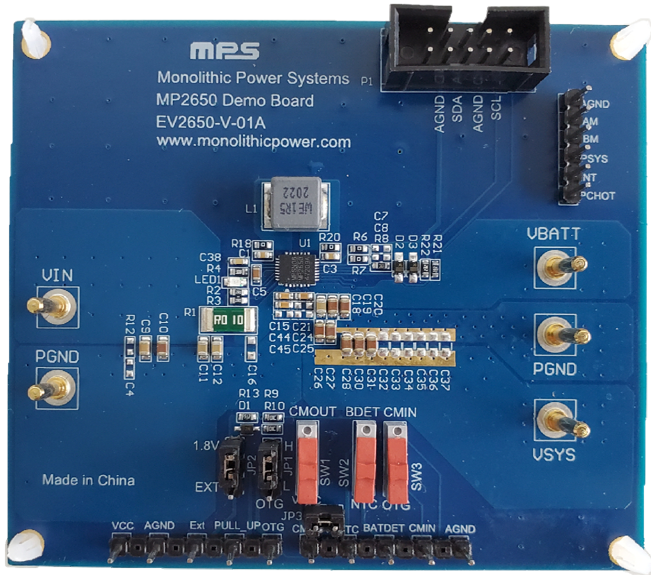
The MP2650 is available in a QFN-30 (4mmx5mm) package.

PERFORMANCE SUMMARY

Specifications are at T_A = 25°C, unless otherwise noted.

Parameters	Conditions	Value
Input voltage (V_{IN})		4V to 21V
Battery charge voltage regulation (V_{BATT_REG})	I²C-configurable	4.2V/cell
Fast charge current (I_{CC})	I²C-configurable	1A
Input voltage clamp limit (V_{IN_MIN})	I²C-configurable	4.5V
Input current limit (I_{IN_LIM})	I²C-configurable	1.5A
OTG output voltage (V_{IN_OTG})	I²C-configurable	5V
OTG output current limit (I_{OLIM})	I²C-configurable	1A

EV2650-V-01A EVALUATION BOARD



LxWxH (8.72cmx7.5cmx0.16cm)

Board Number	MPS IC Number
EV2650-V-01A	MP2650GV

QUICK START GUIDE

The EV2650-V-01A is designed for the MP2650, a buck or boost charger that charges battery packs with NVDC power path management and USB OTG functionality. Its layout accommodates most commonly used capacitors. This board is preset for charge mode by default, and the battery charge voltage regulation is preset to 4.2V/cell. In charge mode, the MP2650 can work in buck or boost mode automatically, depending on the input voltage and battery cell count.

Table 1 lists parameters for charge mode.

Table 1: Charge Mode Operation

V_{IN} (V)	Cell Count	Switcher Mode
5	2, 3, 4	Boost
9	2	Buck
12	2	Buck
15	2, 3	Buck
20	2, 3, 4	Buck

Table 2 lists parameters for USB OTG mode.

Table 2: OTG Mode Operation

V_{IN} (V)	Cell Count	Switcher Mode
5	2, 3, 4	Buck

Evaluation Board Set-Up

The EV2650-V-01A requires a computer with at least one USB port and a USB cable. The MP2650 evaluation software must be properly installed, and an evaluation kit (EVKT-USBI2C-02) must be used to connect the USB and I^2C (see Figure 1).

Figure 1: **USB-to-I^2C Communication Kit**

The MP2650 evaluation kit .exe file can be downloaded from MPS website. Double-click on the "MP2650 Evaluation Kit" .exe file to run the MP2650 evaluation software. The software supports Windows XP, Windows 7, and later operating systems.

To use the software, follow the steps below:

1. Connect the input supply terminals to:
    a. Positive (+): VIN
    b. Negative (-): PGND
2. Connect the load terminals to:
    a. Positive (+): SYS
    b. Negative (-): PGND
3. Connect the battery terminals to:
    a. Positive (+): BATT
    b. Negative (-): PGND

Figure 2 shows the test set-up for the MP2650.

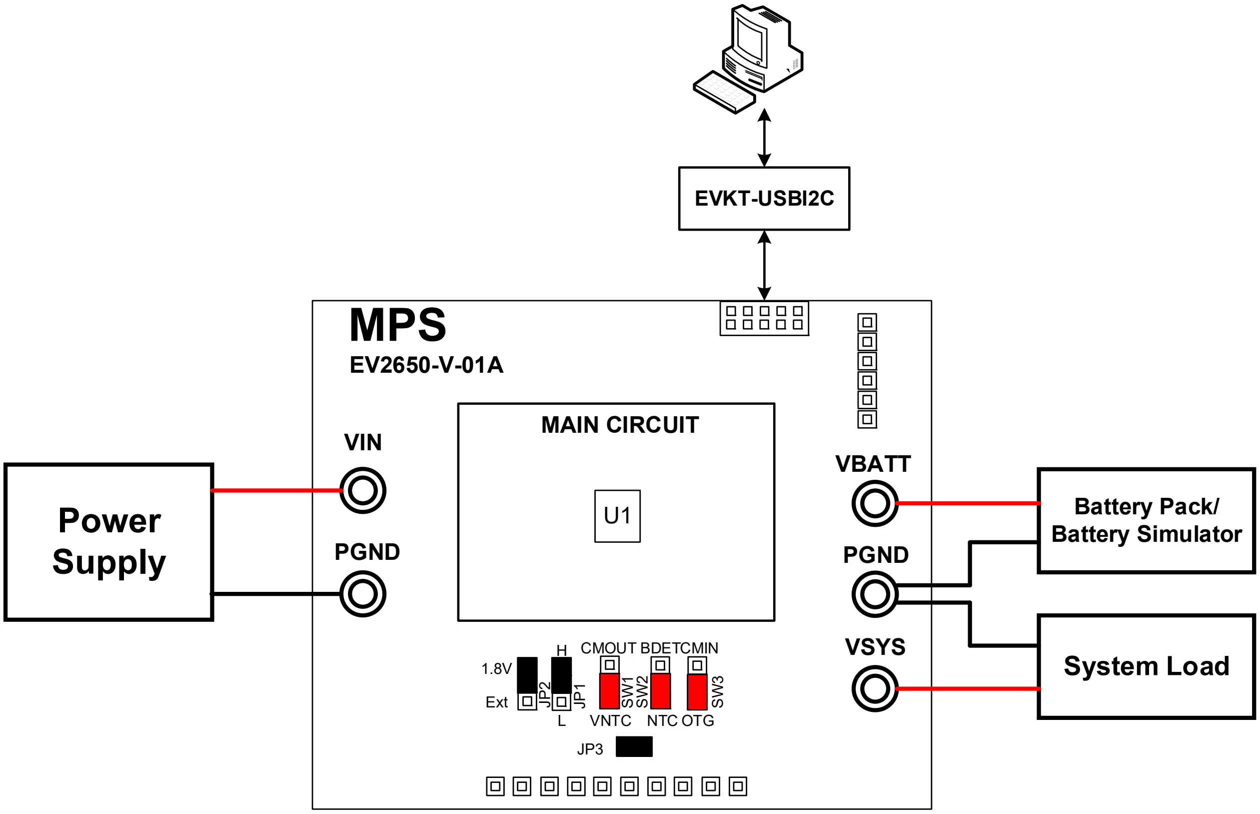


Figure 2: Test Set-Up for MP2650

Table 3 lists how to set the jumpers.

Table 3: Jumper Connections

Jack	Description	Default
SW1, SW2, and SW3 (1)	Dual-purpose pins. If all these pins are pulled down, SW1 = VNTC, SW2 = NTC, and SW3 = OTG. If these pins are pulled up, SW1 = CMOUT, SW2 = BATDET, and SW3 = CMIN.	All pins are pulled down
JP1	Sets the OTG mode. Pull JP1 low to disable OTG mode; pull it high to enable OTG. Note that the OTG register must also be set to enable OTG.	Pull JP1 high; OTG_EN (REG08h, bit[5] = 1)
JP2 (2)	Selects the pull-up voltage. Pull JP2 up to 1.8V, or pull it up to an external power source.	Pull JP2 up to 1.8V
JP3	Battery detection resistor connection. Connect JP3 to detect whether a battery is present. Note that for this function to work, SW1–3 must be pulled up, and REG08h, bit[2] should be set to 0.	Connect JP3

Notes:

1) SW1, SW2, and SW3 must all be pulled up or down at any given time.
2) If an external power source is used, add this source at Ext to AGND (e.g. 3.3V). If selecting 1.8V, no other action is required.

4. Turn the computer on and launch the MP2650 evaluation software. The main software window should appear (see Figure 3 on page 5).

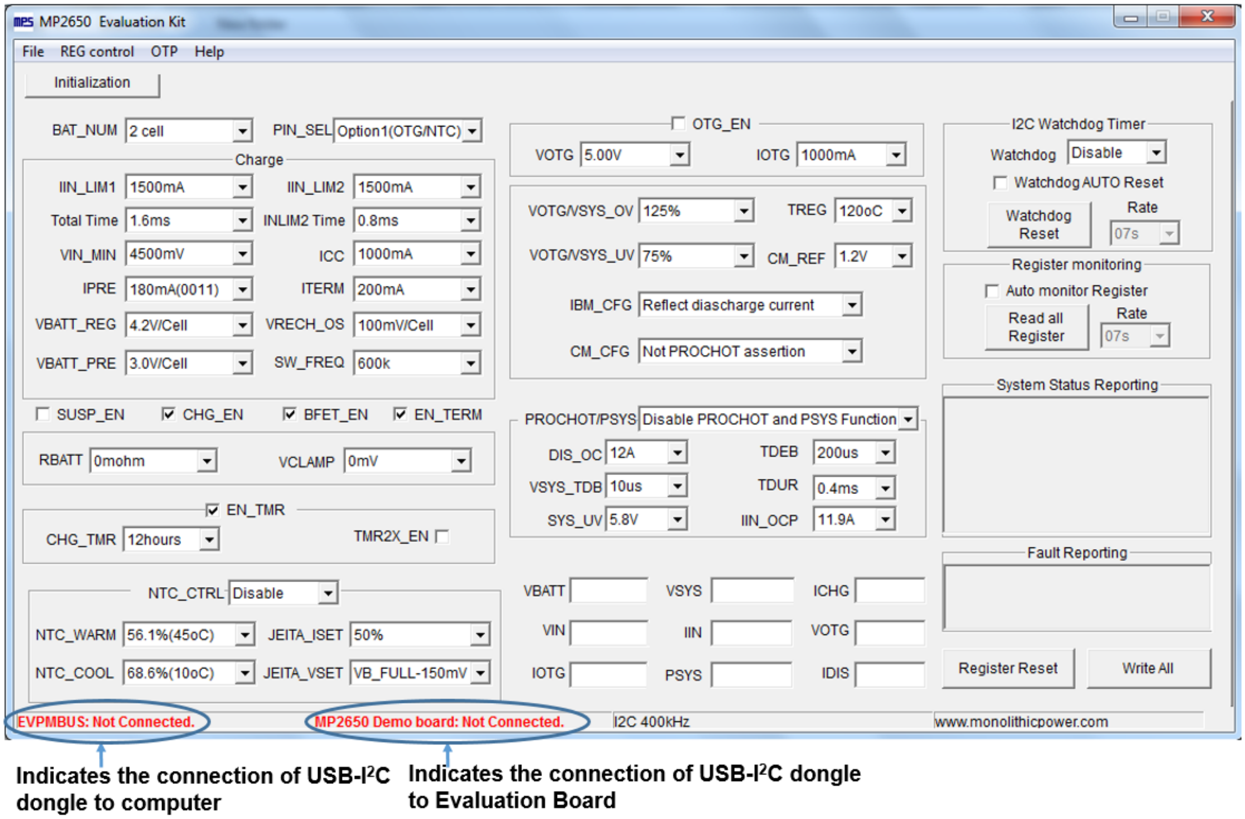


Figure 3: MP2650 Evaluation Software

Procedures

Ensure that the all components (i.e. the EVKT-USBI2C-02 and EV2650-V-01A) are connected correctly before running the program (see Figure 4).

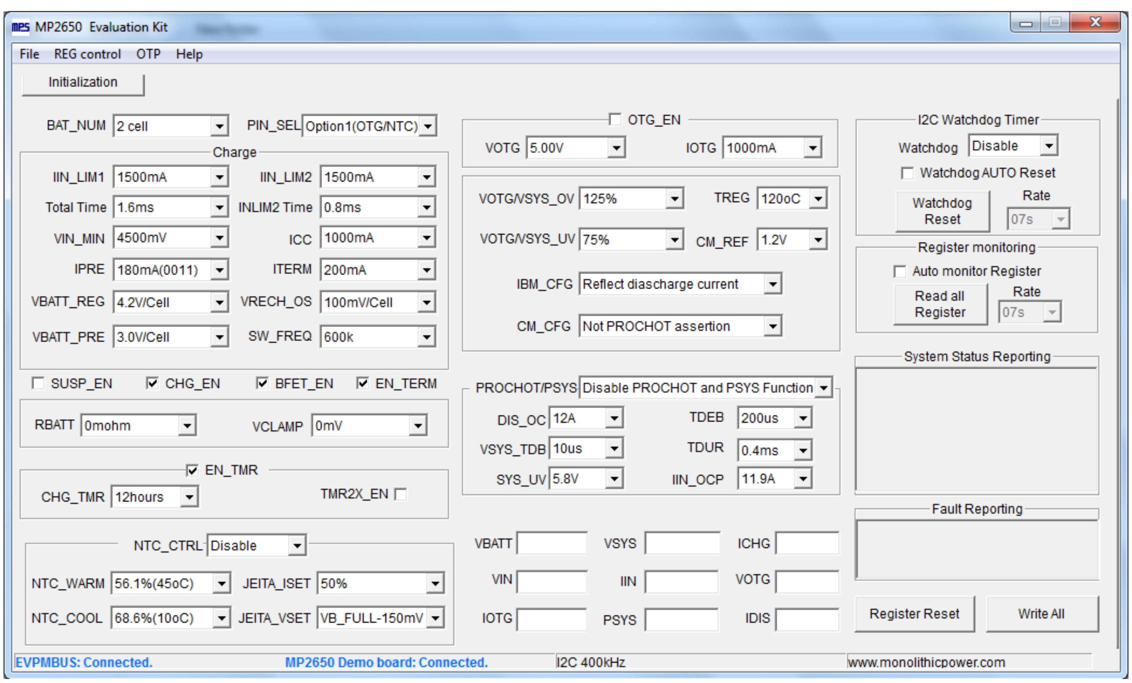


Figure 4: MP2650 Evaluation Software with Proper Connections

Setting Charge Functions

1. Preset the output voltages for the input power supply and battery simulator before turning on any instrument. Then set the charge mode parameters.
2. Plug in the battery or turn the battery simulator on. Ensure that the EVKT-USBI2C-02 is successfully connected to the computer and the evaluation board.
3. Set the battery cell count (see Figure 5).

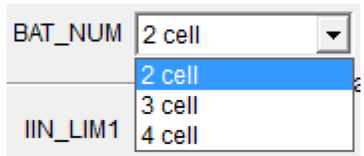


Figure 5: Battery Cell Count Configuration

   a. Ensure that the value set in the register is consistent with the real battery pack value.

4. Set the input current limit (see Figure 6).

Figure 6: Input Current Limit Configuration

   a. Generally, set INLIM1 equal to INLIM2. Set the total time to its maximum value, and set the INLIM2 time to its minimum value.

5. Set the input voltage clamp limit (see Figure 7).

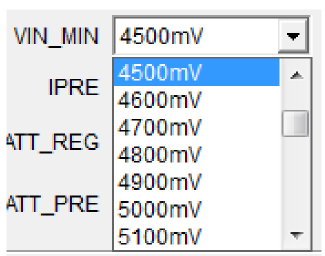


Figure 7: Input Voltage Clamp Limit Configuration

   a. It is recommended to set the input voltage clamp limit to 4500mV.

6. Set the fast charge current (see Figure 8).

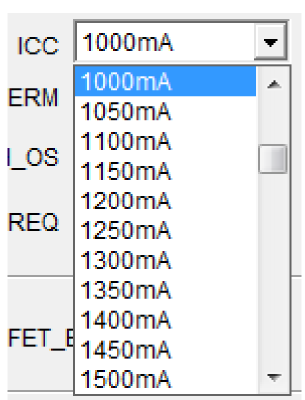


Figure 8: Fast Charge Current Configuration

7. Set the pre-charge current (see Figure 9).

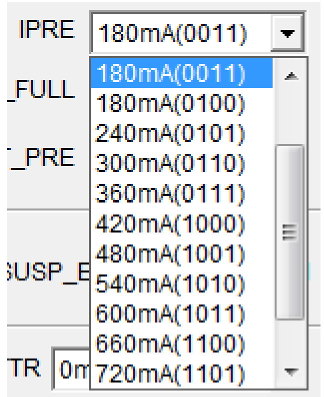


Figure 9: **Pre-Charge Current Configuration**

8. Set the charge termination current (see Figure 10).

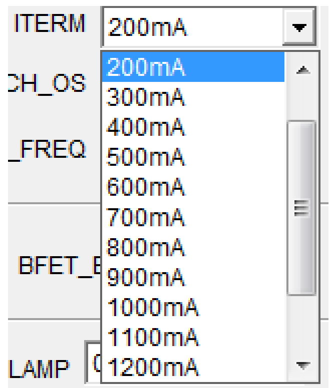


Figure 10: **Charge Termination Current Configuration**

9. Set the battery charge voltage regulation (see Figure 11).

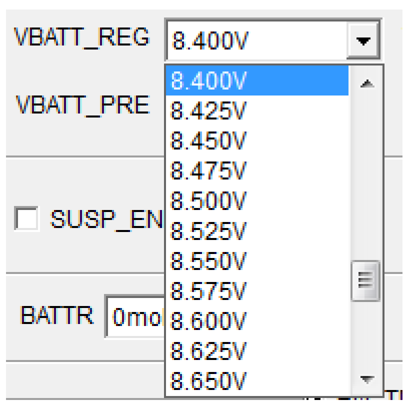


Figure 11: **Battery Charge Voltage Regulation Configuration**

a. Ensure that the battery charge voltage regulation is consistent with the battery pack value.

10. Set the pre-charge to fast charge threshold (see Figure 12).

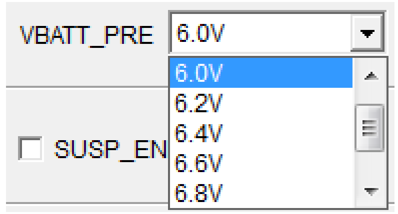


Figure 12: **Pre-Charge to Fast Charge Threshold Configuration**

   a. The minimum system voltage (V_{SYS_MIN}) is also set by this threshold (V_{BATT_PRE} + V_{TRACK}).

11. Set the auto-recharge battery voltage threshold (see Figure 13).

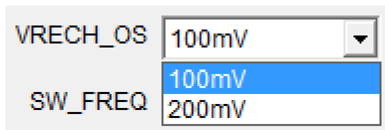


Figure 13: Auto-Recharge Battery Voltage Threshold Configuration

   a. The real auto-recharge threshold is equal to V_{BATT_REG} - V_{RECH_OS} x Cell Count.

12. Set the switching frequency (see Figure 14).

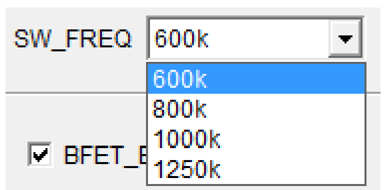


Figure 14: Switching Frequency Configuration

   a. Generally, set the switching frequency between 600kHz and 1000kHz.

13. Set charge mode configuration (see Figure 15).

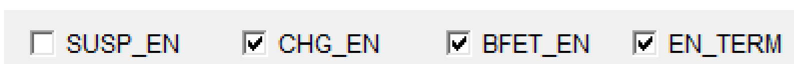


Figure 15: Charge Mode Configuration

   a. SUSP_EN: If SUSP_EN is checked, switching is turned off; if unchecked, switching is turned on.
   b. CHG_EN: If CHG_EN is checked, charging is enabled; if unchecked, charging is disabled.
   c. BFET_EN: If BFET_EN is checked, the BATTFET is turned on; if unchecked, the BATTFET is turned off.
   d. EN_BF: If EN_BF is checked, the charge termination function is enabled; if unchecked, the charge termination function is disabled.

14. Set the charge safety timer (see Figure 16).

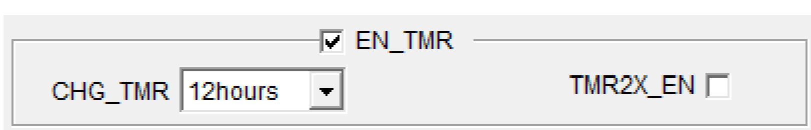


Figure 16: Charge Safety Timer Configuration

   a. EN_TMR: When EN_TMR is checked, the timer function is enabled; when unchecked, the timer function is disabled.

b. CHG_TMR: Sets the total time for the charge safety timer.

c. TMR2X_EN: When checked, TMR2X_EN enables the 2x timer function; when unchecked, the 2x timer function is disabled.

15. Set the NTC functions (see Figure 17).

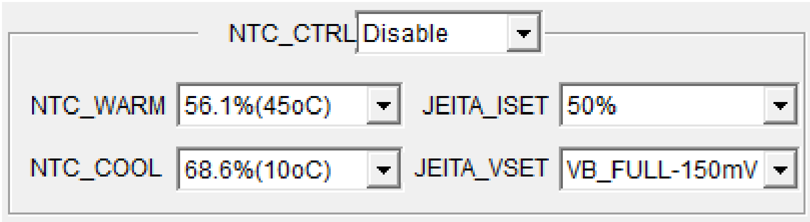


Figure 17: NTC Configuration

a. NTC_CTRL: Selects the NTC type.

b. NTC_WARM: Sets the NTC warm temperature threshold.

c. NTC_COOL: Sets the NTC cool temperature threshold.

d. JEITA_ISET: Sets the JEITA low temperature current.

e. JEITA_VSET: Sets the JEITA high temperature voltage.

16. Click the “Write all” button the update the register settings. Then turn the input power supply on. The changes should be automatically updated.

Setting OTG Functions

1. Turn the power supply off and disconnect it from VIN to PGND. Connect the load from VIN to PGND.
2. Set the jumpers following Table 3 on page 4. Then set the OTG mode parameters.
3. Plug the battery in or turn the battery simulator on. Ensure that the EVKT-USBI2C-02 is successfully connected to the computer and evaluation board.
4. Set the battery cell count (see Figure 18).

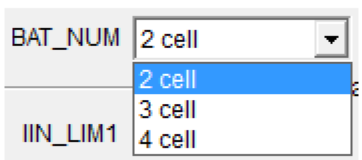


Figure 18: Battery Cell Count Configuration

a. Ensure that the value set in the register is consistent with the real battery pack value.

5. Set the OTG output voltage (see Figure 19).

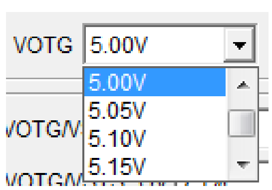


Figure 19: OTG Output Voltage Configuration

6. Set the OTG output current limit (see Figure 20).

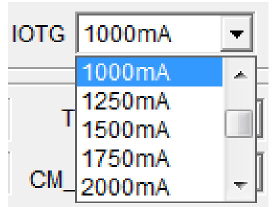


Figure 20: OTG Output Current Limit Configuration

7. Click the "Write all" button to update the register settings.
8. Enable OTG mode (see Figure 21)

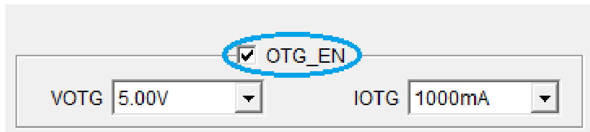


Figure 21: Enable OTG Mode

   a. OTG_EN: If OTG_EN is checked, the OTG function is enabled; if unchecked, the OTG function is disabled.

9. Enable the OTG function then verify the voltages from VIN to PGND.

Additional Parameters

1. Select the inductors.
   a. If the power is below 65W, small 1µH Inductors (e.g. the HTEP32251B-1R0MIR-89; 1µH, DCR = 20mΩ, I_{SAT} = 7A) are sufficient. If the power exceeds 65W, recommend to use inductors with a saturation current exceeding 9A (e.g. the 74437349015; 1.5µH, DCR = 8.6mΩ, I_{SAT} = 14.5A).
2. Set the battery impedance compensation in charge mode (see Figure 22).

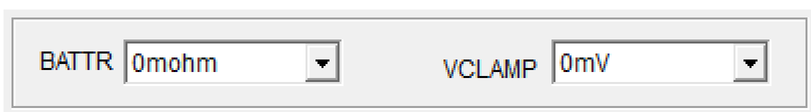


Figure 22: Battery Impedance Compensation

   a. BATTTR: Sets the resistance for battery impedance compensation.
   b. VCLAMP: Sets the maximum regulated voltage for battery impedance compensation.

3. Set the PROCHOT and PSYS functions (see Figure 23).

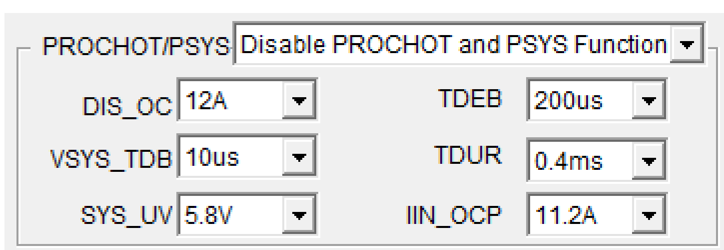


Figure 23: PROCHOT And PSYS Function

   a. PROCHOT/PSYS: Enables the PROCHOT assertion and PSYS function.
   b. DIS_OC: Sets the discharge over-current threshold for PROCHOT assertion.
   c. SYS_UV: Sets the low system voltage threshold for PROCHOT assertion.

   d. IIN_OCP: Sets the input over current threshold for PROCHOT assertion.
   e. VSYS_TDB: Sets the debounce time before the PROCHOT asserts for V_{SYS_UV} only.
   f. TDEB: Sets the debounce time before the next PROCHOT asserts.
   g. TDUR: Sets the duration time once the PROCHOT asserts.

4. Set the remaining controls (see Figure 24)

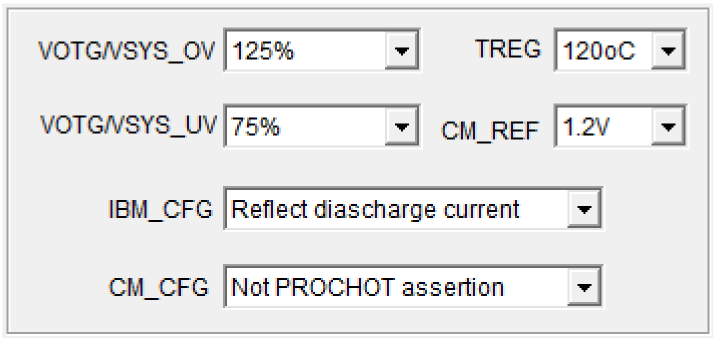


Figure 24: Other Configuration

   a. VOTG/VSYS_OV: Sets the over-voltage protection (OVP) threshold for V_{SYS} and V_{OTG}.
   b. VOTG/VSYS_UV: Sets the under-voltage lockout (UVLO) threshold for V_{SYS} and V_{OTG}.
   c. IBM_CFG: Enables the IBM pin to reflect the charge current or the discharge current.
   d. CM_CFG: Determines whether PROCHOT asserts if the independent comparator outputs low.
   e. TREG: Sets the thermal regulation threshold.
   f. CM_REF: Sets the reference for the independent comparator.

5. Configure the watchdog timer (see Figure 25).

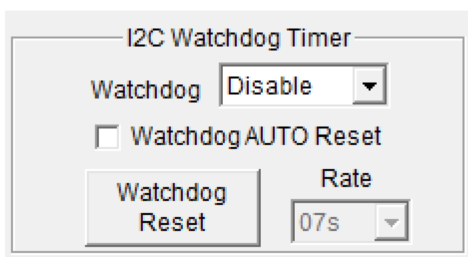


Figure 25: Watchdog Configuration

   a. Watchdog: Enables the watchdog function.
   b. Watchdog AUTO Reset: If Watchdog AUTO Reset is checked, the GUI resets the watchdog automatically; if unchecked, the GUI does not reset the watchdog.
   c. Rate: The interval time for the watchdog auto reset.
   d. Click "Watchdog Reset" to reset the watchdog once.

6. Set the voltage, current, and PSYS monitors (see Figure 26).

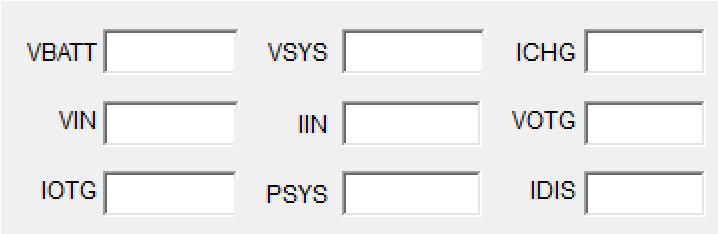


Figure 26: ADC Results

   a. The textboxes indicate the ADC results for the voltages and currents, as well as the calculation result for system power.

7. Configure the status and fault monitor (see Figure 27).

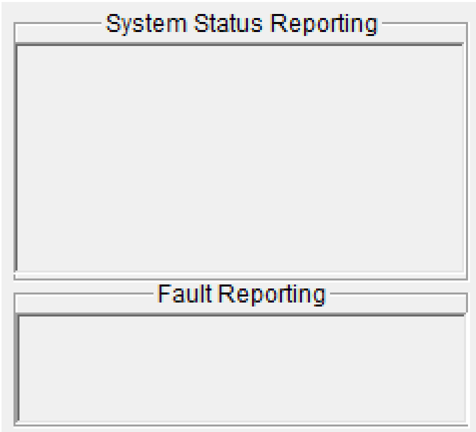


Figure 27: Status and Fault Monitor

   a. The textboxes report the statuses and faults.

EVALUATION BOARD SCHEMATIC

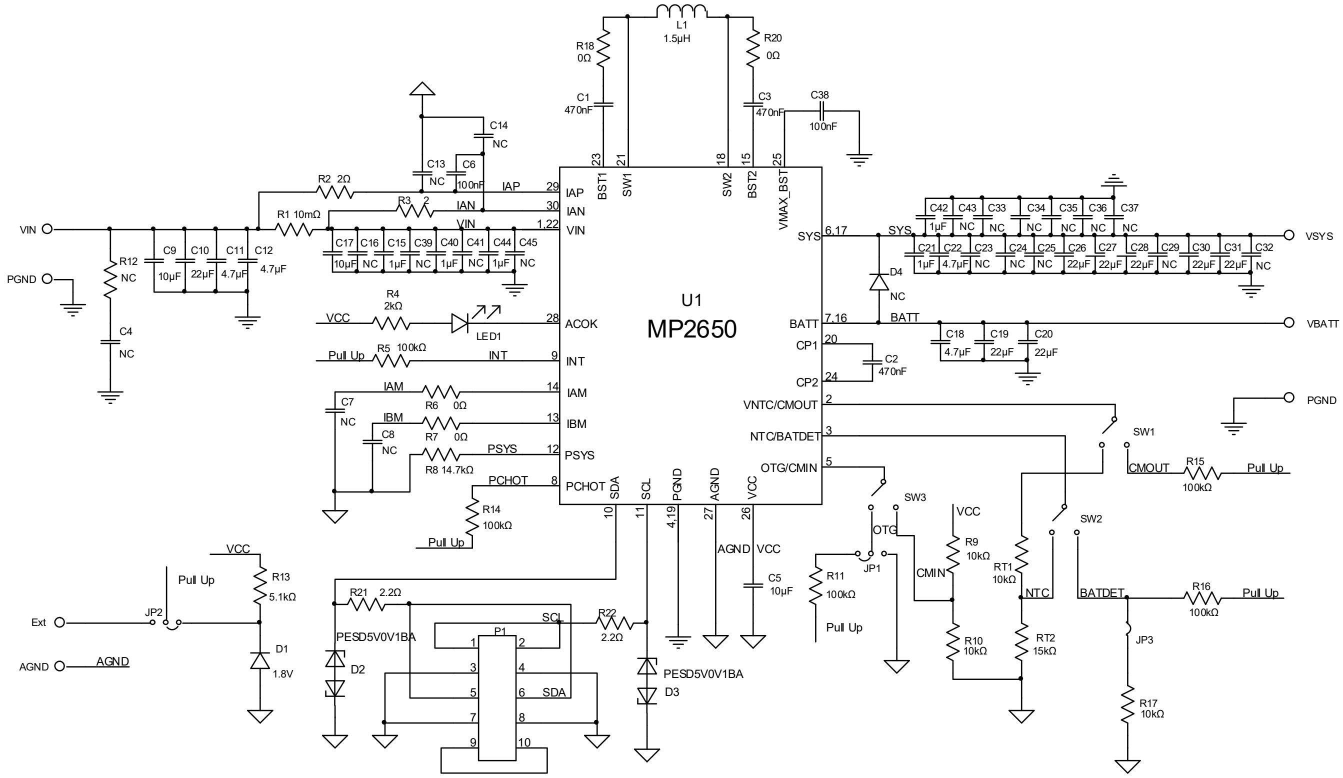


Figure 28: Evaluation Board Schematic

EV2650-V-01A BILL OF MATERIALS

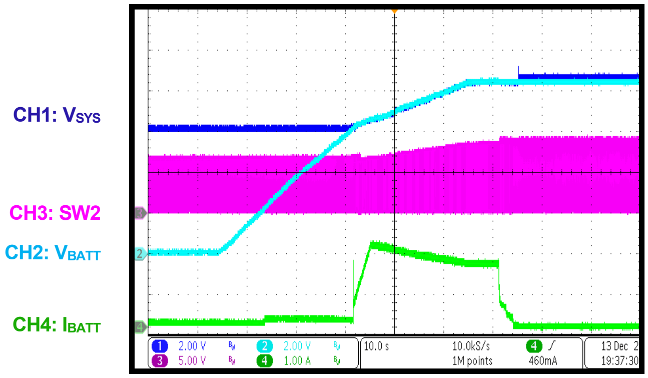
Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
3	C1, C2, C3	470nF	Capacitor, 25V, X5R	0603	Murata	GRM188R61E474KA12D
5	C15, C21, C40, C42, C44	1µF	Ceramic capacitor, 25V, X7R	0603	Murata	GRM188R71E105KA12D
1	C5	10µF	Ceramic capacitor, 25V, X5R	0603	Murata	GRM188R61E106MA73D
2	C9, C17	10µF	Capacitor, 25V, X5R	0805	Murata	GRM21BR61E106KA73
4	C11, C12, C18, C22	4.7µF	Capacitor, 25V, X7R	0805	Murata	GRM21BR71E475KA73L
8	C10, C19, C20, C26, C27, C28, C30, C31	22µF	Capacitor, 25V, X5R	0805	Murata	GRM21BR61E226ME44L
2	C6, C38	100nF	Capacitor, 50V, X7R	0603	Murata	GRM188R71H104KA93D
1	D1	1.8V	Diode, 1.8V, 500µA	SOD-323	Central Semiconductor	8CMDZ1L8TR-LF
2	D2, D3	5.0V	ESD diode	SOD-323	NXP	PESD5V0V1BA
1	LED1	Green	Green LED	0805	BaiHong	BL-HGE35A-AV-TRB
1	L1	1.5µH	Inductor, 1.5µH, 8.6mΩ, 14.5A	SMD	Wurth	74437349015
1	R1	10mΩ	Film resistor, 1%, 1W	2512	CYNTEC	RL3264-6-R010-FN
2	R2, R3	2Ω	Film resistor, 5%	0603	LIZ	CR0603JA02R0G
4	R6, R7, R18, R20	0Ω	Resistor, 1%	0603	Yageo	RC0603FR-070RL
1	R4	2kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-072KL
5	R5, R11, R14, R15, R16	100kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-07100KL
1	R8	14.7kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-0714K7L
4	R9, R10, R17, RT1	10kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-0710KL
2	R21, R22	2.2Ω	Film resistor, 1%	0603	Yageo	RC0603FR-072R2L
1	R13	5.1kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-075K1L
1	RT2	15kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-0715KL
1	U1	MP2650	Charger IC	QFN-30 (4mmx 5mm)	MPS	MP2650GV

EVB TEST RESULTS

Performance curves and waveforms are tested on the evaluation board. V_{IN} = 5V, V_{BATT} = 0V to 8.4V, I_{CC} = 2A, I_{IN_LIM1} = I_{IN_LIM2} = 3A, V_{IN_MIN} = 4.5V, f_{SW} = 600kHz, L = 1.5µH, T_A = 25°C, unless otherwise noted.

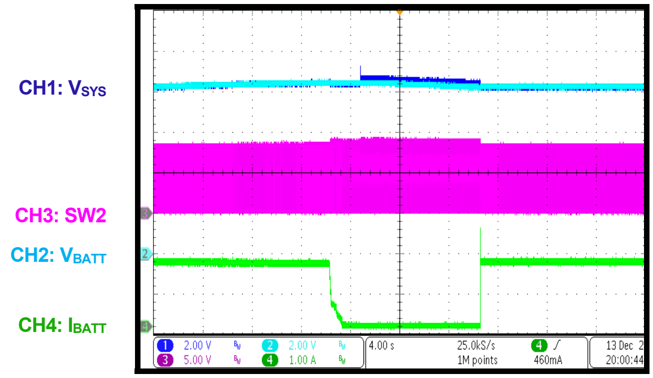
Battery Charge Curve

V_{IN} = 5V, V_{BATT_PRE} = 6.8V, V_{BATT_REG} = 8.4V



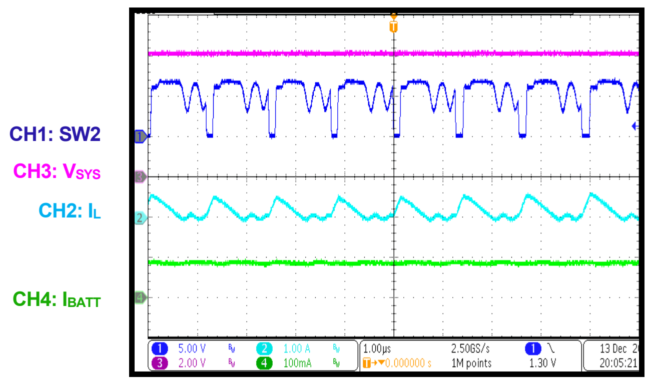
Auto-Recharge

V_{IN} = 5V, V_{BATT_PRE} = 6.8V, V_{BATT_REG} = 8.4V



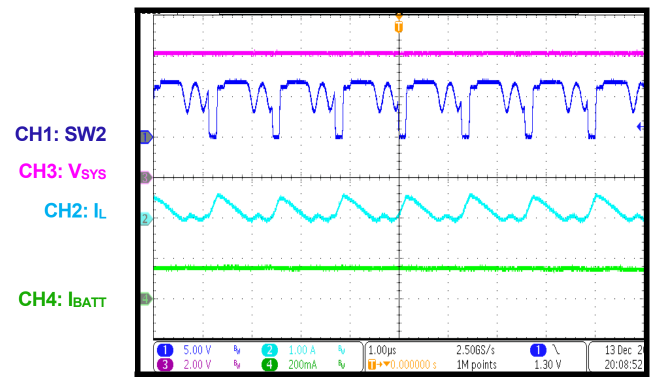
TC Charge Steady State

V_{IN} = 5V, V_{BATT} = 1V



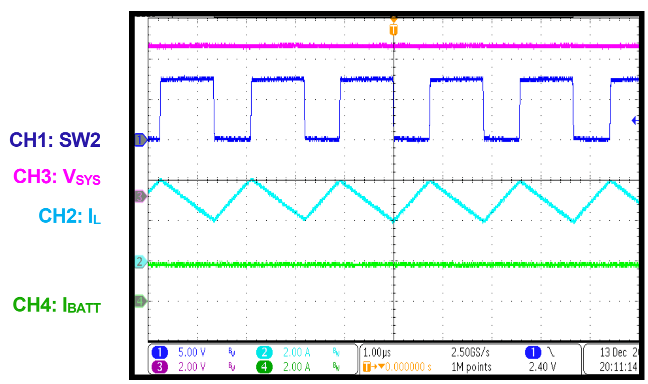
Pre-Charge Steady State

V_{IN} = 5V, V_{BATT} = 5.8V



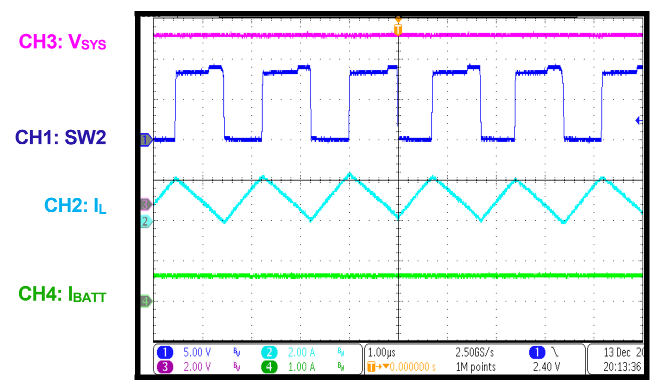
CC Charge Steady State

V_{IN} = 5V, V_{BATT} = 7.4V



CV Charge Steady State

V_{IN} = 5V, V_{BATT} = 8.4V

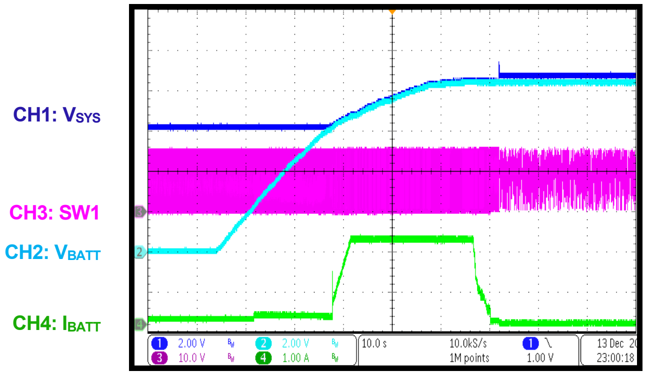


EVB TEST RESULTS

Performance curves and waveforms are tested on the evaluation board. V_{IN} = 15V, V_{BATT} = 0V to 8.4V, I_{CC} = 3A, I_{IN_LIM1} = I_{IN_LIM2} = 3A, V_{IN_MIN} = 4.5V, f_{SW} = 600kHz, L = 1.5µH, T_A = 25°C, unless otherwise noted.

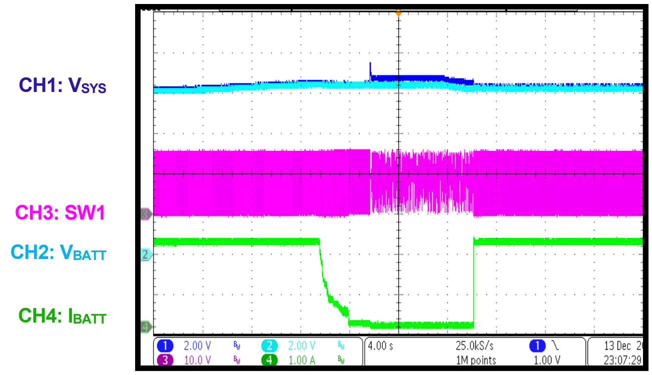
Battery Charge Curve

V_{IN} = 15V, V_{BATT_PRE} = 6.8V, V_{BATT_REG} = 8.4V



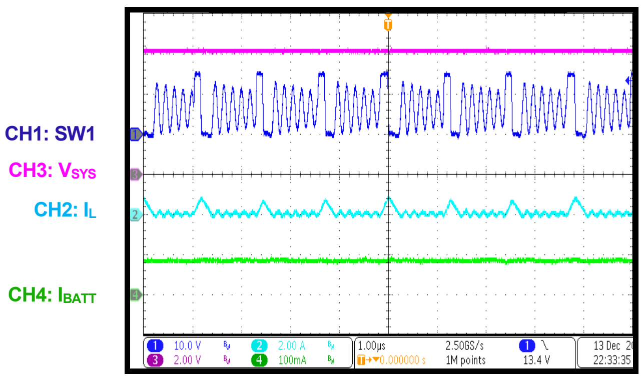
Auto-Recharge

V_{IN} = 15V, V_{BATT_PRE} = 6.8V, V_{BATT_REG} = 8.4V



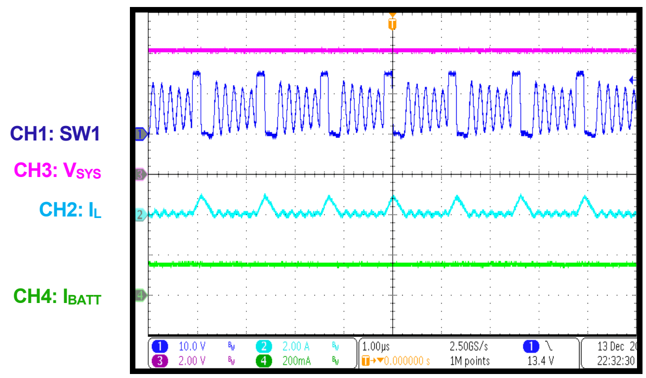
TC Charge Steady State

V_{IN} = 15V, V_{BATT} = 1V



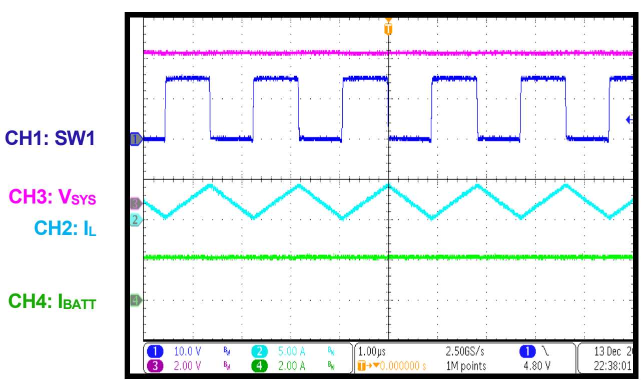
Pre-Charge Steady State

V_{IN} = 15V, V_{BATT} = 5.8V



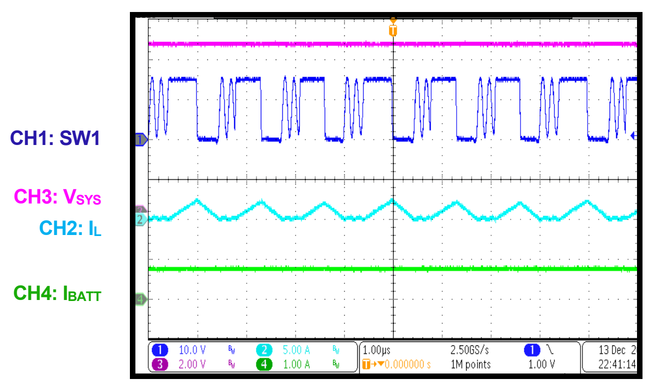
CC Charge Steady State

V_{IN} = 15V, V_{BATT} = 7.4V



CV Charge Steady State

V_{IN} = 15V, V_{BATT} = 8.4V

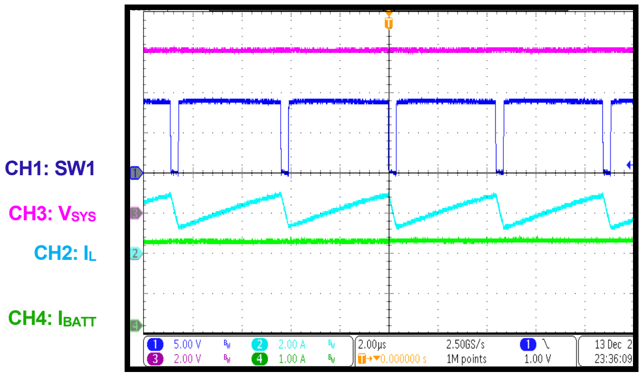


EVB TEST RESULTS

Performance curves and waveforms are tested on the evaluation board. V_{IN} = 5V to 15V, V_{BATT} = 0V to 8.4V, I_{CC} = 2A, I_{IN_LIM1} = I_{IN_LIM2} = 3A, V_{IN_MIN} = 4.5V, f_{SW}=600kHz, L = 1.5µH, T_A = 25°C, unless otherwise noted.

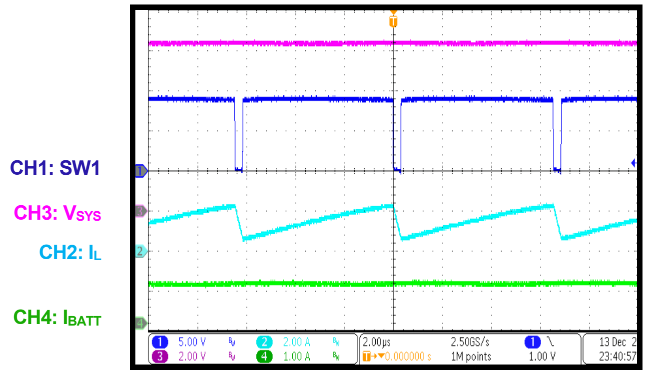
CC Charge Steady State

V_{IN} = 9V, V_{BATT} = 8V, I_{IN_LIM1} = I_{IN_LIM2} = 5A, I_{SYS} = 2A



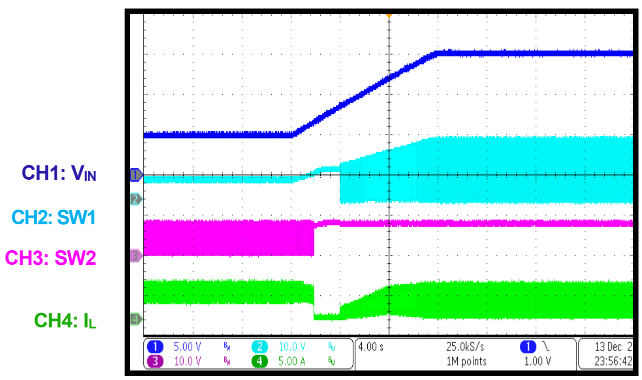
CV Charge Steady State

V_{IN} = 9V, V_{BATT} = 8.4V, I_{IN_LIM1} = I_{IN_LIM2} = 5A, I_{SYS} = 2A



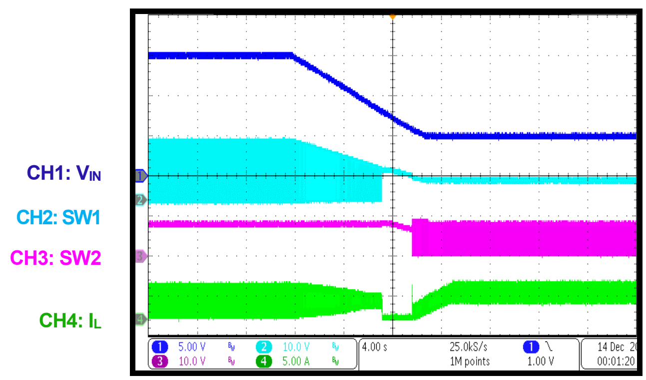
Boost to Buck Transition

V_{IN} = 5V to 15V, V_{BATT} = 7.4V



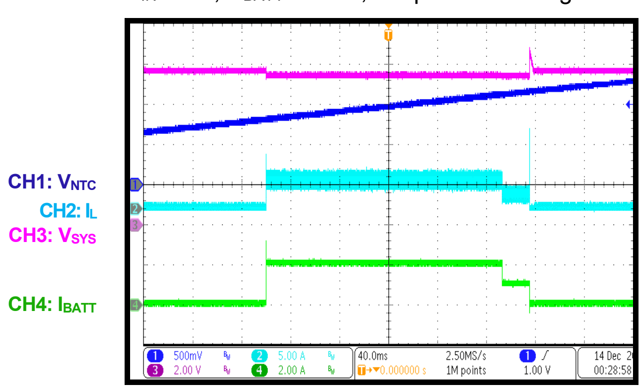
Buck to Boost Transition

V_{IN} = 15V to 5V, V_{BATT} = 7.4V



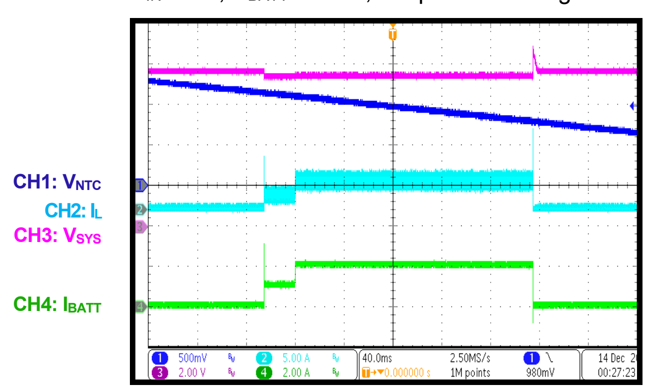
NTC

V_{IN} = 5V, V_{BATT} = 7.4V, temperature falling



NTC

V_{IN} = 5V, V_{BATT} = 7.4V, temperature rising

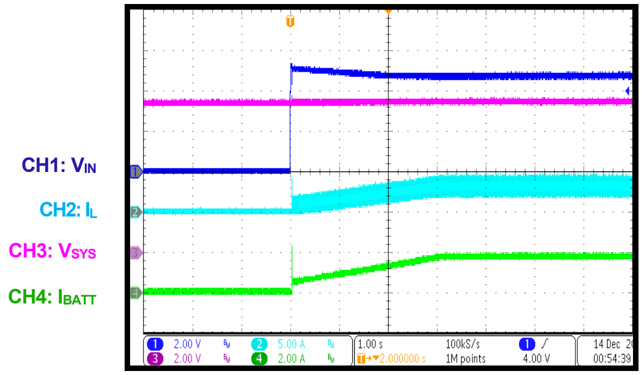


EVB TEST RESULTS

Performance curves and waveforms are tested on the evaluation board. V_{IN} = 5V, V_{BATT} = 0V to 8.4V, I_{CC} = 2A, I_{IN_LIM1} = I_{IN_LIM2} = 3A, V_{IN_MIN} = 4.5V, f_{SW} = 600kHz, L = 1.5µH, T_A = 25°C, unless otherwise noted.

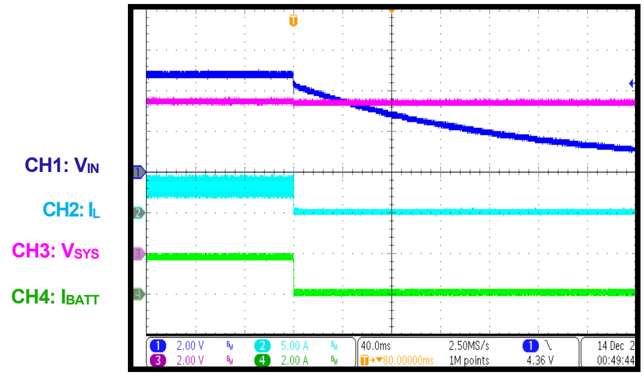
VIN Start-Up

V_{IN} = 5V, V_{BATT} = 7.4V



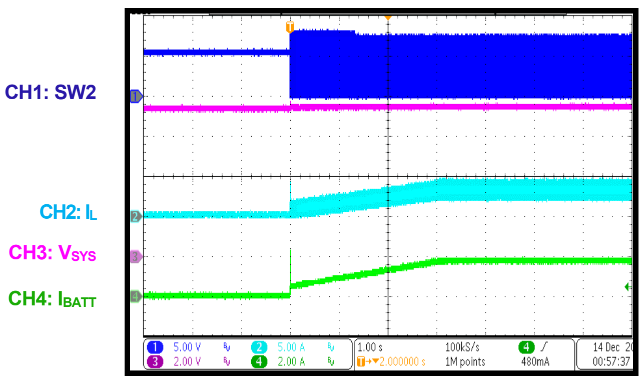
VIN Shutdown

V_{IN} = 5V, V_{BATT} = 7.4V



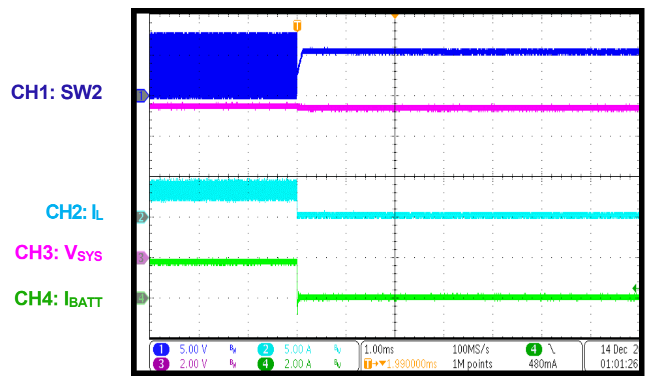
EN On

V_{IN} = 5V, V_{BATT} = 7.4V



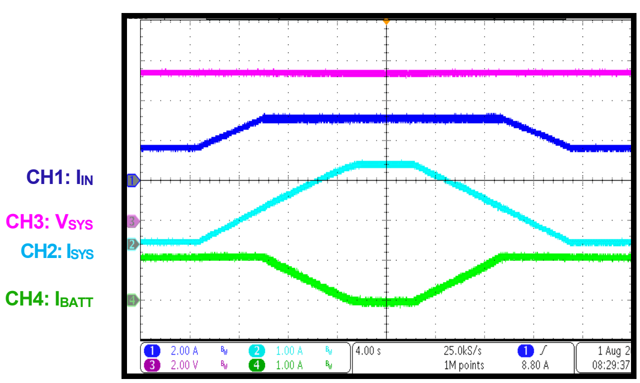
EN Off

V_{IN} = 5V, V_{BATT} = 7.4V



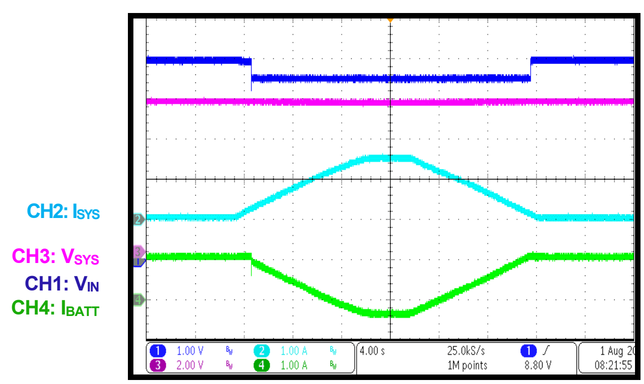
Input Current Limit

V_{IN} = 5V, V_{BATT} = 7.4V, I_{CC} = 1A



Input Voltage Limit

V_{IN} = 5V (2A), V_{BATT} = 7.4V, I_{CC} = 1A

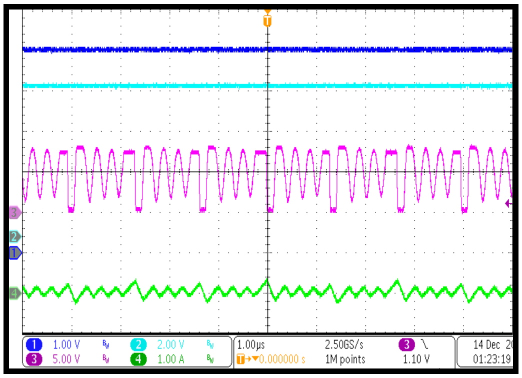


EVB TEST RESULTS

Performance curves and waveforms are tested on the evaluation board. V_{IN_OTG} = 5V, V_{BATT} = 0V to 8.4V, I_{OLIM} = 3A, f_{SW} = 600kHz, L = 1.5µH, T_A = 25°C, unless otherwise noted.

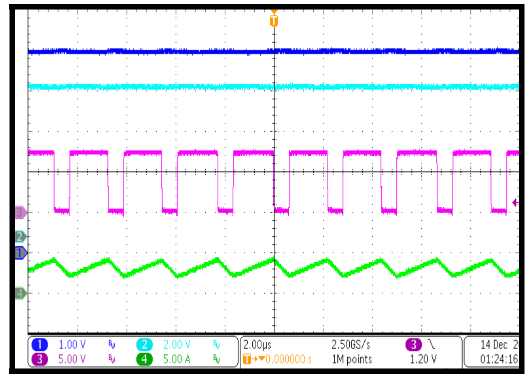
OTG Steady State

V_{BATT} = 7.4V, I_{OTG} = 0A



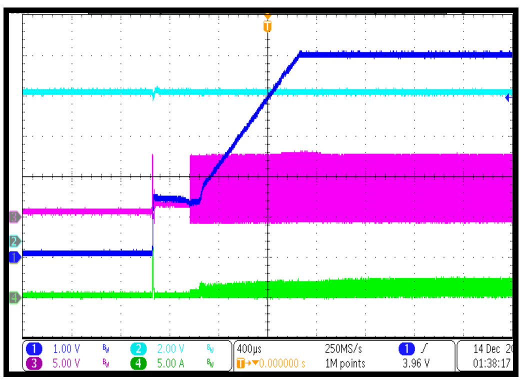
OTG Steady State

V_{BATT} = 7.4V, I_{OTG} = 3A



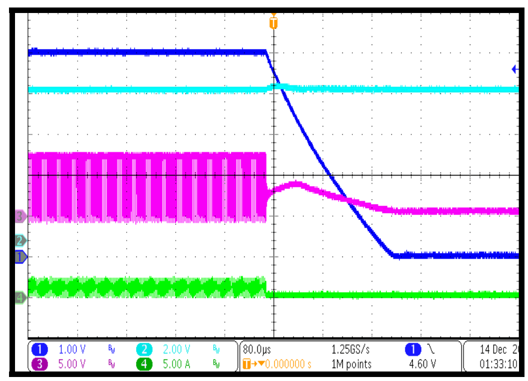
OTG EN On

V_{BATT} = 7.4V, I_{OTG} = 1A



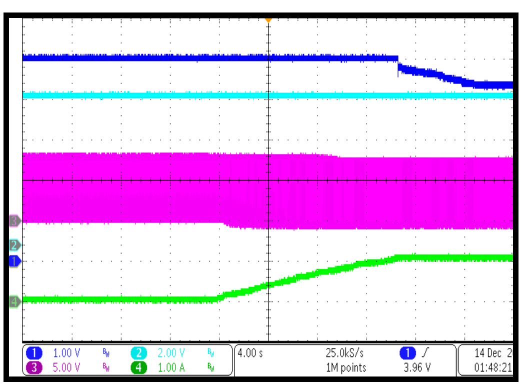
OTG EN Off

V_{BATT} = 7.4V, I_{OTG} = 1A



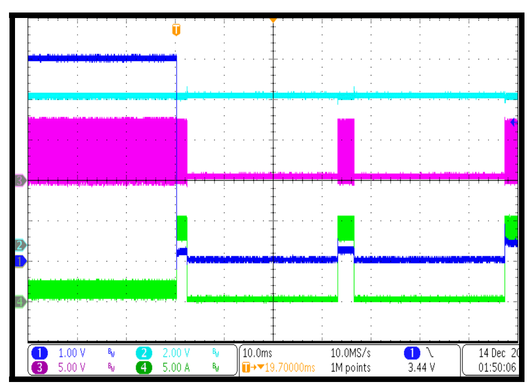
OTG Output Current Limit

V_{BATT} = 7.4V, I_{OLIM} = 1A



OTG SCP

V_{BATT} = 7.4V, I_{OTG} = 1A



PCB LAYOUT

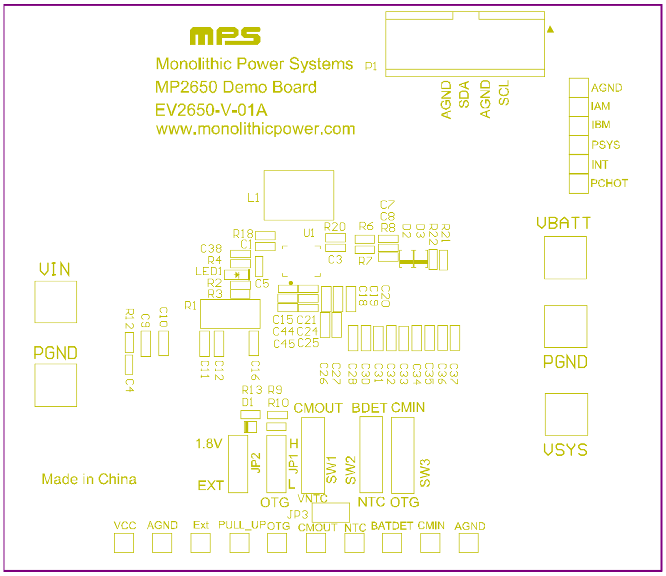


Figure 29: Top Silk

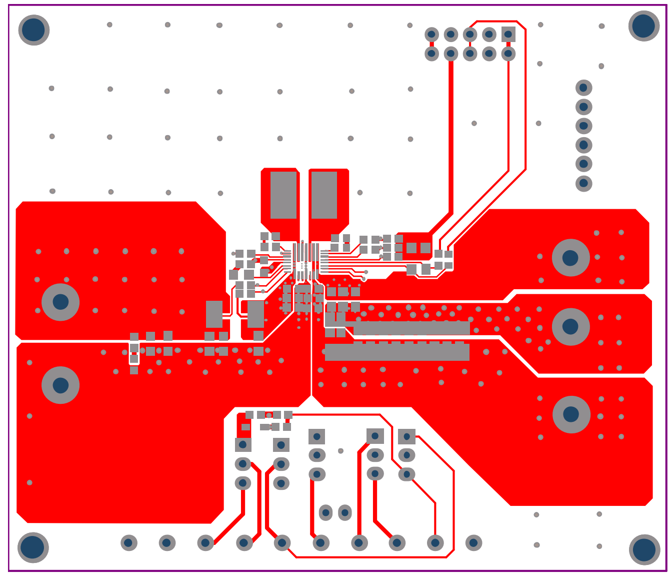


Figure 30: Top Layer

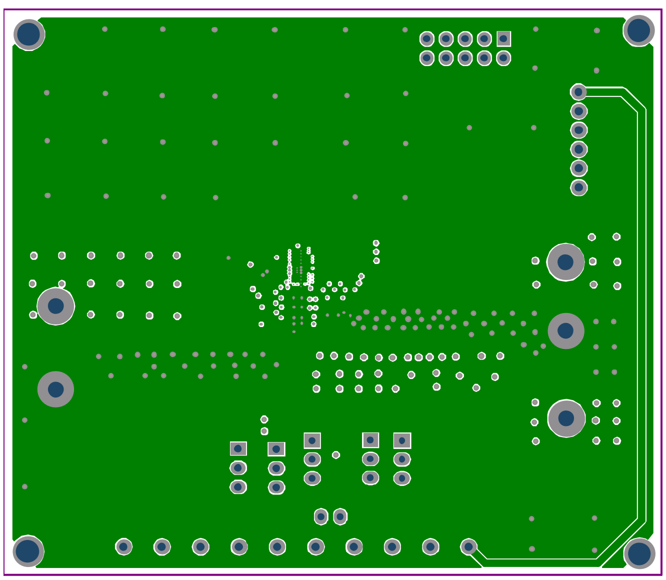


Figure 31: Mid-Layer 1

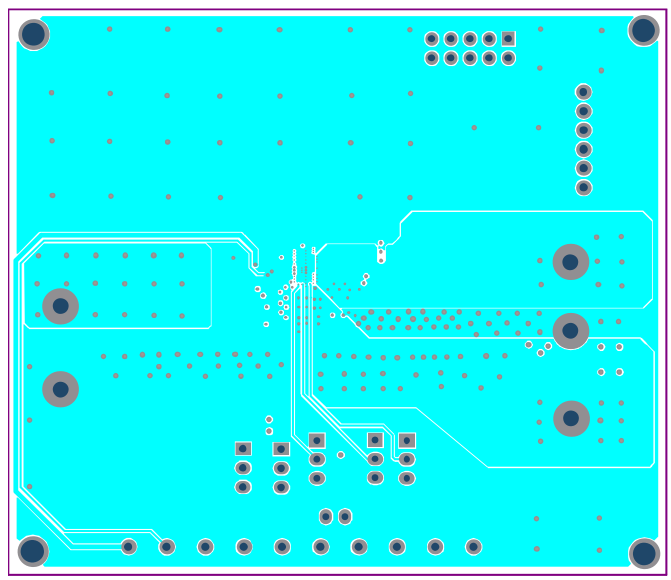


Figure 32: Mid-Layer 2

PCB LAYOUT *(continued)*

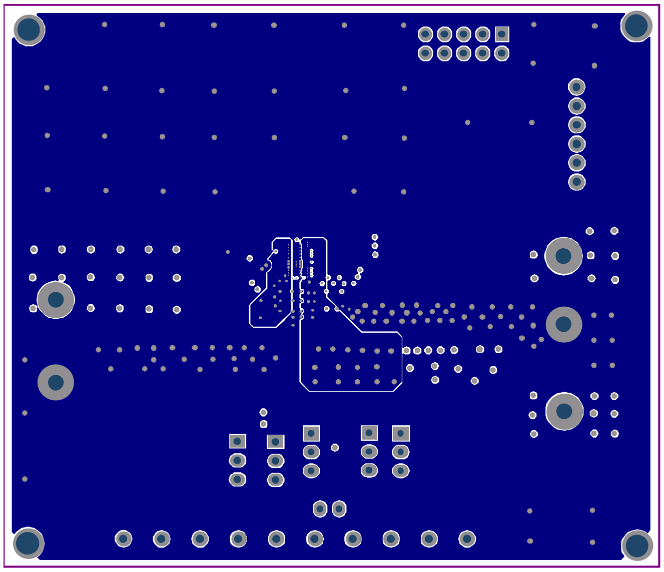


Figure 33: Mid-Layer 3

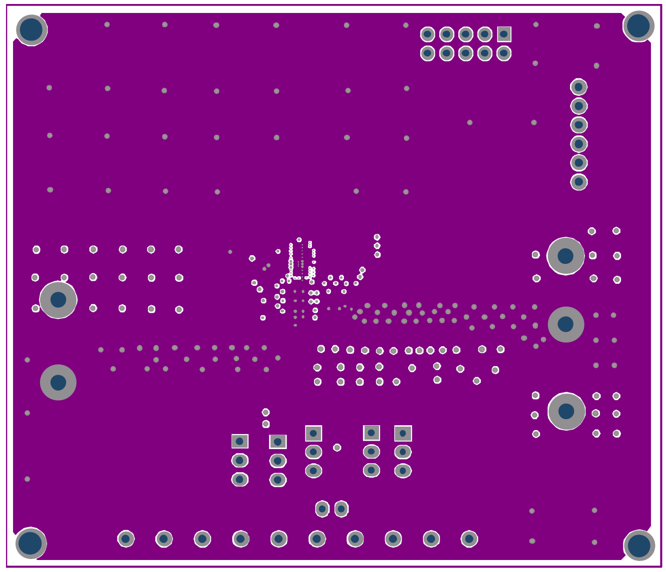


Figure 34: Mid-Layer 4

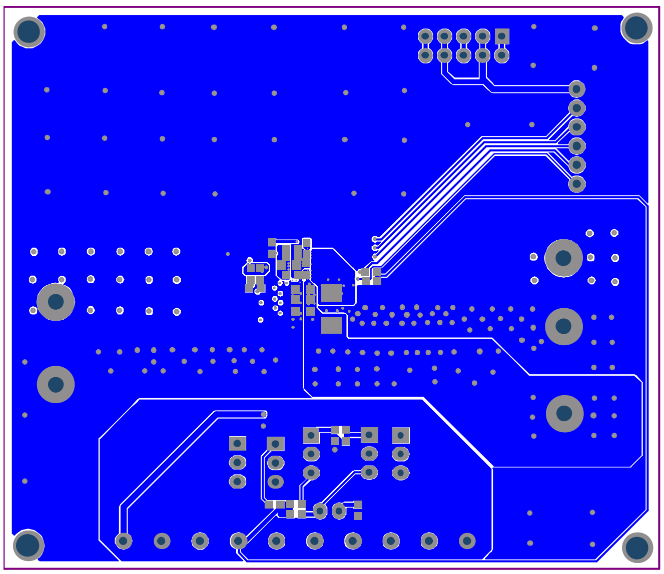


Figure 35: Bottom Layer

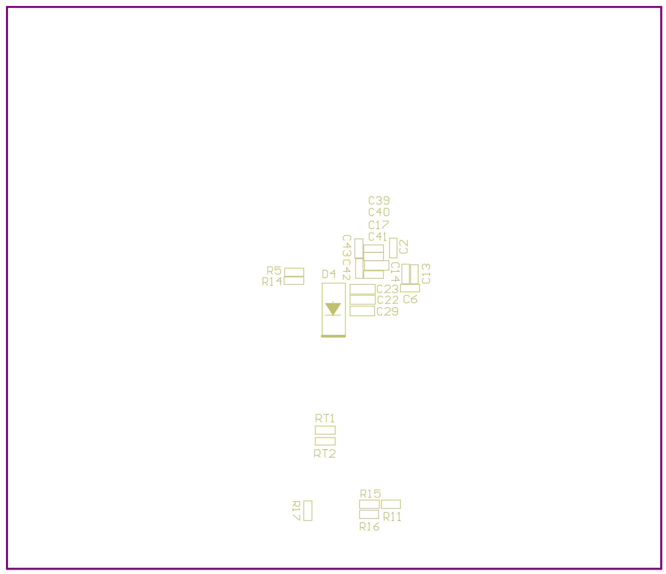


Figure 36: Bottom Silk

PCB Layout Guidelines

Efficient PCB layout is critical for specified nosie, efficiency, and stability requirements. A 4-layer PCB (or greater) is recommended. For the best performance, refer to Figure 37 and follow the guidelines below:

1. The VMAX_BST capacitor should be connected to PGND. Place one 100Ω resistor in series with the VMAX_BST capacitor.
2. Connect AGND to PGND, and to each decoupling capacitor via a single-point connection.
3. Place a 470nF capacitor between the CP1 and CP2.
4. Place the VCC capacitor as close as possible to the VCC and AGND pins.
5. Use a Kelvin connection for the input current-sense resistor.
6. Place the capacitors between VIN and PGND, as close as possible to the pins.
7. Use CM and DM filter for the input current sense.

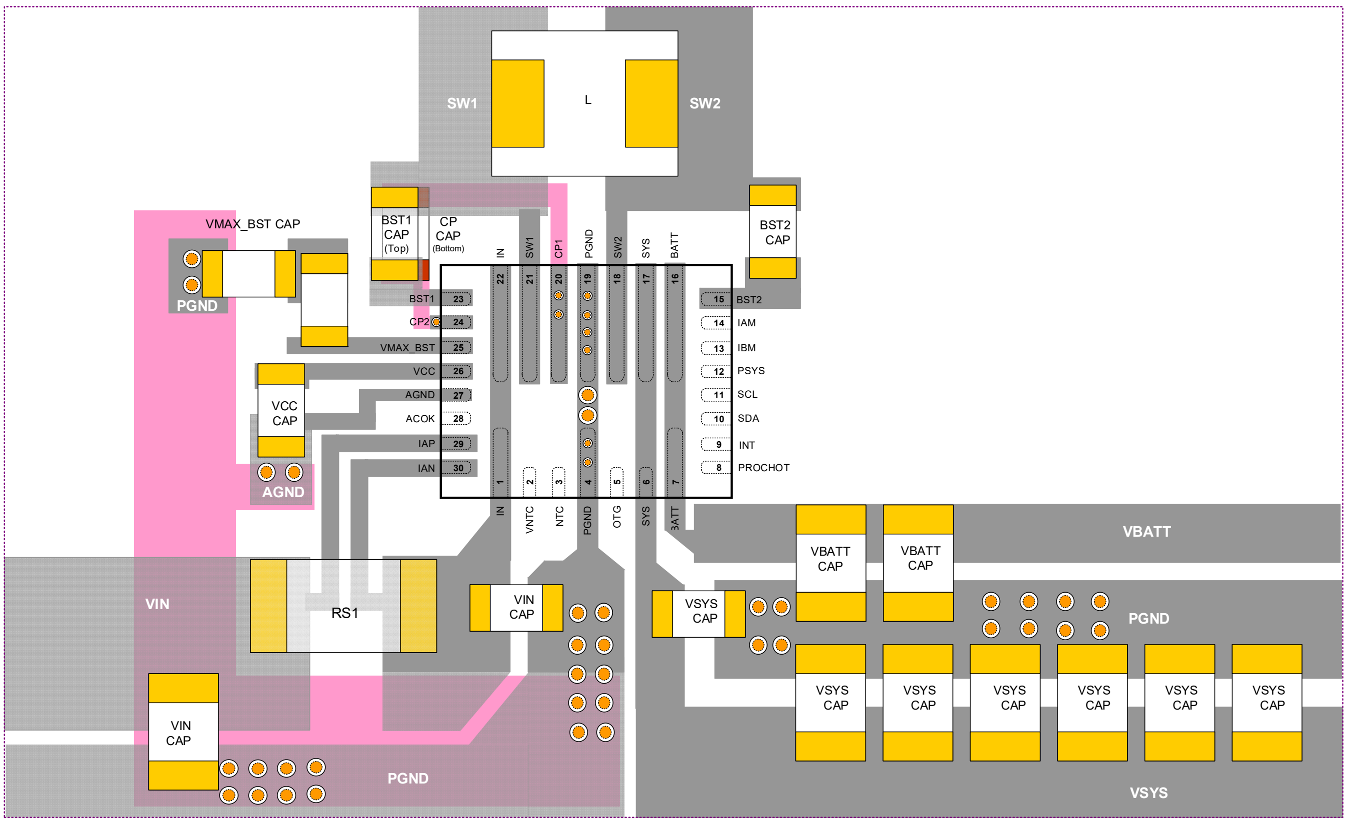


Figure 37: Recommended PCB Layout

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	4/4/2022	Initial Release	-