

**LTCC Multi Layer Ceramic Chip Antenna- 3216 (1206) size****- AMANT3216110Y1T****FEATURES**

1. Surface Mounted Devices with a small dimension of 3.2 X 1.6 X1.1 mm<sup>3</sup> meet future miniaturization trend.
2. LTCC process
3. High stability in Temperature / Humidity Change
4. Multilayer ceramic antenna (chip antenna)
5. Automotive, Qualified to AEC-Q200

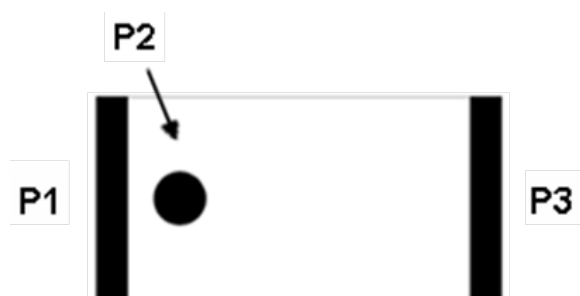
**APPLICATIONS**

1. 6240 – 8500 MHz working Frequency

**Recommended Link Parts**

Product Category	Walsin PN	Remark
capacitor	RTxxN	high Q MLCC for fine tune matching (automotive version)

## CONSTRUCTION



PIN	Connection
1	Feeding
2	Identification Mark
3	Soldering terminal

## DIMENSIONS

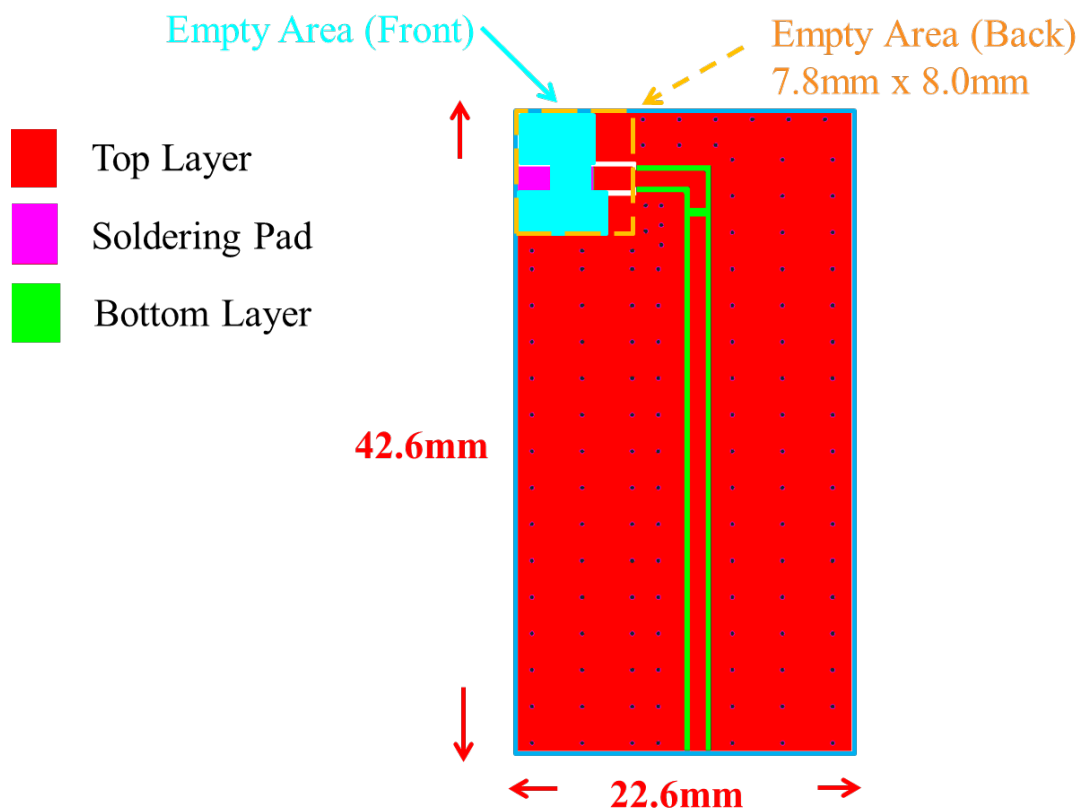
Figure	Symbol	Dimension (mm)
	L	$3.20 \pm 0.20$
	W	$1.60 \pm 0.10$
	T	$1.10 \pm 0.10$
	A	$0.25 \pm 0.15$

**ELECTRICAL CHARACTERISTICS**

<b>AMANT3216110Y1T</b>	<b>Specification</b>
Working Frequency Range	6240 - 8500 MHz
Fc	7370 MHz
VSWR	2 max.
Gain	3 – 4.5 dBi
Efficiency	70 – 80 %
Power Capacity	3 W max.
Maximum Input Power	5 Watts for 5 minutes
Polarization	Linear
Azimuth Beamwidth	Omni - Directional
Moisture sensitivity levels	MSL is LEVEL 1 (Refer to : IPC/JEDEC J-STD-020)
HBM ESD	Pass 1KV on all pins (Base on AEC-Q200-002)
MM ESD	Pass 200V (Base on EIA/JESD22-A115)
<b>Operating &amp; Storage Condition (Component)</b> Operation Temperature Range: -55 ~ +125 °C Storage Temperature Range: -55 ~ +125 °C	
<b>Storage Condition before Soldering (Included packaging material)</b> Storage Temperature Range: +5 ~ +40 °C Humidity: 30 to 70% relative humidity	

**SOLDER LAND PATTERN DESIGN**

Figure

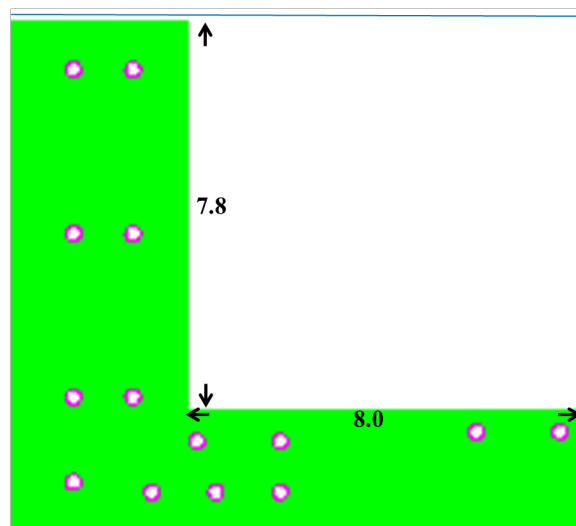
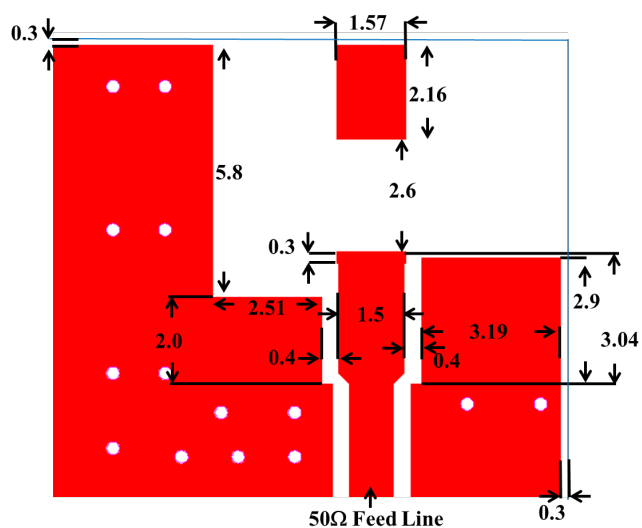


Antenna on Test Board ( Thickness 0.8 mm)

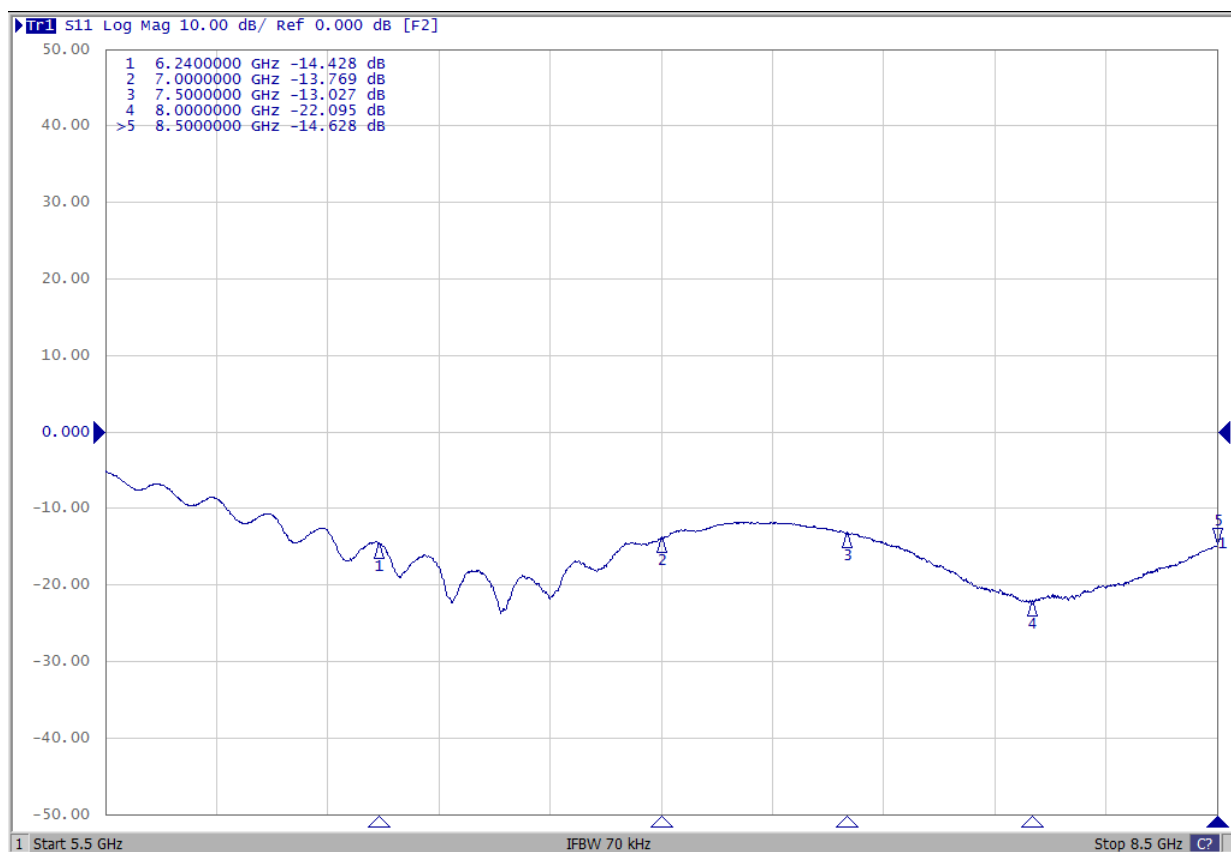
Unit : mm

Front

Back

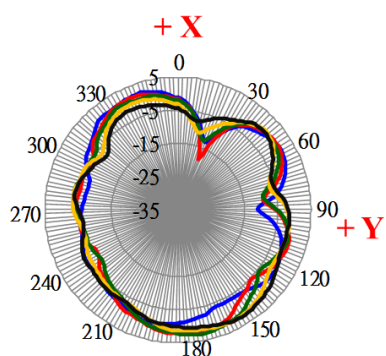
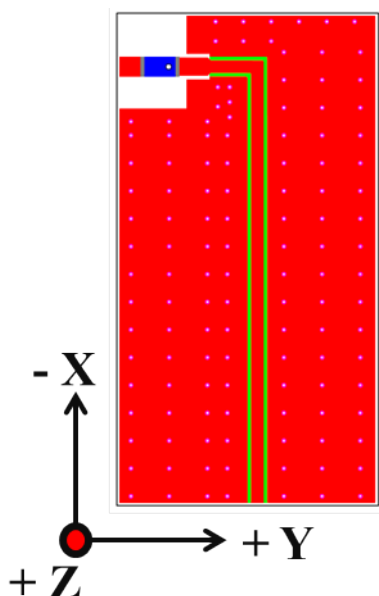


Antenna S11 on Test Board

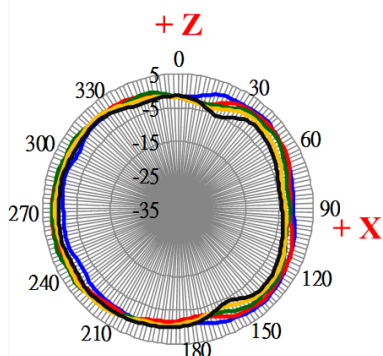
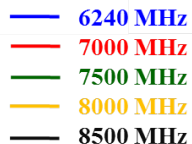


## RADIATION PATTERNS

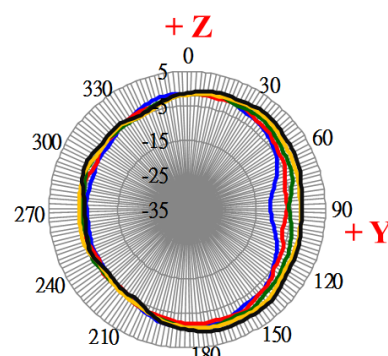
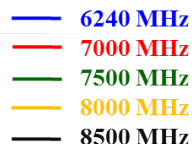
Radiation Pattern and Gain were dependent on measurement board design. The specification of AMANT3216110Y1T antenna was measured based on the PCB size and installation position as shown in the below figure Test Board.



XY Plane



ZX Plane



ZY Plane