Datasheet

Operational Amplifiers

Input/Output Rail to Rail Low Input Offset Voltage Operational Amplifier

BD5291GWL

General Description

The BD5291GWL is a single operational amplifier with Input/Output Rail-to-Rail. This features Input/Output Rail-to-Rail operation with a supply voltage as low as 1.7 V, wide Input/Output range when operated at low voltage. In addition, ultra low input bias current (1 pA typical) due to MOSFET input, it is suitable for using sensor amplifiers.

Features

- Low Operating Supply Voltage
- Input/Output Rail-to-Rail
- Low Input Offset Voltage
- High Common Mode Rejection Ratio
- High Slew Rate
- Small Package WLCSP

Applications

- Buffer
- Active Filter
- Sensor Amplifier
- Battery-powered Equipment

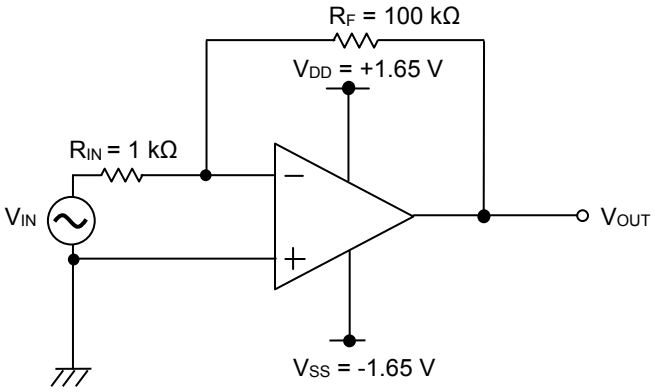
Key Specifications

- Operating Supply Voltage Range (Single Supply): 1.7 V to 5.5 V
- Slew Rate: 2.5 V/µs (Typ)
- Operating Temperature Range: -40 °C to +85 °C
- Input Common-mode Voltage Range: V_{SS} to V_{DD}
- Input Offset Voltage: ±2.5 mV (Max)
- Common-mode Rejection Ratio: 70 dB (Min)

Package

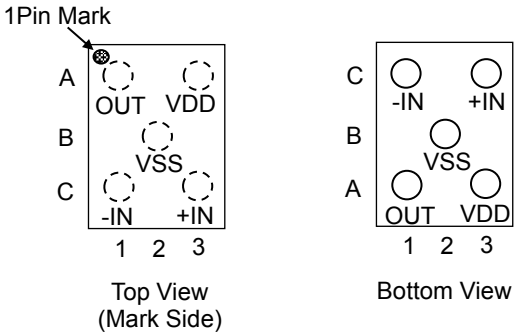
	W (Typ) x D (Typ) x H (Max)
UCSP50L1 (5Pin)	0.84 mm x 1.14 mm x 0.55 mm

Typical Application Circuit



$$V_{OUT} = -\frac{R_F}{R_{IN}} V_{IN}$$

Pin Configuration



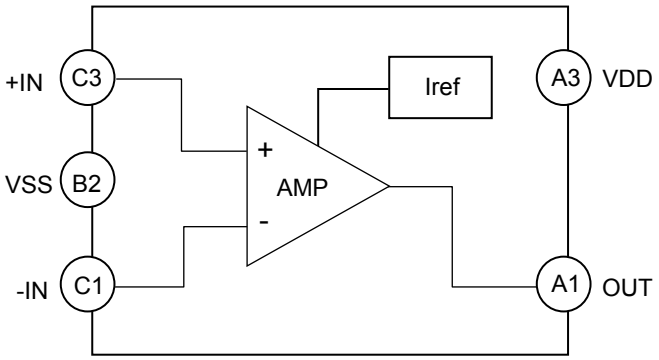
Land Number	Pin Name
A1	OUT
A3	VDD
B2	VSS
C1	-IN
C3	+IN

Figure 1. Pin Configuration

Pin Description

Pin No.	Pin Name	Function
A1	OUT	Output
A3	VDD	Positive power supply
B2	VSS	Negative power supply / Ground
C1	-IN	Inverting input
C3	+IN	Non-inverting input

Block Diagram



Description of Blocks

1. AMP:
   This block is a full-swing output operational amplifier with class-AB output circuit and Rail-to-Rail differential input stage.

2. Iref:
   This block supplies reference current which is needed to operate AMP block.

Ordering Information

B D 5 2 9 1 G W L	-	E2

Part Number	Package	Packaging and forming specification
BD5291GWL	GWL: UCSP50L1	E2: Embossed tape and reel (UCSP50L1)

Absolute Maximum Ratings(Ta = 25 °C)

Parameter	Symbol	Ratings	Unit
Supply Voltage	V_{DD}-V_{SS}	7	V
Differential Input Voltage*(Note 1)*	V_{ID}	V_{DD} - V_{SS}	V
Input Common-mode Voltage Range	V_{ICMR}	(V_{SS} – 0.3) to (V_{DD} + 0.3)	V
Input Current*(Note 2)*	I_I	±10	mA
Storage Temperature Range	Tstg	-55 to +150	°C
Maximum Junction Temperature	Tjmax	150	°C

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

(Note 1) The differential input voltage indicates the voltage difference between inverting input and non-inverting input. The input pin voltage is set to V_{SS} or more.

(Note 2) An excessive input current will flow when input voltages of more than V_{DD} + 0.6 V or less than V_{SS} - 0.6 V are applied. The input current can be set to less than the rated current by adding a limiting resistor.

Thermal Resistance *(Note 3)*

Parameter	Symbol	Thermal Resistance (Typ)	Unit
		2s2p*(Note 5)*	
UCSP50L1			
Junction to Ambient	θ_{JA}	322.5	°C/W
Junction to Top Characterization Parameter*(Note 4)*	Ψ_{JT}	4.0	°C/W

(Note 3) Based on JESD51-2A (Still-Air).

(Note 4) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.

(Note 5) Using a PCB board based on JESD51-9.

Layer Number of Measurement Board	Material	Board Size
4 Layers	FR-4	114.5 mm x 101.5 mm x 1.6 mmt

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 µm	99.5 mm x 99.5 mm	35 µm	99.5 mm x 99.5 mm	70 µm

Recommended Operating Conditions

Parameter		Symbol	Min	Typ	Max	Unit
Operating Supply Voltage	Single Supply	Vopr	1.7	3.3	5.5	V
	Dual Supply		±0.85		±2.75	
Operating Temperature		Topr	-40	+25	+85	°C

Electrical Characteristics

(Unless otherwise specified V_{DD} = 3.3 V, V_{SS} = 0 V, Ta = 25 °C)

Parameter	Symbol	Temperature Range	Limits			Unit	Condition
			Min	Typ	Max		
Input Offset Voltage *(Note 1) (Note 2)*	V_{IO}	25 °C	-	0.1	2.5	mV	V_{DD} = 1.8 V, 3.3 V
		Full range	-	-	3.8		
Input Offset Voltage Temperature Drift *(Note 1) (Note 2)*	$\Delta V_{IO}/\Delta T$	Full range	-	0.8	-	µV/°C	-
Input Offset Current *(Note 1)*	I_{IO}	25 °C	-	1	-	pA	-
Input Bias Current *(Note 1)*	I_B	25 °C	-	1	-	pA	-
Supply Current *(Note 2)*	I_{DD}	25 °C	-	650	900	µA	R_L = ∞, Av = 0 dB, V_{+IN} = V_{DD}/2
		Full range	-	-	970		
Maximum Output Voltage (High) *(Note 2)*	V_{OH}	25 °C	V_{DD}-0.1	-	-	V	R_L = 10 kΩ
		Full range	V_{DD}-0.1	-	-		
Maximum Output Voltage (Low) *(Note 2)*	V_{OL}	25 °C	-	-	V_{SS}+0.1	V	R_L = 10 kΩ
		Full range	-	-	V_{SS}+0.1		
Large Signal Voltage Gain *(Note 2)*	A_V	25 °C	80	105	-	dB	V_{DD} = 1.8 V
		Full range	80	-	-		
		25 °C	80	110	-		V_{DD} = 3.3 V
		Full range	80	-	-		
Input Common-mode Voltage Range	V_{ICMR}	25 °C	0	-	1.8	V	V_{DD} = 1.8 V, V_{SS} to V_{DD}
			0	-	3.3		V_{DD} = 3.3 V, V_{SS} to V_{DD}
Common-mode Rejection Ratio *(Note 2)*	CMRR	25 °C	70	90	-	dB	-
		Full range	68	-	-		
Power Supply Rejection Ratio *(Note 2)*	PSRR	25 °C	70	90	-	dB	-
		Full range	68	-	-		
Output Source Current *(Note 3)*	I_{SOURCE}	25 °C	4	6	-	mA	V_{OUT} = V_{DD} - 0.4 V
			-	17	-		output short current
Output Sink Current *(Note 3)*	I_{SINK}	25 °C	9	15	-	mA	V_{OUT} = V_{SS} + 0.4 V
			-	35	-		output short current
Slew Rate	SR	25 °C	-	2.5	-	V/µs	C_L = 25 pF
Gain Bandwidth	GBW	25 °C	-	3.0	-	MHz	V_{DD} = 1.8 V, f = 100 kHz, Open loop
			-	3.2	-	MHz	V_{DD} = 3.3 V, f = 100 kHz, Open loop
Phase Margin	θ	25 °C	-	40	-	deg	Open loop
Input Referred Noise Voltage	Vn	25 °C	-	18	-	nV/$\sqrt{Hz}$	Av = 40 dB, f = 1 kHz
Total Harmonics Distortion	THD+N	25 °C	-	0.005	-	%	V_{OUT} = 0.4 V_{P-P}, f = 1 kHz

(Note 1) Absolute value

(Note 2) Full range: Ta = -40 °C to +85 °C

(Note 3) Under the high temperature environment, consider the thermal resistance of IC when selecting the output current.
When the pin short circuits are continuously output, the output current is reduced to climb to the temperature inside IC.

Description of Electrical Characteristics

Described here are the terms of electric characteristics used in this datasheet. Items and symbols used are also shown. Note that item name and symbol and their meaning may differ from those on another manufacture's document or general document.

1. Absolute maximum ratings

Absolute maximum rating item indicates the condition which must not be exceeded. Application of voltage in excess of absolute maximum rating or use out of absolute maximum rated temperature environment may cause deterioration of characteristics.

(1) Power supply voltage (VDD/VSS)
Indicates the maximum voltage that can be applied between the VDD pin and the VSS pin without deterioration or destruction of characteristics of internal circuit.

(2) Differential input voltage (V_{ID})
Indicates the maximum voltage that can be applied between the +IN pin and the -IN pin without deterioration and destruction of characteristics of IC.

(3) Input common-mode voltage range (V_{ICMR})
Indicates the maximum voltage that can be applied to the +IN pin and the -IN pin without deterioration or destruction of characteristics of IC. Input common-mode voltage range of the maximum ratings do not assure normal operation of IC. When normal Operation of IC is desired, the input common-mode voltage range of electrical characteristics item must be followed.

2.Electrical characteristics item

(1) Input offset voltage (V_{IO})
Indicates the voltage difference between the +IN pin and the -IN pin. It can be translated into the input voltage difference required for setting the output voltage at 0 V.

(2) Input offset voltage drift ($\Delta V_{IO}/\Delta T$)
Denotes the ratio of the input offset voltage fluctuation to the ambient temperature fluctuation.

(3) Input offset current (I_{IO})
Indicates the difference of input bias current between the +IN pin and the -IN pin.

(4) Input bias current (I_B)
Indicates the current that flows into or out of the input pin. It is defined by the average of input bias current at the +IN pin and input bias current at the -IN pin.

(5) Supply current (I_{DD})
Indicates the IC current that flows under specified conditions and no-load steady status.

(6) Maximum Output Voltage (High) / Maximum Output Voltage (Low) (V_{OH}/V_{OL})
Indicates the voltage range that can be output by the IC under specified load condition. It is typically divided into maximum output voltage high and low. Maximum output voltage high indicates the upper limit of output voltage. Maximum output voltage low indicates the lower limit.

(7) Large signal voltage gain (Av)
Indicates the amplifying rate (gain) of output voltage against the voltage difference between the +IN pin and the -IN pin. It is normally the amplifying rate (gain) with reference to DC voltage.
Av = (Output voltage)/(Differential Input voltage)

(8) Input common-mode voltage range (V_{ICMR})
Indicates the input voltage range where IC operates normally.

(9) Common-mode rejection ratio (CMRR)
Indicates the ratio of fluctuation of input offset voltage when in-phase input voltage is changed. It is normally the fluctuation of DC.
CMRR = (Change of Input common-mode voltage)/(Input offset voltage fluctuation)

(10) Power supply rejection ratio (PSRR)
Indicates the ratio of fluctuation of input offset voltage when supply voltage is changed. It is normally the fluctuation of DC.
PSRR = (Change of power supply voltage)/(Input offset voltage fluctuation)

(11) Output source current/ output sink current (I_{SOURCE}/I_{SINK})
The maximum current that can be output under specific output conditions such as output voltage, load conditions. It is divided into output source current and output sink current. The output source current indicates the current flowing out of the IC, and the output sink current the current flowing into the IC.

(12) Slew Rate (SR)
SR is a parameter that shows movement speed of operational amplifier. It indicates rate of variable output voltage as specified unit time.

(13) Gain Bandwidth (GBW)
Indicates to multiply by the gain and the frequency where the voltage gain decreases 6 dB/octave.

Description of Electrical Characteristics – continued

(14) Phase Margin (θ)
Indicates the margin of phase from 180 degree phase lag at the frequency at which the gain of operational amplifier becomes 1.
(15) Input referred noise voltage (Vn)
Indicates a noise voltage generated inside the operational amplifier equivalent by ideal voltage source connected in series with input pin.
(16) Total harmonic distortion (THD+N)
Indicates the fluctuation of harmonic components and noise components in the output signal.

Typical Performance Curves

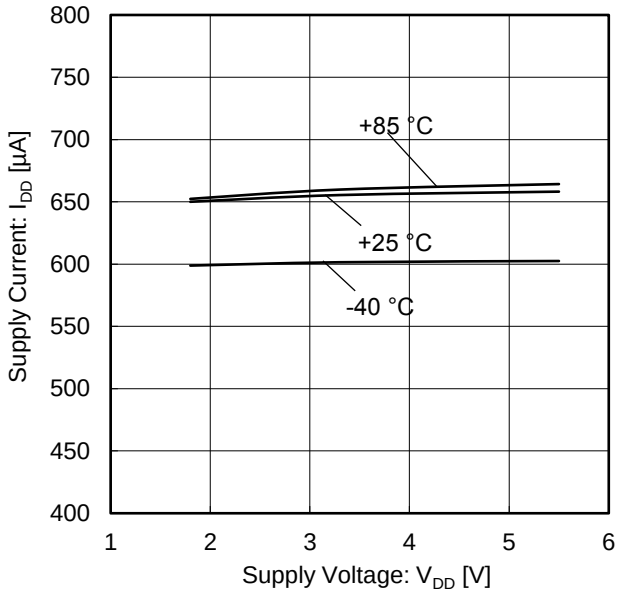


Figure 2. Supply Current vs Supply Voltage

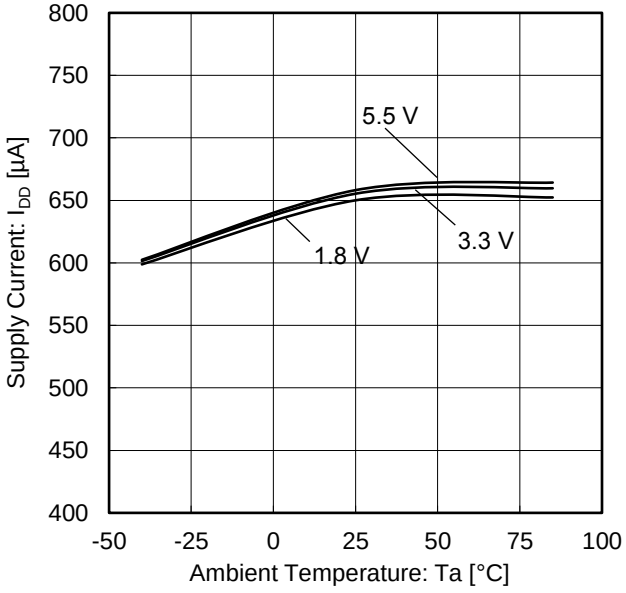


Figure 3. Supply Current vs Ambient Temperature

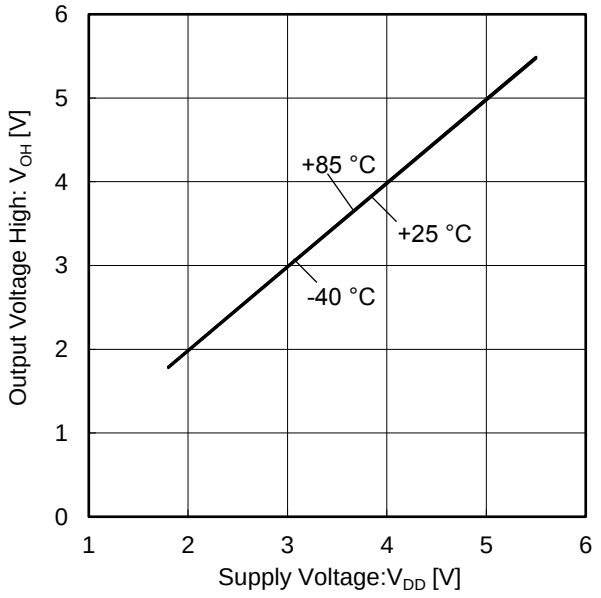


Figure 4. Maximum Output Voltage (High) vs Supply Voltage
(R_L = 10 kΩ)

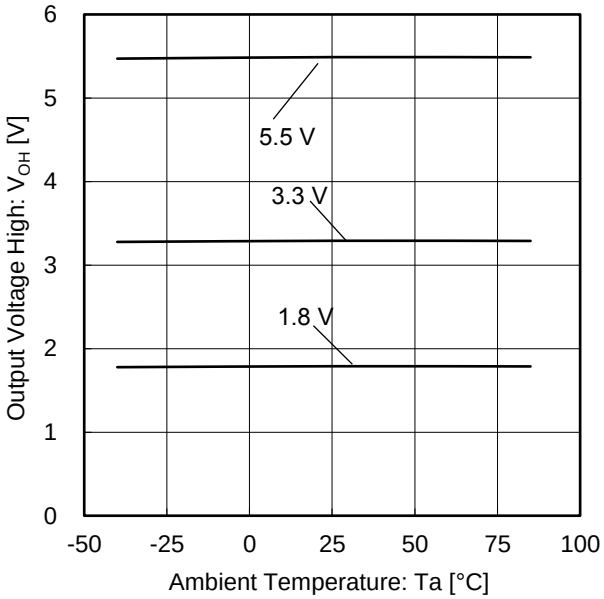


Figure 5. Maximum Output Voltage (High)
vs Ambient Temperature
(R_L = 10 kΩ)

(*)The above characteristics are measurements of typical sample, they are not guaranteed.

Typical Performance Curves - continued

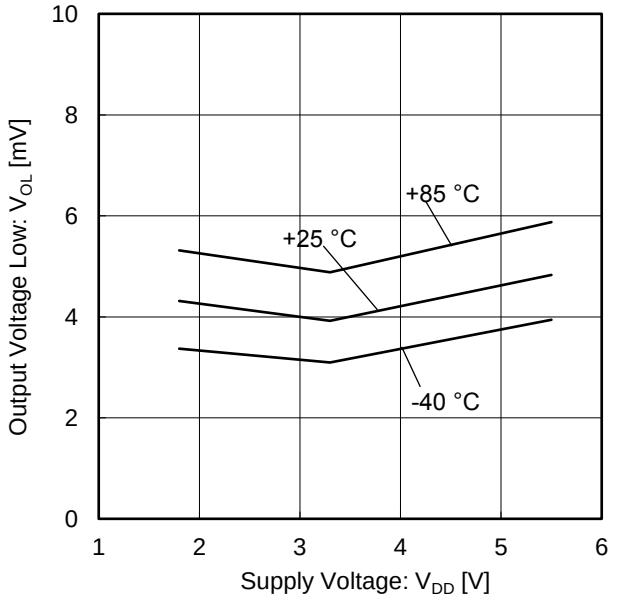


Figure 6. Maximum Output Voltage (Low) vs Supply Voltage
(R_L = 10 kΩ)

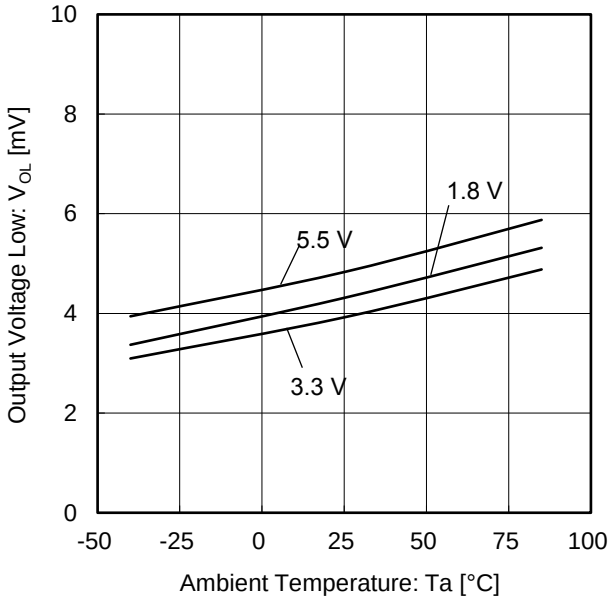


Figure 7. Maximum Output Voltage (Low) vs Ambient Temperature
(R_L = 10 kΩ)

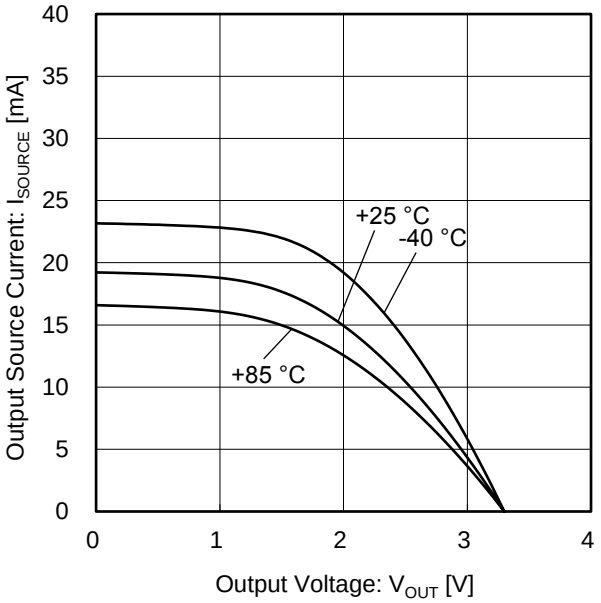


Figure 8. Output Source Current vs Output Voltage
(V_{DD} = 3.3 V)

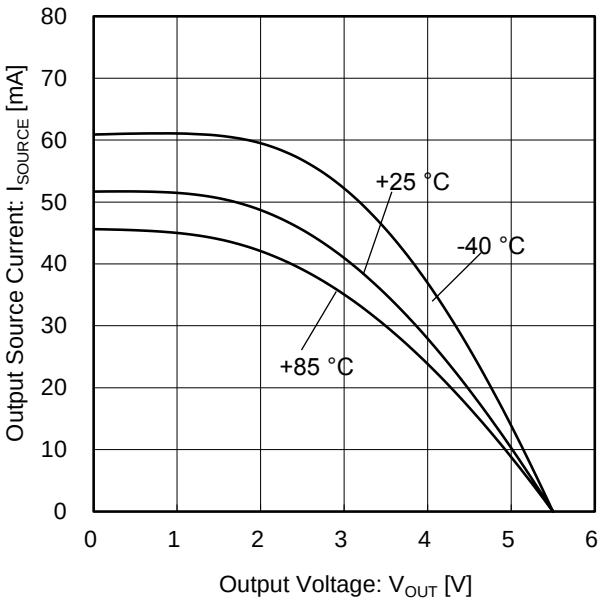


Figure 9. Output Source Current vs Output Voltage
(V_{DD} = 5.5 V)

(*)The above characteristics are measurements of typical sample, they are not guaranteed.

Typical Performance Curves - continued

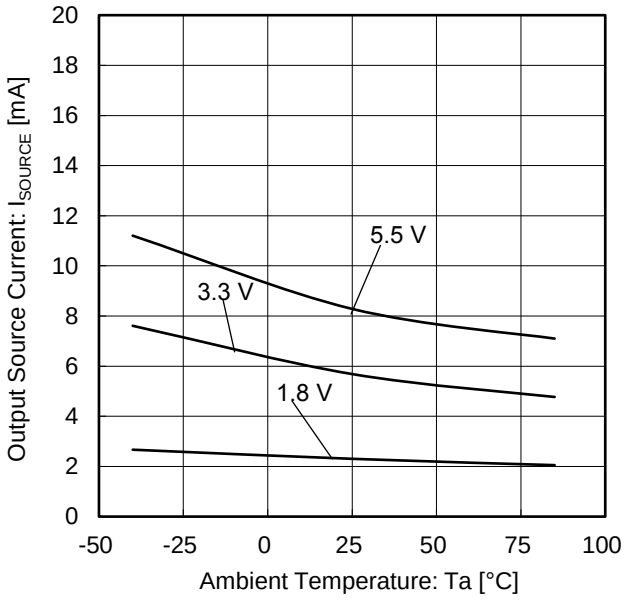


Figure 10. Output Source Current vs Ambient Temperature
(V_{OUT} = V_{DD} - 0.4 V)

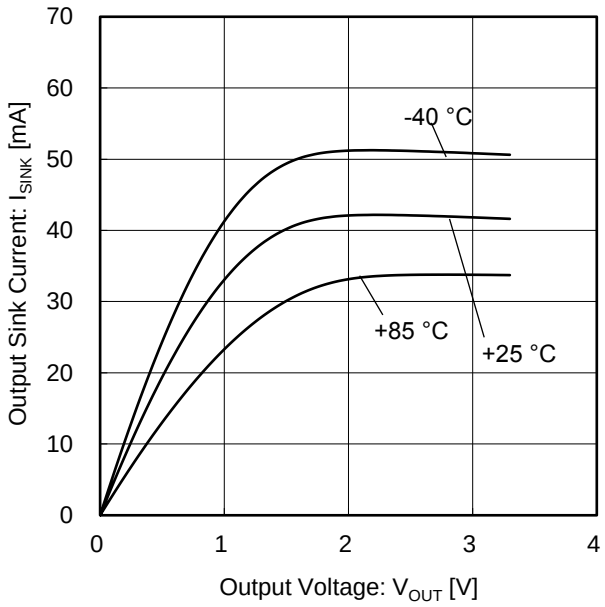


Figure 11. Output Sink Current vs Output Voltage
(V_{DD} = 3.3 V)

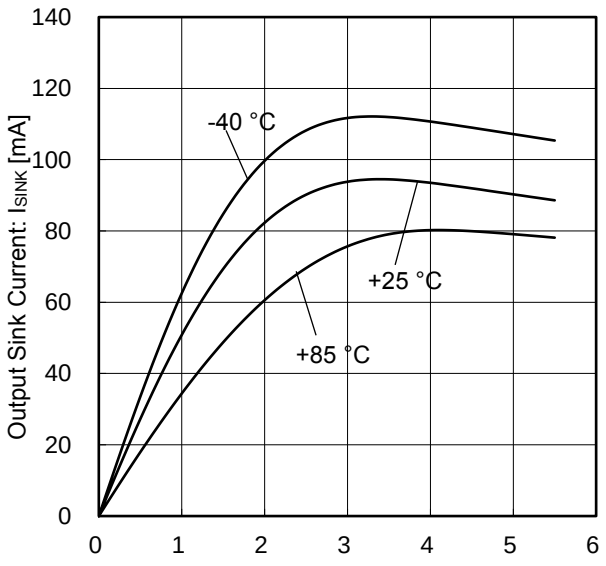


Figure 12. Output Sink Current vs Output Voltage
(V_{DD} = 5.5 V)

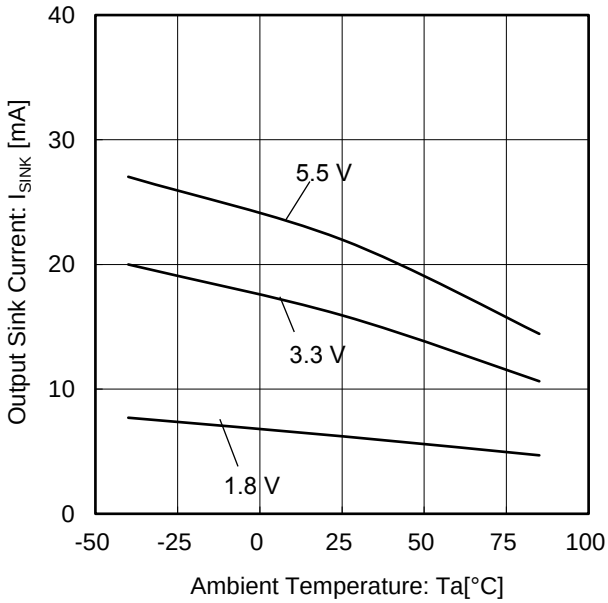


Figure 13. Output Sink Current
vs Ambient Temperature
(V_{OUT} = V_{SS} + 0.4 V)

(*)The above characteristics are measurements of typical sample, they are not guaranteed.

Typical Performance Curves - continued

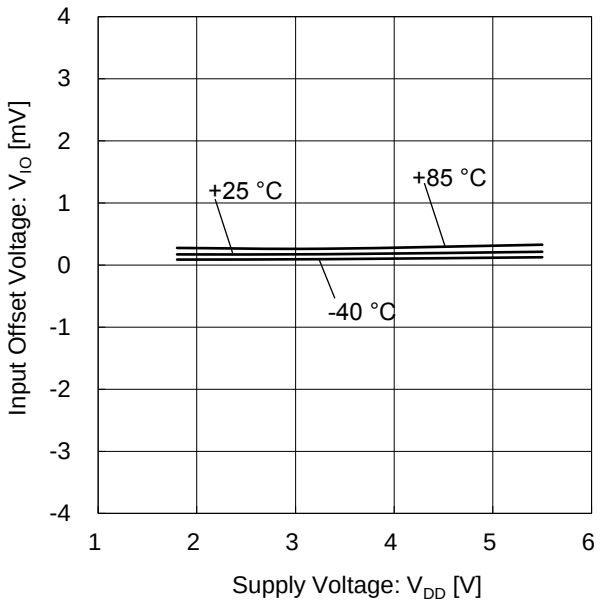


Figure 14. Input Offset Voltage vs Supply Voltage

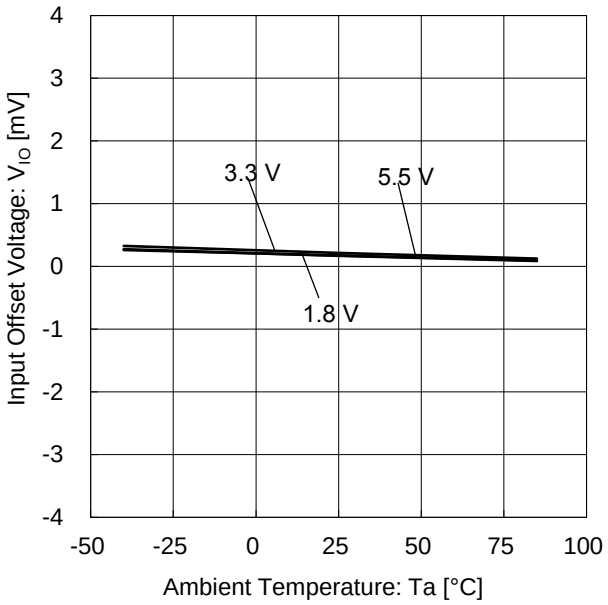


Figure 15. Input Offset Voltage vs Ambient Temperature

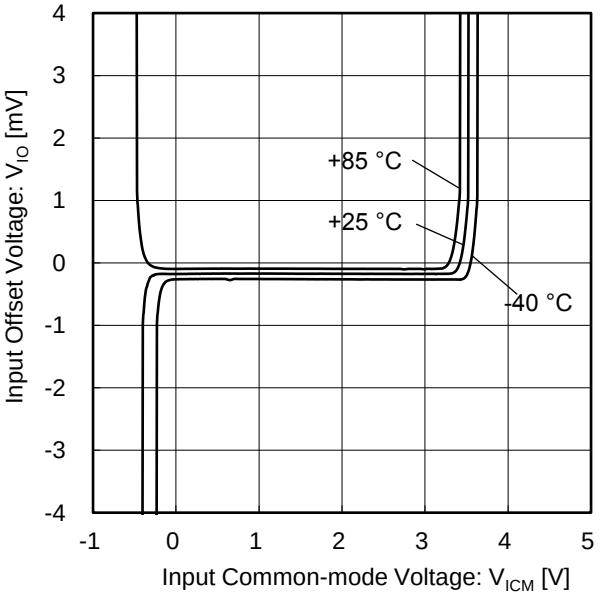


Figure 16. Input Offset Voltage vs Input Common-mode Voltage (V_{DD} = 3.3 V)

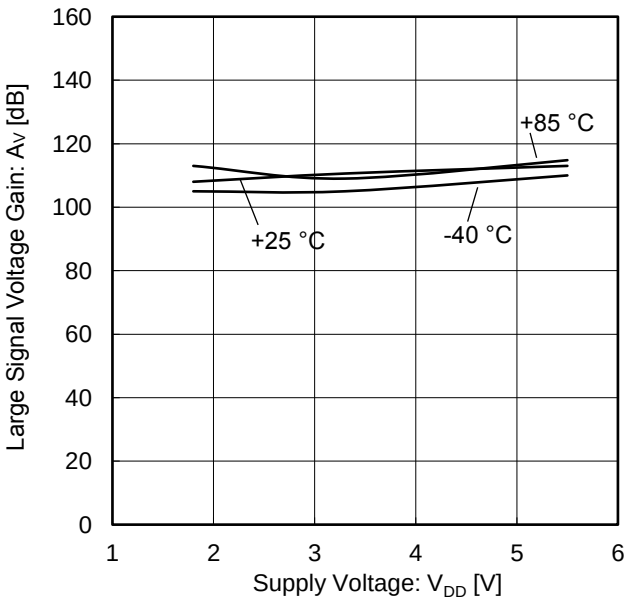


Figure 17. Large Signal Voltage Gain vs Supply Voltage

(*)The above characteristics are measurements of typical sample, they are not guaranteed.

Typical Performance Curves - continued

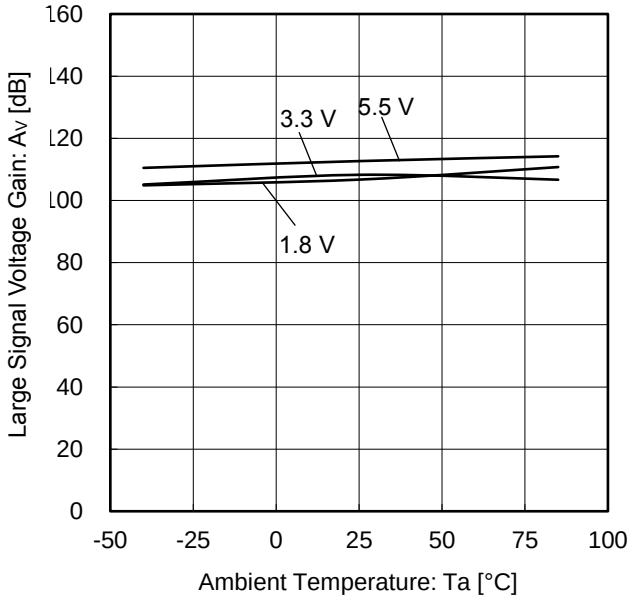


Figure 18. Large Signal Voltage Gain vs Ambient Temperature

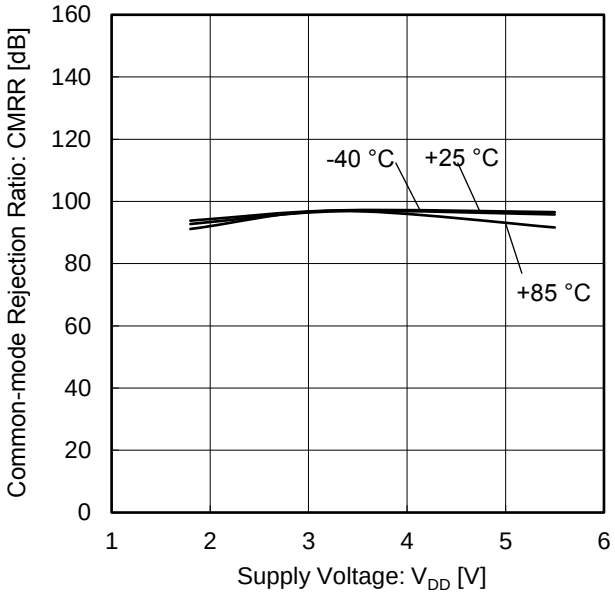


Figure 19. Common-mode Rejection Ratio vs Supply Voltage

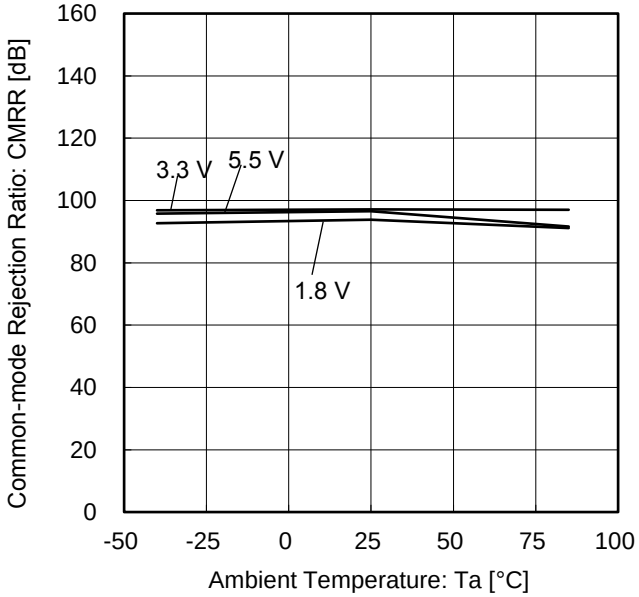


Figure 20. Common-mode Rejection Ratio vs Ambient Temperature

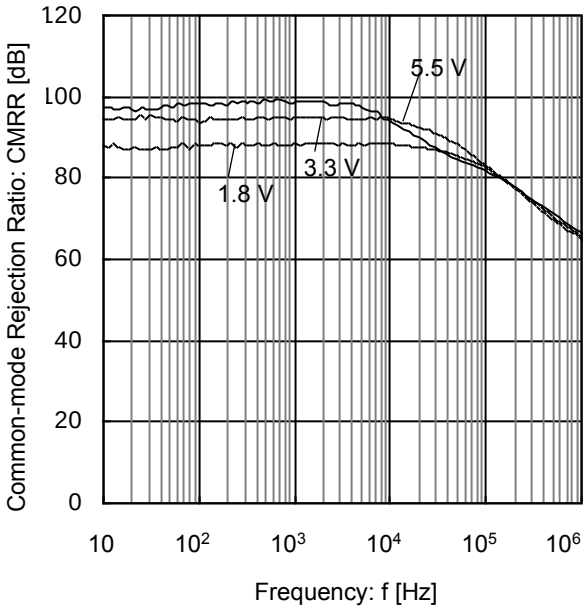


Figure 21. Common-mode Rejection Ratio vs Frequency

(*)The above characteristics are measurements of typical sample, they are not guaranteed.

Typical Performance Curves - continued

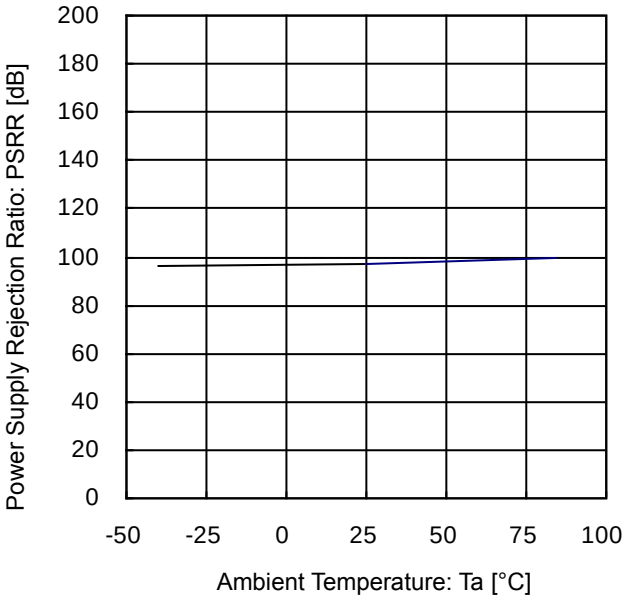


Figure 22. Power Supply Rejection Ratio vs Ambient Temperature (V_{DD} = 1.7 V to 5.5 V)

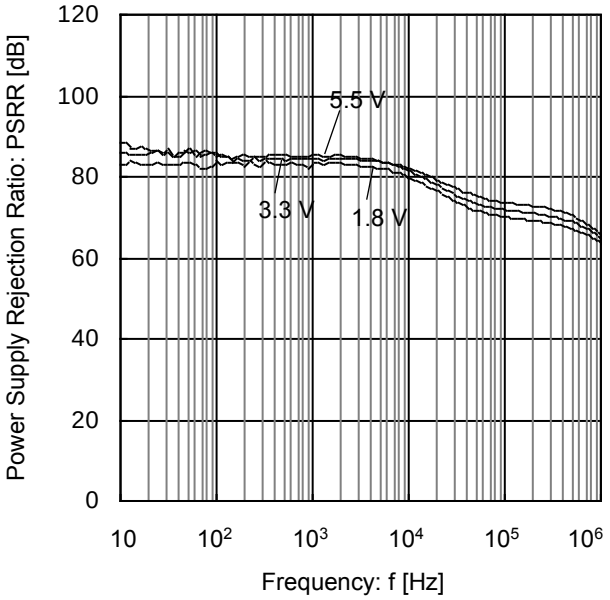


Figure 23. Power Supply Rejection Ratio vs Frequency

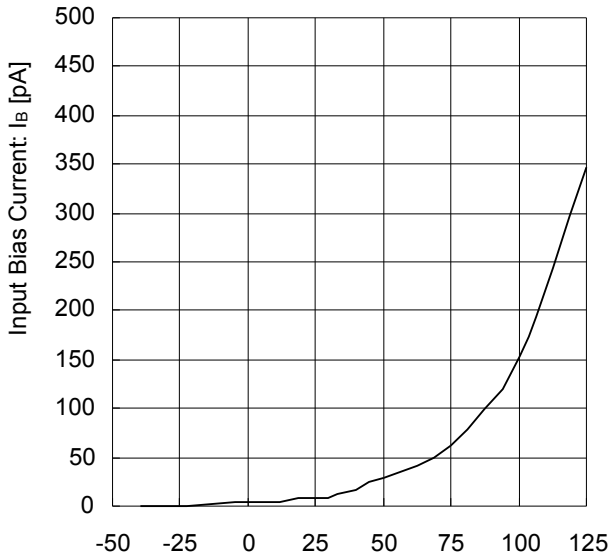


Figure 24. Input Bias Current vs Ambient Temperature (V_{DD} = 3.3 V)

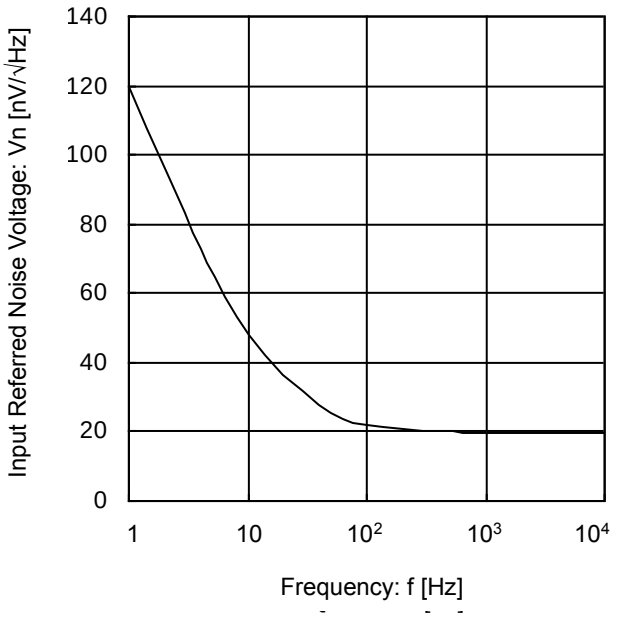


Figure 25. Input Referred Noise Voltage vs Frequency (V_{DD} = 3.3 V)

(*)The above characteristics are measurements of typical sample, they are not guaranteed.

Typical Performance Curves – continued

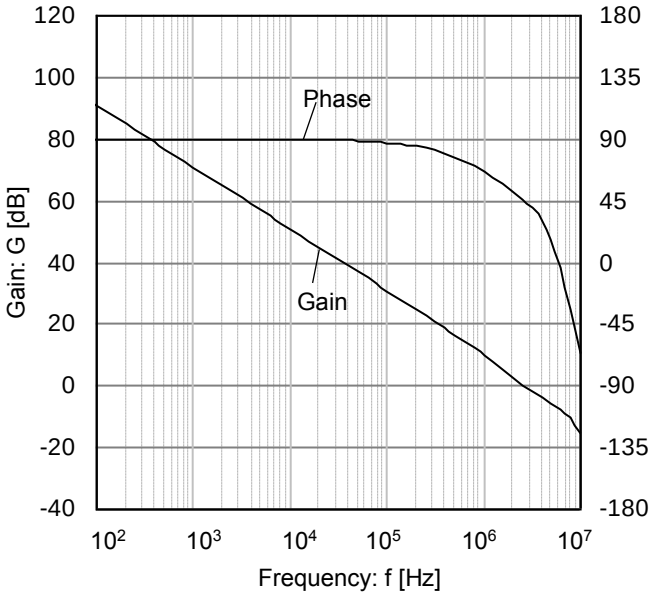


Figure 26. Voltage Gain, Phase vs Frequency
(V_{DD} = 3.3 V, Open loop)

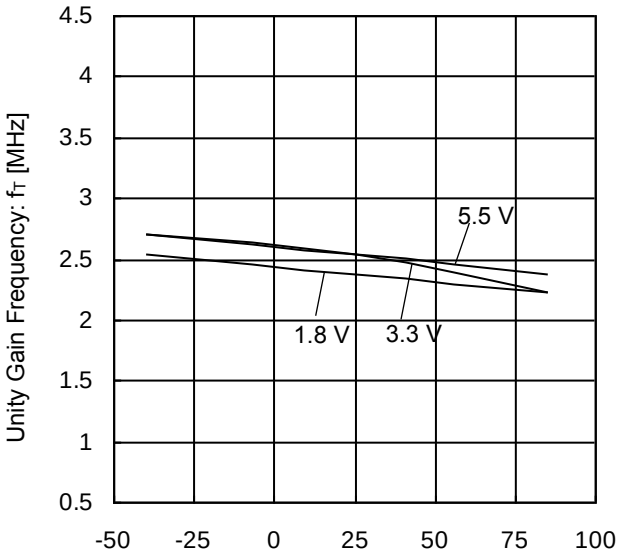


Figure 27. Unity Gain Frequency
vs Ambient Temperature

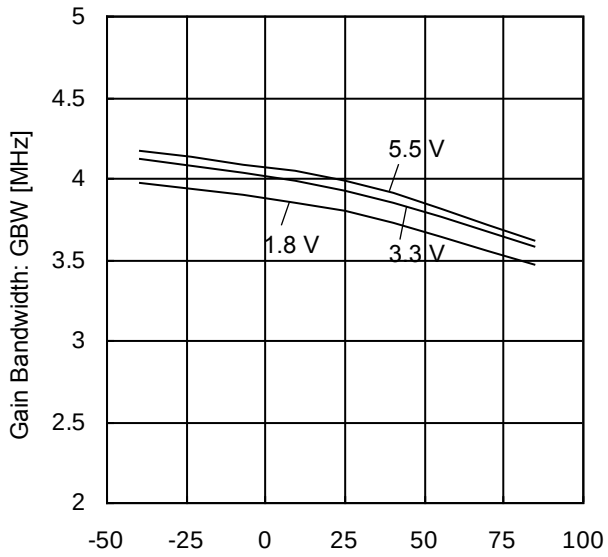


Figure 28. Gain Bandwidth
vs Ambient Temperature

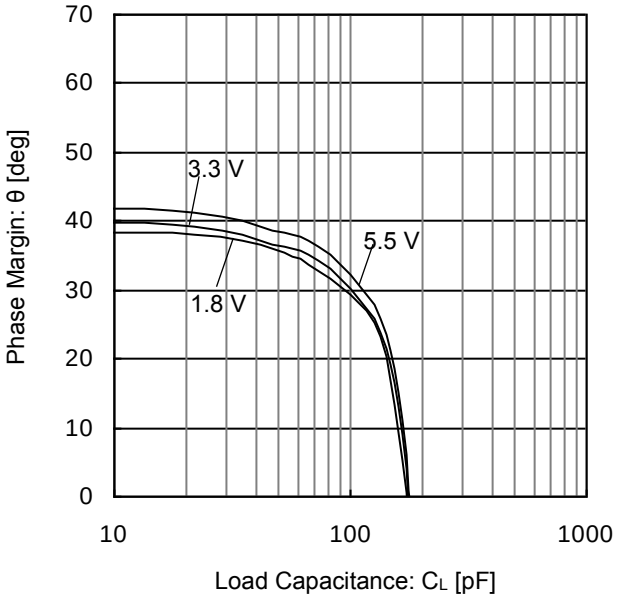


Figure 29. Phase Margin
vs Load Capacitance

(*)The above characteristics are measurements of typical sample, they are not guaranteed.

Typical Performance Curves – continued

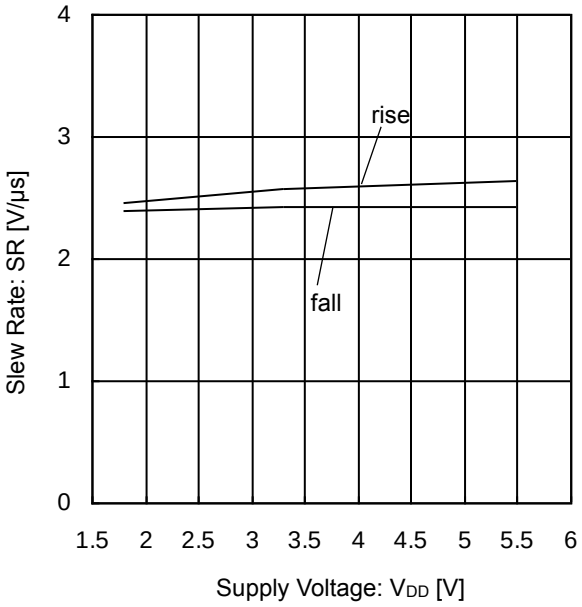


Figure 30. Slew Rate vs Supply Voltage

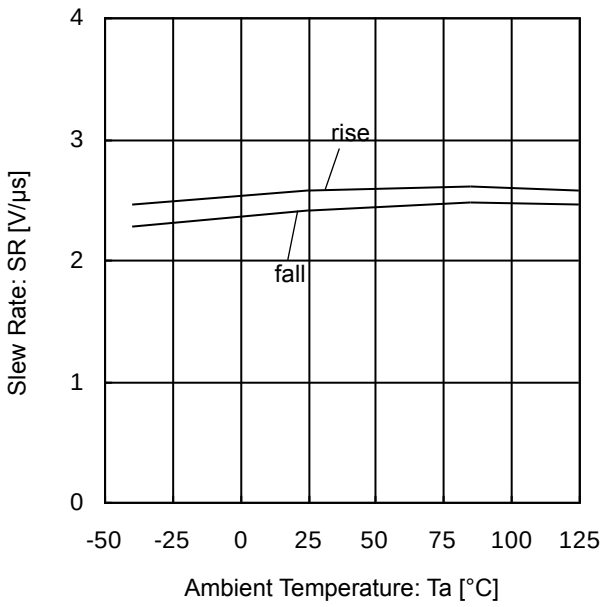


Figure 31. Slew Rate vs Ambient Temperature (V_{DD} = 3.3 V)

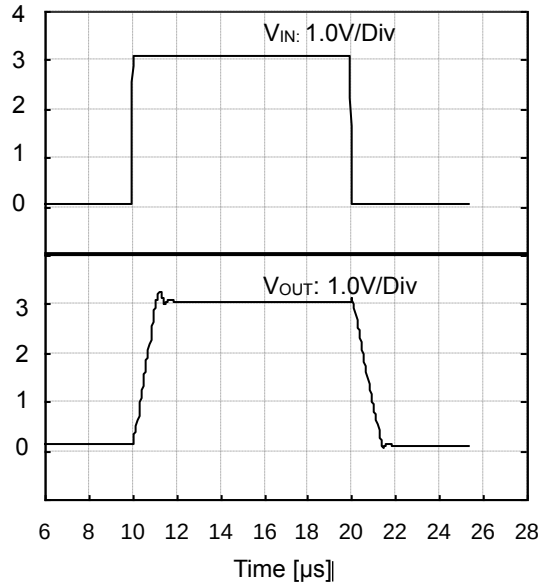


Figure 32. Input and Output Wave Form (V_{DD} = 5 V, A_V = 1, R_L = 2 kΩ, C_L = 10 pF V_{IN} = 3 V_{P-P}, Ta = 25 °C)

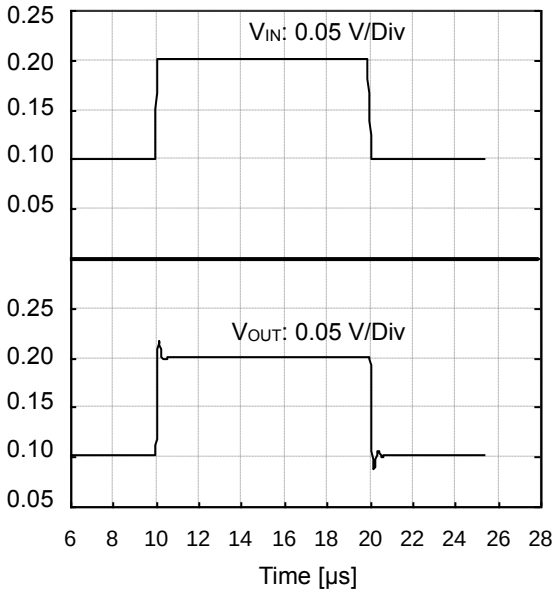


Figure 33. Input and Output Wave Form (V_{DD} = 5 V, A_V = 1, R_L = 2 kΩ, C_L = 10 pF V_{IN} = 100 mV_{P-P}, Ta = 25 °C)

(*)The above characteristics are measurements of typical sample, they are not guaranteed.

Typical Performance Curves - continued

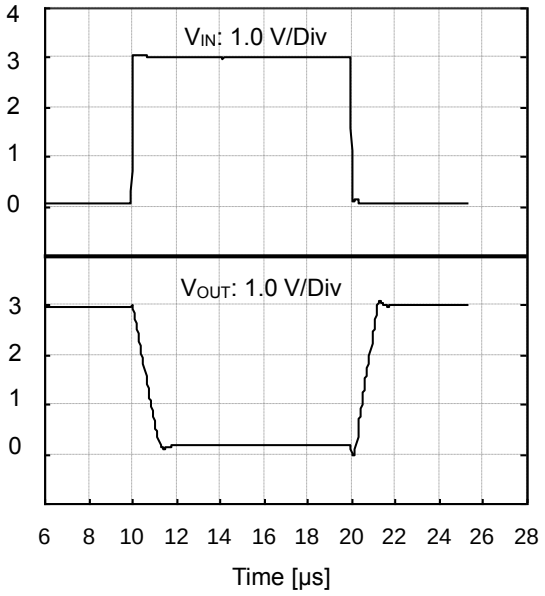


Figure 34. Input and Output Wave Form
(V_{DD} = 5 V, A_V = -1, R_L = 2 kΩ, C_L = 10 pF
V_{IN} = 3 V_{P-P}, Ta = 25 °C)

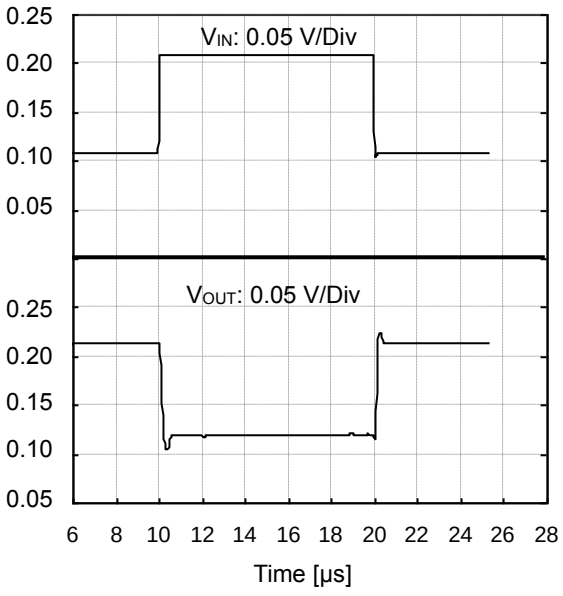


Figure 35. Input and Output Wave Form
(V_{DD} = 5 V, A_V = -1, R_L = 2 kΩ, C_L = 10 pF
V_{IN} = 100 mV_{P-P}, Ta = 25 °C)

(*)The above characteristics are measurements of typical sample, they are not guaranteed.

Application Information

NULL method condition for Test Circuit 1

V_{DD}, V_{SS}, E_K, V_{ICM}, V_{RL} Unit: V

Parameter	V_F	SW1	SW2	SW3	V_{DD}	V_{SS}	E_K	V_{ICM}	V_{RL}	Calculation
Input Offset Voltage	V_{F1}	ON	ON	OFF	3.3	0	-1.65	1.65	-	1
Large Signal Voltage Gain	V_{F2}	ON	ON	ON	3.3	0	-0.5	0.9	1.65	2
	V_{F3}						-2.5		1.65	
Common-mode Rejection Ratio (Input Common-mode Voltage Range)	V_{F4}	ON	ON	OFF	3.3	0	-1.5	0	-	3
	V_{F5}							3.3	-	
Power Supply Rejection Ratio	V_{F6}	ON	ON	OFF	1.7	0	-0.9	0	-	4
	V_{F7}				5.5				-	

Calculation

1. Input Offset Voltage (V_{IO})

$$V_{IO} = \frac{|V_{F1}|}{1+R_F/R_S} \text{ [V]}$$

2. Large Signal Voltage Gain (Av)

$$A_V = 20Log\frac{\Delta V_{EK} \times (1+R_F/R_S)}{|V_{F2}-V_{F3}|} \text{ [dB]}$$

3. Common-mode Rejection Ratio (CMRR)

$$CMRR = 20Log\frac{\Delta V_{ICM} \times (1+R_F/R_S)}{|V_{F4}-V_{F5}|} \text{ [dB]}$$

4. Power Supply Rejection Ratio (PSRR)

$$PSRR = 20Log\frac{\Delta V_{DD} \times (1+R_F/R_S)}{|V_{F6}-V_{F7}|} \text{ [dB]}$$

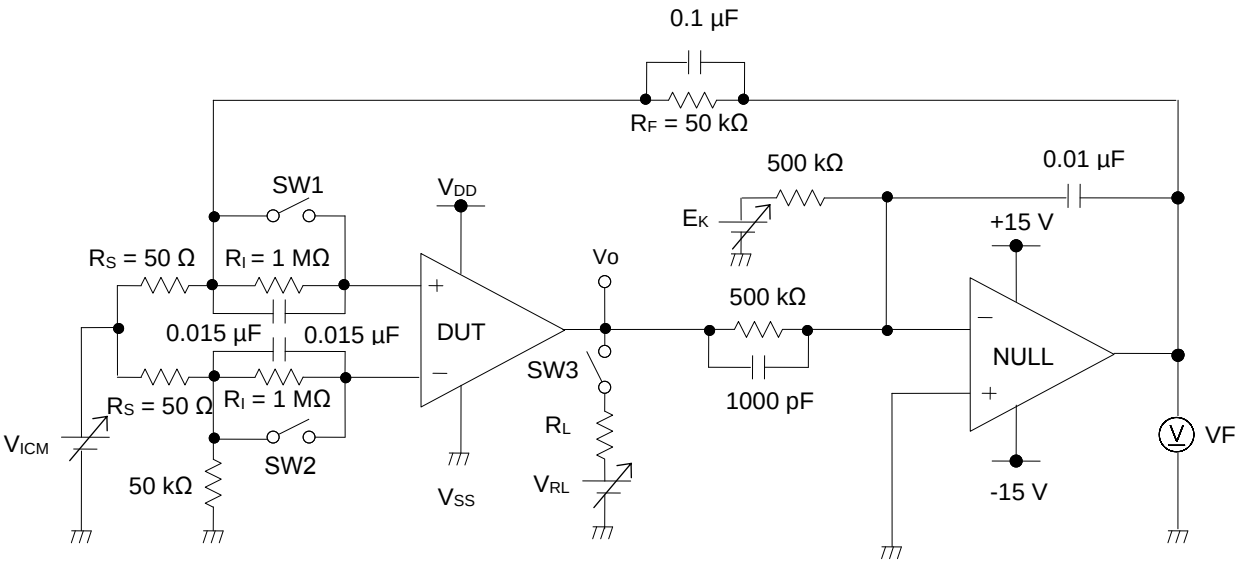


Figure 36. Test circuit 1

Application Information - continued

Switch Condition for Test Circuit 2

Parameter	SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8	SW9	SW10	SW11	SW12
Supply Current	OFF	OFF	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF
Maximum Output Voltage R_L = 10 kΩ	OFF	ON	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	ON	OFF
Output Current	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	ON	OFF	OFF
Slew Rate	OFF	OFF	ON	OFF	OFF	OFF	ON	OFF	ON	OFF	OFF	ON
Unit gain frequency	ON	OFF	OFF	ON	ON	OFF	OFF	OFF	ON	OFF	OFF	ON

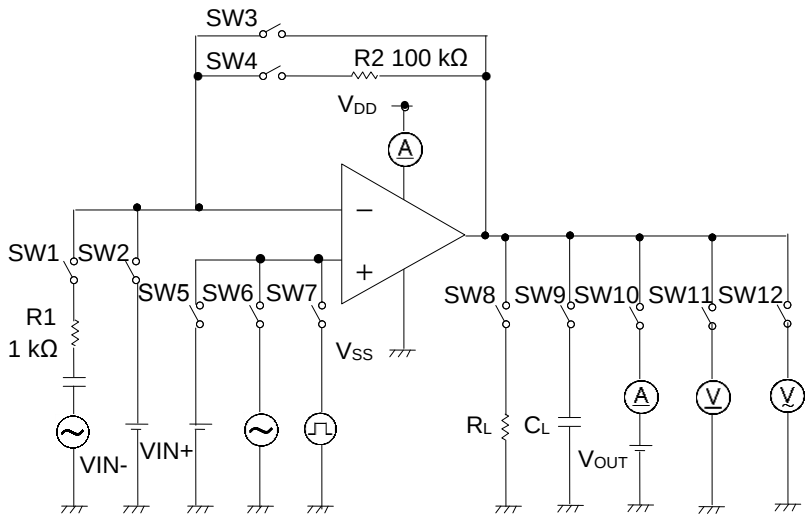


Figure 37. Test circuit 2

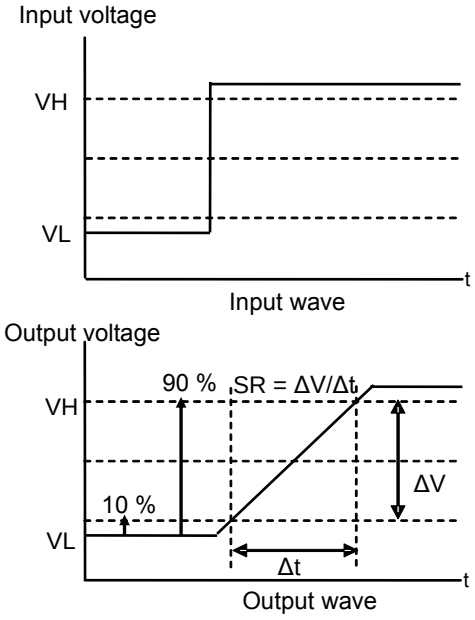


Figure 38. Slew rate input output wave

Application Information - continued

1. Unused Circuits
   When there are unused circuits, it is recommended that they are connected as in right figure, and set the non-inverting input pin to electric potential within the input common-mode voltage range (V_{ICMR}).

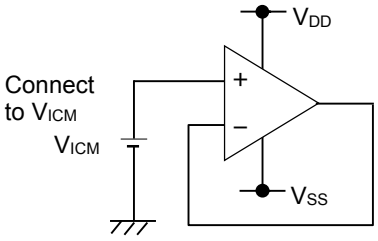


Figure 39. Example of application unused circuit processing

2. Input Voltage
   Applying V_{DD} + 0.3 V to the input pin is possible without causing deterioration of the electrical characteristics or destruction, regardless of the supply voltage. However, this does not ensure circuit operation. Note that the circuit operates normally only when the input voltage is within the common-mode input voltage range of the electric characteristics.

3. Power Supply (single/dual)
   The Op-Amp operates when the voltage is supplied between the VDD and VSS pins. Therefore, the single supply Op-Amp can be used as dual supply Op-Amp as well.

4. Output Capacitor
   When the VDD pin is shorted to VSS (GND) electric potential in a state where electric charge is accumulated in the external capacitor that is connected to the output pin, the accumulated electric charge flow through parasitic elements or pin protection elements inside the circuit and discharges to the VDD pin. It may cause damage to the elements inside the circuit (thermal destruction). When using this IC as an application circuit which does not constitute a negative feedback circuit and does not occur the oscillation by an output capacitive load such as a voltage comparator, connect a capacitor of 0.1 µF or less to the output pin to prevent IC damage due to accumulated discharge of the capacitor connected to the output pin as mentioned above.

5. Oscillation by Output Capacitor
   Phase margin of this IC is 40°. When using an application circuit that constitutes a feedback circuit, be careful about oscillation due to a capacitive load. If the circuits has large size capacitor that is connected to output pin, insert of isolation resistor between output pin and capacitive load.

6. Operation Under Strong Electromagnetic Field
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

Application Example

Voltage follower

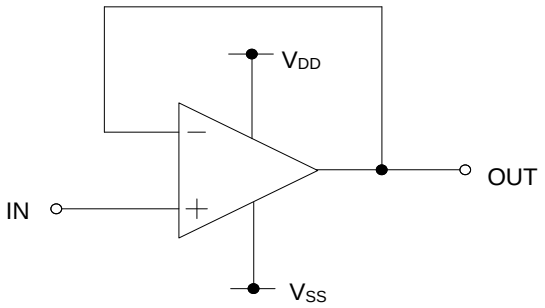


Figure 40. Voltage follower

Voltage gain is 0 dB.
Using this circuit, the output voltage (OUT) is configured to be equal to the input voltage (IN). This circuit also stabilizes the output voltage (OUT) due to high input impedance and low output impedance. Expression for output voltage (OUT) is shown below.

$$OUT = IN$$

Inverting amplifier

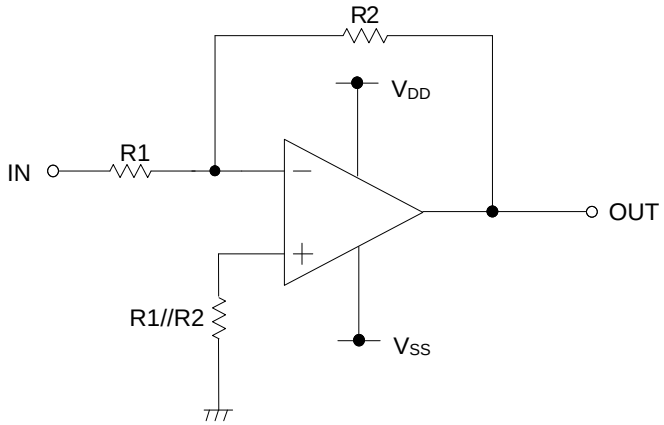


Figure 41. Inverting amplifier circuit

For inverting amplifier, input voltage (IN) is amplified by a voltage gain and depends on the ratio of R1 and R2. The out-of-phase output voltage is shown in the next expression.

$$OUT = -(R2/R1) \times IN$$

This circuit has input impedance equal to R1.

Non-inverting amplifier

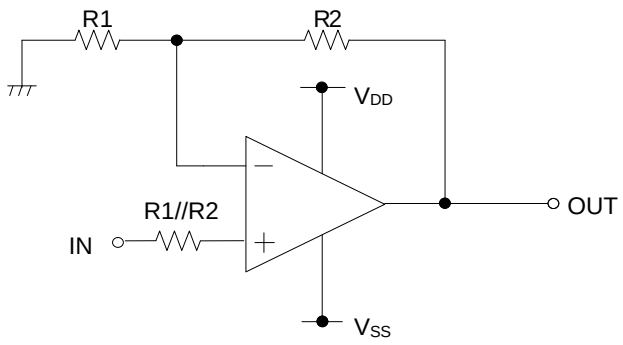


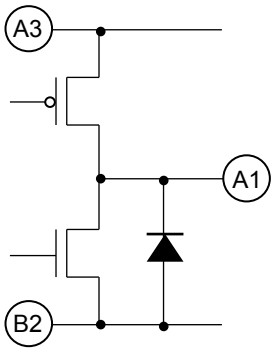
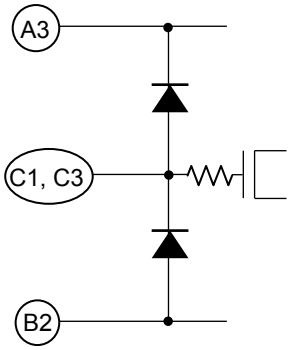
Figure 42. Non-inverting amplifier circuit

For non-inverting amplifier, input voltage (IN) is amplified by a voltage gain, which depends on the ratio of R1 and R2. The output voltage (OUT) is in-phase with the input voltage (IN) and is shown in the next expression.

$$OUT = (1 + R2/R1) \times IN$$

Effectively, this circuit has high input impedance since its input side is the same as that of the operational amplifier.

I/O Equivalence Circuits

Pin No.	Pin Name	Pin Description	Equivalence Circuit
A1	OUT	Output	
C1 C3	-IN +IN	Input	

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. **Unused Input Pins**
   Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

10. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

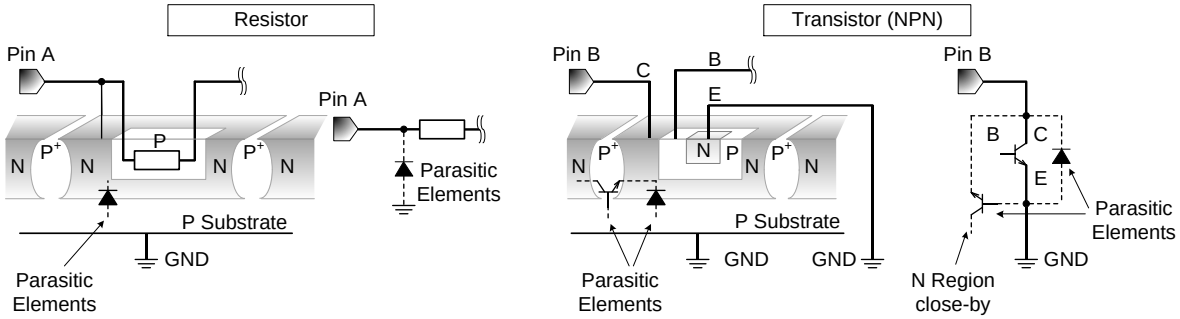


Figure 43. Example of monolithic IC structure

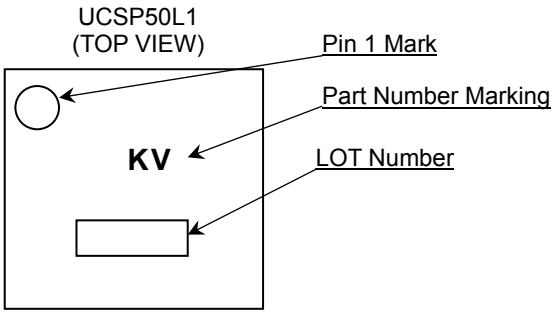
11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

12. Disturbance Light

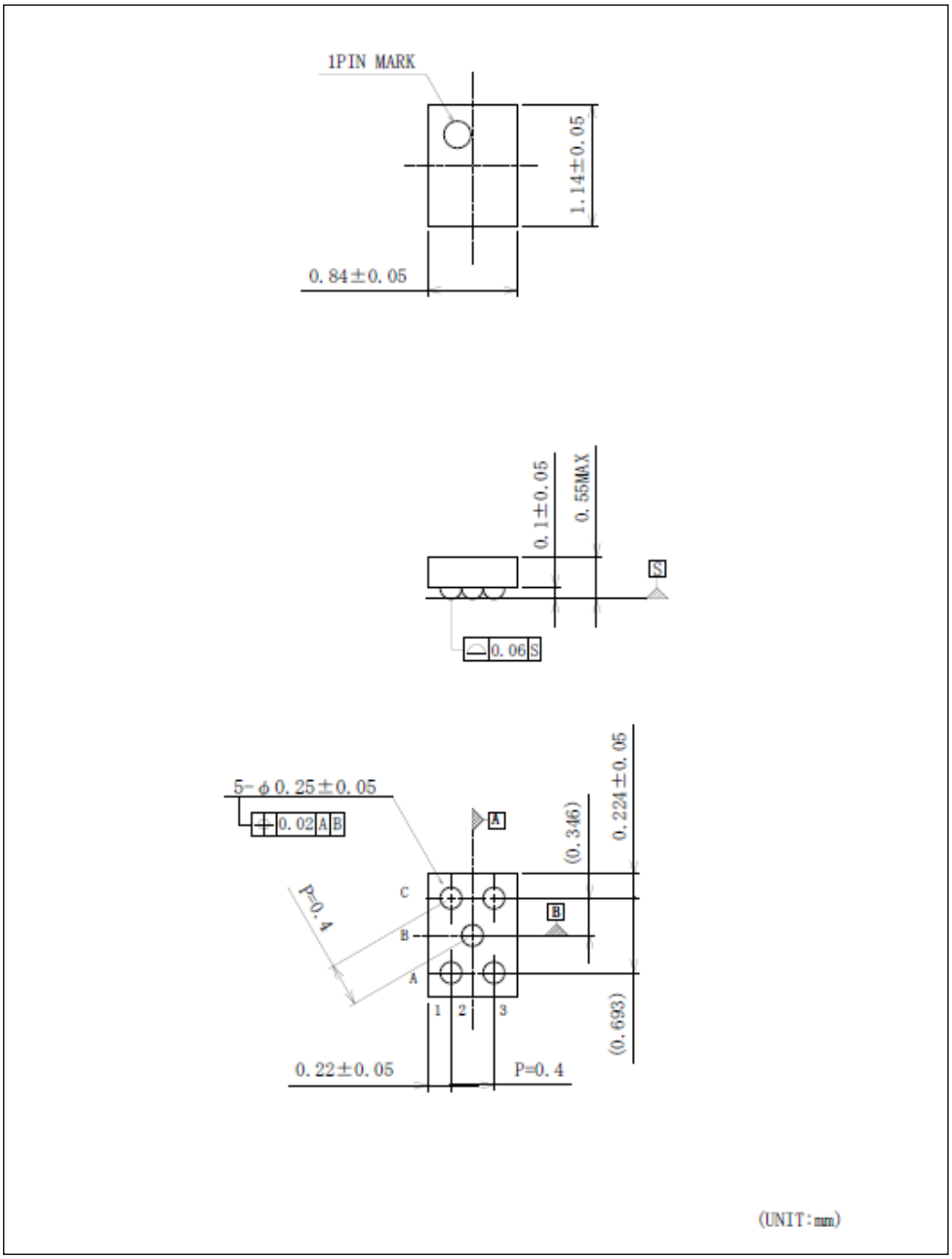
In a device where a portion of silicon is exposed to light such as in a WL-CSP and chip products, IC characteristics may be affected due to photoelectric effect. For this reason, it is recommended to come up with countermeasures that will prevent the chip from being exposed to light.

Marking Diagram



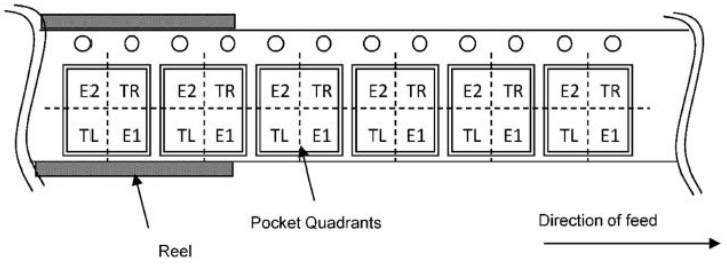
Physical Dimension and Packing Information

Package Name	UCSP50L1 (BD5291GWL)



< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



Revision History

Date	Revision	Changes
02.Sep.2022	001	New Release

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CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.) ; or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

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2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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