



## Product Change Notification / SYST-27NPXN861

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### Date:

29-Jun-2023

### Product Category:

8-bit Microcontrollers

### PCN Type:

Document Change

### Notification Subject:

ERRATA - AVR64EA28/32/48 Silicon Errata and Data Sheet Clarifications

### Affected CPNs:

[SYST-27NPXN861\\_Affected\\_CPN\\_06292023.pdf](#)

[SYST-27NPXN861\\_Affected\\_CPN\\_06292023.csv](#)

### Notification Text:

SYST-27NPXN861

Microchip has released a new Errata for the AVR64EA28/32/48 Silicon Errata and Data Sheet Clarifications of devices. If you are using one of these devices please read the document located at [AVR64EA28/32/48 Silicon Errata and Data Sheet Clarifications](#).

**Notification Status:** Final

#### Description of Change:

Added errata:

- 2.2.3. Write Operation Lost if Consecutive Writes to Specific Address Spaces
- 2.4.2. Flash-Self Programming Failing When Flash Read During Programming

Removed errata:

- NVMCTRL: Flash Page Erase/Write Operation Non-Functional

**Impacts to Data Sheet:** None

**Reason for Change:** To Improve Productivity

**Change Implementation Status:** Complete

**Date Document Changes Effective:** 29 Jun 2023

**NOTE:** Please be advised that this is a change to the document only the product has not been changed.

**Markings to Distinguish Revised from Unrevised Devices:** N/A

## **Attachments:**

[AVR64EA28/32/48 Silicon Errata and Data Sheet Clarifications](#)

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Affected Catalog Part Numbers (CPN)

AVR64EA28-I/SP  
AVR64EA28-I/SS  
AVR64EA28-I/STX  
AVR64EA28T-I/SS  
AVR64EA32-I/PT  
AVR64EA32-I/RXB  
AVR64EA32T-I/PT  
AVR64EA32T-I/RXB  
AVR64EA48-I/6LX  
AVR64EA48-I/PT  
AVR64EA48T-I/6LX  
AVR64EA48T-I/6LXC01  
AVR64EA48T-I/PT

# Silicon Errata and Data Sheet Clarifications

AVR64EA28/32/48



The AVR64EA28/32/48 devices you have received conform functionally to the current device data sheet ([www.microchip.com/DS40002443](http://www.microchip.com/DS40002443)), except for the anomalies described in this document. The errata described in this document will likely be addressed in future revisions of the AVR64EA28/32/48 devices.

## Notes:

- This document summarizes all the silicon errata issues from all the silicon revisions, previous and current
- Refer to the Device/Revision ID section in the current device data sheet ([www.microchip.com/DS40002443](http://www.microchip.com/DS40002443)) for more detailed information on Device Identification and Revision IDs for your specific device, or contact your local Microchip sales office for assistance

# 1. Silicon Issue Summary

## Legend

- Erratum is not applicable.
- X Erratum is applicable.

| Peripheral | Short Description                                                                    | Valid for Silicon Revision |
|------------|--------------------------------------------------------------------------------------|----------------------------|
|            |                                                                                      | Rev. B1 <sup>(1)</sup>     |
| Device     | 2.2.1. NVM Programming Does Not Work Below 2.7V                                      | X                          |
|            | 2.2.2. Reduced Flash Endurance for VDD Below BODLEVEL3                               | X                          |
|            | 2.2.3. Write Operation Lost if Consecutive Writes to Specific Address Spaces         | X                          |
| CRCSCAN    | 2.3.1. Running CRC Scan on Part of The Flash is Non-Functional                       | X                          |
| NVMCTRL    | 2.4.1. Flash Multi Page Erase Non-Functional from UPDI                               | X                          |
|            | 2.4.2. Flash-Self Programming Failing When Flash Read During Programming             | X                          |
| USART      | 2.5.1. Receiver Non-Functional after Detection of Inconsistent Synchronization Field | X                          |

## Note:

1. This revision is the initial release of the silicon.

## 2. Silicon Errata Issues

### 2.1 Errata Details

- Erratum is not applicable.
- X Erratum is applicable.

### 2.2 Device

#### 2.2.1 NVM Programming Does Not Work Below 2.7V

Performing an erase or write operation when  $V_{DD}$  is below 2.7V may fail. Recommending to make sure that  $V_{DD}$  is above 2.7V before starting an erase or a write operation. Alternatively, BOD can be enabled with a level set to BODLEVEL2 or higher.

##### Work Around

None.

##### Affected Silicon Revisions

| Rev. B1 |
|---------|
| X       |

#### 2.2.2 Reduced Flash Endurance for $V_{DD}$ Below BODLEVEL3

If operating at  $V_{DD}$  below BODLEVEL3, Flash endurance is reduced to 1k erase/write cycles. The reduction is independent of the  $V_{DD}$  level during erase/write.

##### Work Around

None

##### Affected Silicon Revisions

| Rev. B1 |
|---------|
| X       |

#### 2.2.3 Write Operation Lost if Consecutive Writes to Specific Address Spaces

An ST/STD/STS instruction to address  $\geq 64$  followed by an ST/STD instruction to address  $< 64$  or SLPCTRL.CTRLA will cause loss of the last write.

##### Work Around

To avoid loss of write operation, use one of the following workarounds depending on address space:

- Insert a NOP instruction before writing to address  $< 64$ , or use the OUT instruction instead of ST/STD
- Insert a NOP instruction before writing to SLPCTRL.CTRLA

##### Affected Silicon Revisions

| Rev. B1 |
|---------|
| X       |

### 2.3 CRCSCAN - Cyclic Redundancy Check Memory Scan

#### 2.3.1 Running CRC Scan on Part of The Flash is Non-Functional

- Running CRC scan on the boot section does not work if FUSE.BOOTSIZE is different from 0x00
- Running CRC scan on the boot and application section does not work if FUSE.CODESIZE is different from 0x00

- Running CRC scan on the entire Flash works

### Work Around

None

### Affected Silicon Revisions

| Rev. B1 |
|---------|
| X       |

## 2.4 NVMCTRL - Nonvolatile Memory Controller

### 2.4.1 Flash Multi Page Erase Non-Functional from UPDI

Performing a Flash multi-page erase (writing the CMD bitfield in NVMCTRL.CTRLA to FLMPERn) from UPDI does not work on the boot section. It is not recommended to use multi-page erase on any Flash section.

### Work Around

Use Flash page erase (writing the CMD bitfield in NVMCTRL.CTRLA to 0x08).

### Affected Silicon Revisions

| Rev. B1 |
|---------|
| X       |

### 2.4.2 Flash-Self Programming Failing When Flash Read During Programming

If data are read from the Flash NRWW section while the Flash RWW section is being written to or erased (Flash Page Write or Flash Page Erase), the erase or write may fail. Instruction fetch from the Flash NRWW section does not affect erase or write operation to the Flash RWW section.

### Work Around

Alternative 1: RWW functionality not needed

- Do not use flash self-programming when executing from the NRWW section

Alternative 2: RWW functionality needed

- Enable BOD in continuous mode (in FUSE.BODCFG, set bitfield LVL to BODLEVEL1 or higher and bitfield ACTIVE to 0x3)
- Do not use the *Flash Page Erase and Page Write* operation (writing the CMD bitfield in NVMCTRL.CTRLA to 0x05). Execute Flash Page Erase and Flash Page Write as two separate operations instead.

### Affected Silicon Revisions

| Rev. B1 |
|---------|
| X       |

## 2.5 USART - Universal Synchronous and Asynchronous Receiver and Transmitter

### 2.5.1 Receiver Non-Functional after Detection of Inconsistent Synchronization Field

The USART Receiver becomes non-functional when the Inconsistent Synchronization Field Interrupt Flag (ISFIF) in the Status (USARTn.STATUS) register is set. The ISFIF interrupt flag is set when the Receiver Mode (RXMODE) bit field in the Control B (USARTn.CTRLB) register is configured to Generic Auto-Baud (GENAUTO) or LIN Constrained Auto-Baud (LINAUTO) mode, and the received synchronization frame does not conform to the conditions described in the data sheet. Clearing the flag does not re-enable the USART Receiver.

### Work Around

When the ISFIF interrupt flag is set, disable and re-enable the USART Receiver by first writing a '0' and then a '1' to the Receiver Enable (RXEN) bit in the Control B (USARTn.CTRLB) register.

### Affected Silicon Revisions

| Rev. B1 |
|---------|
| X       |

### 3. Data Sheet Clarifications

Note the following typographic corrections and clarifications for the latest version of the device data sheet ([www.microchip.com/DS40002443](http://www.microchip.com/DS40002443)).

**Note:** Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

#### 3.1 Electrical Characteristics - RSTCTRL and BOD

A clarification has been made to change the Brown-out Detect Voltage ( $V_{BOD}$ ) in the *Reset*, *WDT*, *Oscillator Start-up Timer*, *Power-up Timer*, *Brown-out Detector Specifications* table.

Table 35-15. Reset, WDT, Oscillator Start-up Timer, Power-up Timer, Brown-out Detector Specifications

| Symbol          | Description                                            | Min. | Typ. †      | Max.        | Unit   | Conditions                |
|-----------------|--------------------------------------------------------|------|-------------|-------------|--------|---------------------------|
| $t_{RST}^*$     | RESET pin pulse-width low to ensure a Reset            | 2.5  | —           | —           | μs     |                           |
| $R_{RST\_UP}^*$ | RESET pin pull-up resistor                             | —    | 35          | —           | kΩ     |                           |
| $T_{OST}^*$     | Oscillator start-up timer period <sup>(1)</sup>        | —    | 1024        | —           | cycles |                           |
| $V_{BOD+}$      | Brown-out Detect Voltage, rising slope <sup>(2)</sup>  | —    | 1.75        | —           | V      | BODLEVEL0                 |
|                 |                                                        |      | 1.90        | <b>2.10</b> | V      | BODLEVEL1                 |
|                 |                                                        |      | 2.60        | <b>2.80</b> | V      | BODLEVEL2                 |
|                 |                                                        |      | 4.30        | <b>4.60</b> | V      | BODLEVEL3                 |
| $V_{BOD-}$      | Brown-out Detect Voltage, falling slope <sup>(2)</sup> | —    | 1.75        | —           | V      | BODLEVEL0                 |
|                 |                                                        |      | 1.90        | —           | V      | BODLEVEL1                 |
|                 |                                                        |      | 2.60        | —           | V      | BODLEVEL2                 |
|                 |                                                        |      | 4.30        | —           | V      | BODLEVEL3                 |
| $V_{BOD\_HYS}$  | Brown-out Detect hysteresis                            | —    | 25          | —           | mV     |                           |
| $t_{BOD\_ST}$   | Brown-out Detect start-up time from sleep              | —    | 30          | —           | μs     |                           |
| $t_{BOD}$       | BOD sampling time when used in Sampling mode           | —    | $1/f_{BOD}$ | —           | ms     |                           |
| $t_{BOD\_RST}$  | Brown-out Reset response time                          | —    | 4           | —           | μs     | $V_{DD} = V_{BOD} - 0.1V$ |

† Data in the "Typ." column is at  $T_A = 25^\circ C$  and  $V_{DD} = 3.0V$  unless otherwise specified. These parameters are not tested and are for design guidance only.

\* These parameters are characterized but not tested in production.

**Notes:**

- By design, the Oscillator Start-up Timer ( $T_{OST}$ ) counts the first 1024 cycles, independent of frequency.
- $V_{DD}$  and GND must be capacitively decoupled as close to the device as possible to ensure these voltage tolerances. Recommended values are 0.1 μF and 0.01 μF in parallel.

## 4. Document Revision History

**Note:** The document revision is independent of the silicon revision.

### 4.1 Revision History

| Doc. Rev. | Date    | Comments                                                                                                                                                                                                                                                                                                                                                                                                             |
|-----------|---------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| B         | 06/2023 | <p>Added errata:</p> <ul style="list-style-type: none"> <li>• <a href="#">2.2.3. Write Operation Lost if Consecutive Writes to Specific Address Spaces</a></li> <li>• <a href="#">2.4.2. Flash-Self Programming Failing When Flash Read During Programming</a></li> </ul> <p>Removed errata:</p> <ul style="list-style-type: none"> <li>• NVMCTRL: <i>Flash Page Erase/Write Operation Non-Functional</i></li> </ul> |
| A         | 02/2023 | Initial document release                                                                                                                                                                                                                                                                                                                                                                                             |

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