Product Change Notification / SYST-06XKDI494

Date:

07-Jul-2023

Product Category:

16-Bit - Microcontrollers and Digital Signal Controllers

PCN Type:

Document Change

Notification Subject:

ERRATA - dsPIC33CK1024MP710 Family Silicon Errata and Data Sheet Clarification

Affected CPNs:

SYST-06XKDI494_Affected_CPN_07072023.pdf
SYST-06XKDI494_Affected_CPN_07072023.csv

Notification Text:

SYST-06XKDI494

Microchip has released a new Errata for the dsPIC33CK1024MP710 Family Silicon Errata and Data Sheet Clarification of devices. If you are using one of these devices please read the document located at dsPIC33CK1024MP710 Family Silicon Errata and Data Sheet Clarification.

Notification Status: Final

Description of Change:
- Added silicon errata issue 7 (Reset)

Impacts to Data Sheet: None

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 07 Jul 2023

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachments:

dsPIC33CK1024MP710 Family Silicon Errata and Data Sheet Clarification

Please contact your local Microchip sales office with questions or concerns regarding this notification.

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Affected Catalog Part Numbers (CPN)

DSPIC33CK1024MP705-E/M7
DSPIC33CK512MP705-E/M7
DSPIC33CK256MP705-E/M7
DSPIC33CK1024MP706-E/MR
DSPIC33CK512MP706-E/MR
DSPIC33CK256MP706-E/MR
DSPIC33CK1024MP706-E/PT
DSPIC33CK512MP706-E/PT
DSPIC33CK256MP706-E/PT
DSPIC33CK1024MP710-E/PT
DSPIC33CK512MP710-E/PT
DSPIC33CK256MP710-E/PT
DSPIC33CK1024MP710-E/PTVAO
DSPIC33CK1024MP708-E/PT
DSPIC33CK512MP708-E/PT
DSPIC33CK256MP708-E/PT
DSPIC33CK1024MP708-E/PTVAO
DSPIC33CK1024MP705-E/PT
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DSPIC33CK256MP705-E/PT
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DSPIC33CK256MP706-I/PT
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DSPIC33CK256MP705-H/M7
DSPIC33CK1024MP706-H/MR
DSPIC33CK512MP706-H/MR
DSPIC33CK256MP706-H/MR
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DSPIC33CK512MP706-H/PT

DSPIC33CK256MP706-H/PT
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DSPIC33CK256MP705T-I/M7
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DSPIC33CK512MP706T-I/MR
DSPIC33CK256MP706T-I/MR
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DSPIC33CK1024MP705T-E/PT
DSPIC33CK512MP705T-E/PT
DSPIC33CK256MP705T-E/PT

dsPIC33CK1024MP710

dsPIC33CK1024MP710 Family Silicon Errata and Data Sheet Clarification

The dsPIC33CK1024MP710 family devices that you have received conform functionally to the current Device Data Sheet (DS70005496**B**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the dsPIC33CK1024MP710 silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A1**).

Data Sheet clarifications and corrections start on page 5, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers and emulation tools, which are available at the Microchip corporate website (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
   a) For MPLAB IDE 8, select *Programmer > Reconnect*.
   b) For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note:	If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various dsPIC33CK1024MP710 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Device	Device ID[1]	Revision ID for Silicon Revision	Device	Device ID[1]	Revision ID for Silicon Revision
		A1			A1
dsPIC33CK1024MP710 Family with CAN FD			**dsPIC33CK1024MP710 Family without CAN FD**		
dsPIC33CK1024MP710	0xA065	0x0001	dsPIC33CK1024MP410	0xA025	0x0001
dsPIC33CK1024MP708	0xA064		dsPIC33CK1024MP408	0xA024	
dsPIC33CK1024MP706	0xA063		dsPIC33CK1024MP406	0xA023	
dsPIC33CK1024MP705	0xA062		dsPIC33CK1024MP405	0xA022	
dsPIC33CK512MP710	0xA055		dsPIC33CK512MP410	0xA015	
dsPIC33CK512MP708	0xA054		dsPIC33CK512MP408	0xA014	
dsPIC33CK512MP706	0xA053		dsPIC33CK512MP406	0xA013	
dsPIC33CK512MP705	0xA052		dsPIC33CK512MP405	0xA012	
dsPIC33CK256MP710	0xA045		dsPIC33CK256MP410	0xA005	
dsPIC33CK256MP708	0xA044		dsPIC33CK256MP408	0xA004	
dsPIC33CK256MP706	0xA043		dsPIC33CK256MP406	0xA003	
dsPIC33CK256MP705	0xA042		dsPIC33CK256MP405	0xA002	

Note 1: The Device IDs (DEVID and DEVREV) are located at the last two implemented addresses of configuration memory space. They are shown in hexadecimal in the format “DEVID DEVREV”.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)
				A1
I²C	Idle	1.	Address cannot be received in Idle mode.	X
CPU	DIV.SD Instruction	2.	Overflow bit is not getting set when an overflow occurs.	X
I²C	Collision Detection	3.	Bus collision is not detected during Host reception if there is a Start/Stop condition.	X
I²C	Client Mode	4.	Unexpected Client interrupt if there is a Stop bit in the 9th clock, followed by a Start bit.	X
I²C	Client Mode	5.	When data hold is enabled and software sends a NACK, a Client interrupt is asserted if there are more bytes on the bus.	X
ADC	Differential-Mode	6.	Errors may occur when enabling Differential-mode when F_{SRC} is greater than 50 MHz.	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A1**).

1. Module: I²C

In Client mode, an address cannot be received when the device is in Idle and the module is set for discontinue in Idle (I2CSIDL = 1).

Work around

None.

Affected Silicon Revisions

A1							
X							

2. Module: CPU

When using the Signed 32/16-bit Division instruction, DIV.SD, the Overflow bit may not always get set when an overflow occurs.

Work around

Test for, and handle, Overflow conditions outside of the DIV.SD instruction.

Affected Silicon Revisions

A1							
X							

3. Module: I²C

Bus collision detection can fail during a Start/ Stop condition when a Host is receiving data from a Client. This condition can occur in a noisy environment or hot swapping I²C.

Work around

None.

Affected Silicon Revisions

A1							
X							

4. Module: I²C

An unexpected Client interrupt will occur if the Host sends a NACK and a Stop bit, followed by a Start bit in the ACK phase (9th clock) during Client transmit.

Work around

Software should ignore the Client interrupt that is asserted after sending a NACK.

Affected Silicon Revisions

A1							
X							

5. Module: I²C

In Client mode with DHEN = 1 (Data Hold Enable), if software sends a NACK, the Client interrupt is asserted if there are any bytes on the bus.

Work around

Software should ignore the Client interrupt that is asserted after sending a NACK.

Affected Silicon Revisions

A1							
X							

6. Module: ADC

When operating ADC with an Input Frequency (F_{SRC}) above 50 MHz, conversion errors may occur when enabling Differential-mode (DIFFx = 1).

Work around

During initialization of the ADC to write the ADMODxL/H registers, use a slower input frequency of 50 MHz or less. After completion of the 1st conversion of each channel in Differential-mode, Input Frequency, F_{SRC}, can be increased to the maximum specified in the **"Electrical Characteristics"**.

Affected Silicon Revisions

A1							
X							

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS70005496**B**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

None.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (5/2022)

Initial version of this document; issued for revision **A1**.

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ISBN: 978-1-6683-0490-7

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