

MDT0400GIHC-LVDS	1920 x 1080	LVDS Interface	TFT Module
Specification			
Version: 1		Date: 14/04/2023	
Revision			
1	12/04/2023	First issue	

Display Features			
Display Size			4.00"
Resolution			1920 x 1080
Orientation			Landscape
Appearance			RGB
Logic Voltage			3.3V
Interface			LVDS
Brightness			1000 cd/m ²
Touchscreen			CTP
Module Size	104.87 x 72.22 x 4.76 mm		
Operating Temperature			-20°C ~ +70°C
Pinout	50 way FFC		Box Quantity
Pitch	0.50mm		Weight / Display



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* - For full design functionality, please use this specification in conjunction with the SC5010 specification.(Provided Separately)

Display Accessories	
Part Number	Description
MPBV5	50 Way FFC to cable and wires. Driven by any driver board that can be wired to a 1mm pitch SHDR-50V-S-B receptacle.
MDIB-CC1	The MDIB-CC1 is a interconnect board for standard pitch pinouts to fine pitch wires. Ideal for prototyping of TFT and COG LCDs.

Optional Variants	
Appearances	Voltage



* Description

This is a color active matrix LTPS LCD using Low Temperature Poly-silicon TFT's (Thin Film Transistors) as an active switching devices. This module is composed of a Transmissive type LTPS-LCD Panel, driver circuit, back-light unit. The resolution of a 4.0" LTPS-LCD contains 1920X1080 pixels, and can display up to 16.7M colors.

* Features

General Information Items	Specification	Unit	Note
	Main Panel		
Display area(AA)	88.5888(H)*49.8312(V) (4.0 inch)	mm	
Driver element	LTPS	-	
Display colors	16.7M	colors	
Number of pixels	1920(RGB)*1080	dots	
Pixel arrangement	RGB vertical stripe	-	
Pixel pitch	0.04614(H)*0.04614(V)	mm	
Viewing angle	ALL	o'clock	
Controller IC	SC5010	-	
LCM Interface	1 or 2 Port LVDS,VESA mode	-	
Display mode	Transmissive /Normally Black	-	
Operating temperature	-20~+70	°C	
Storage temperature	-30~+80	°C	
Module bonding technology	Use Optical bonding between LCM and CTP	-	

*CTP Features

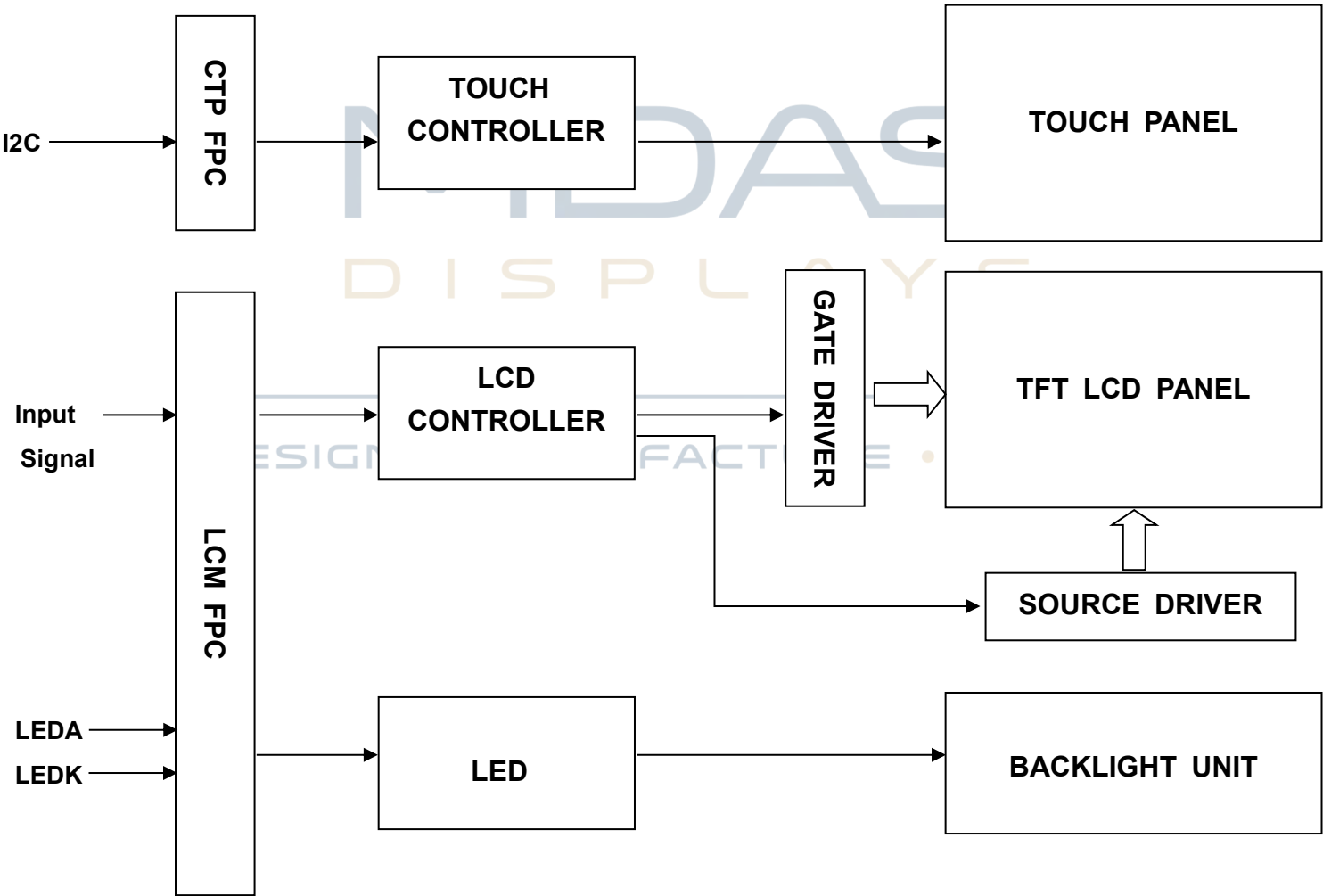
General Information Items	Specification	Unit	Note
	Main Panel		
Resolution	1920(H)*1080(V)	-	
Structure	G+G	-	
Controller IC	ST1633i	-	
Interface	I2C	-	
Slave Adress	0x55	-	Note1
Touch mode	Five points	-	-
Logic level	3.3	V	



*** Mechanical Information**

Item		Min.	Typ.	Max.	Unit	Note
Module size	Horizontal(H)	-	104.87	-	mm	
	Vertical(V)	-	72.22	-	mm	
	Depth(D)	-	4.76	--		
Weight		-	66	-	g	

Block Diagram



Input terminal Pin Assignment

1. TFT PIN Define

NO.	SYMBOL	DISCRIPTION	I/O
1	YU(NC)	--	--
2	XL(NC)	--	--
3	YD(NC)	--	--
4	XR(NC)	T--	--
5	VDD_MTP	Please open this PIN.	--
6	VCC	Digital power-3.3v	P
7	NC	--	--
8	BIST	Built-in self test function: "H":Enable "L":Disable	I
9	IFSEL0	Interface select: "H":2-Port LVDS "L":1-Port LVDS	I
10	SELB	Data format: "H":8Bit "L":6Bit	I
11	L/R	Horizontal shift direction (source output) selection(NOTE1)	Note1
12	U/D	Vertical shift direction (gate output) selection(NOTE1)	Note1
13	RESET	Reset Pin. Low active.	I
14	STBYB	Standby mode: 'H': Power on (Default) . 'L': Power off.	I
15	GND	Ground.	P
16	OD0-	Odd LVDS Negative data signal (-)	I
17	OD0+	Odd LVDS Positive data signal (+)	
18	GND	Ground.	P
19	OD1-	Odd LVDS Negative data signal (-)	I
20	OD1+	Odd LVDS Positive data signal (+)	

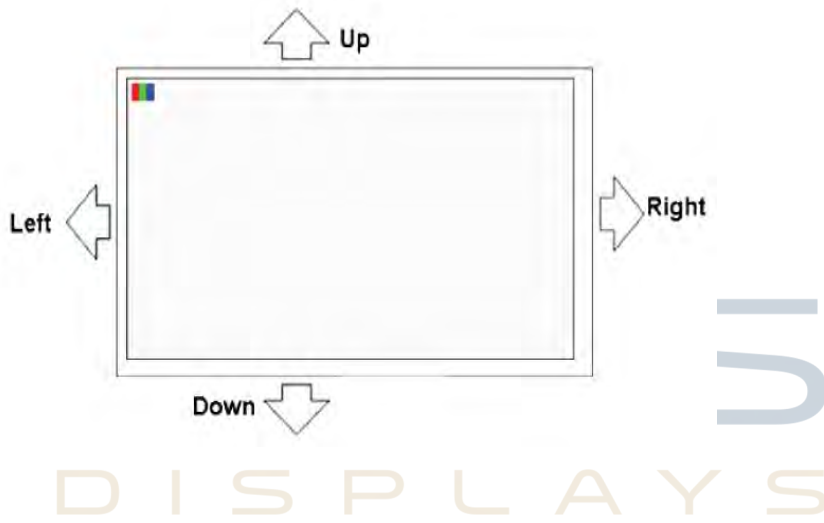


21	GND	Ground.	P
22	OCLK-	Odd LVDS Negative CLK signal (-)	I
23	OCLK+	Odd LVDS Positive CLK signal (+)	
24	GND	Ground.	P
25	OD2-	Odd LVDS Negative data signal (-)	I
26	OD2+	Odd LVDS Positive data signal (+)	
27	GND	Ground.	P
28	OD3-	Odd LVDS Negative data signal (-)	I
29	OD3+	Odd LVDS Positive data signal (+)	
30	GND	Ground.	P
31	ED0-	EVEN LVDS Negative data signal (-)	I
32	ED0+	EVEN LVDS Positive data signal (+)	
33	GND	Ground.	P
34	ED1-	EVEN LVDS Negative data signal (-)	I
35	ED1+	EVEN LVDS Positive data signal (+)	
36	GND	Ground.	P
37	ECLK-	EVEN LVDS Negative CLK signal (-)	I
38	ECLK+	EVEN LVDS Positive CLK signal (+)	
39	GND	Ground.	P
40	ED2-	EVEN LVDS Negative data signal (-)	I
41	ED2+	EVEN LVDS Positive data signal (+)	
42	GND	Ground.	P
43	ED3-	EVEN LVDS Negative data signal (-)	I
44	ED3+	EVEN LVDS Positive data signal (+)	
45	GND	Ground.	P
46	SPI_CS	Please open this PIN.	--
47	SPI_SCL	Please open this PIN.	--



48	SPI_SDA	Please open this PIN.	--
49	LEDK	Cathode pin of backlight.	P
50	LEDA	Anode pin of backlight.	P

Note1: When L/R="1", set left to right scan direction.
 When L/R="0", set right to left scan direction.
 When U/D="1", set up to down scan direction.
 When U/D="0", set down to up scan direction.



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2. CTP PIN Define

NO.	SYMBOL	DISCRIPTION	I/O
1	GND	Ground	P
2	NC	No Connection	--
3	VDD	Supply voltage	P
4	SCL	I2C clock input	I
5	SDA	I2C data input and output	I
6	INT	External interrupt to the host	I
7	RST	External Reset, Low is active	I
8	GND	Ground	P



LCD Optical Characteristics

1. Optical specification

Item	Symbol	Condition	Min.	Typ.	Max.	Unit.	Note
Contrast Ratio	CR	$\Theta=0$	900	1200	--		(1)(2)
Response time	Rising	T_{R+T_F}	--	40	45	msec	(1)(3)
	Falling						
Color Gamut	S(%)		39	42	--	%	
Color Filter Chromacicity	White	W_X	-0.04	0.3167	+0.04		CA-310 test
		W_Y		0.3279			
	Red	R_X		0.5573			
		R_Y		0.3449			
	Green	G_X		0.3567			
		G_Y		0.5249			
	Blue	B_X		0.1511			
		B_Y		0.0912			
Viewing angle	Hor.	Θ_L	70	80	--		(1)(4)
		Θ_R	70	80	--		
	Ver.	Θ_U	70	80	--		
		Θ_D	70	80	--		
Option View Direction			ALL				

Measuring Condition

Measuring surrounding : dark room

Ambient temperature : 25±2°C

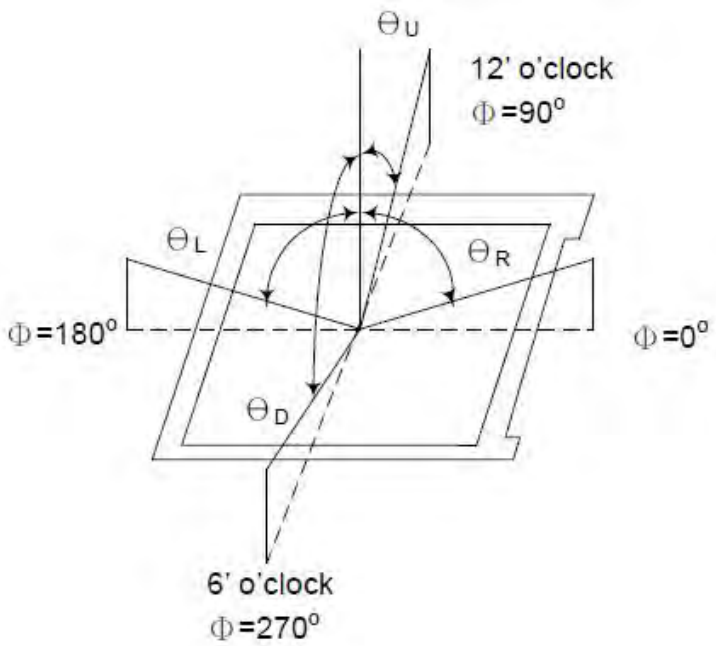
15min. warm-up time.

Measuring Equipment

FPM520 of Westar Display technologies, INC., which utilized SR-3 for Chromaticity and BM-5A for other optical characteristics.



Note (1): Definition of Viewing Angle :

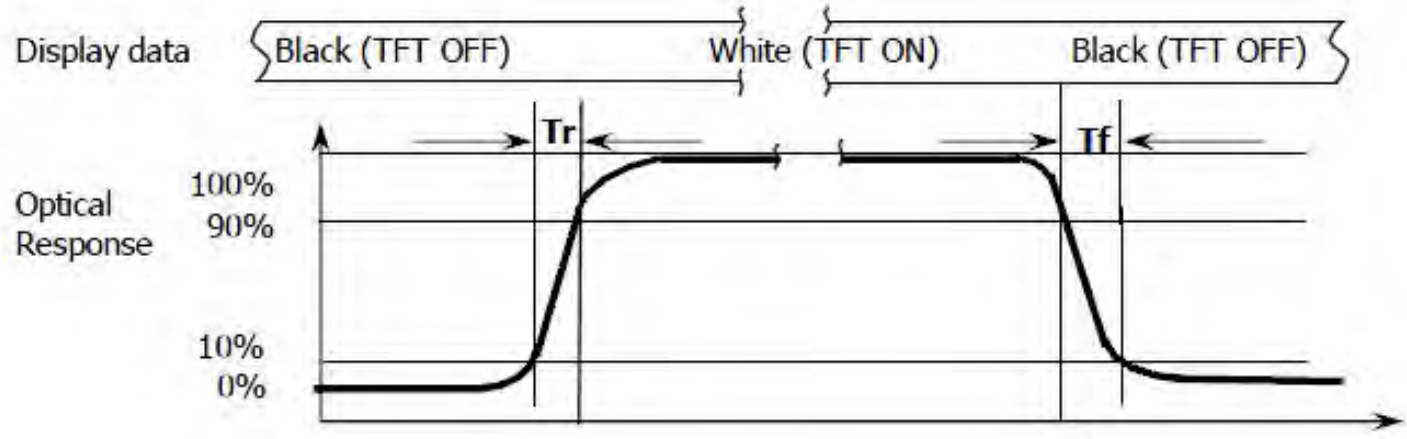


Note (2): Definition of Contrast Ratio(CR) :measured at the center point of panel

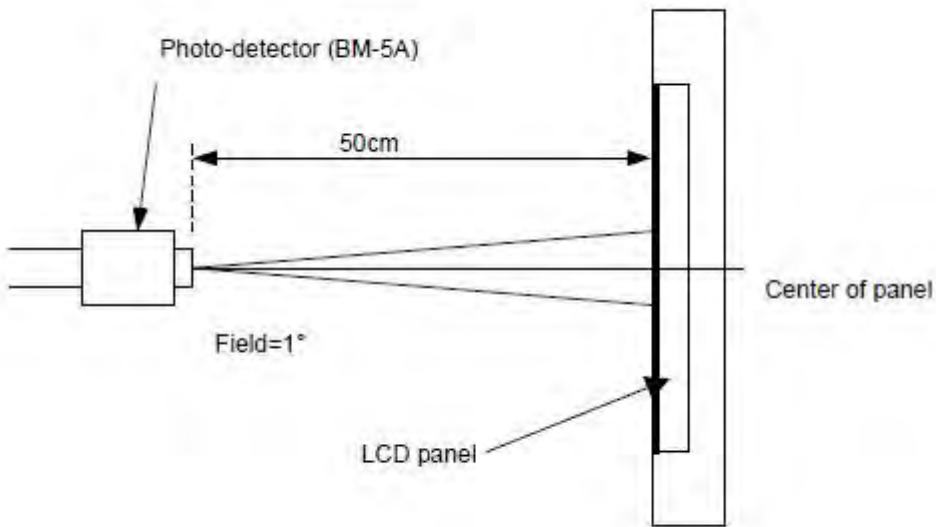
$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

Note (3): Response Time

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Note (4): Definition of optical measurement setup



MIDAS
DISPLAYS

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Electrical Characteristics

1. Absolute Maximum Rating

Characteristics	Symbol	Min.	Max.	Unit	Note
Digital Supply Voltage	VCC	-0.3	6.0	V	Note1
Operating temperature	T _{OP}	-20	+70	°C	
Storage temperature	T _{ST}	-30	+80	°C	

NOTE1: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

2. DC Electrical Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Note
Digital Supply Voltage	VCC	3.0	3.3	3.6	V	
Normal mode Current consumption	I _{DD}	--	111	220	mA	
Level input voltage	V _{IH}	0.7*V _{CC}	--	VCC	V	
	V _{IL}	GND	--	0.3*V _{CC}	V	
Level output voltage	V _{OH}	0.8*V _{CC}	--	VCC	V	
	V _{OL}	GND	--	GND+0.4	V	



3. LED Backlight Characteristics

The back-light system is edge-lighting type with 12 chips LED

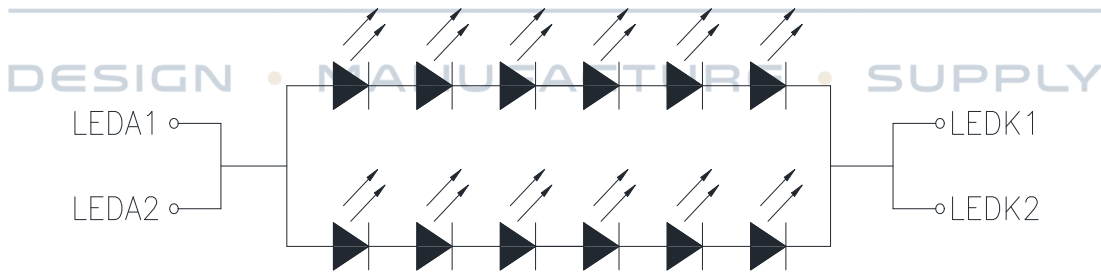
Item	Symbol	Min.	Typ.	Max.	Unit	Note
Forward Current	I_F	--	40	--	mA	
Forward Voltage	V_F	16.2	19.2	20.4	V	
LCM Luminance	LV	950	1000	--	cd/m ²	$I_F=40\text{mA}$
LED life time	Hr	--	50000	--	Hour	Note1,2
Uniformity	Avg	80	--	--	%	Note3

Note1: LED life time (Hr) can be defined as the time in which it continues to operate under the condition:

$T_a=25\pm 3\text{ }^\circ\text{C}$, typical I_L value indicated in the above table until the brightness becomes less than 50%.

Note 2: The "LED life time" is defined as the module brightness decrease to 50% original brightness at

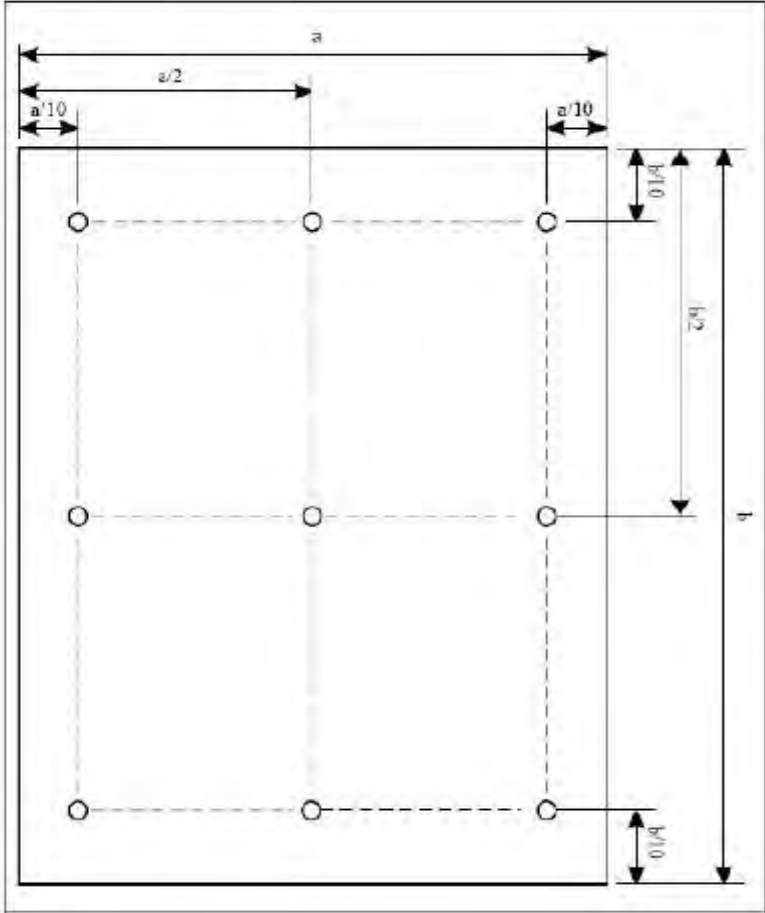
$T_a=25\text{ }^\circ\text{C}$ and $I_L=40\text{mA}$. The LED lifetime could be decreased if operating I_L is larger than 40mA. The constant current driving method is suggested.



LED (B/L) CIRCUIT



Note (3) Luminance Uniformity of these 9 points is defined as below:



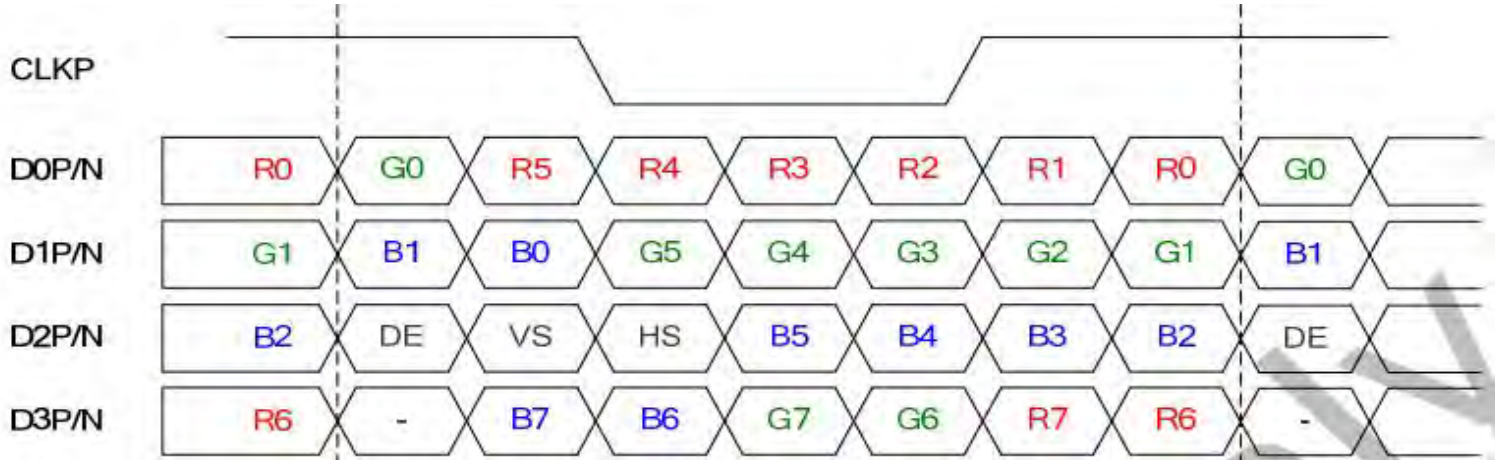
$$\text{Uniformity} = \frac{\text{minimum luminance in 9 points (1-9)}}{\text{maximum luminance in 9 points (1-9)}}$$



AC Characteristics

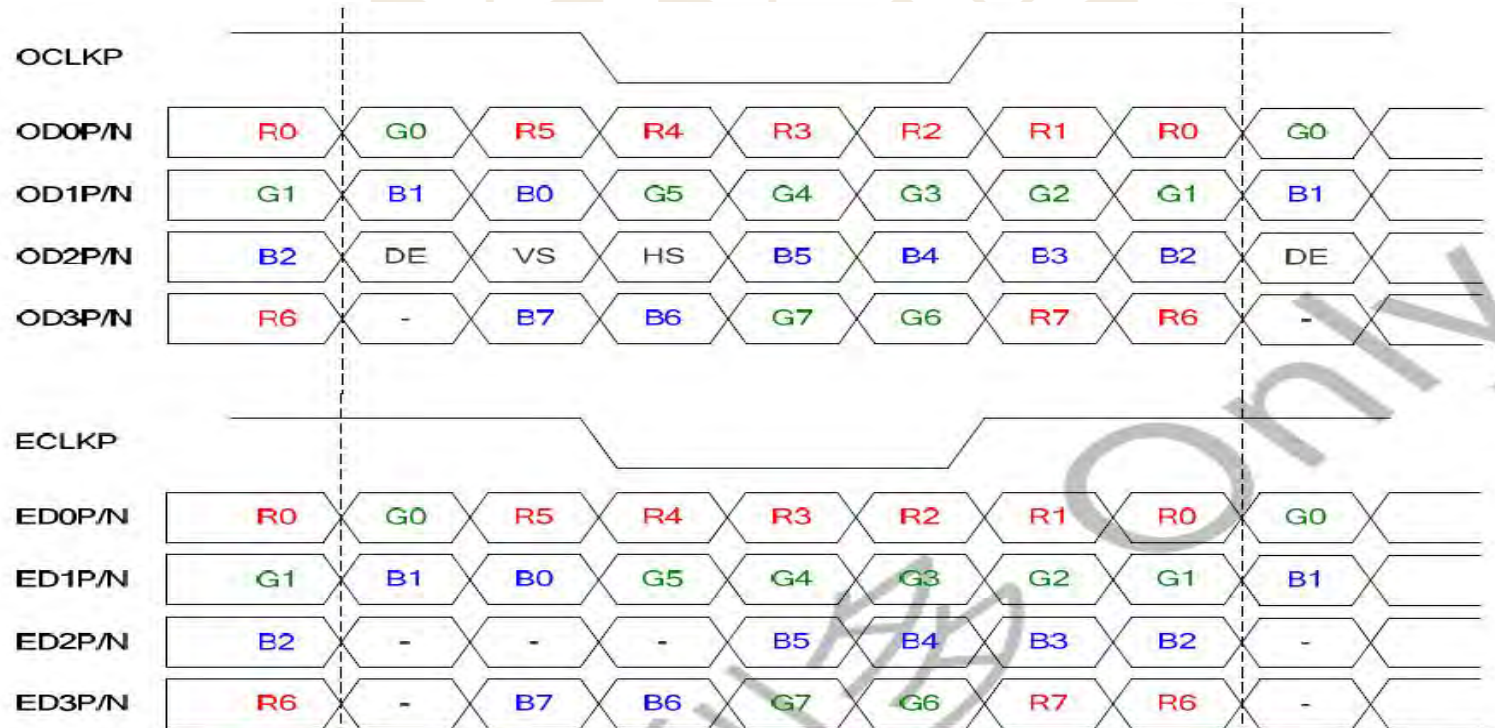
1. LVDS Interface

1.1 1-Port LVDS VESA Data Mapping



Note 1 : for 6 bit mode, MSB are R/G/B[5] and R/G/B[0] are LSB
 Note 2 : for 8 bit mode, MSB are R/G/B[7] and R/G/B[0] are LSB

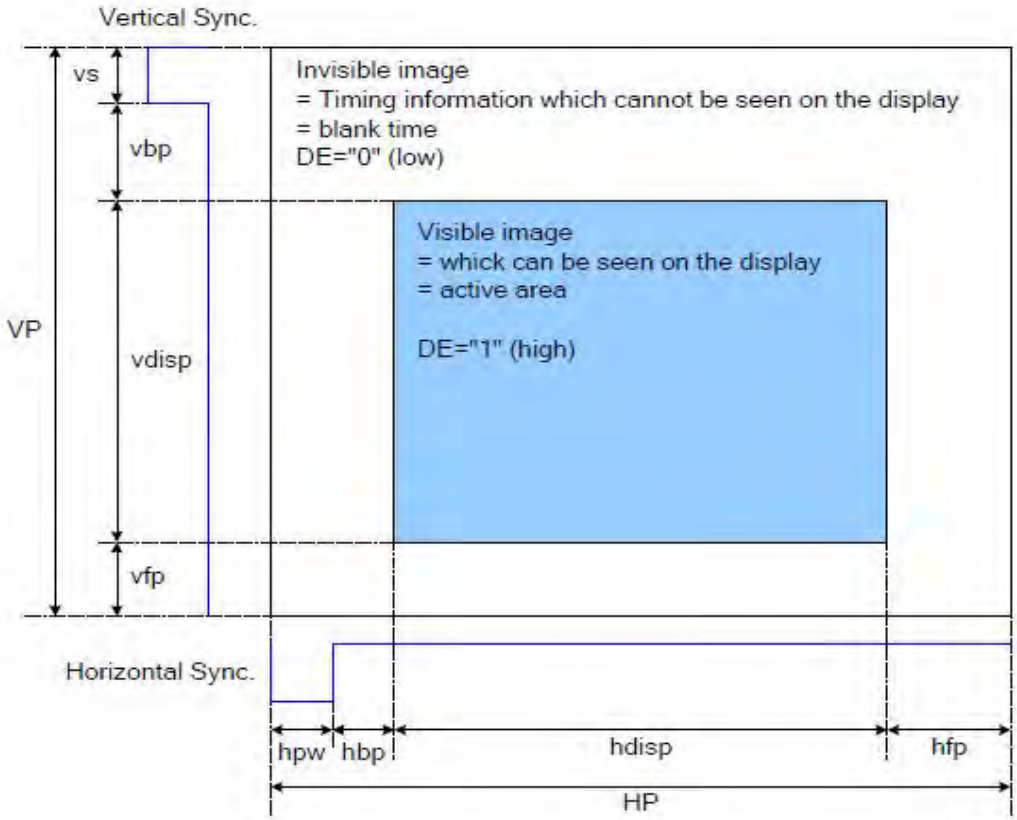
1.2 2-Port LVDS VESA Data Mapping



Note 1 : for 6 bit mode, MSB are R/G/B[5] and R/G/B[0] are LSB
 Note 2 : for 8 bit mode, MSB are R/G/B[7] and R/G/B[0] are LSB



2. Timing for LVDS mode



DRAM Access Area by RGB Interface

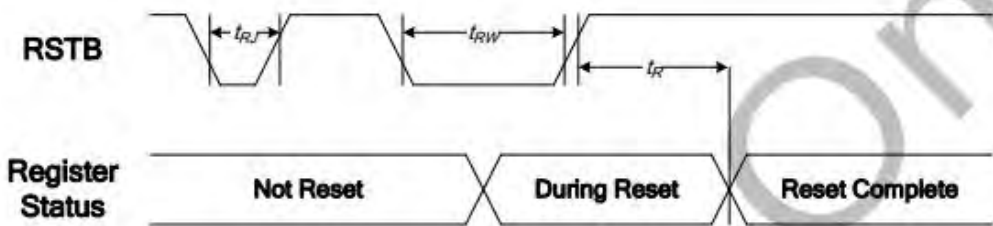
Please refer to the following table for the setting limitation of RGB interface signals.(Only 2-Port)

Parameter	Symbol	Min.	Typ.	Max.	Unit
DCLK frequency	FCLK	--	(132)	--	MHz
Horizontal display area	HDISP	--	1920	--	Line
Horizontal Sync. Width	hpw	1	4	--	Line
Horizontal Sync. Back Porch	hbp	1	10	--	Line
Horizontal Sync. Front Porch	hfp	1	40	--	Line
Vertical display area	VDISP	--	1080	--	Line
Vertical Sync. Width	vs	2	4	--	Line
Vertical Sync. Back Porch	vbp	2	10	--	Line
Vertical Sync. Front Porch	vfp	2	20	--	Line
Frame-Rate		--	60	--	Hz

Note: Typical value are related to the setting frame rate is 60Hz.

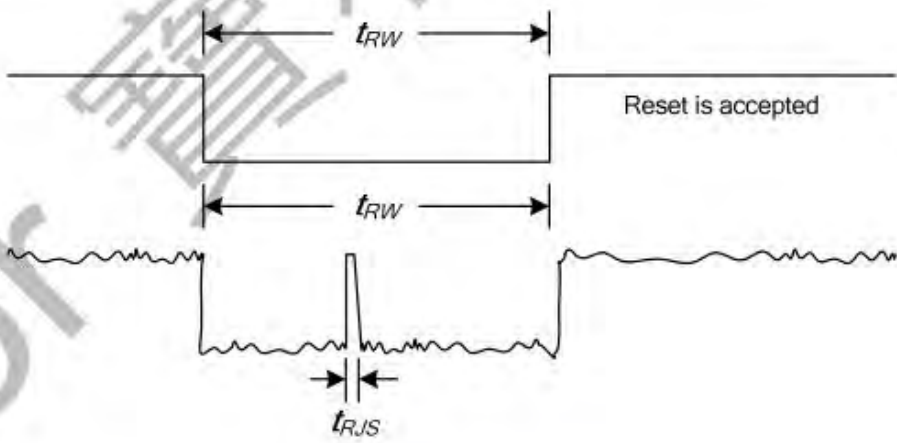


3. Hardware Reset Timing



VSSI = VSSRX = VSSP = 0V, VDDI = VDDP = VDDR = 3.0 ~ 3.3V, Ta = -40 ~ 85°C

Item	Signal	Symbol	Condition	Rating		Unit
				Min.	Max.	
Reset time	RSTB	t_R		—	5	us
Reset "L" pulse width		t_{RW}		15	—	
Reset rejection		t_{RJ}		—	5	
Reset rejection (for noise spike)		t_{RJS}		—	10	ns



Note:

1. For PROM related operation, it takes 50ms at least for PROM Registers to load PROM contents. Do not use any PROM related command during this period.
2. When the system issues a RSTB low pulse, the reset procedure of IC will start if the low pulse is longer than t_{RW} specified above. If the low pulse is less than t_{RJ} specified above, the reset procedure of IC will not start. If the low pulse is longer than t_{RJ} and less than t_{RW} , the reset procedure of IC is not guaranteed.



CTP Specification

1. Electrical Characteristics

1.1 Absolute Maximum Rating

Item	Symbol	Min.	Max.	Unit	Note
Power Supply Voltage	VDD	-0.3	6	V	
Operating temperature	T _{OP}	-20	+70	°C	
Storage temperature	T _{ST}	-30	+80	°C	

*Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. All the ranges are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended.

Exposed to the absolute maximum rating conditions for extended periods may affect device reliability.

1.2 DC Electrical Characteristics (Ta=25°C)

(Ambient temperature:25°C, VDD=3.3V, VDDIO=1.8V or VDDIO=VDD)

Item	Min.	Typ.	Max.	Unit	Note
Power Supply Voltage/VDD	2.7	3.3	3.6	V	
Normal mode operating current	--	16.1	24	mA	
Green mode operating current	--	8.1	12.2	mA	
Power Down Current	--	--	20	uA	
Digital Input low voltage/VIL	--	--	0.15*VDD	V	
Digital Input high voltage/VIH	0.85*VDD	--	--	V	



2. AC Electrical Characteristics

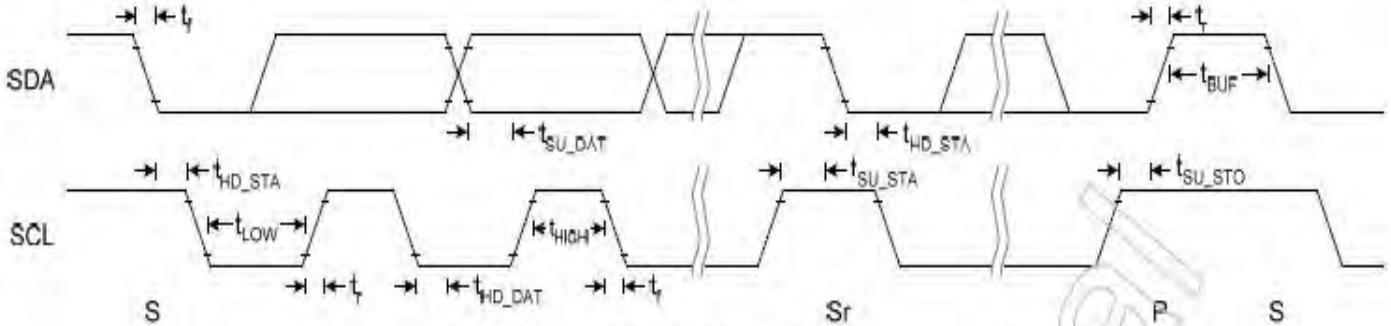


Figure 5-1 I2C Fast Mode Timing

Table 5-3 I2C Fast Mode Timing Characteristic

Conditions: VDD = 3.3V, GND = 0V, T_A = 25°C

Symbol	Parameter	Rating			Unit
		Min.	Typ.	Max.	
f _{SCL}	SCL clock frequency	0	-	400	kHz
t _{LOW}	Low period of the SCL clock	1.3	-	-	us
t _{HIGH}	High period of the SCL clock	0.6	-	-	us
t _f	Signal falling time	-	-	300	ns
t _r	Signal rising time	-	-	300	ns
t _{SU_STA}	Set up time for a repeated START condition	0.6	-	-	us
t _{HD_STA}	Hold time (repeated) START condition. After this period, the first clock pulse is generated	0.6	-	-	us
t _{SU_DAT}	Data set up time	100	-	-	ns
t _{HD_DAT}	Data hold time	0	-	0.9	us
t _{SU_STO}	Set up time for STOP condition	0.6	-	-	us
t _{BUF}	Bus free time between a STOP and START condition	1.3	-	-	us
C _b	Capacitive load for each bus line	-	-	400	pF

3. SYSTEM MANAGEMENT

3.1 Power Down

In power down mode, all of the clocks of ST1633i are stopped. The way to exit power down mode is by a hardware reset or I2C.

3.2 Reset

Master can reset ST1633i through RESET pin. RESET pin is low active and needs hold low for 1us to take effect.

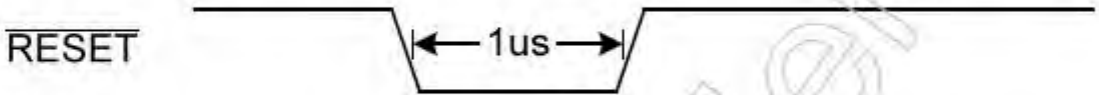


Figure 3-1 $\overline{\text{RESET}}$ Pin Low Pulse Width

3.3 Power On/Off Sequence

RESET pin should be held low before power on and power off. During power on, after both VDD and IOVDD reach normal voltage, RESET pin needs to be held low for 5ms to ensure internal block stable. Note: IOVDD and VDD had connected together.

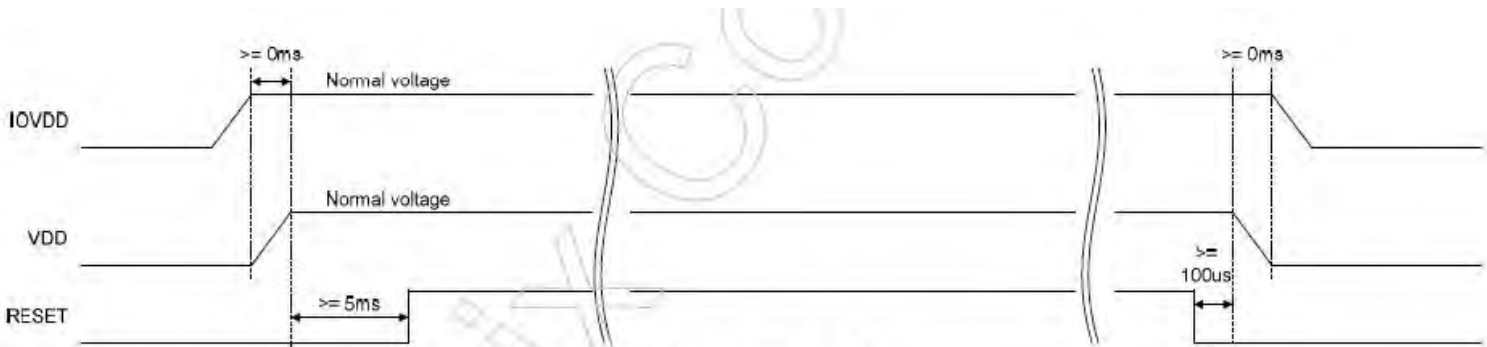


Figure 3-2 Power On/Off Sequence



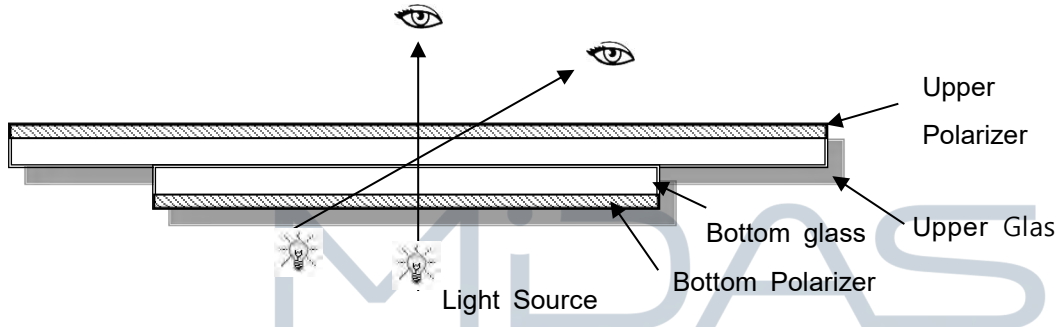
LCD Module Out-Going Quality Level

1. VISUAL & FUNCTION INSPECTION STANDARD

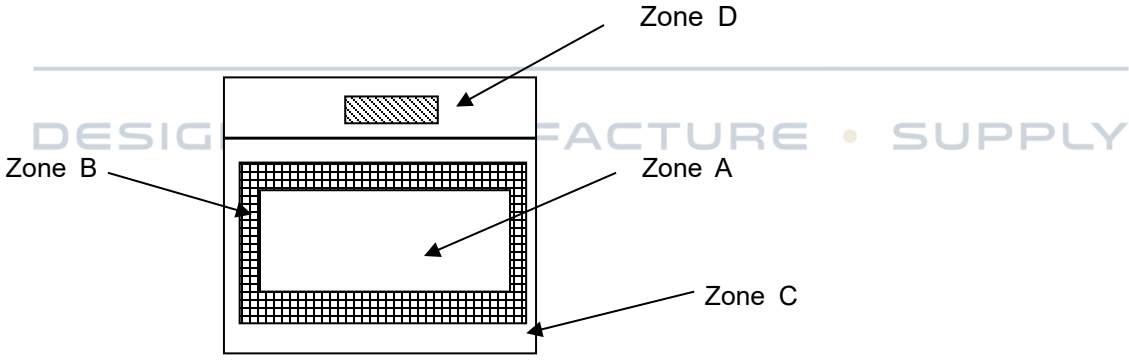
1.1 Inspection conditions

Inspection performed under the following conditions is recommended.

- Temperature : $25 \pm 5^{\circ}\text{C}$
- Humidity : $65\% \pm 10\% \text{RH}$
- Viewing Angle : Normal viewing Angle.
- Illumination: Single fluorescent lamp (300 to 700Lux)
- Viewing distance: 30-50cm



1.2 Definition



- Zone A : Effective Viewing Area(Character or Digit can be seen)
- Zone B : Viewing Area except Zone A
- Zone C : Outside (Zone A+Zone B) which can not be seen after assembly by customer
- Zone D : IC Bonding Area

Note:As a general rule ,visual defects in Zone C can be ignored when it doesn't effect product function or appearance after assembly by customer



1.3 Sampling Plan

According to GB/T 2828-2003 ; , normal inspection, Class II

AQL:

Major defect	Minor defect
0.65	1.5

LCD: Liquid Crystal Display , LCM: Liquid Crystal Module, CTP: Capacitive Touch Panel

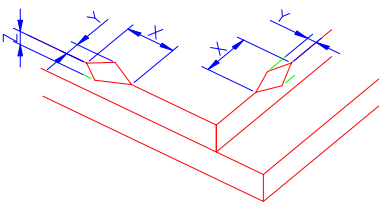
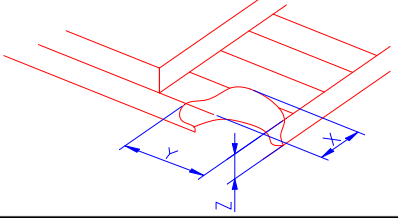
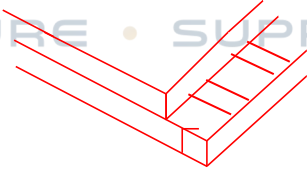
No	Items to be inspected	Criteria	Classification of defects
1	Functional defects	1) No display, Open or miss line 2) Display abnormally, Short 3) Backlight no lighting, abnormal lighting. etc	Major
2	Missing	Missing components and etc	
3	Outline dimension	Overall outline dimension beyond the drawing is not allowed, deformation and etc	
4	Color tone	Color unevenness, refer to limited sample	Minor
5	Spot/Line defect	Light dot, Dim spot, (Note1) Polarizer Air Bubble, Polarizer accidented spot and etc.	
6	Soldering appearance	Good soldering , Peeling off is not allowed and etc.	
7	LCD/Polarizer/CTP	Black/White spot/line, scratch, crack, etc.	

Note1: a) Light dot: Dots appear bright and unchanged in size in which LCD panel is displaying under black pattern.

b) Dim dot: Dots appear dark and unchanged in size in which LCD panel is displaying under pure red, green, blue picture.



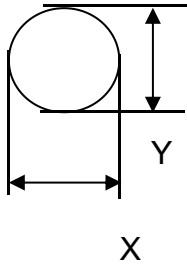
1.4 Criteria (Visual)

Number	Items	Criteria(mm)						
1.0 LCD Crack/Broken NOTE: X: Length Y: Width Z: Height L: Length of IT O, T: Height of LCD	(1) The edge of LCD broken	 <table border="1" data-bbox="756 600 1453 745"> <thead> <tr> <th>X</th> <th>Y</th> <th>Z</th> </tr> </thead> <tbody> <tr> <td>≤3.0mm</td> <td><Inner border line of the seal</td> <td>≤T</td> </tr> </tbody> </table>	X	Y	Z	≤3.0mm	<Inner border line of the seal	≤T
	X	Y	Z					
	≤3.0mm	<Inner border line of the seal	≤T					
(2) LCD corner broken	 <table border="1" data-bbox="834 1055 1372 1155"> <thead> <tr> <th>X</th> <th>Y</th> <th>Z</th> </tr> </thead> <tbody> <tr> <td>≤3.0mm</td> <td>≤L</td> <td>≤T</td> </tr> </tbody> </table>	X	Y	Z	≤3.0mm	≤L	≤T	
X	Y	Z						
≤3.0mm	≤L	≤T						
(3) LCD crack	 <p style="text-align: center;">Crack Not allowed</p>							



2.0

Spot defect



$$\Phi = (X + Y) / 2$$

① light dot (black/white spot , pinhole, stain, etc.)

Zone Size (mm)	Acceptable Qty		
	A	B	C
$\Phi \leq 0.15$	Ignore		
$0.15 < \Phi \leq 0.25$	3(distance ≥ 6 mm)		
$0.25 < \Phi \leq 0.4$	2(distance ≥ 6 mm)		
$\Phi > 0.4$	0		

② Dim spot (light leakage, dent, dark spot, etc)

Zone Size (mm)	Acceptable Qty		
	A	B	C
$\Phi \leq 0.15$	Ignore		
$0.15 < \Phi \leq 0.25$	3(distance ≥ 6 mm)		
$0.25 < \Phi \leq 0.4$	2(distance ≥ 6 mm)		
$\Phi > 0.4$	0		

③ Polarizer accidented spot

Zone Size (mm)	Acceptable Qty		
	A	B	C
$\Phi \leq 0.2$	Ignore		
$0.2 < \Phi \leq 0.5$	2(distance ≥ 6 mm)		
$\Phi > 0.5$	0		

④ Polarizer Bubble

Zone Size (mm)	Acceptable Qty		
	A	B	C
$\Phi \leq 0.2$	Ignore		
$0.2 < \Phi \leq 0.4$	3(distance ≥ 6 mm)		
$\Phi > 0.4$	0		



3.0 LCD Pixel defect

Pixel bad points

Item	Zone A	Acceptable Qt
Bright dot	Random	$N \leq 2$
	2 dots adjacent	$N \leq 0$
	3 dots adjacent	$N \leq 0$
Dark dot	Random	$N \leq 2$
	2 dots adjacent	$N \leq 0$
	3 dots adjacent	$N \leq 0$
Distance	1. Minimum Distance Between Bright dots. 2. Minimum Distance Between dark dots 3. Minimum Distance Between dark and bright dot.	5mm
Total bright and dark dot		$N \leq 4$

Note:

A) Bright dot: Dots appear bright and unchanged in size in which LCD panel is displaying under black pattern.

B) Dark dot: Dots appear dark and unchanged in size in which LCD panel is displaying under pure red, green, blue picture.

C) 2 dot adjacent = 1 pair = 2 dots

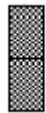
Picture:



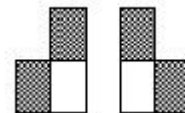
2 dot adjacent



2 dot adjacent




2 dot adjacent (vertical)



2 dot adjacent (slant)



4.0	Line defect (LCD /Polarizer backlight black/white line, scratch, stain)  W: width, L : length N : Count	<table border="1"> <thead> <tr> <th rowspan="2">Width(mm)</th> <th rowspan="2">Length(m)</th> <th colspan="3">Acceptable Qty</th> </tr> <tr> <th>A</th> <th>B</th> <th>C</th> </tr> </thead> <tbody> <tr> <td>$\Phi \leq 0.03$</td> <td>Ignore</td> <td colspan="2">Ignore</td> <td rowspan="3">Ignore</td> </tr> <tr> <td>$0.03 < W \leq 0.04$</td> <td>$L \leq 3.0$</td> <td colspan="2">$N \leq 2$</td> </tr> <tr> <td>$0.04 < W \leq 0.05$</td> <td>$L \leq 2.0$</td> <td colspan="2">$N \leq 1$</td> </tr> <tr> <td>$W > 0.05$</td> <td colspan="4">Define as spot defect</td> </tr> </tbody> </table>	Width(mm)	Length(m)	Acceptable Qty			A	B	C	$\Phi \leq 0.03$	Ignore	Ignore		Ignore	$0.03 < W \leq 0.04$	$L \leq 3.0$	$N \leq 2$		$0.04 < W \leq 0.05$	$L \leq 2.0$	$N \leq 1$		$W > 0.05$	Define as spot defect			
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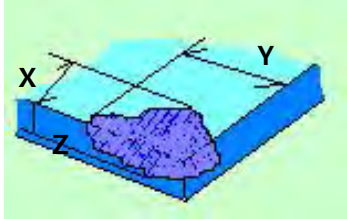
5.0	Electronic Components SMT.	Not allow missing parts, solderless connection, cold solder joint, mismatch, The positive and negative polarity opposite
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6.0	Display color & Brightness.	1. Color: Measuring the color coordinates, The measurement standard according to the datasheet or samples. 2. Brightness: Measuring the brightness of White screen, The measurement standard according to the datasheet or Samples.
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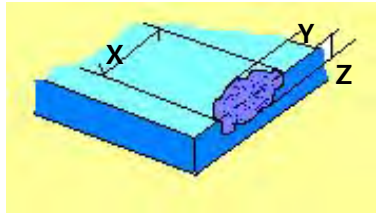
7.0	LCD Mura/Waving/ Hot spot	Not visible through 5% ND filter in 50% gray or judge by limit sample if necessary.
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8.0	CTP Related	CTP Cover sensor accidented black/white spot	<table border="1"> <thead> <tr> <th rowspan="2">Size Φ(mm)</th> <th colspan="3">Acceptable Qty</th> </tr> <tr> <th>A</th> <th>B</th> <th>C</th> </tr> </thead> <tbody> <tr> <td>$\Phi \leq 0.1$</td> <td colspan="2">Ignore</td> <td rowspan="4">Ignore</td> </tr> <tr> <td>$0.1 < \Phi \leq 0.2$</td> <td colspan="2">2 (distance $> 2mm$)</td> </tr> <tr> <td>$0.20 < \Phi \leq 0.25$</td> <td colspan="2">2 (distance $> 5mm$)</td> </tr> <tr> <td>$\Phi > 0.25$</td> <td colspan="2">0</td> </tr> </tbody> </table>	Size Φ (mm)	Acceptable Qty			A	B	C	$\Phi \leq 0.1$	Ignore		Ignore	$0.1 < \Phi \leq 0.2$	2 (distance $> 2mm$)		$0.20 < \Phi \leq 0.25$	2 (distance $> 5mm$)		$\Phi > 0.25$	0	
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		CTP Cover	<table border="1"> <thead> <tr> <th rowspan="2">Width(mm)</th> <th rowspan="2">Ignore (mm)</th> <th colspan="3">Acceptable Qty</th> </tr> <tr> <th>A</th> <th>B</th> <th>C</th> </tr> </thead> <tbody> <tr> <td>$\Phi \leq 0.03$</td> <td>Ignore</td> <td colspan="3">Ignore</td> </tr> <tr> <td>$0.03 < W \leq 0.04$</td> <td>$L \leq 3.0$</td> <td colspan="3">$N \leq 2$</td> </tr> <tr> <td>$0.04 < W \leq 0.05$</td> <td>$L \leq 2.0$</td> <td colspan="3">$N \leq 1$</td> </tr> <tr> <td>$0.05 < W$</td> <td colspan="4">Define as spot defect</td> </tr> </tbody> </table>	Width(mm)	Ignore (mm)	Acceptable Qty			A	B	C	$\Phi \leq 0.03$	Ignore	Ignore			$0.03 < W \leq 0.04$	$L \leq 3.0$	$N \leq 2$			$0.04 < W \leq 0.05$	$L \leq 2.0$	$N \leq 1$			$0.05 < W$	Define as spot defect			
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		CTP Cover Pinhole/ Lack of ink	<table border="1"> <thead> <tr> <th>Zone Size (mm)</th> <th>Acceptable Qty</th> </tr> </thead> <tbody> <tr> <td>$\Phi \leq 0.1$</td> <td>Ignore</td> </tr> <tr> <td>$0.1 < \Phi \leq 0.25$</td> <td>3(distance ≥ 6mm)</td> </tr> <tr> <td>$0.25 < \Phi \leq 0.3$</td> <td>2(distance ≥ 6mm)</td> </tr> <tr> <td>$\Phi > 0.3$</td> <td>0</td> </tr> </tbody> </table>	Zone Size (mm)	Acceptable Qty	$\Phi \leq 0.1$	Ignore	$0.1 < \Phi \leq 0.25$	3(distance ≥ 6 mm)	$0.25 < \Phi \leq 0.3$	2(distance ≥ 6 mm)	$\Phi > 0.3$	0																		
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		CTP Bonding bubble/accident spot	<table border="1"> <thead> <tr> <th rowspan="2">Size Φ(mm)</th> <th colspan="2">Acceptable Qty</th> </tr> <tr> <th>A</th> <th>B</th> </tr> </thead> <tbody> <tr> <td>$\Phi \leq 0.1$</td> <td colspan="2">Ignore</td> </tr> <tr> <td>$0.1 < \Phi \leq 0.2$</td> <td colspan="2">2(distance ≥ 6mm)</td> </tr> <tr> <td>$0.2 < \Phi \leq 0.25$</td> <td colspan="2">2(distance ≥ 6mm)</td> </tr> <tr> <td>$\Phi > 0.25$</td> <td colspan="2">0</td> </tr> </tbody> </table>	Size Φ (mm)	Acceptable Qty		A	B	$\Phi \leq 0.1$	Ignore		$0.1 < \Phi \leq 0.2$	2(distance ≥ 6 mm)		$0.2 < \Phi \leq 0.25$	2(distance ≥ 6 mm)		$\Phi > 0.25$	0												
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		Assembly deflection	beyond the edge of backlight ≤ 0.2 mm																												
		CTP cover broken	<table border="1"> <thead> <tr> <th>X</th> <th>Y</th> <th>Z</th> </tr> </thead> <tbody> <tr> <td>$X \leq 0.5$mm</td> <td>$Y \leq 0.5$mm</td> <td>$Z < \text{cover thickness}$</td> </tr> </tbody> </table> <p>* Circuitry broken is not allowed.</p>	X	Y	Z	$X \leq 0.5$ mm	$Y \leq 0.5$ mm	$Z < \text{cover thickness}$																						
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		CTP cover broken	X	Y	Z	
			$X \leq 0.3\text{mm}$	$Y \leq 0.3\text{mm}$	$Z < \text{cover thickness}$	
		X : length	* Circuitry broken is not allowed.			
		Y : width				
		Z : height				

Criteria (functional items)

Number	Items	Criteria (mm)
1	No display	Not allowed
2	Missing segment	Not allowed
3	Short	Not allowed
4	Backlight no lighting	Not allowed

MIDAS
DISPLAYS

DESIGN • MANUFACTURE • SUPPLY



Reliability Test Result

Item	Condition	Inspection after test
High Temperature Operating	70°C,96HR	Inspection after 2~4hours storage at room temperature, the sample shall be free from defects: 1.Air bubble in the LCD; 2.Non-display; 3.Missing segments/line; 4.Glass crack; 5.Current IDD is twice higher than initial value.
Low Temperature Operating	-20°C, 96HR	
High Temperature Storage	80°C, 96HR	
Low Temperature Storage	-30°C, 96HR	
High Temperature & High Humidity Operating	+60°C, 90% RH ,96 hours.	
Thermal Shock (Non-operation)	-30°C,30 min ↔ +80°C,30 min, Change time:5min 20CYC.	
ESD test	C=150pF, R=330,5points/panel Air:±8KV, 5times; Contact:±6KV, 5 times; (Environment: 15°C~35°C, 30%~60%).	
Vibration (Non-operation)	Frequency range:10~55Hz, Stroke:1.5mm Sweep:10Hz~55Hz~10Hz 2 hours for each direction of X.Y.Z. (6 hours for total) (Package condition).	
Box Drop Test	1 Corner 3 Edges 6 faces,80cm(MEDIUM BOX)	

- Remark:
- 1.The test samples should be applied to only one test item.
 - 2.Sample size for each test item is 5~10pcs.
 - 3.For Damp Proof Test, Pure water(Resistance > 10MΩ) should be used.
 - 4.In case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting, it would be judged as a good part.
 - 5.Failure Judgment Criterion: Basic Specification, Electrical Characteristic, Mechanical Characteristic, Optical Characteristic.
 6. The color fading mura of polarizing filter should not care.



Cautions and Handling Precautions

1. Handling and Operating the Module

(1) When the module is assembled, it should be attached to the system firmly.

Do not warp or twist the module during assembly work.

(2) Protect the module from physical shock or any force. In addition to damage, this may cause improper operation or damage to the module and back-light unit.

(3) Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.

(4) Do not allow drops of water or chemicals to remain on the display surface.

If you have the droplets for a long time, staining and discoloration may occur.

(5) If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.

(6) The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane.

Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.

(7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.

(8) Protect the module from static; it may cause damage to the CMOS ICs.

(9) Use finger-stalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.

(10) Do not disassemble the module.

(11) Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.

(12) Pins of I/F connector shall not be touched directly with bare hands.

(13) Do not connect, disconnect the module in the "Power ON" condition.

(14) Power supply should always be turned on/off by the item 6.1 Power On Sequence & 6.2 Power Off Sequence

2. Storage and Transportation.

(1) Do not leave the panel in high temperature, and high humidity for a long time.

It is highly recommended to store the module with temperature from 0 to 35 °C and relative humidity of less than 70%

(2) Do not store the TFT-LCD module in direct sunlight.

(3) The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.

(4) It is recommended that the modules should be stored under a condition where no condensation is allowed. Formation of dewdrops may cause an abnormal operation or a failure of the module.

In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.

(5) This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.

