Product Change Notification / SYST-02CCIL063

Date:

03-Aug-2023

Product Category:

Memory

PCN Type:

Document Change

Notification Subject:

Data Sheet - 23LCV512 - 512-Kbit SPI Serial SRAM with Battery Backup and SDI Interface

Affected CPNs:

SYST-02CCIL063_Affected_CPN_08032023.pdf
SYST-02CCIL063_Affected_CPN_08032023.csv

Notification Text:

SYST-02CCIL063

Microchip has released a new Datasheet for the 23LCV512 - 512-Kbit SPI Serial SRAM with Battery Backup and SDI Interface of devices. If you are using one of these devices please read the document located at 23LCV512 - 512-Kbit SPI Serial SRAM with Battery Backup and SDI Interface.

Notification Status: Final

Description of Change: Updated Section 5.0 VBAT.

Impacts to Data Sheet: See above details.

Reason for Change: To Improve Productivity
Change Implementation Status: Complete

Date Document Changes Effective: 03 Aug 2023

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachments:

23LCV512 - 512-Kbit SPI Serial SRAM with Battery Backup and SDI Interface

Please contact your local Microchip sales office with questions or concerns regarding this notification.

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Affected Catalog Part Numbers (CPN)

23LCV512-I/P
23LCV512-I/SN
23LCV512-I/ST
23LCV512T-I/SN
23LCV512T-I/ST

23LCV512

512-Kbit SPI Serial SRAM with Battery Backup and SDI Interface

Device Selection Table

Part Number	Vcc Range	Dual I/O (SDI)	Battery Backup	Max. Clock Frequency	Packages
23LCV512	2.5V-5.5V	Yes	Yes	20 MHz	SN, ST, P

Features

- SPI-Compatible Bus Interface:
  - 20 MHz Clock rate
  - SPI/SDI mode
- Low-Power CMOS Technology:
  - Read Current: 3 mA at 5.5V, 20 MHz
  - Standby Current: 4 μA at +85°C
- Unlimited Read and Write Cycles
- External Battery Backup Support
- Zero Write Time
- 64K x 8-bit Organization:
  - 32-byte page
- Byte, Page and Sequential Mode for Reads and Writes
- High Reliability
- Temperature Range Supported:
  - Industrial (I): -40°C to +85°C
- RoHS Compliant, Halogen Free.

Packages

- 8-Lead SOIC, 8-Lead TSSOP and 8-Lead PDIP

Pin Function Table

Name	Function
$\overline{CS}$	Chip Select Input
SO/SIO1	Serial Output/SDI pin
Vss	Ground
SI/SIO0	Serial Input/SDI pin
SCK	Serial Clock
VBAT	External Backup Supply Input
Vcc	Power Supply

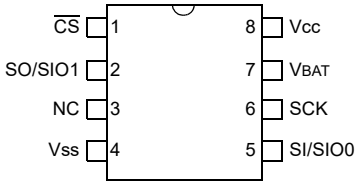
Description

The Microchip Technology Inc. 23LCV512 is a 512-Kbit Serial SRAM device. The memory is accessed via a simple Serial Peripheral Interface (SPI) compatible serial bus. The bus signals required are a clock input (SCK) plus separate data in (SI) and data out (SO) lines. Access to the device is controlled through a Chip Select ($\overline{CS}$) input. Additionally, SDI (Serial Dual Interface) is supported if your application needs faster data rates.

This device also supports unlimited reads and writes to the memory array and supports data backup via an external battery/coin cell connected to VBAT (pin 7).

Package Types (not to scale)

SOIC/TSSOP/PDIP



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (†)

VCC.....6.5V

All inputs and outputs w.r.t. VSS ..... -0.3V to VCC +0.3V

Storage temperature .....-65°C to +150°C

Ambient temperature under bias .....-40°C to +85°C

† NOTICE**:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for an extended period of time may affect device reliability.

TABLE 1-1: DC CHARACTERISTICS

DC CHARACTERISTICS			Industrial (I): TA = -40°C to +85°C				
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Typ.(1)**	**Max.**	**Units**	**Test Conditions**
D001	VCC	Supply voltage	2.5	—	5.5	V	23LCV512
D002	VIH	High-level input voltage	0.7 x VCC	—	VCC + 0.3	V	
D003	VIL	Low-level input voltage	-0.3	—	0.10 x VCC	V	23LCV512
D004	VOL	Low-level output voltage	—	—	0.2	V	IOL = 1 mA
D005	VOH	High-level output voltage	VCC - 0.5	—	—	V	IOH = -400 µA
D006	ILI	Input leakage current	—	—	±1	µA	$\overline{CS}$ = VCC, VIN = VSS OR VCC
D007	ILO	Output leakage current	—	—	±1	µA	$\overline{CS}$ = VCC, VOUT = VSS OR VCC
D008	ICC Read	Operating current	—	3	10	mA	FCLK = 20 MHz; SO = O, 5.5V
D009	ICCS	Standby current	—	4	10	µA	$\overline{CS}$ = VCC = 5.5V, Inputs tied to VCC or VSS
D010	CINT	Input capacitance	—	—	7	pF	VCC = 0V, f = 1 MHz, TA = 25°C **(Note 1)**
D011	VDR	RAM data retention voltage	—	1.0	—	V	**(Note 2)**
D012	VTRIP	VBAT Change Over	1.6	1.8	2.0	V	Typical at TA = 25°C **(Note 1)**
D013	VBAT	VBAT Voltage Range	1.4	—	3.6	V	**(Note 1)**
D014	IBAT	VBAT Current	—	1	—	µA	Typical at 2.5V, TA = 25°C **(Note 1)**

Note 1: This parameter is periodically sampled and not 100% tested. Typical measurements taken at room temperature (25°C).

2: This is the limit to which VDD can be lowered without losing RAM data. This parameter is periodically sampled and not 100% tested.

TABLE 1-2: AC CHARACTERISTICS

AC CHARACTERISTICS			Industrial (I): T_A = -40°C to +85°C			
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Max.**	**Units**	**Test Conditions**
1	FCLK	Clock frequency	—	20	MHz	
2	TCSS	$\overline{CS}$ setup time	25	—	ns	
3	TCSH	$\overline{CS}$ hold time	50	—	ns	
4	TCSD	$\overline{CS}$ disable time	25	—	ns	
5	Tsu	Data setup time	10	—	ns	
6	THD	Data hold time	10	—	ns	
7	TR	CLK rise time	—	20	ns	**Note 1**
8	TF	CLK fall time	—	20	ns	**Note 1**
9	THI	Clock high time	25	—	ns	
10	TLO	Clock low time	25	—	ns	
11	TCLD	Clock delay time	25	—	ns	
12	TV	Output valid from clock low	—	25	ns	
13	THO	Output hold time	0	—	ns	**Note 1**
14	TDIS	Output disable time	—	20	ns	

Note 1: This parameter is periodically sampled and not 100% tested.

TABLE 1-3: AC TEST CONDITIONS

AC Waveform:	
Input pulse level	0.1 x VCC to 0.9 x VCC
Input rise/fall time	5 ns
Operating temperature	-40°C to +85°C
CL = 30 pF	—
Timing Measurement Reference Level:	
Input	0.5 x VCC
Output	0.5 x VCC

FIGURE 1-1: SERIAL INPUT TIMING (SPI MODE)

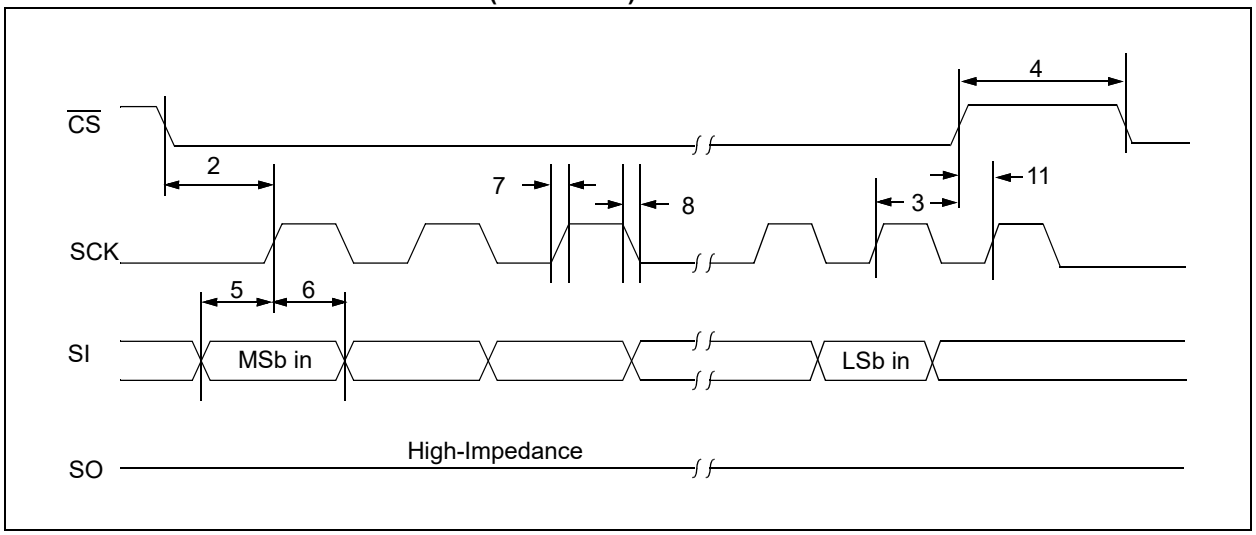
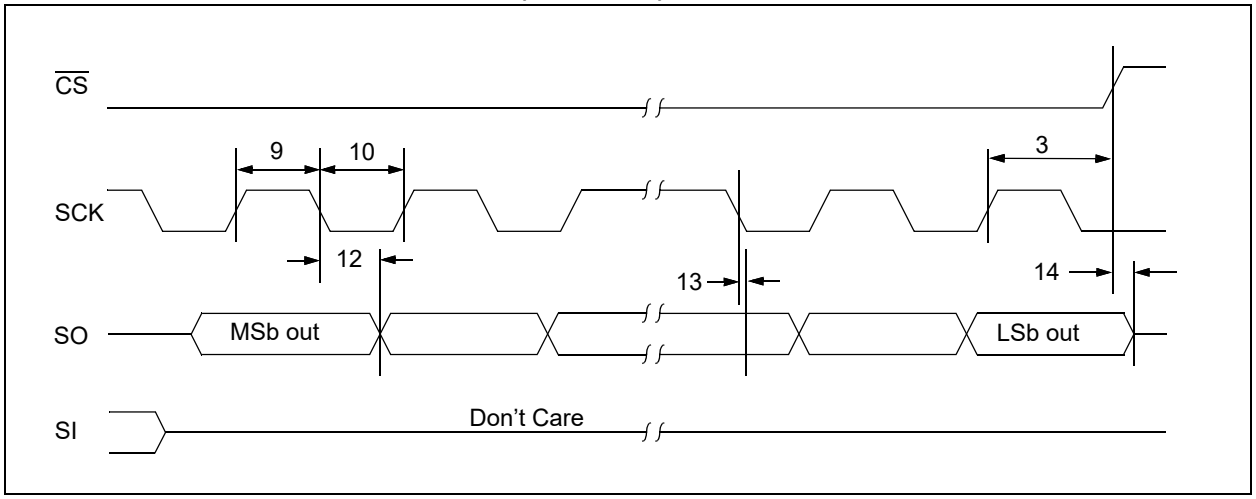


FIGURE 1-2: SERIAL OUTPUT TIMING (SPI MODE)



2.0 FUNCTIONAL DESCRIPTION

2.1 Principles of Operation

The 23LCV512 is a 512-Kbit Serial SRAM designed to interface directly with the Serial Peripheral Interface (SPI) port of many of today's popular microcontroller families, including Microchip's PIC® microcontrollers. It may also interface with microcontrollers that do not have a built-in SPI port by using discrete I/O lines programmed properly in firmware to match the SPI protocol. In addition, the 23LCV512 is capable of operating in SDI (or dual SPI) mode.

The 23LCV512 contains an 8-bit instruction register. The device is accessed via the SI pin, with data being clocked in on the rising edge of SCK. The $\overline{CS}$ pin must be low for the entire operation.

Table 2-1 contains a list of the possible instruction bytes and formats for device operation. All instructions, addresses and data are transferred MSb (Most Significant bit) first, LSb (Least Significant bit) last.

2.2 Modes of Operation

The 23LCV512 has three modes of operation that are selected by setting bits 7 and 6 in the MODE register. The modes of operation are Byte, Page and Sequential.

Byte Operation – is selected when bits 7 and 6 in the MODE register are set to `00`. In this mode, the read/write operations are limited to only one byte. The command followed by the 16-bit address is clocked into the device and the data to/from the device is transferred on the next eight clocks (Figure 2-1, Figure 2-2).

Page Operation – is selected when bits 7 and 6 in the MODE register are set to `10`. The 23LCV512 has 2048 pages of 32 bytes. In this mode, the read and write operations are limited to within the addressed page (the address is automatically incremented internally). If the data being read or written reaches the page boundary, the internal address counter will increment to the start of the page (Figure 2-3, Figure 2-4).

Sequential Operation – is selected when bits 7 and 6 in the MODE register are set to `01`. Sequential operation allows the entire array to be written to and read from. The internal address counter is automatically incremented and page boundaries are ignored. When the internal address counter reaches the end of the array, the address counter will roll over to `0x0000` (Figure 2-5, Figure 2-6).

2.3 Read Sequence

The device is selected by pulling $\overline{CS}$ low. The 8-bit `READ` instruction is transmitted to the 23LCV512 followed by the 16-bit address. After the correct `READ` instruction and address are sent, the data stored in the memory at the selected address is shifted out on the SO pin.

If operating in Sequential mode, the data stored in the memory at the next address can be read sequentially by continuing to provide clock pulses. The internal Address Pointer is automatically incremented to the next higher address after each byte of data is shifted out. When the highest address is reached (FFFFh), the address counter rolls over to address 0000h, allowing the read cycle to continue indefinitely. The read operation is terminated by raising the $\overline{CS}$ pin.

2.4 Write Sequence

Prior to any attempt to write data to the 23LCV512, the device must be selected by bringing $\overline{CS}$ low.

Once the device is selected, the Write command can be started by issuing a `WRITE` instruction, followed by the 16-bit address and then the data to be written. A write is terminated by bringing the $\overline{CS}$ high.

If operating in Page mode, after the initial data byte is shifted in, additional bytes can be shifted into the device. The Address Pointer is automatically incremented. This operation can continue for the entire page (32 bytes) before data will start to be overwritten.

If operating in Sequential mode, after the initial data byte is shifted in, additional bytes can be clocked into the device. The internal Address Pointer is automatically incremented. When the Address Pointer reaches the highest address (FFFFh), the address counter rolls over to (0000h). This allows the operation to continue indefinitely, however, previous data will be overwritten.

TABLE 2-1: INSTRUCTION SET

Instruction Name	Instruction Format	Hex Code	Description
READ	0000 0011	0x03	Read data from memory array beginning at selected address
WRITE	0000 0010	0x02	Write data to memory array beginning at selected address
EDIO	0011 1011	0x3B	Enter Dual I/O access
RSTIO	1111 1111	0xFF	Reset Dual I/O access
RDMR	0000 0101	0x05	Read Mode Register
WRMR	0000 0001	0x01	Write Mode Register

FIGURE 2-1: BYTE READ SEQUENCE (SPI MODE)

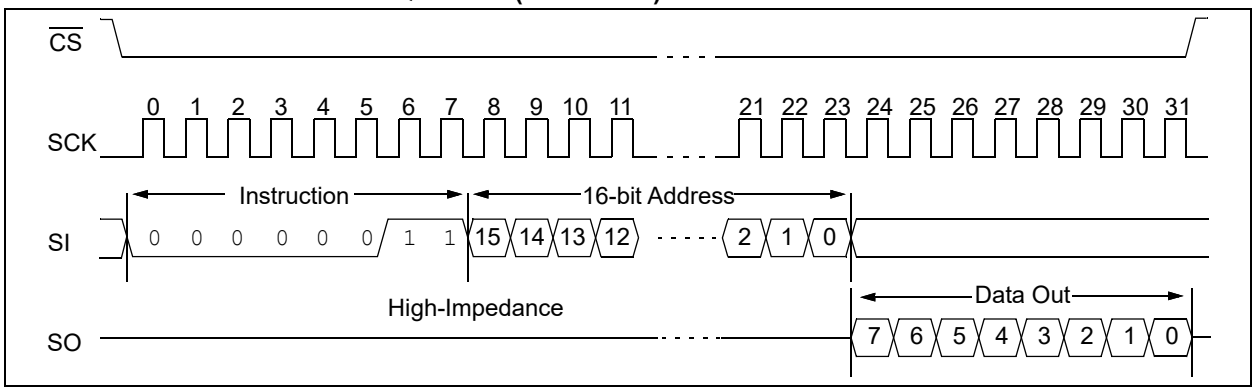


FIGURE 2-2: BYTE WRITE SEQUENCE (SPI MODE)

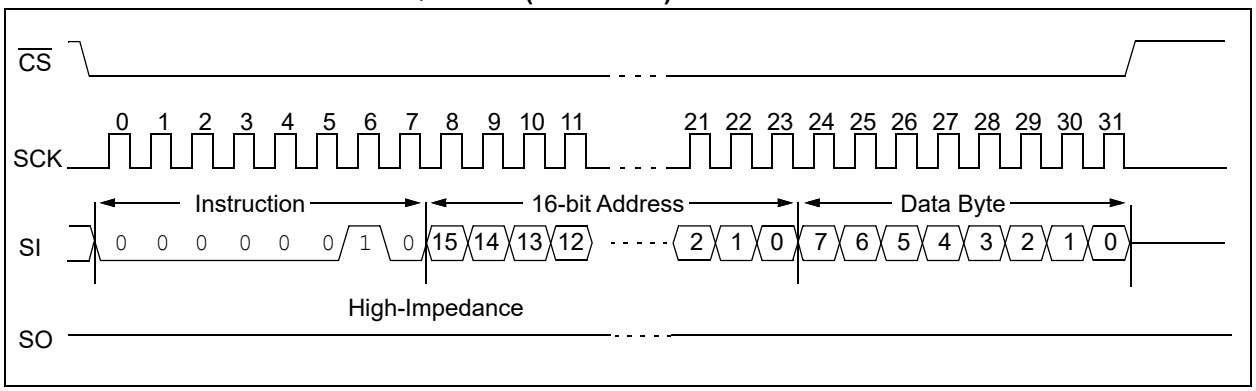


FIGURE 2-3: PAGE READ SEQUENCE (SPI MODE)

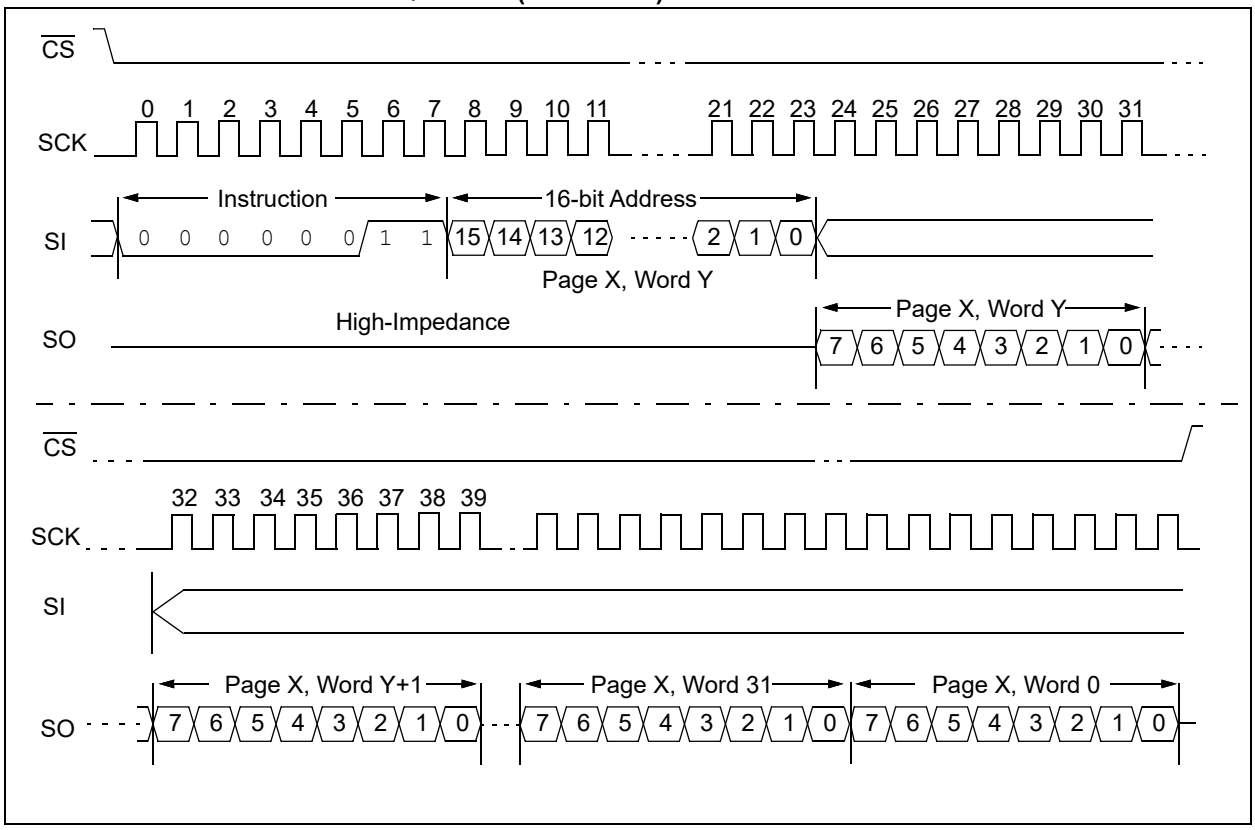


FIGURE 2-4: PAGE WRITE SEQUENCE (SPI MODE)

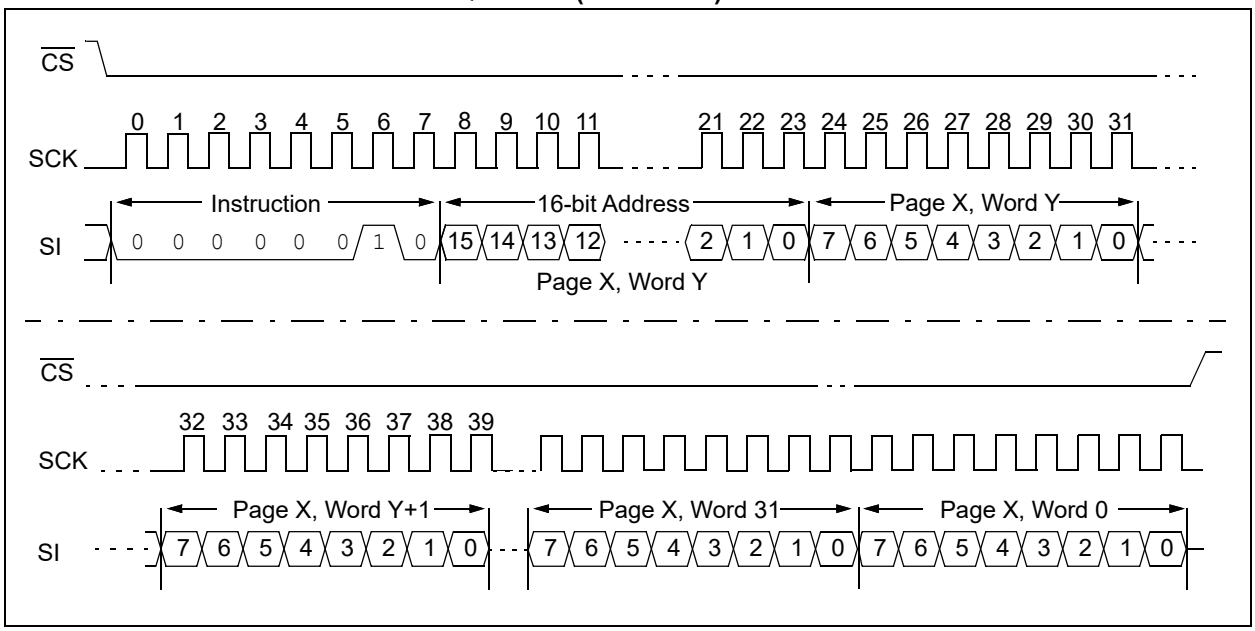


FIGURE 2-5: SEQUENTIAL READ SEQUENCE (SPI MODE)

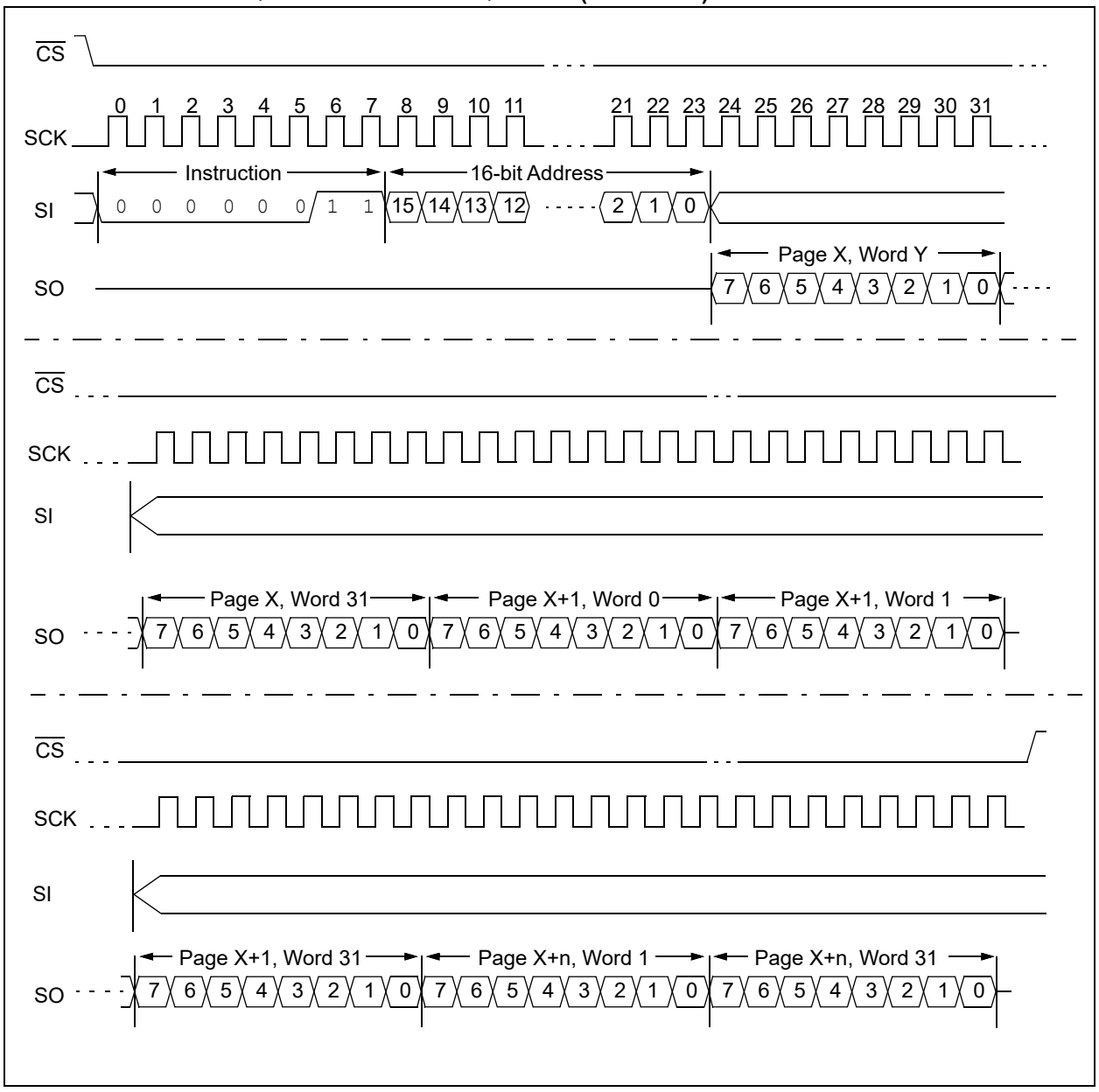
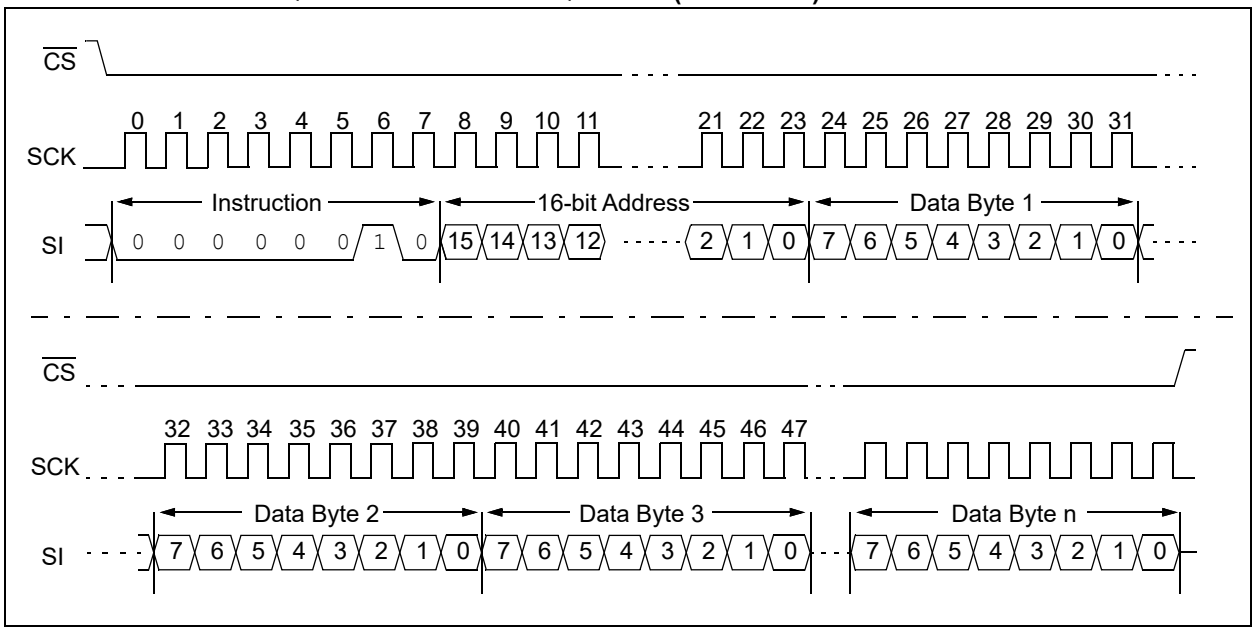


FIGURE 2-6: SEQUENTIAL WRITE SEQUENCE (SPI MODE)



2.5 Read Mode Register Instruction (RDMR)

The Read Mode Register instruction (RDMR) provides access to the MODE register. The MODE register may be read at any time. The MODE register is formatted as follows:

TABLE 2-2: MODE REGISTER

7	6	5	4	3	2	1	0
W/R	W/R	–	–	–	–	–	–
MODE	MODE	0	0	0	0	0	0
W/R = writable/readable							

The mode bits indicate the operating mode of the SRAM. The possible modes of operation are:

0 0 = Byte mode

1 0 = Page mode

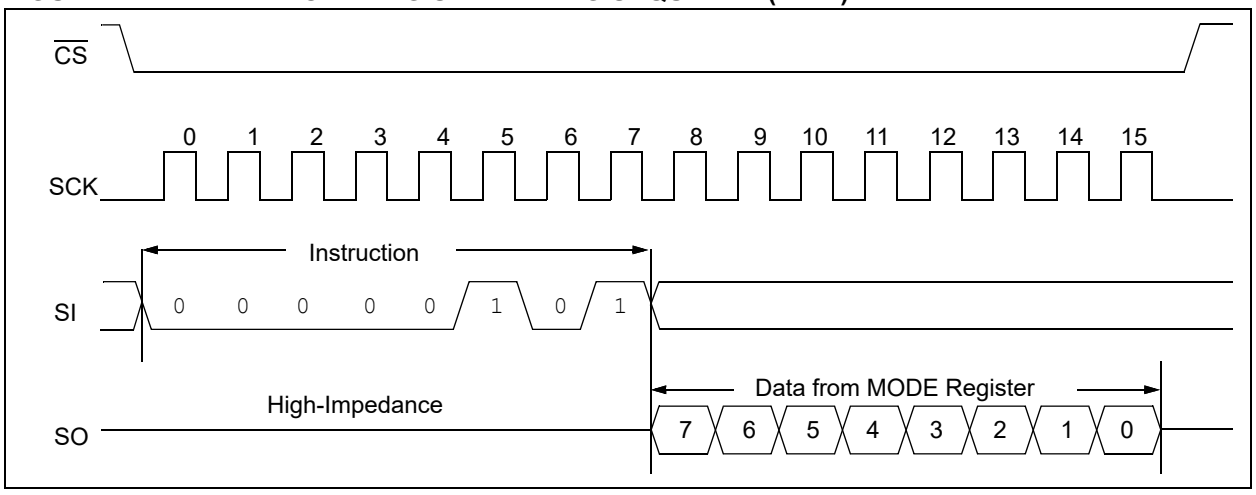
0 1 = Sequential mode (default operation)

1 1 = Reserved

Bits 0 through 5 are reserved and should always be set to '0'.

See Figure 2-7 for the RDMR timing sequence.

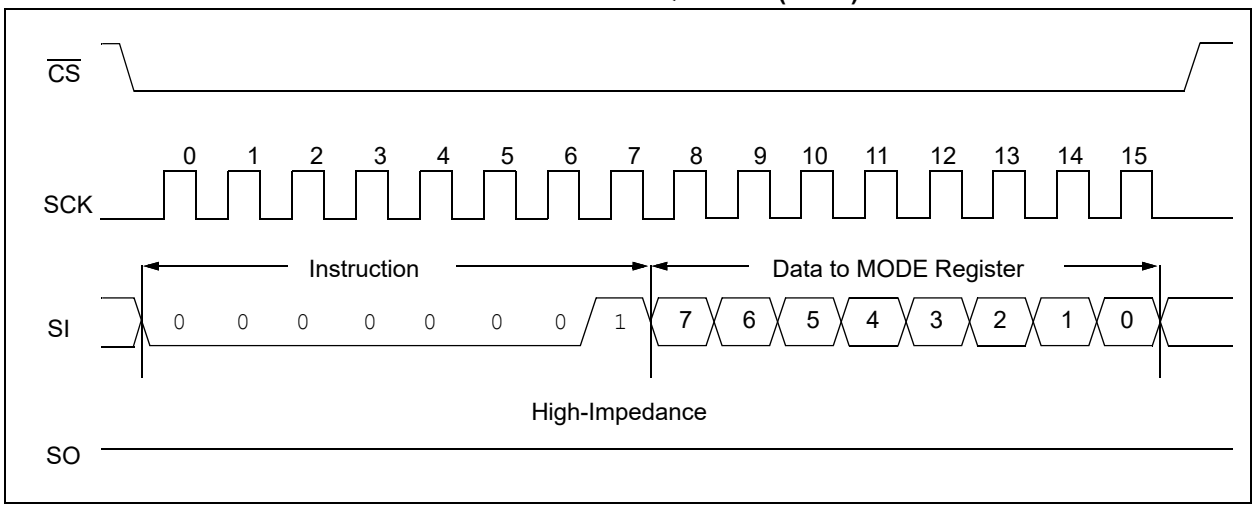
FIGURE 2-7: READ MODE REGISTER TIMING SEQUENCE (RDMR)



2.6 Write Mode Register Instruction (WRMR)

The Write Mode Register instruction (WRMR) allows the user to write to the bits in the MODE register as shown in Table 2-2. This allows for setting of the Device Operating mode. Several of the bits in the MODE register must be cleared to '0'. See Figure 2-8 for the WRMR timing sequence.

FIGURE 2-8: WRITE MODE REGISTER TIMING SEQUENCE (WRMR)



2.7 Power-On State

The 23LCV512 powers on in the following state:

- The device is in low-power Standby mode ($\overline{CS}$ = 1)
- A high-to-low-level transition on $\overline{CS}$ is required to enter active state

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Name	SOIC/ PDIP TSSOP	Function
$\overline{CS}$	1	Chip Select Input
SO/SIO1	2	Serial Data Output/SDI Pin
NC	3	No Connect
VSS	4	Ground
SI/SIO0	5	Serial Data Input/SDI Pin
SCK	6	Serial Clock Input
VBAT	7	External Backup Supply
VCC	8	Power Supply

3.1 Chip Select ($\overline{CS}$)

A low level on this pin selects the device. A high level deselects the device and forces it into Standby mode. When the device is deselected, SO goes to the high-impedance state, allowing multiple parts to share the same SPI bus. After power-up, a low level on $\overline{CS}$ is required prior to any sequence being initiated.

3.2 Serial Output (SO)

The SO pin is used to transfer data out of the 23LCV512. During a read cycle, data is shifted out on this pin after the falling edge of the serial clock.

3.3 Serial Input (SI)

The SI pin is used to transfer data into the device. It receives instructions, addresses and data. Data is latched on the rising edge of the serial clock.

3.4 Serial Dual Interface Pins (SIO0, SIO1)

The SIO0 and SIO1 pins are used for SDI mode of operation. Functionality of these I/O pins is shared with SO and SI.

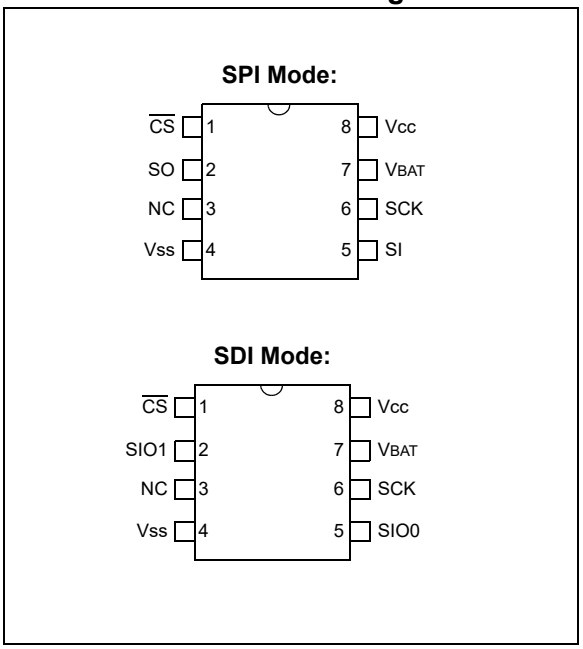
3.5 Serial Clock (SCK)

The SCK is used to synchronize the communication between a host and the 23LCV512. Instructions, addresses or data present on the SI pin are latched on the rising edge of the clock input, while data on the SO pin is updated after the falling edge of the clock input.

3.6 VBAT supply Input

The VBAT pin is used as an input for external backup supply to maintain SRAM data when VCC is below the VTRIP point. If the VBAT function is not being used, it is recommended to connect this pin to VSS.

3.7 SPI and SDI Pin Designations



4.0 DUAL SERIAL MODE

The 23LCV512 also supports SDI (Serial Dual) mode of operation when used with compatible host devices. As a convention for SDI mode of operation, two bits are entered per clock using the SIO0 and SIO1 pins. Bits are clocked MSb first.

4.1 Dual Interface Mode

The 23LCV512 supports SDI (Serial Dual) mode of operation. To enter SDI mode, the EDIO command must be clocked in (Figure 4-1). It should be noted that if the MCU resets before the SRAM, the user will need to determine the serial mode of operation of the SRAM and reset it accordingly. Byte read and write sequence in SDI mode is shown in Figure 4-2 and Figure 4-3.

FIGURE 4-1: ENTER SDI MODE (EDIO) FROM SPI MODE

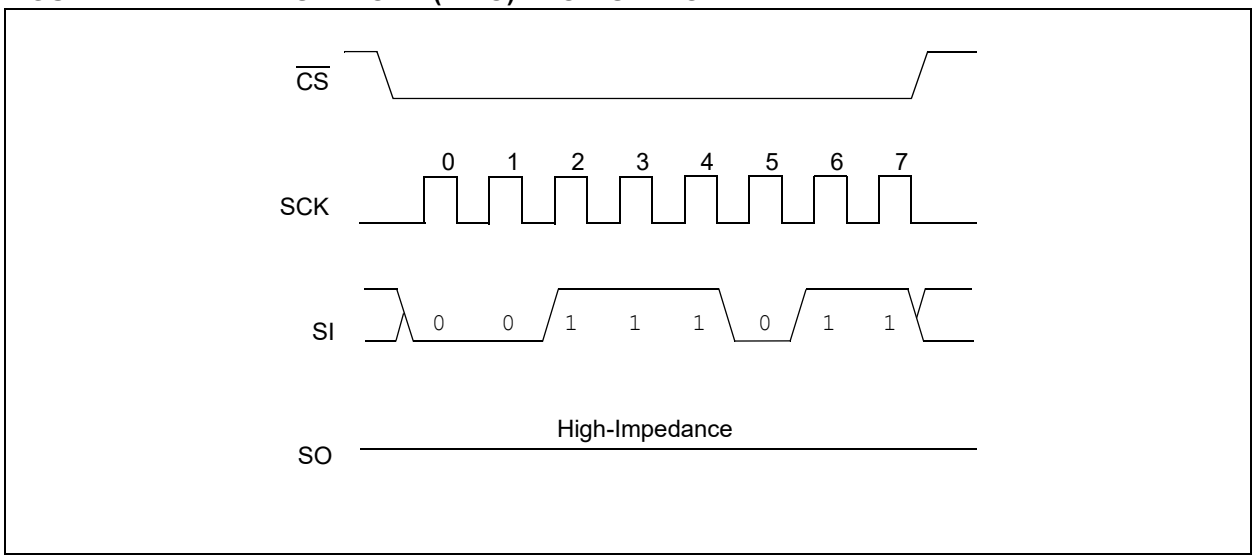
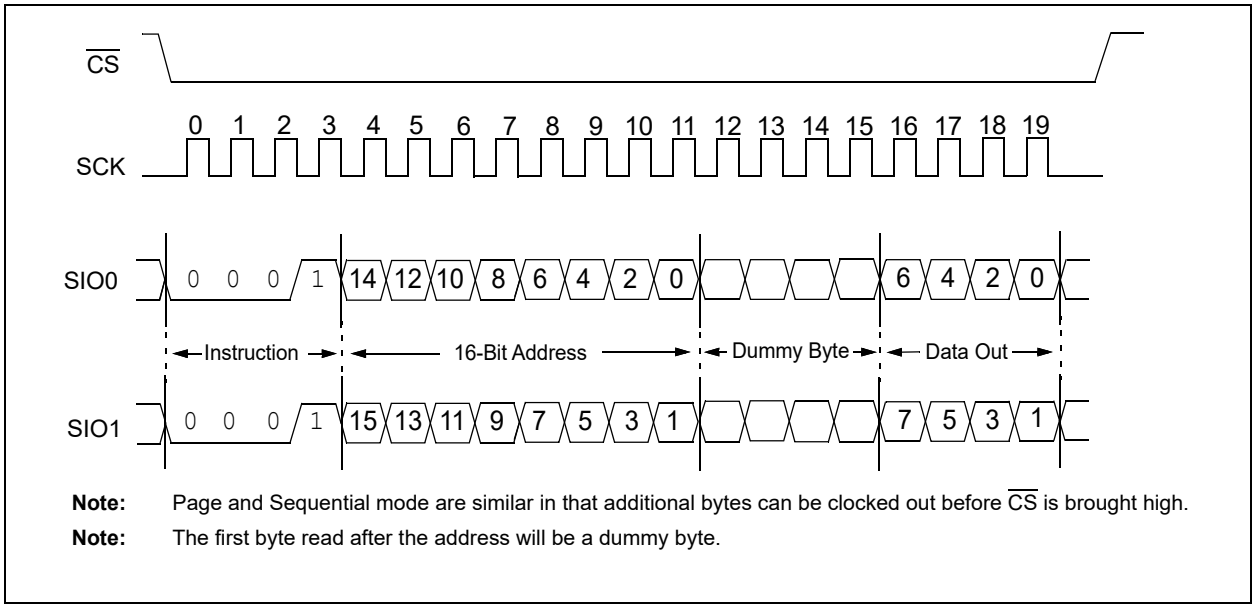


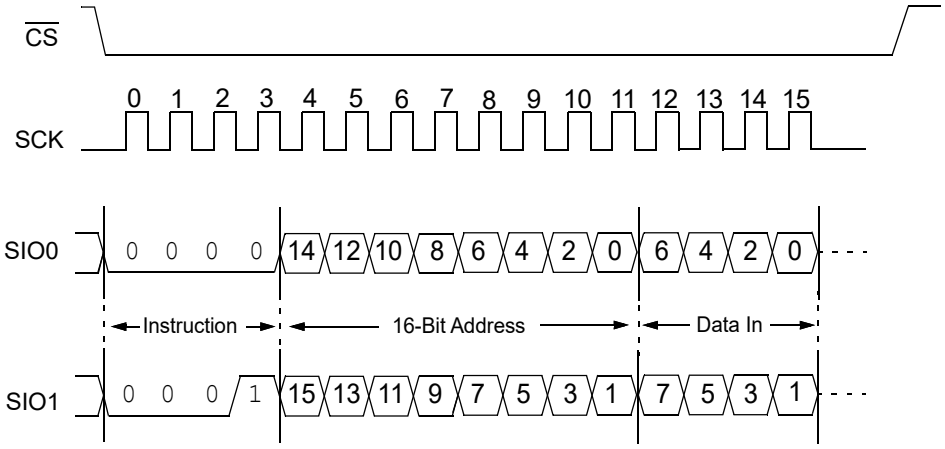
FIGURE 4-2: BYTE READ MODE SDI



Note: Page and Sequential mode are similar in that additional bytes can be clocked out before $\overline{CS}$ is brought high.

Note: The first byte read after the address will be a dummy byte.

FIGURE 4-3: BYTE WRITE MODE SDI

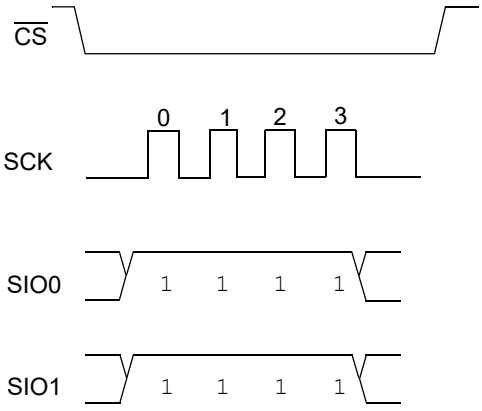


Note: Page and Sequential mode are similar in that additional bytes can be clocked in before $\overline{CS}$ is brought high.

4.2 Exit SDI Mode

To exit from SDI mode, the RSTIO command must be issued. The command must be entered in the current device configuration (see Figure 4-4).

FIGURE 4-4: RESET SDI MODE (RSTIO) – FROM SDI MODE



5.0 VBAT

The 23LCV512 features an internal switch that will maintain the SRAM contents. In the event that the VCC supply is not available, the voltage applied to the VBAT pin serves as the backup supply.

The VBAT trip point is the point at which the internal switch operates the device from the VBAT supply and is typically 1.8V (VTRIP specification D012). When VCC falls below the VTRIP point, the system will continue to maintain the SRAM contents.

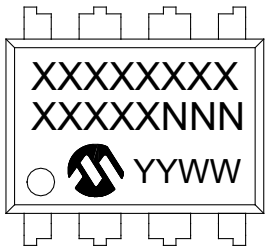
The following conditions apply:

Supply Condition	Read/Write Access	Powered By
VCC < VTRIP	No	VBAT
VCC > VTRIP	Yes	VCC

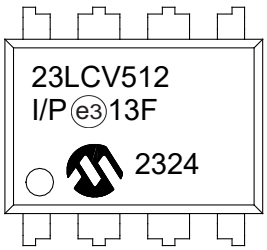
6.0 PACKAGING INFORMATION

6.1 Package Marking Information

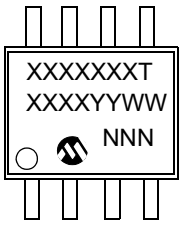
8-Lead PDIP (300 mil)



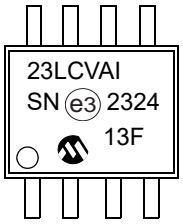
Example



8-Lead SOIC (3.90 mm)



Example:



8-Lead TSSOP

Example:

Part Number	First Line Marking Code		
	PDIP	SOIC	TSSOP
23LCV512	23LCV512	23LCVAI	3LVA

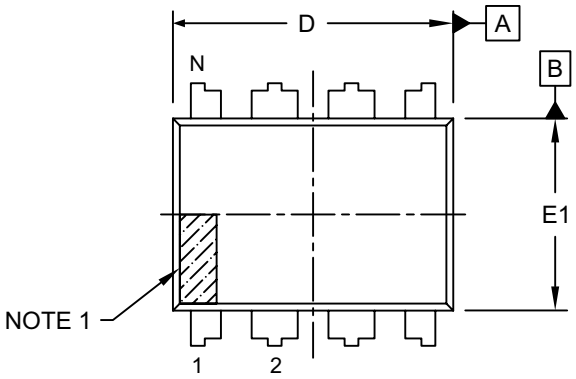
Legend:	XX...X	Part number or part number code
	T	Temperature (I, E)
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code (2 characters for small packages)
	(e3)	RoHS-compliant JEDEC designator for Matte Tin (Sn)

Note: For very small packages with no room for the RoHS-compliant JEDEC designator (e3), the marking will only appear on the outer carton or reel label.

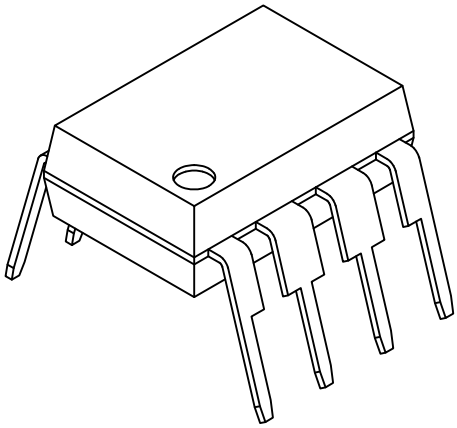
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

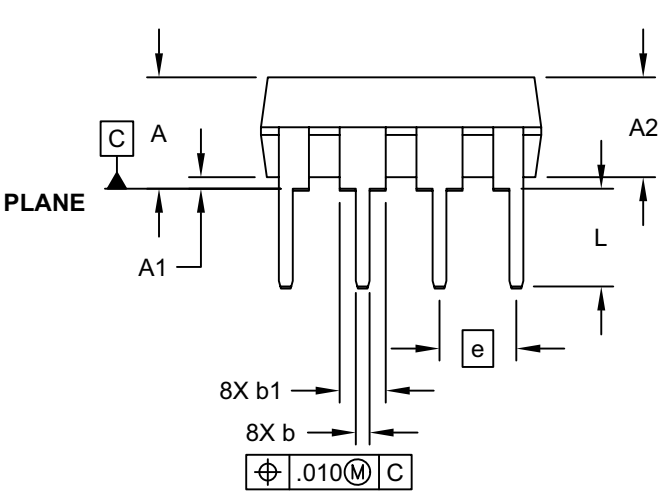
8-Lead Plastic Dual In-Line (P) - 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

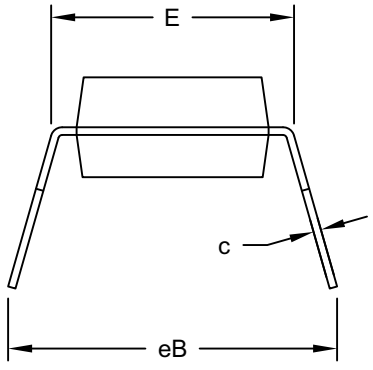


TOP VIEW





SIDE VIEW

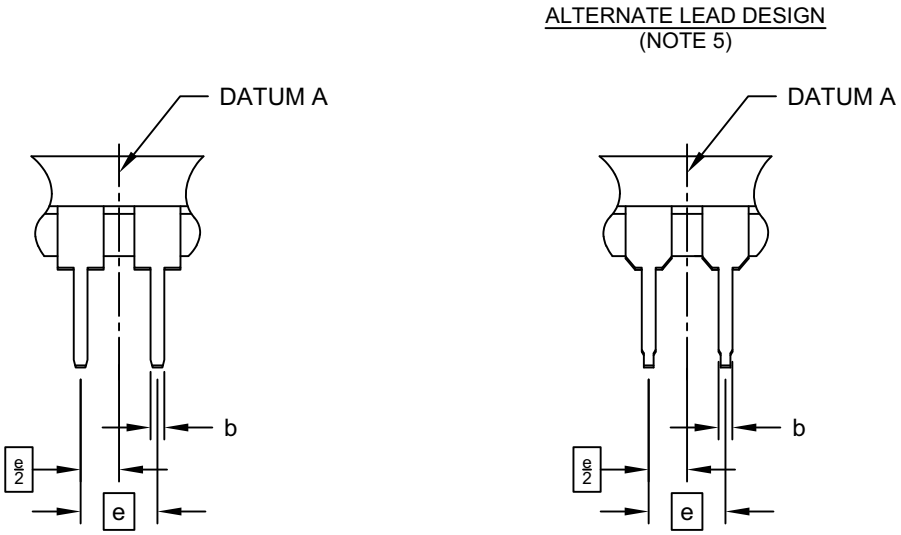


END VIEW

Microchip Technology Drawing No. C04-018-P Rev F Sheet 1 of 2

8-Lead Plastic Dual In-Line (P) - 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		.100 BSC	
Top to Seating Plane	A	-	-	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	-	-
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.348	.365	.400
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	-	-	.430

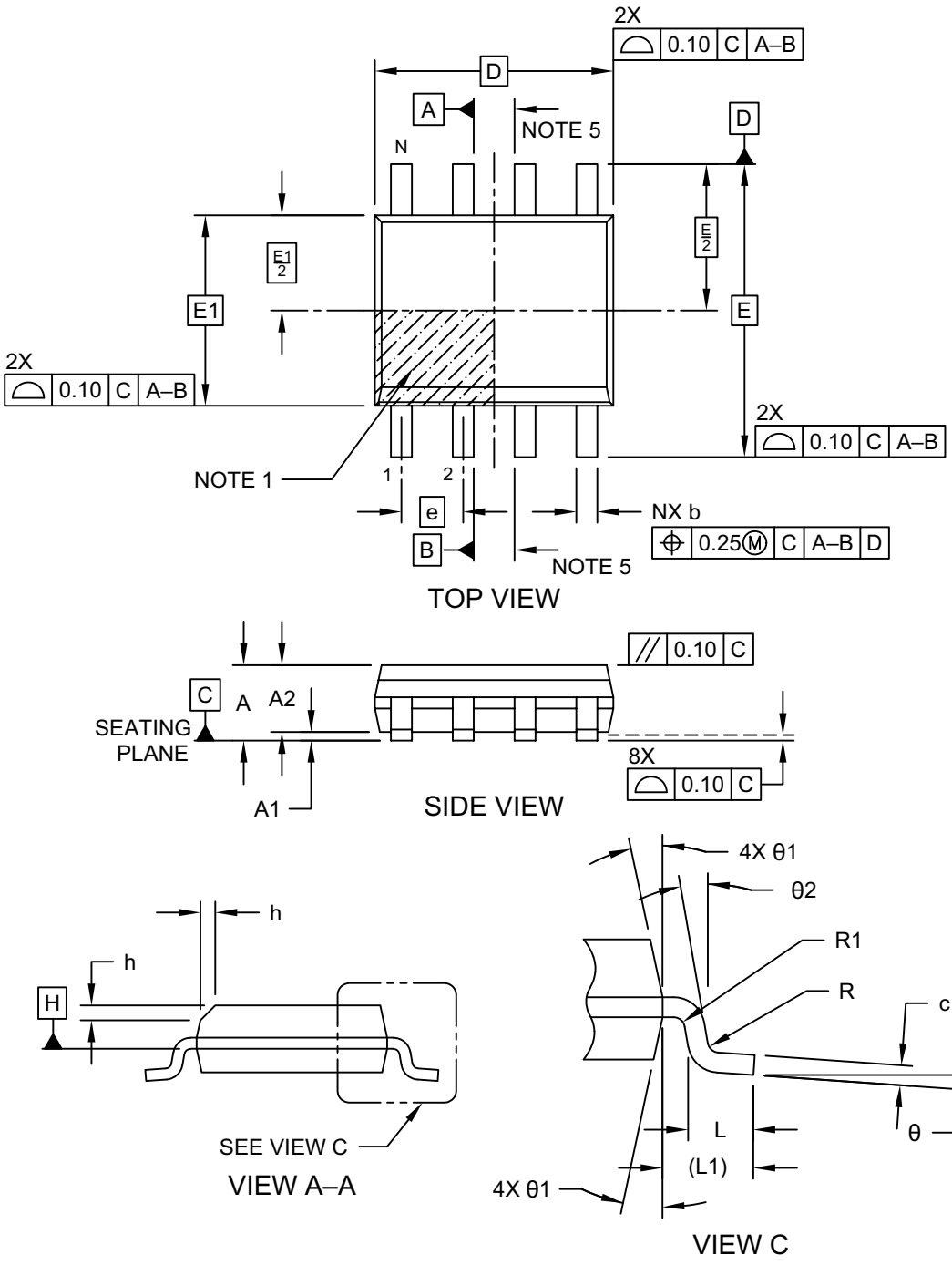
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
5. Lead design above seating plane may vary, based on assembly vendor.

Microchip Technology Drawing No. C04-018-P Rev F Sheet 2 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

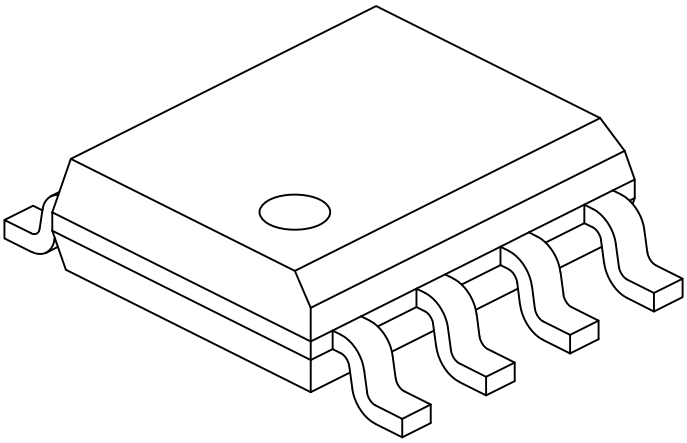
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing No. C04-057-SN Rev K Sheet 1 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	–	–	1.75
Molded Package Thickness	A2	1.25	–	-
Standoff §	A1	0.10	–	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Chamfer (Optional)	h	0.25	–	0.50
Foot Length	L	0.40	–	1.27
Footprint	L1		1.04 REF	
Lead Thickness	c	0.17	–	0.25
Lead Width	b	0.31	–	0.51
Lead Bend Radius	R	0.07	–	–
Lead Bend Radius	R1	0.07	–	–
Foot Angle	θ	0°	–	8°
Mold Draft Angle	θ1	5°	–	15°
Lead Angle	θ2	0°	–	–

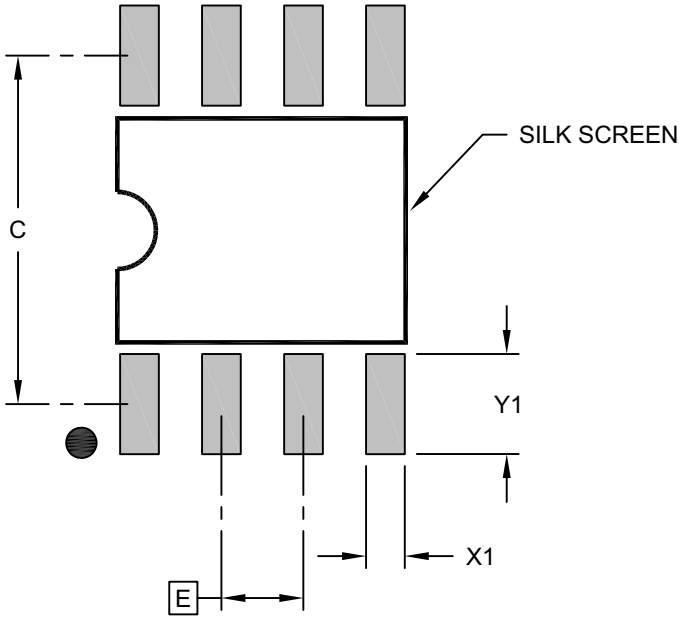
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-057-SN Rev K Sheet 2 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

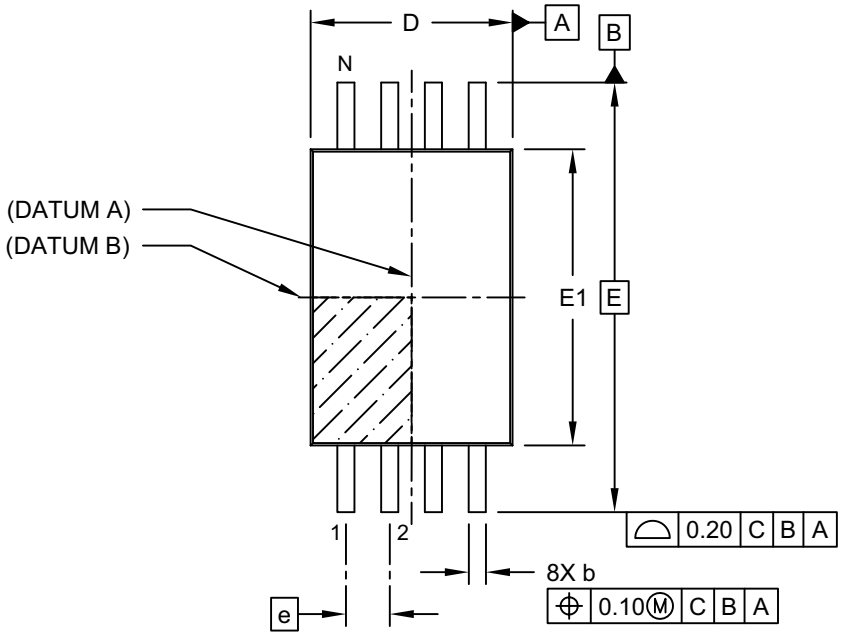
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

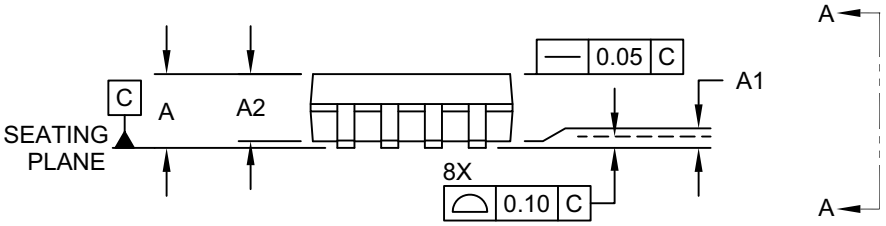
Microchip Technology Drawing C04-2057-SN Rev K

8-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

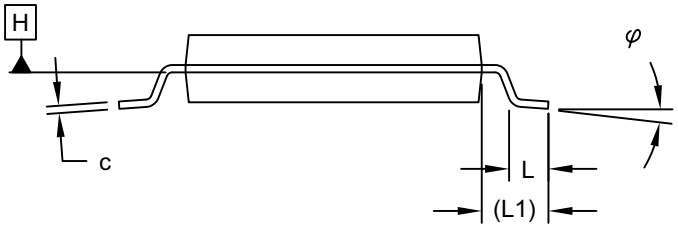
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW

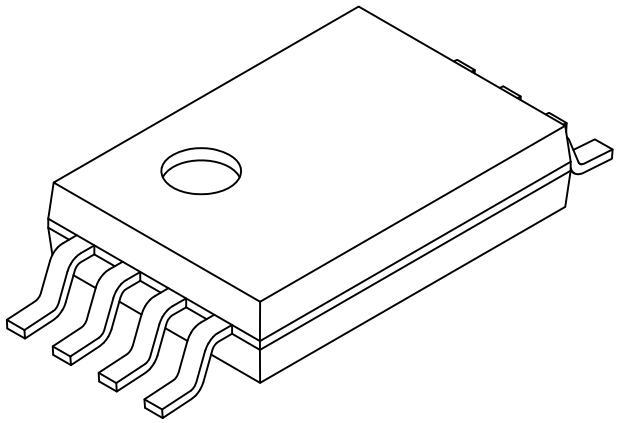


VIEW A-A

Microchip Technology Drawing C04-086 Rev C Sheet 1 of 2

8-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.65 BSC	
Overall Height	A	-	-	1.20
Molded Package Thickness	A2	0.80	1.00	1.05
Standoff	A1	0.05	-	-
Overall Width	E		6.40 BSC	
Molded Package Width	E1	4.30	4.40	4.50
Overall Length	D	2.90	3.00	3.10
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Lead Thickness	c	0.09	-	0.25
Foot Angle	φ	0°	4°	8°
Lead Width	b	0.19	-	0.30

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M

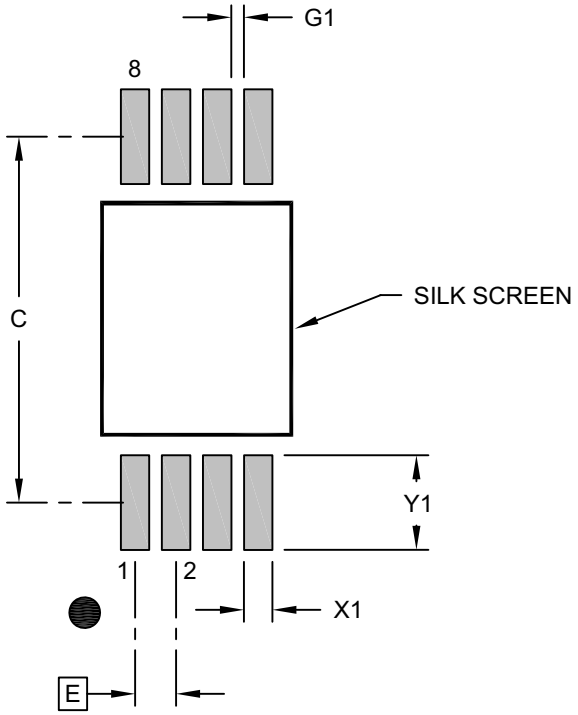
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-086 Rev C Sheet 2 of 2

8-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		5.80	
Contact Pad Width (X8)	X1			0.45
Contact Pad Length (X8)	Y1			1.50
Contact Pad to Center Pad (X6)	G1	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2086 Rev B

APPENDIX A: REVISION HISTORY

Revision C (08/2023)

Updated **Section 5.0 VBAT**.

Revision B (06/2021)

Replaced “Master” and “Slave” terminology with “Host” and “Client”, respectively. Removed “Preliminary” status. Updated PDIP, SOIC and TSSOP package drawings.

Revision A (09/2012)

Initial release.

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Device:	23LCV512 =		512 Kbit, 2.5V - 5.5V, SPI Serial SRAM, V_{BAT}
Tape and Reel Option:	Blank	=	Standard packaging (tube)
	T	=	Tape & Reel[1]
Temperature Range:	I	=	-40°C to +85°C
Package:	SN	=	Plastic SOIC (3.90 mm body), 8-lead
	ST	=	Plastic TSSOP (4.4 mm body), 8-lead
	P	=	Plastic PDIP (300 mil body), 8-lead

Examples:

a) 23LCV512-I/ST = 512 Kbit, 2.5V - 5.5V Serial SRAM, Industrial temp., TSSOP package

b) 23LCV512-I/SN = 512 Kbit, 2.5V - 5.5V Serial SRAM, Industrial temp., SOIC package

c) 23LCV512-I/P = 512 Kbit, 2.5V - 5.5V Serial SRAM, Industrial temp., PDIP package

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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