



Product Change Notification / SYST-04ZWJY480

Date:

07-Aug-2023

Product Category:

Memory

PCN Type:

Document Change

Notification Subject:

Data Sheet - AT28C64B - 64-Kbit (8K x 8) Industrial Parallel EEPROM with Page Write and Software Data Protection

Affected CPNs:

[SYST-04ZWJY480_Affected_CPN_08072023.pdf](#)
[SYST-04ZWJY480_Affected_CPN_08072023.csv](#)

Notification Text:

SYST-04ZWJY480

Microchip has released a new Datasheet for the AT28C64B - 64-Kbit (8K x 8) Industrial Parallel EEPROM with Page Write and Software Data Protection of devices. If you are using one of these devices please read the document located at [AT28C64B - 64-Kbit \(8K x 8\) Industrial Parallel EEPROM with Page Write and Software Data Protection](#)

Notification Status: Final

Description of Change: Removed 28-Lead TSOP package. Updated 32-Lead PLCC package drawing to latest revision (no change to form, fit or function).

Impacts to Data Sheet: None

Reason for change: To correct / revise datasheet.

Change Implementation Status: Complete

Date Document Changes Effective: 07 Aug 2023

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachments:

AT28C64B - 64-Kbit (8K x 8) Industrial Parallel EEPROM with Page Write and Software Data Protection

Please contact your local **Microchip sales office** with questions or concerns regarding this notification.

Terms and Conditions:

If you wish to receive Microchip PCNs via email please register for our PCN email service at our **PCN home page** select register then fill in the required fields. You will find instructions about registering for Microchips PCN email service in the **PCN FAQ** section.

If you wish to change your PCN profile, including opt out, please go to the **PCN home page** select login and sign into your myMicrochip account. Select a profile option from the left navigation bar and make the applicable selections.

Affected Catalog Part Numbers (CPN)

AT28C64B-W

AT28C64B-DWF

AT28C64B-15SU

AT28C64B-15TU

AT28C64B-15JU

AT28C64B-15PU

AT28C64B-15SU-T

AT28C64B-15TU-T

AT28C64B-15JU-235

AT28C64B-15JU-T

64-Kbit (8K x 8) Industrial Parallel EEPROM with Page Write and Software Data Protection

AT28C64B



Features

- Fast Read Access Time: 150 ns
- Automatic Page Write Operation:
 - Internal address and data latches for 64 bytes
- Fast Write Cycle Time:
 - Page Write cycle time: 2 ms or 10 ms maximum
 - 1 to 64-byte Page Write operation
- Low-Power Dissipation:
 - 40 mA active current
 - 100 μ A CMOS standby current
- Hardware and Software Data Protection
- $\overline{\text{DATA}}$ Polling and Toggle Bit for End of Write Detection
- High Reliability CMOS Technology:
 - Endurance: 100,000 cycles
 - Data retention: 10 years
- Single 5V \pm 10% Supply
- CMOS and TTL Compatible Inputs and Outputs
- JEDEC[®] Approved Byte-Wide Pinout
- Industrial Temperature Ranges
- Green (RoHS-compliant) Packaging Option Only

Packages

- 28-Lead PDIP, 32-Lead PLCC and 28-Lead SOIC

Table of Contents

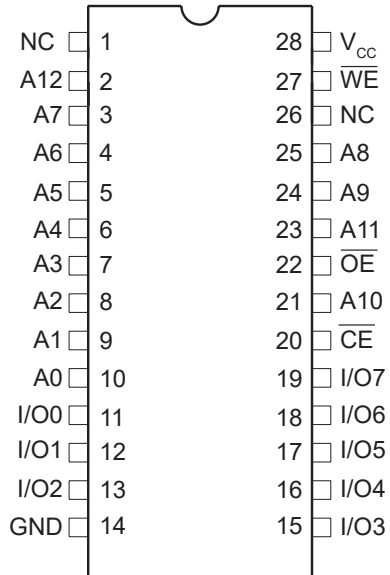
Features.....	1
Packages.....	1
1. Package Types (Not to Scale).....	4
2. Pin Descriptions.....	5
3. Description.....	6
3.1. Block Diagram.....	6
4. Electrical Characteristics.....	7
4.1. Absolute Maximum Ratings.....	7
4.2. DC and AC Operating Range.....	7
4.3. DC Characteristics.....	7
4.4. Pin Capacitance.....	7
5. Normalized I_{CC} Graphics.....	8
6. Device Operation.....	9
6.1. Read.....	9
6.2. Byte Write.....	9
6.3. Page Write.....	9
6.4. \overline{Data} Polling.....	9
6.5. Toggle Bit.....	9
6.6. Data Protection.....	9
6.7. Device Identification.....	10
6.8. Operating Modes.....	10
6.9. AC Read Characteristics.....	11
6.10. AC Read Waveforms ^(1,2,3,4)	11
6.11. Input Test Waveforms and Measurement Level.....	12
6.12. Output Test Load.....	12
6.13. AC Write Characteristics.....	12
6.14. AC Write Waveforms.....	13
6.15. Page Mode Characteristics.....	14
6.16. Page Mode Write Waveforms ^(1,2)	14
6.17. Chip Erase Waveforms.....	15
6.18. Software Data Protection Enable Algorithm ⁽¹⁾	16
6.19. Software Data Protection Disable Algorithm ⁽¹⁾	17
6.20. Software Protected Write Cycle Waveform ^(1,2)	18
6.21. \overline{Data} Polling Characteristics ⁽¹⁾	18
6.22. \overline{Data} Polling Waveforms.....	18
6.23. Toggle Bit Characteristics ⁽¹⁾	19
6.24. Toggle Bit Waveforms ^(1,2,3)	19
7. Packaging Information.....	20
7.1. Package Marking Information.....	20
8. Revision History.....	28

Microchip Information.....	29
The Microchip Website.....	29
Product Change Notification Service.....	29
Customer Support.....	29
Product Identification System.....	30
Microchip Devices Code Protection Feature.....	30
Legal Notice.....	31
Trademarks.....	31
Quality Management System.....	32
Worldwide Sales and Service.....	33

1. Package Types (Not to Scale)

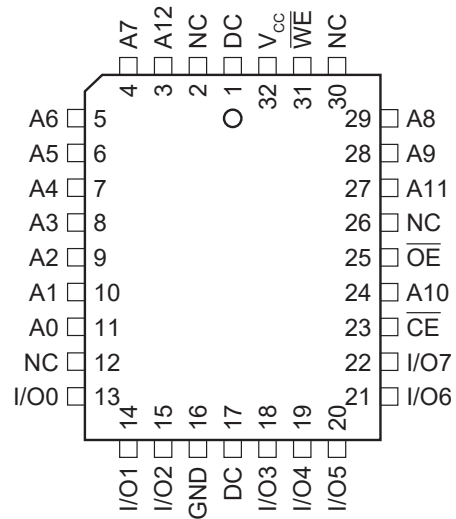
28-Lead PDIP/SOIC

Top View



32-Lead PLCC

Top View



2. Pin Descriptions

The descriptions of the pins are listed in [Table 2-1](#).

Table 2-1. Pin Function Table

Name	28-Lead PDIP	32-Lead PLCC	28-Lead SOIC	Function
DC	—	1	—	Don't Connect
NC	1	2	1	No Connect
A12	2	3	2	Address
A7	3	4	3	Address
A6	4	5	4	Address
A5	5	6	5	Address
A4	6	7	6	Address
A3	7	8	7	Address
A2	8	9	8	Address
A1	9	10	9	Address
A0	10	11	10	Address
NC	—	12	—	No Connect
I/O0	11	13	11	Data Input/Output
I/O1	12	14	12	Data Input/Output
I/O2	13	15	13	Data Input/Output
GND	14	16	14	Ground
DC	—	17	—	Don't Connect
I/O3	15	18	15	Data Input/Output
I/O4	16	19	16	Data Input/Output
I/O5	17	20	17	Data Input/Output
I/O6	18	21	18	Data Input/Output
I/O7	19	22	19	Data Input/Output
\overline{CE}	20	23	20	Chip Enable
A10	21	24	21	Address
\overline{OE}	22	25	22	Output Enable
NC	—	26	—	No Connect
A11	23	27	23	Address
A9	24	28	24	Address
A8	25	29	25	Address
NC	26	30	26	No Connect
\overline{WE}	27	31	27	Write Enable
V _{CC}	28	32	28	Device Power Supply

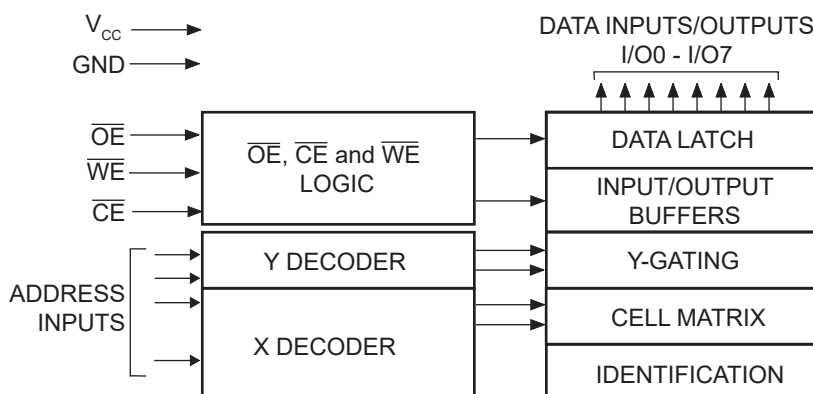
3. Description

The AT28C64B is a high-performance Electrically Erasable and Programmable Read-Only Memory (EEPROM). Its 64-Kbit memory is organized as 8,192 words by 8 bits. Manufactured with Microchip's advanced nonvolatile CMOS technology, the device offers access times to 150 ns with power dissipation of just 220 mW. When the device is deselected, the CMOS standby current is less than 100 μ A.

The AT28C64B is accessed like a Static RAM for the read or write cycle without the need for external components. The device contains a 64-byte page register to allow for writing up to 64 bytes simultaneously. During a write cycle, the addresses and one to 64 bytes of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a write cycle, the device will automatically write the latched data using an internal control timer. The end of a write cycle can be detected by $\overline{\text{DATA}}$ Polling of I/O7. Once the end of a write cycle is detected, a new access for a read or write can begin.

The AT28C64B has additional features to ensure high quality and manufacturability. An optional software data protection mechanism is available to guard against inadvertent writes. The device also includes an extra 64 bytes of EEPROM for device identification or tracking.

3.1 Block Diagram



4. Electrical Characteristics

4.1 Absolute Maximum Ratings

Temperature under bias	-55°C to +125°C
Storage temperature	-65°C to +150°C
All input voltages (including NC pins) with respect to ground	-0.6V to +6.25V
All output voltages with respect to ground	-0.6V to $V_{CC} + 0.6V$
Voltage on OE and A9 with respect to ground	-0.6V to +13.5V

Note: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

4.2 DC and AC Operating Range

Table 4-1. DC and AC Operating Range

		AT28C64B-15
Operating Temperature (Case)	Industrial	-40°C to +85°C
V_{CC} Power Supply		5V \pm 10%

4.3 DC Characteristics

Table 4-2. DC Characteristics

Parameter	Symbol	Minimum	Maximum	Units	Test Conditions
Input Load Current	I_{LI}	—	10	μA	$V_{IN} = 0V$ to $V_{CC} + 1V$
Output Leakage Current	I_{LO}	—	10	μA	$V_{IO} = 0V$ to V_{CC}
V_{CC} Standby Current CMOS	I_{SB}	—	100	μA	$\overline{CE} = V_{CC} - 0.3V$ to $V_{CC} + 1V$
V_{CC} Active Current	I_{CC}	—	40	mA	$f = 5\text{ MHz}$; $I_{OUT} = 0\text{ mA}$
Input Low Voltage	V_{IL}	—	0.8	V	
Input High Voltage	V_{IH}	2.0	—	V	
Output Low Voltage	V_{OL}	—	0.45	V	$I_{OL} = 1.6\text{ mA}$
Output High Voltage	V_{OH}	2.0	—	V	$I_{OH} = -100\text{ }\mu A$

4.4 Pin Capacitance

Table 4-3. Pin Capacitance^(1,2)

Symbol	Typical	Maximum	Units	Conditions
C_{IN}	4	6	pF	$V_{IN} = 0V$
C_{OUT}	8	12	pF	$V_{OUT} = 0V$

Notes:

1. This parameter is characterized but is not 100% tested in production.
2. $f = 1\text{ MHz}$, $T_A = 25^\circ C$

5. Normalized I_{CC} Graphics

Figure 5-1. Normalized Supply Current vs. Temperature

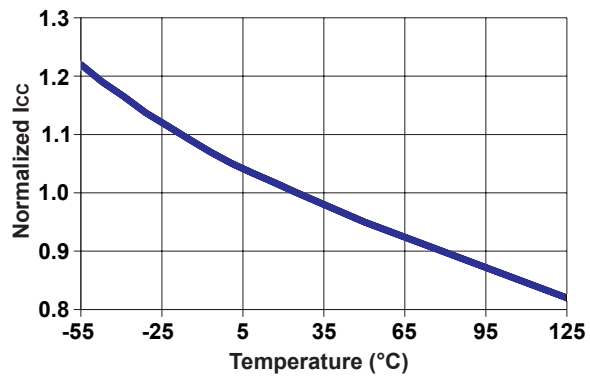


Figure 5-2. Normalized Supply Current vs. Address Frequency

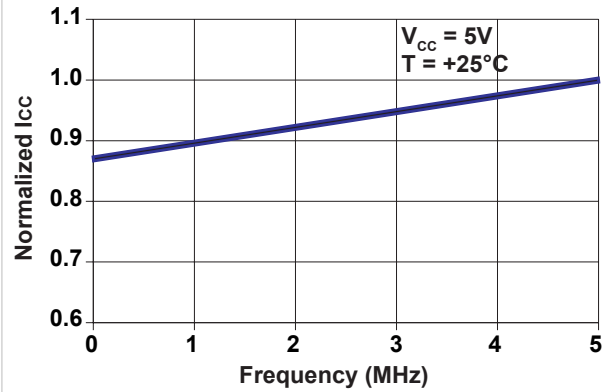
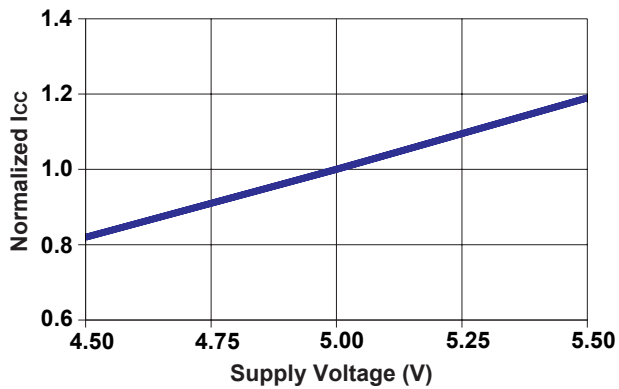


Figure 5-3. Normalized Supply Current vs. Supply Voltage



6. Device Operation

6.1 Read

The AT28C64B is accessed like a Static RAM. When \overline{CE} and \overline{OE} are low and \overline{WE} is high, the data stored at the memory location determined by the address pins are asserted on the outputs. The outputs are put in the high-impedance state when either \overline{CE} or \overline{OE} is high. This dual-line control gives designers flexibility in preventing bus contention in their system.

6.2 Byte Write

A low pulse on the \overline{WE} or \overline{CE} input with \overline{CE} or \overline{WE} low (respectively) and \overline{OE} high initiates a write cycle. The address is latched on the falling edge of \overline{CE} or \overline{WE} , whichever occurs last. The data is latched by the first rising edge of \overline{CE} or \overline{WE} . Once a byte write is started, it will automatically time itself to completion. Once a programming operation is initiated and for the duration of t_{WC} , a read operation will effectively be a polling operation.

6.3 Page Write

The page write operation of the AT28C64B allows one to 64 bytes of data to be written into the device during a single internal programming period. A page write operation is initiated in the same manner as a byte write; the first byte written can then be followed by one to 63 additional bytes. Each successive byte must be written within 150 μs (t_{BLC}) of the previous byte. If the t_{BLC} limit is exceeded, the AT28C64B will cease accepting data and commence the internal programming operation. All bytes during a page write operation must reside on the same page as defined by the state of the A6-A12 inputs. For each \overline{WE} high-to-low transition during the page write operation, A6-A12 must be the same. The A0 to A5 inputs are used to specify which bytes within the page are to be written. The bytes may be loaded in any order and may be altered within the same load period. Only bytes which are specified for writing will be written; unnecessary cycling of other bytes within the page does not occur.

6.4 Data Polling

The AT28C64B features \overline{DATA} Polling to indicate the end of a write cycle. During a byte or page write cycle, an attempted read of the last byte written will result in the complement of the written data to be presented on I/O7. Once the write cycle was completed, true data is valid on all outputs and the next write cycle may begin. \overline{DATA} Polling may begin at any time during the write cycle.

6.5 Toggle Bit

In addition to \overline{DATA} Polling, the AT28C64B provides another method for determining the end of a write cycle. During the write operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the write is completed, I/O6 will stop toggling and valid data will be read. Reading the toggle bit may begin at any time during the write cycle.

6.6 Data Protection

If precautions are not taken, inadvertent writes may occur during transitions of the host system power supply. Microchip incorporated both hardware and software features that will protect the memory against inadvertent writes.

6.6.1 Hardware Data Protection

Hardware features protect against inadvertent writes to the AT28C64B in the following ways:

- V_{CC} sense – if V_{CC} is below 3.8V (typical), the write function is inhibited
- V_{CC} power-on delay – once V_{CC} has reached 3.8V, the device will automatically time out 5 ms (typical) before allowing a write
- Write inhibit – holding any one of \overline{OE} low, \overline{CE} high or \overline{WE} high inhibits write cycles
- Noise filter – pulses of less than 15 ns (typical) on the \overline{WE} or \overline{CE} inputs will not initiate a write cycle

6.6.2 Software Data Protection

Software-controlled data protection is available on the AT28C64B and, when enabled, the Software Data Protection (SDP) feature will prevent inadvertent writes. SDP may be enabled or disabled by the user; the AT28C64B is shipped from Microchip with SDP disabled.

SDP is enabled when the user issues a series of three write commands in which three specific bytes of data are written to three specific addresses (see [Software Data Protection Enable Algorithm](#) and [Software Data Protection Disable Algorithm](#)). After writing the 3-byte command sequence and waiting t_{WC} , the entire AT28C64B will be protected against inadvertent writes.

It should be noted that even after SDP is enabled, the user may still perform a byte or page write to the AT28C64B by preceding the data to be written by the same 3-byte command sequence used to enable SDP. Once set, SDP remains active unless the disable command sequence is issued. Power transitions do not disable SDP and SDP protects the AT28C64B during power-up and power-down conditions. All command sequences must conform to the page write timing specifications. The data in the enable and disable command sequences are not actually written into the device; their addresses may still be written with user data in either a byte or page write operation. After setting SDP, any attempt to write to the device without the 3-byte command sequence will start the internal write timers. No data will be written to the device. However, for the duration of t_{WC} , read operations will effectively be polling operations.

6.7 Device Identification

An extra 64 bytes of EEPROM memory are available to the user for device identification. By raising A9 to $12V \pm 0.5V$ and using address locations 1FC0H to 1FFFH, the additional bytes may be written to or read from in the same manner as the regular memory array.

6.8 Operating Modes

Table 6-1. Operating Modes

Mode	\overline{CE}	\overline{OE}	\overline{WE}	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write ⁽¹⁾	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write Inhibit	V_{IH}	X ⁽²⁾	X	High-Z
Write Inhibit	X	X	V_{IH}	—
Write Inhibit	X	V_{IL}	X	—
Output Disable	X	V_{IH}	X	High-Z
Chip Erase	V_{IL}	V_H ⁽³⁾	V_{IL}	High-Z

Notes:

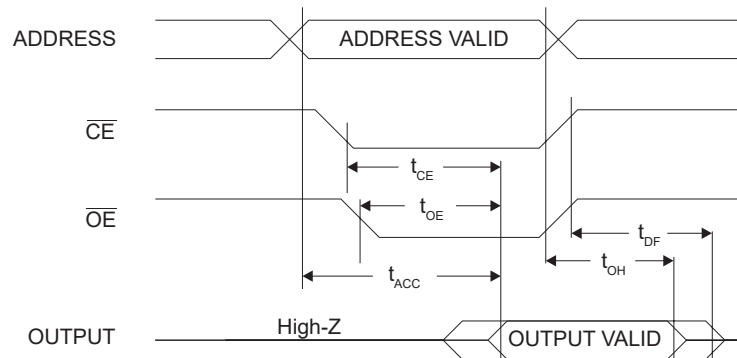
1. Refer to [AC Write Waveforms](#).
2. X can be V_{IL} or V_{IH} .
3. $V_H = 12.0V \pm 0.5V$

6.9 AC Read Characteristics

Table 6-2. AC Read Characteristics

Parameter	Symbol	AT28C64B-15		Units
		Min.	Max.	
Address to Output Delay	t_{ACC}	—	150	ns
\overline{CE} to Output Delay	$t_{CE}^{(1)}$	—	150	ns
\overline{OE} to Output Delay	$t_{OE}^{(2)}$	0	70	ns
\overline{CE} or \overline{OE} to Output Float	$t_{DF}^{(3,4)}$	0	50	ns
Output Hold from \overline{OE} , \overline{CE} or Address, whichever occurred first	t_{OH}	0	—	ns

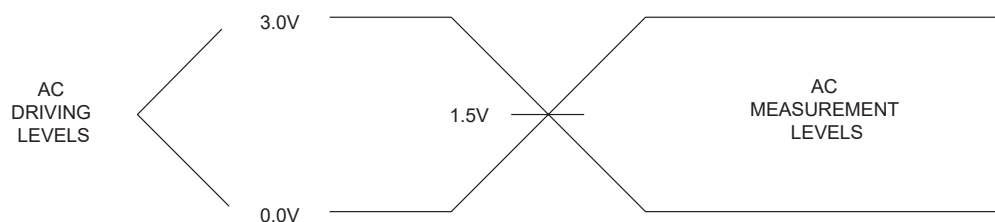
6.10 AC Read Waveforms^(1,2,3,4)



Notes:

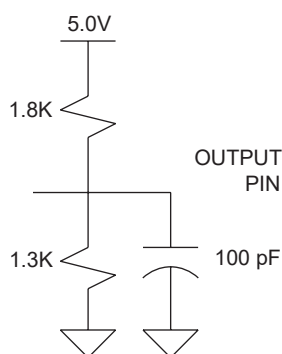
1. \overline{CE} may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC} .
2. \overline{OE} may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of \overline{CE} without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact in t_{ACC} .
3. t_{DF} is specified from \overline{OE} or \overline{CE} , whichever occurs first ($C_L = 5$ pF).
4. This parameter is characterized and is not 100% tested.

6.11 Input Test Waveforms and Measurement Level



Note: $t_R, t_F < 5$ ns.

6.12 Output Test Load



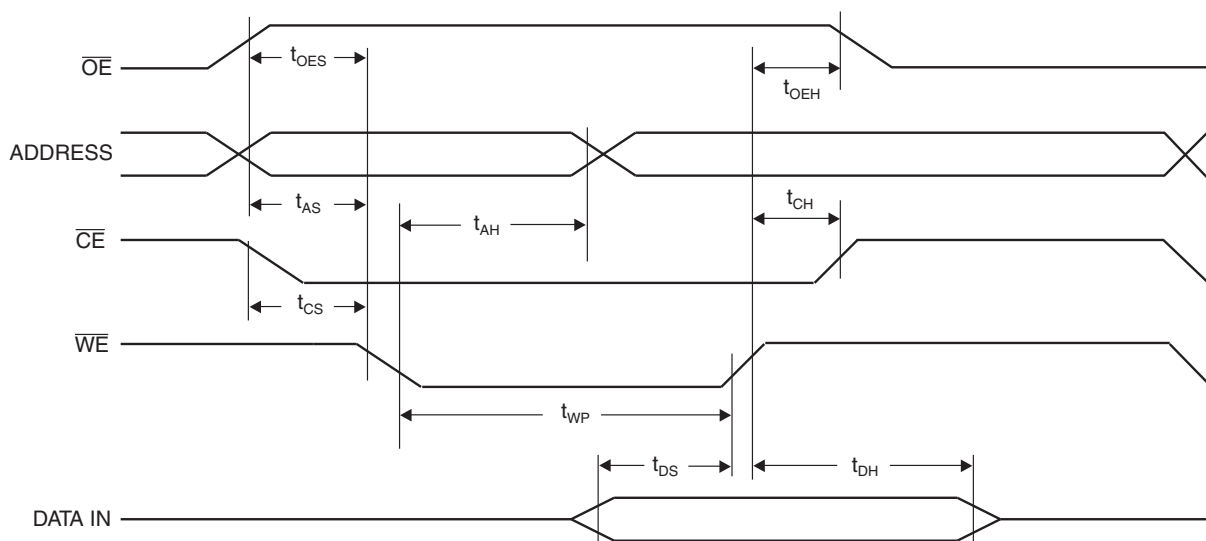
6.13 AC Write Characteristics

Table 6-3. AC Write Characteristics

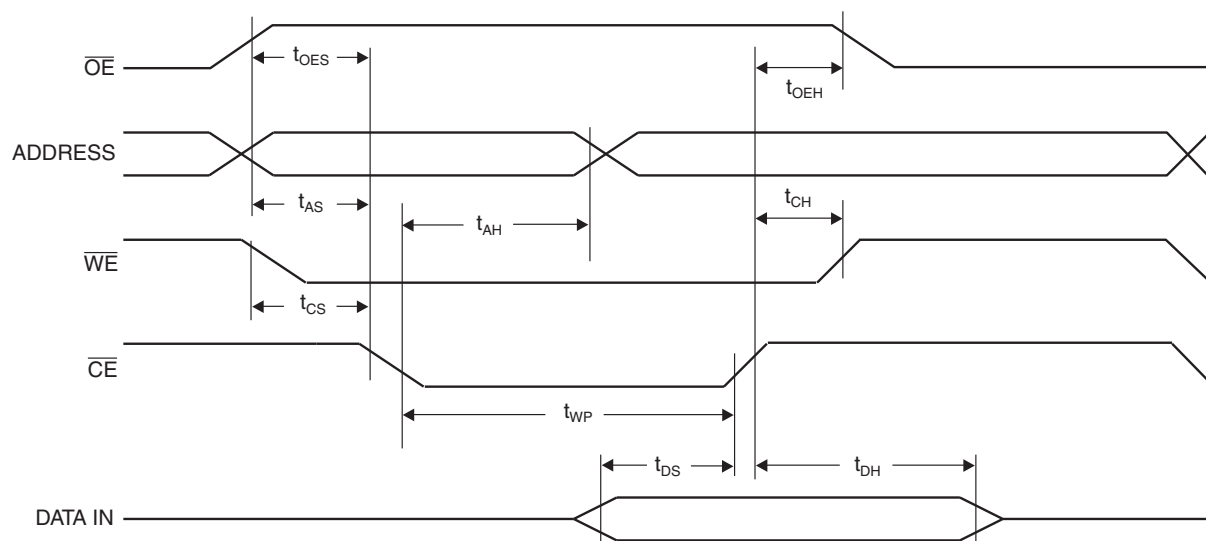
Parameter	Symbol	Minimum	Maximum	Units
Address, \overline{OE} Setup Time	t_{AS}, t_{OES}	0	—	ns
Address Hold Time	t_{AH}	50	—	ns
Chip Select Setup Time	t_{CS}	0	—	ns
Chip Select Hold Time	t_{CH}	0	—	ns
Write Pulse Width (\overline{WE} or \overline{CE})	t_{WP}	100	—	ns
Data Setup Time	t_{DS}	50	—	ns
Data, \overline{OE} Hold Time	t_{DH}, t_{OEH}	0	—	ns

6.14 AC Write Waveforms

6.14.1 $\overline{\text{WE}}$ Controlled



6.14.2 $\overline{\text{CE}}$ Controlled



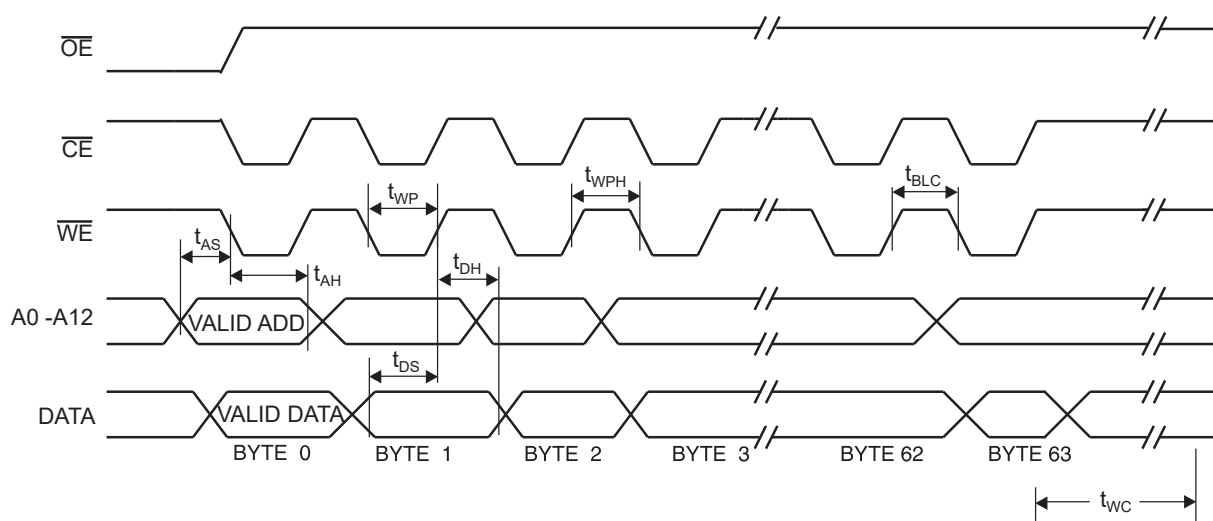
6.15 Page Mode Characteristics

Table 6-4. Page Mode Characteristics

Parameter		Symbol	Minimum	Maximum	Units
Write Cycle Time	AT28C64B	t_{WC}	—	10	ms
	AT28C64BF ⁽¹⁾		—	2	ms
Address Setup Time		t_{AS}	0	—	ns
Address Hold Time		t_{AH}	50	—	ns
Data Setup Time		t_{DS}	50	—	ns
Data Hold Time		t_{DH}	0	—	ns
Write Pulse Width		t_{WP}	100	—	ns
Byte Load Cycle Time		t_{BLC}	—	150	μ s
Write Pulse Width High		t_{WPH}	50	—	ns

Note: See AT28C64BF data sheet.

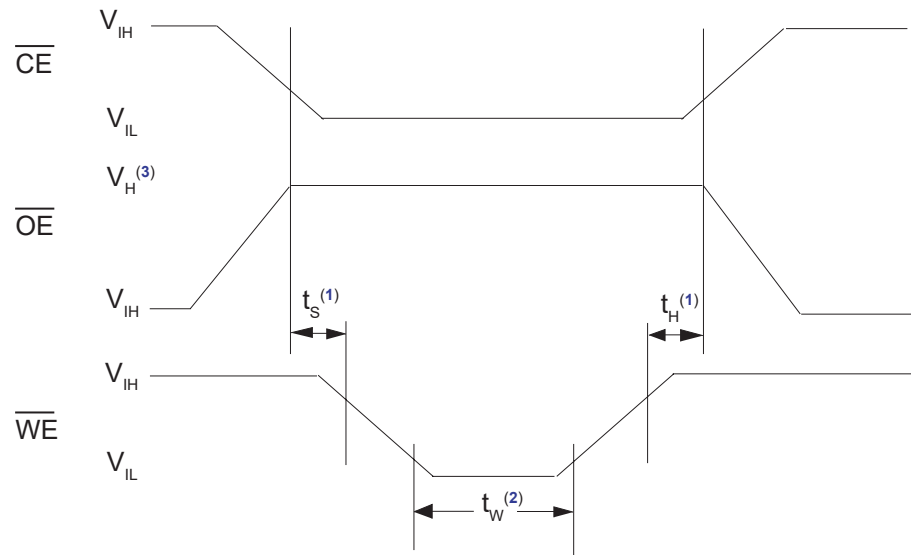
6.16 Page Mode Write Waveforms^(1,2)



Notes:

1. A6 through A12 must specify the same page address during each high-to-low transition of \overline{WE} (or \overline{CE}).
2. \overline{OE} must be high only when \overline{WE} and \overline{CE} are both low.

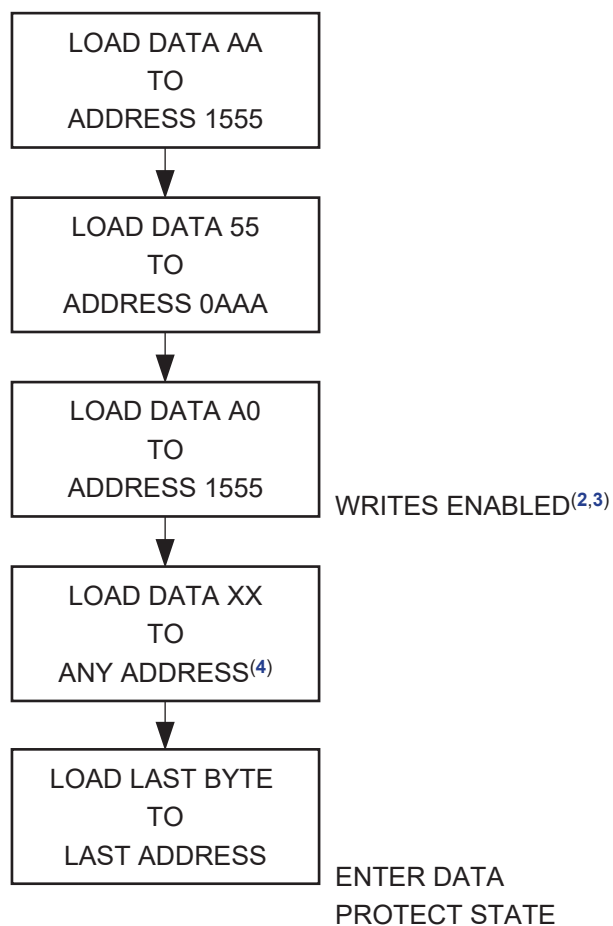
6.17 Chip Erase Waveforms



Notes:

1. $t_S = t_H = 1 \mu\text{sec}$ (minimum)
2. $t_W = 10 \text{ msec}$ (minimum)
3. $V_H = 12.0\text{V} \pm 0.5\text{V}$

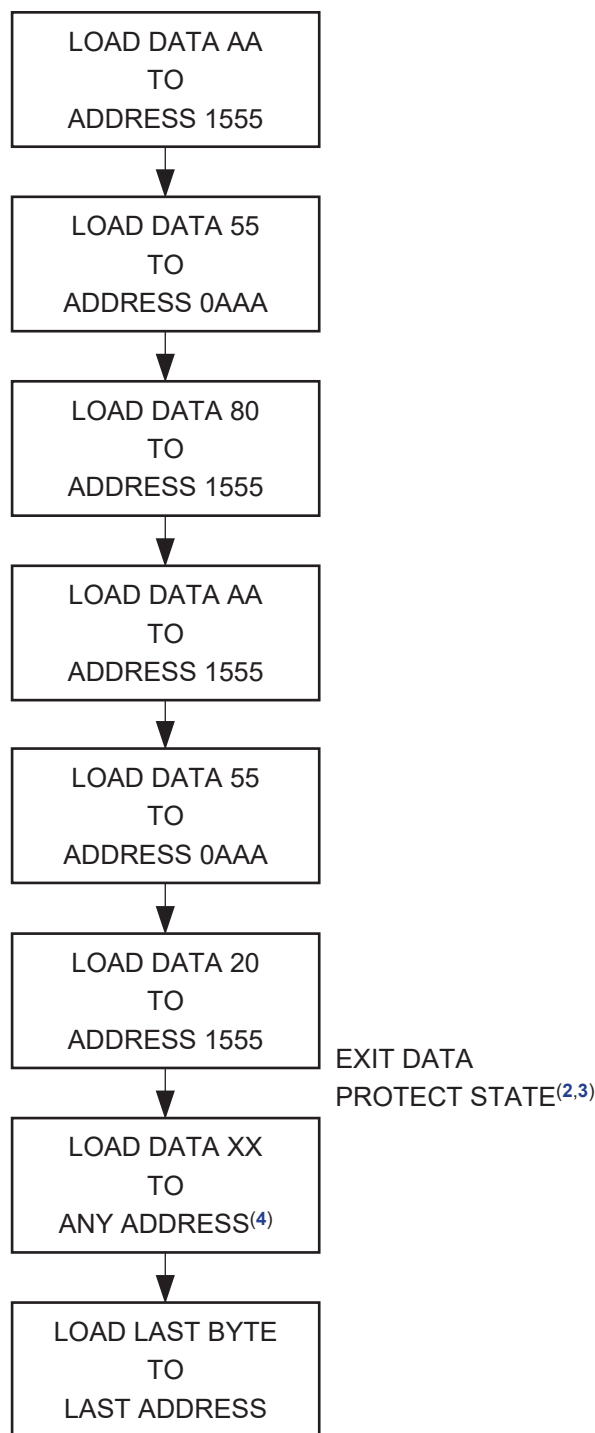
6.18 Software Data Protection Enable Algorithm⁽¹⁾



Notes:

1. Data format: I/O7-I/O0 (Hex); Address format: A12-A0 (Hex).
2. Write-Protect state will be activated at end of write even if no other data is loaded.
3. Write-Protect state will be deactivated at end of write period even if no other data is loaded.
4. One to 64 bytes of data are loaded.

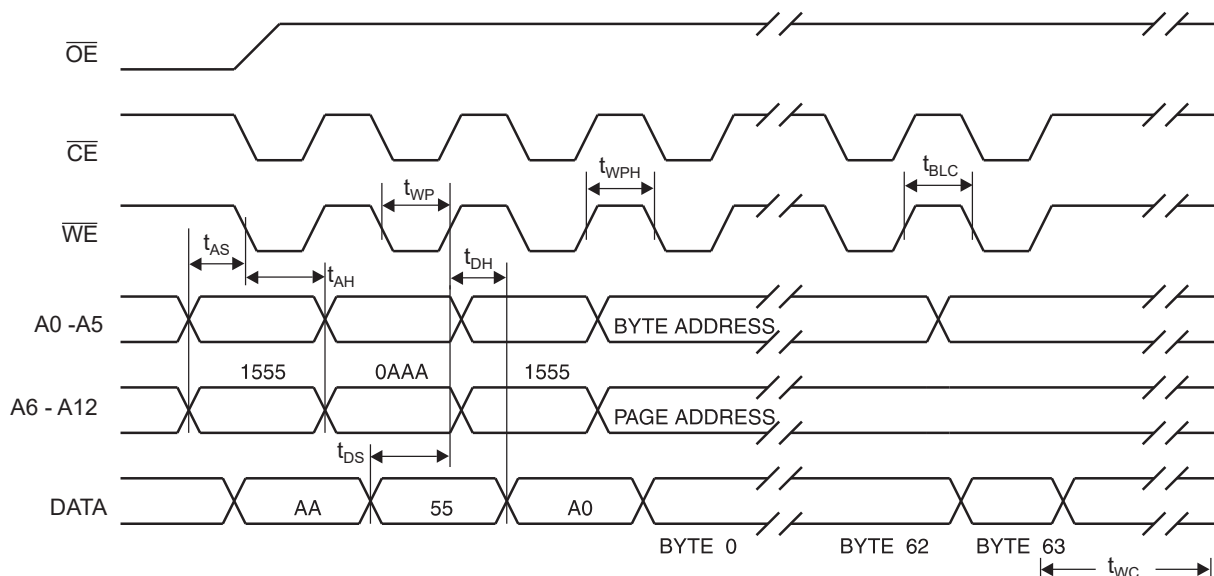
6.19 Software Data Protection Disable Algorithm⁽¹⁾



Notes:

1. Data format: I/O7-I/O0 (Hex); Address format: A12-A0 (Hex).
2. Write-Protect state will be activated at end of write period even if no other data is loaded.
3. Write-Protect state will be deactivated at end of write period even if no other data is loaded.
4. One to 64 bytes of data are loaded.

6.20 Software Protected Write Cycle Waveform^(1,2)



Notes:

1. A6 through A12 must specify the same page address during each high-to-low transition of \overline{WE} (or \overline{CE}) after the software code was entered.
2. \overline{OE} must be high only when \overline{WE} and \overline{CE} are both low.

6.21 Data Polling Characteristics⁽¹⁾

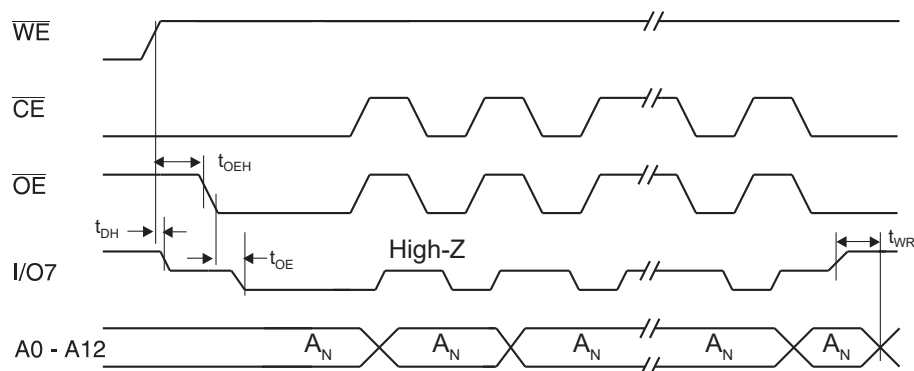
Table 6-5. Data Polling Characteristics

Parameter	Symbol	Minimum	Typical	Maximum	Units
Data Hold Time	t_{DH}	0	—	—	ns
\overline{OE} Hold Time	t_{OE}	0	—	—	ns
\overline{OE} to Output Delay ⁽²⁾	t_{OE}	—	—	—	ns
Write Recovery Time	t_{WR}	0	—	—	ns

Notes:

1. These parameters are characterized and not 100% tested.
2. See [AC Read Characteristics](#).

6.22 Data Polling Waveforms



6.23 Toggle Bit Characteristics⁽¹⁾

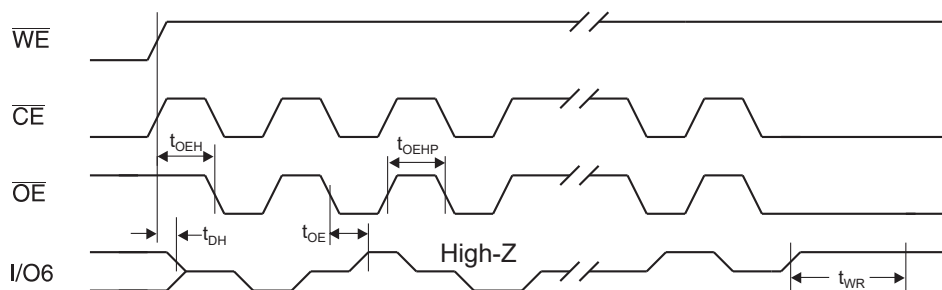
Table 6-6. Toggle Bit Characteristics

Parameter	Symbol	Minimum	Typical	Maximum	Units
Data Hold Time	t_{DH}	10	—	—	ns
\overline{OE} Hold Time	$t_{OE H}$	10	—	—	ns
\overline{OE} to Output Delay ⁽²⁾	t_{OE}	—	—	—	ns
\overline{OE} High Pulse	t_{OEHP}	150	—	—	ns
Write Recovery Time	t_{WR}	0	—	—	ns

Notes:

1. These parameters are characterized and not 100% tested.
2. See [AC Read Characteristics](#).

6.24 Toggle Bit Waveforms^(1,2,3)



Notes:

1. Toggling either \overline{OE} or \overline{CE} or both \overline{OE} and \overline{CE} will operate toggle bit.
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.

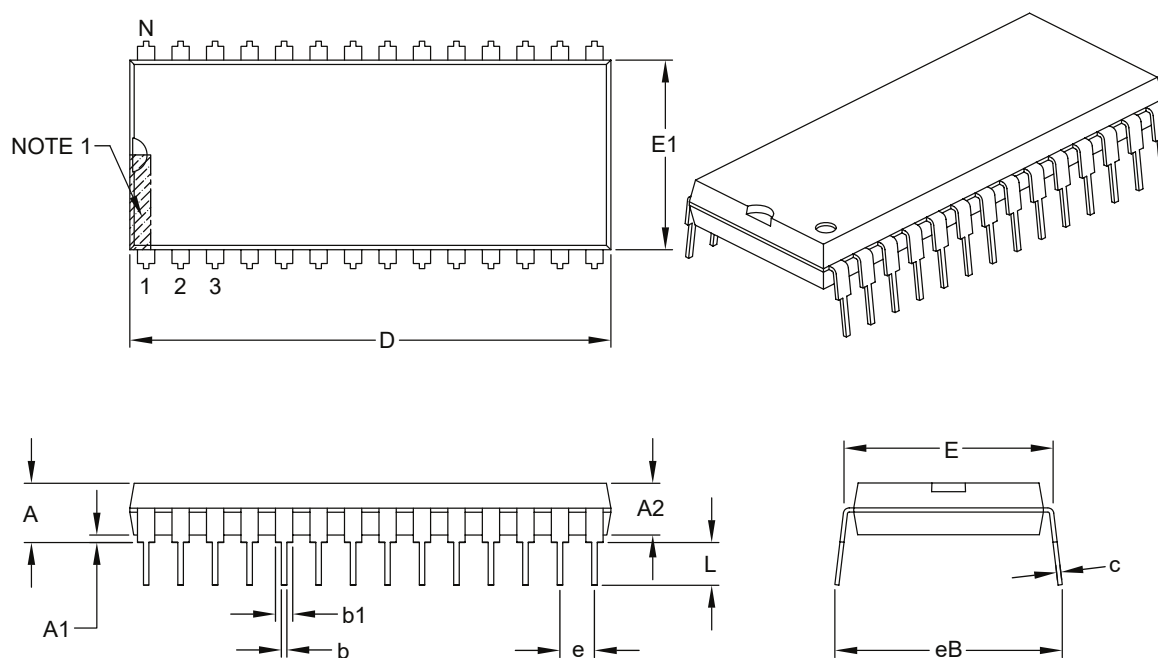
7. Packaging Information

7.1 Package Marking Information

AT28C64B: Package Marking Information			
28-Lead PDIP			
Topside		Backside	
<div>ATMEL AT28C64B %%U-19803A YYWWNNN</div>			
32-Lead PLCC		28-Lead SOIC	
Topside		Topside	
<div>ATMEL AT28C64B %%U-19803A YYWWNNN</div>		<div>ATMEL 19803A 28C64B-%%U YYWWNNN</div>	
Backside		Backside	
Note: no backside markings			
		%% = Access Time	
		15: 150 ns	
		Lot Trace Code	
		YYWWNNN: Lot Trace Code YY: Year, WW: Work Week NNN = Assembly Trace Code	

28-Lead Plastic Dual In-Line (P) – 600 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



		Units	INCHES		
Dimension Limits			MIN	NOM	MAX
Number of Pins	N		28		
Pitch	e		.100 BSC		
Top to Seating Plane	A		–	–	.250
Molded Package Thickness	A2		.125	–	.195
Base to Seating Plane	A1		.015	–	–
Shoulder to Shoulder Width	E		.590	–	.625
Molded Package Width	E1		.485	–	.580
Overall Length	D		1.380	–	1.565
Tip to Seating Plane	L		.115	–	.200
Lead Thickness	c		.008	–	.015
Upper Lead Width	b1		.030	–	.070
Lower Lead Width	b		.014	–	.022
Overall Row Spacing §	eB		–	–	.700

Notes:

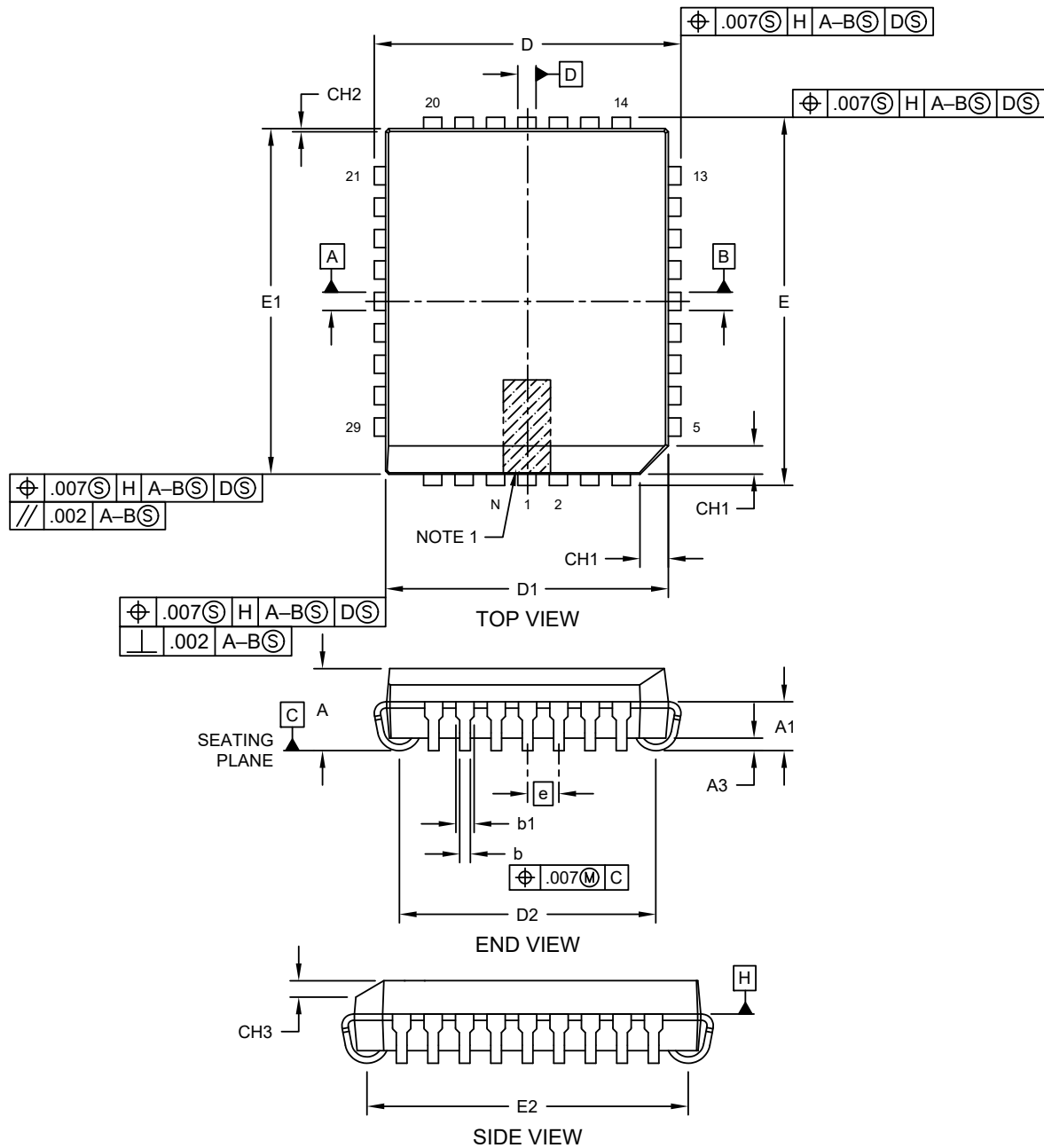
- Pin 1 visual index feature may vary, but must be located within the hatched area.
- § Significant Characteristic.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-079B

32-Lead Plastic Leaded Chip Carrier (L) - Rectangle [PLCC]

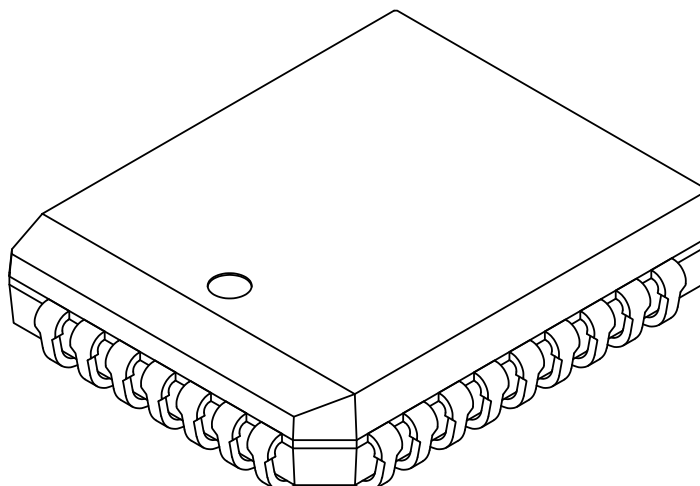
Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Microchip Technology Drawing C04-023 Rev C Sheet 1 of 2

32-Lead Plastic Leaded Chip Carrier (L) - Rectangle [PLCC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	32		
Pitch	e	.050 BSC		
Pins along Length	ND	7		
Pins along Width	NE	9		
Overall Height	A	.125	.132	.140
Contact Height	A1	.060	.0775	.095
Standoff ϕ	A3	.015	-	-
Corner Chamfer	CH1	.042	.045	.048
Chamfers	CH2	-	-	.020
Side Chamfer Height	CH3	.023	.026	.029
Overall Length	D	.485	.490	.495
Overall Width	E	.585	.590	.595
Molded Package Length	D1	.447	.450	.453
Molded Package Width	E1	.547	.550	.553
Footprint Length	D2	.376	.411	.446
Footprint Width	E2	.476	.511	.546
Lead Thickness	c	.008	.010	.013
Upper Lead Width	b1	.026	.029	.032
Lower Lead Width	b	.013	.017	.021

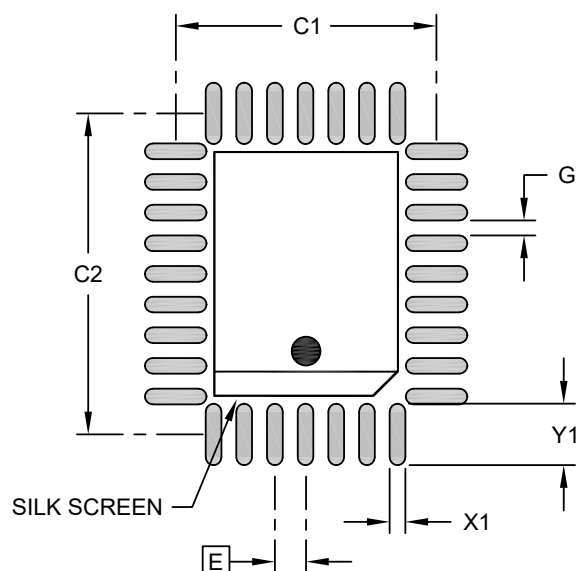
Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-023 Rev C Sheet 2 of 2

32-Lead Plastic Leaded Chip Carrier (L) - Rectangle [PLCC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	.050 BSC		
Contact Pad Spacing	C1		.425	
Contact Pad Spacing	C2		.524	
Contact Pad Width (X32)	X1			.026
Contact Pad Length (X32)	Y1			.100
Contact Pad to Center Pad (X28)	G	.008		

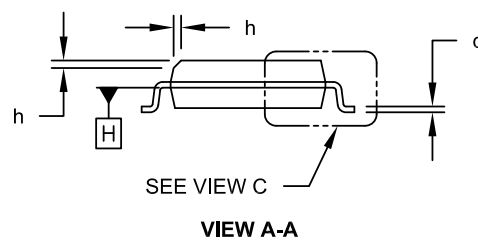
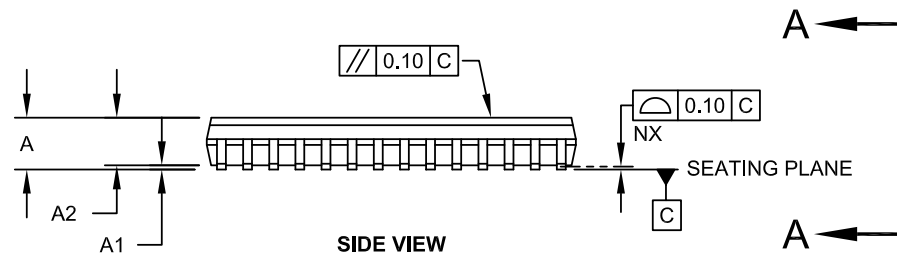
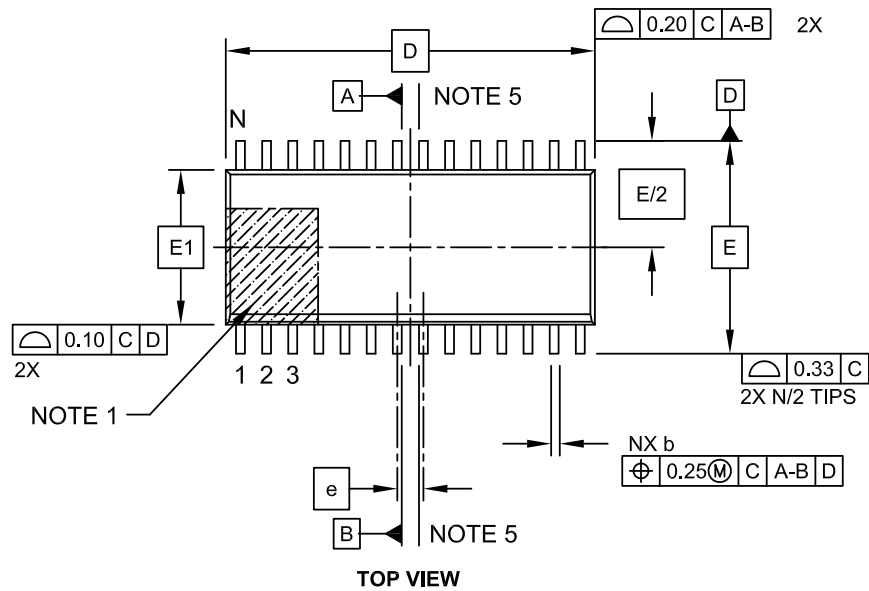
Notes:

- Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
- For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2023 Rev C

28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

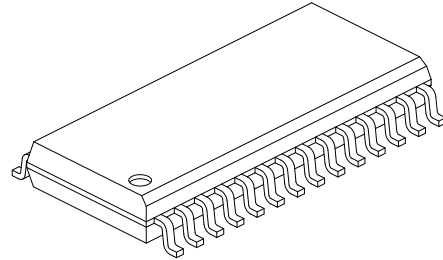
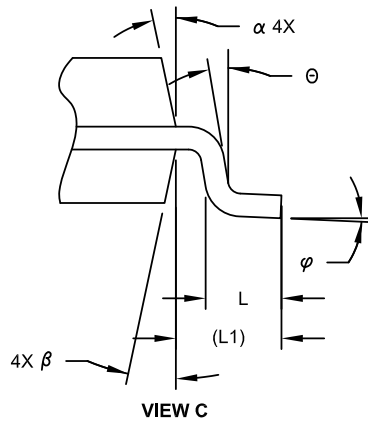
Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/package3>



Microchip Technology Drawing C04-052C Sheet 1 of 2

28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	28		
Pitch	e	1.27 BSC		
Overall Height	A	-	-	2.65
Molded Package Thickness	A2	2.05	-	-
Standoff §	A1	0.10	-	0.30
Overall Width	E	10.30 BSC		
Molded Package Width	E1	7.50 BSC		
Overall Length	D	17.90 BSC		
Chamfer (Optional)	h	0.25	-	0.75
Foot Length	L	0.40	-	1.27
Footprint	L1	1.40 REF		
Lead Angle	θ	0°	-	-
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.18	-	0.33
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

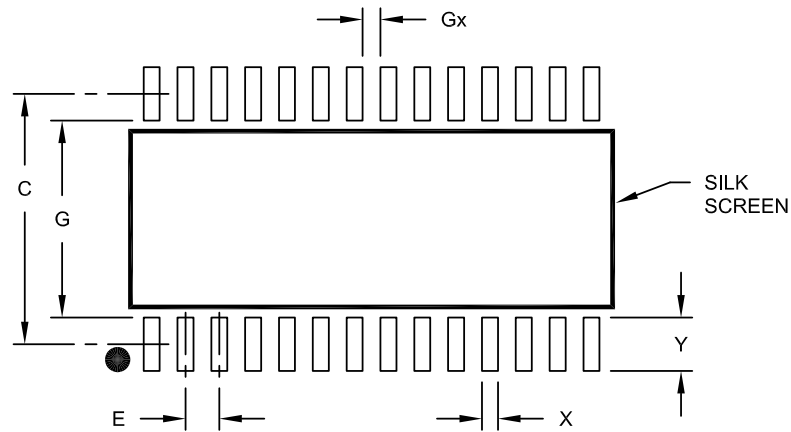
Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- § Significant Characteristic
- Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M
 - BSC: Basic Dimension. Theoretically exact value shown without tolerances.
 - REF: Reference Dimension, usually without tolerance, for information purposes only.
- Datums A & B to be determined at Datum H.

Microchip Technology Drawing C04-052C Sheet 2 of 2

28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		9.40	
Contact Pad Width (X28)	X			0.60
Contact Pad Length (X28)	Y			2.00
Distance Between Pads	Gx	0.67		
Distance Between Pads	G	7.40		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2052A

8. Revision History

Revision B (August 2023)

Removed 28-Lead TSOP package. Updated 32-Lead PLCC package drawing to latest revision (no change to form, fit or function).

Revision A (October 2020)

Updated to the Microchip template. Microchip DS20006432 replaces Atmel document 0270. Added updated Part Markings to include new trace code format.

Microchip Information

The Microchip Website

Microchip provides online support via our website at www.microchip.com/. This website is used to make files and information easily available to customers. Some of the content available includes:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQs), technical support requests, online discussion groups, Microchip design partner program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

Product Change Notification Service

Microchip's product change notification service helps keep customers current on Microchip products. Subscribers will receive email notification whenever there are changes, updates, revisions or errata related to a specified product family or development tool of interest.

To register, go to www.microchip.com/pcn and follow the registration instructions.

Customer Support

Users of Microchip products can receive assistance through several channels:

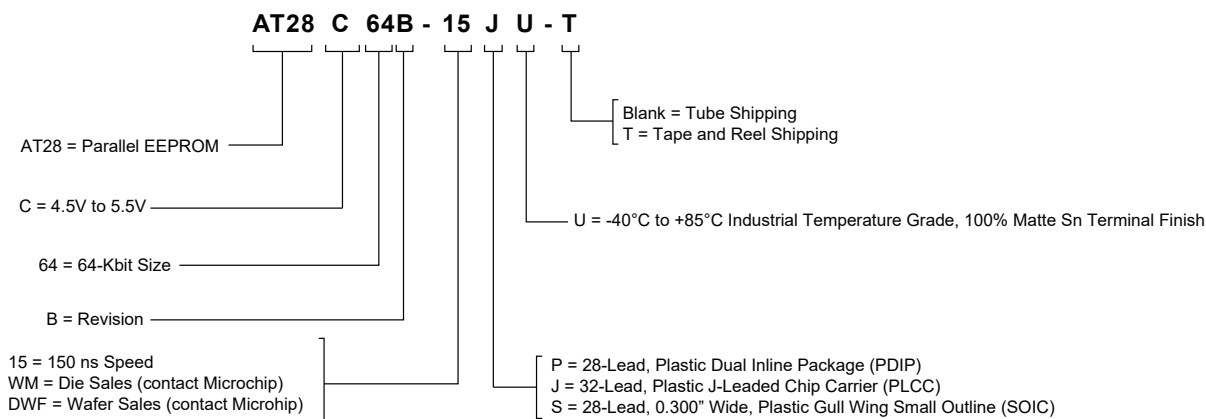
- Distributor or Representative
- Local Sales Office
- Embedded Solutions Engineer (ESE)
- Technical Support

Customers should contact their distributor, representative or ESE for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in this document.

Technical support is available through the website at: www.microchip.com/support

Product Identification System

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.



Examples

Table 9-1. Ordering Information

Ordering Code	Package Drawing Code	Package Option	t _{ACC} (ns)	Quantity	Operating Range
AT28C64B-15JU	L	J	150	32 Tube	Industrial Temperature (-40°C to +85°C)
AT28C64B-15JU-T				750 Reel	
AT28C64B-15PU	P	P		14 Tube	
AT28C64B-15SU	SO	S		27 Tube	
AT28C64B-15SU-T				1000 Reel	

Note: Contact Microchip Sales.

Package Types	
P	28-Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
J	32-Lead, Plastic J-leaded Chip Carrier (PLCC)
S	28-Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)

Microchip Devices Code Protection Feature

Note the following details of the code protection feature on Microchip products:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner, within operating specifications, and under normal conditions.
- Microchip values and aggressively protects its intellectual property rights. Attempts to breach the code protection features of Microchip product is strictly prohibited and may violate the Digital Millennium Copyright Act.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not mean that we are guaranteeing the product is “unbreakable”. Code protection is constantly evolving. Microchip is committed to continuously improving the code protection features of our products.

Legal Notice

This publication and the information herein may be used only with Microchip products, including to design, test, and integrate Microchip products with your application. Use of this information in any other manner violates these terms. Information regarding device applications is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. Contact your local Microchip sales office for additional support or, obtain additional support at www.microchip.com/en-us/support/design-help/client-support-services.

THIS INFORMATION IS PROVIDED BY MICROCHIP "AS IS". MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION INCLUDING BUT NOT LIMITED TO ANY IMPLIED WARRANTIES OF NON-INFRINGEMENT, MERCHANTABILITY, AND FITNESS FOR A PARTICULAR PURPOSE, OR WARRANTIES RELATED TO ITS CONDITION, QUALITY, OR PERFORMANCE.

IN NO EVENT WILL MICROCHIP BE LIABLE FOR ANY INDIRECT, SPECIAL, PUNITIVE, INCIDENTAL, OR CONSEQUENTIAL LOSS, DAMAGE, COST, OR EXPENSE OF ANY KIND WHATSOEVER RELATED TO THE INFORMATION OR ITS USE, HOWEVER CAUSED, EVEN IF MICROCHIP HAS BEEN ADVISED OF THE POSSIBILITY OR THE DAMAGES ARE FORESEEABLE. TO THE FULLEST EXTENT ALLOWED BY LAW, MICROCHIP'S TOTAL LIABILITY ON ALL CLAIMS IN ANY WAY RELATED TO THE INFORMATION OR ITS USE WILL NOT EXCEED THE AMOUNT OF FEES, IF ANY, THAT YOU HAVE PAID DIRECTLY TO MICROCHIP FOR THE INFORMATION.

Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights unless otherwise stated.

Trademarks

The Microchip name and logo, the Microchip logo, Adaptec, AVR, AVR logo, AVR Freaks, BesTime, BitCloud, CryptoMemory, CryptoRF, dsPIC, flexPWR, HELDO, IGLOO, JukeBlox, KeeLoq, Kleer, LANCheck, LinkMD, maXStylus, maXTouch, MediaLB, megaAVR, Microsemi, Microsemi logo, MOST, MOST logo, MPLAB, OptoLyzer, PIC, picoPower, PICSTART, PIC32 logo, PolarFire, Prochip Designer, QTouch, SAM-BA, SenGenuity, SpyNIC, SST, SST Logo, SuperFlash, Symmetricom, SyncServer, Tachyon, TimeSource, tinyAVR, UNI/O, Vectron, and XMEGA are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

AgileSwitch, APT, ClockWorks, The Embedded Control Solutions Company, EtherSynch, Flashtec, Hyper Speed Control, HyperLight Load, Libero, motorBench, mTouch, Powermite 3, Precision Edge, ProASIC, ProASIC Plus, ProASIC Plus logo, Quiet-Wire, SmartFusion, SyncWorld, Temux, TimeCesium, TimeHub, TimePictra, TimeProvider, TrueTime, and ZL are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Adjacent Key Suppression, AKS, Analog-for-the-Digital Age, Any Capacitor, AnyIn, AnyOut, Augmented Switching, BlueSky, BodyCom, Clockstudio, CodeGuard, CryptoAuthentication, CryptoAutomotive, CryptoCompanion, CryptoController, dsPICDEM, dsPICDEM.net, Dynamic Average Matching, DAM, ECAN, Espresso T1S, EtherGREEN, GridTime, IdealBridge, In-Circuit Serial Programming, ICSP, INICnet, Intelligent Paralleling, IntelliMOS, Inter-Chip Connectivity, JitterBlocker, Knob-on-Display, KoD, maxCrypto, maxView, memBrain, Mindi, MiWi, MPASM, MPF, MPLAB Certified logo, MPLIB, MPLINK, MultiTRAK, NetDetach, Omniscient Code Generation, PICDEM, PICDEM.net, PICkit, PICtail, PowerSmart, PureSilicon, QMatrix, REAL ICE, Ripple Blocker, RTAX, RTG4, SAM-ICE, Serial Quad I/O, simpleMAP, SimpliPHY, SmartBuffer, SmartHLS, SMART-I.S., storClad, SQL, SuperSwitcher, SuperSwitcher II, Switchtec, SynchroPHY, Total Endurance, Trusted Time, TSHARC, USBCheck, VariSense, VectorBlox, VeriPHY, ViewSpan, WiperLock, XpressConnect, and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

The Adaptec logo, Frequency on Demand, Silicon Storage Technology, and Symmcom are registered trademarks of Microchip Technology Inc. in other countries.

GestIC is a registered trademark of Microchip Technology Germany II GmbH & Co. KG, a subsidiary of Microchip Technology Inc., in other countries.

All other trademarks mentioned herein are property of their respective companies.

© 2020-2023, Microchip Technology Incorporated and its subsidiaries. All Rights Reserved.

ISBN: 978-1-6683-2856-9

AMBA, Arm, Arm7, Arm7TDMI, Arm9, Arm11, Artisan, big.LITTLE, Cordio, CoreLink, CoreSight, Cortex, DesignStart, DynamIQ, Jazelle, Keil, Mali, Mbed, Mbed Enabled, NEON, POP, RealView, SecurCore, Socrates, Thumb, TrustZone, ULINK, ULINK2, ULINK-ME, ULINK-PLUS, ULINKpro, μ Vision, Versatile are trademarks or registered trademarks of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

Quality Management System

For information regarding Microchip's Quality Management Systems, please visit www.microchip.com/quality.

Worldwide Sales and Service

AMERICAS	ASIA/PACIFIC	ASIA/PACIFIC	EUROPE
Corporate Office 2355 West Chandler Blvd. Chandler, AZ 85224-6199 Tel: 480-792-7200 Fax: 480-792-7277 Technical Support: www.microchip.com/support Web Address: www.microchip.com	Australia - Sydney Tel: 61-2-9868-6733 China - Beijing Tel: 86-10-8569-7000 China - Chengdu Tel: 86-28-8665-5511 China - Chongqing Tel: 86-23-8980-9588 China - Dongguan Tel: 86-769-8702-9880 China - Guangzhou Tel: 86-20-8755-8029 China - Hangzhou Tel: 86-571-8792-8115 China - Hong Kong SAR Tel: 852-2943-5100 China - Nanjing Tel: 86-25-8473-2460 China - Qingdao Tel: 86-532-8502-7355 China - Shanghai Tel: 86-21-3326-8000 China - Shenyang Tel: 86-24-2334-2829 China - Shenzhen Tel: 86-755-8864-2200 China - Suzhou Tel: 86-186-6233-1526 China - Wuhan Tel: 86-27-5980-5300 China - Xian Tel: 86-29-8833-7252 China - Xiamen Tel: 86-592-2388138 China - Zhuhai Tel: 86-756-3210040	India - Bangalore Tel: 91-80-3090-4444 India - New Delhi Tel: 91-11-4160-8631 India - Pune Tel: 91-20-4121-0141 Japan - Osaka Tel: 81-6-6152-7160 Japan - Tokyo Tel: 81-3-6880-3770 Korea - Daegu Tel: 82-53-744-4301 Korea - Seoul Tel: 82-2-554-7200 Malaysia - Kuala Lumpur Tel: 60-3-7651-7906 Malaysia - Penang Tel: 60-4-227-8870 Philippines - Manila Tel: 63-2-634-9065 Singapore Tel: 65-6334-8870 Taiwan - Hsin Chu Tel: 886-3-577-8366 Taiwan - Kaohsiung Tel: 886-7-213-7830 Taiwan - Taipei Tel: 886-2-2508-8600 Thailand - Bangkok Tel: 66-2-694-1351 Vietnam - Ho Chi Minh Tel: 84-28-5448-2100	Austria - Wels Tel: 43-7242-2244-39 Fax: 43-7242-2244-393 Denmark - Copenhagen Tel: 45-4485-5910 Fax: 45-4485-2829 Finland - Espoo Tel: 358-9-4520-820 France - Paris Tel: 33-1-69-53-63-20 Fax: 33-1-69-30-90-79 Germany - Garching Tel: 49-8931-9700 Germany - Haan Tel: 49-2129-3766400 Germany - Heilbronn Tel: 49-7131-72400 Germany - Karlsruhe Tel: 49-721-625370 Germany - Munich Tel: 49-89-627-144-0 Fax: 49-89-627-144-44 Germany - Rosenheim Tel: 49-8031-354-560 Israel - Ra'anana Tel: 972-9-744-7705 Italy - Milan Tel: 39-0331-742611 Fax: 39-0331-466781 Italy - Padova Tel: 39-049-7625286 Netherlands - Drunen Tel: 31-416-690399 Fax: 31-416-690340 Norway - Trondheim Tel: 47-72884388 Poland - Warsaw Tel: 48-22-3325737 Romania - Bucharest Tel: 40-21-407-87-50 Spain - Madrid Tel: 34-91-708-08-90 Fax: 34-91-708-08-91 Sweden - Gothenberg Tel: 46-31-704-60-40 Sweden - Stockholm Tel: 46-8-5090-4654 UK - Wokingham Tel: 44-118-921-5800 Fax: 44-118-921-5820