MPQ4345/4345J

36V, 2A, Ultra-Low Quiescent Current, Synchronous Step-Down Converter, AEC-Q100 Qualified

DESCRIPTION

The MPQ4345/4345J is a synchronous, step-down switching regulator with a 350kHz to 2.5MHz configurable frequency and an integrated internal high-side MOSFET (HS-FET) and low side MOSFET (LS-FET). The device provides up to 2A of highly efficient output current (I_{OUT}) with fixed-frequency, zero-delay pulse-width modulation (PWM) control to optimize transient response.

The wide 3.3V to 36V input voltage (V_{IN}) range and 42V load dump tolerance accommodate a variety of step-down applications in automotive input environments. A 1μA quiescent current (I_Q) in shutdown mode allows the device to be used in battery-powered applications.

High power conversion efficiency across a wide load range is achieved by scaling down the switching frequency (f_{SW}) under light-load conditions to reduce switching and gate driving losses.

An open-drain power good (PG) signal indicates that the output is within 94% to 106% of its nominal voltage.

Thermal shutdown provides reliable, fault-tolerant operation. A high duty cycle and low-dropout (LDO) mode are provided for automotive cold-crank conditions.

The MPQ4345 is available in a QFN-17 (3mmx4mm) package. The MPQ4345J is available in a QFN-19 (3mmx4mm) package.

FEATURES

- Designed for Automotive Applications:
  - Survives 42V Load Dump
  - Supports 3.1V Cold Crank
  - Low-Dropout (LDO) Mode
  - 2A Continuous Output Current (I_{OUT})
  - Continuous Operation Up to 36V
  - Zero-Delay Pulse-Width Modulation (PWM) Control
  - 20ns Minimum On Time (t_{ON_MIN})
  - -40°C to +150°C Operating Junction Temperature (T_J)
  - Available in AEC-Q100 Grade 1
- Increases Battery Life:
  - 1μA Low Shutdown Supply Current
  - 3μA Sleep Mode Quiescent Current (I_Q)
  - Advanced Asynchronous Modulation (AAM) Mode Increases Efficiency under Light Loads
- High Performance for Improved Thermals:
  - Internal 60mΩ HS-FET and 35mΩ LS-FET
- Optimized for EMC and EMI:
  - 350kHz to 2.5MHz Configurable Switching Frequency (f_{SW})
  - Symmetric VIN Pinout
  - Frequency Spread Spectrum (FSS) Modulation
  - MeshConnect™ Flip-Chip Package
- Additional Features:
  - Fixed Output Options (1): 1V, 1.1V, 1.8V, 2.5V, 3V, 3.3V, 3.8V, 5V
  - Power Good (PG) Output
  - Synchronizable to External Clock
  - Synchronized Clock Output
  - External Soft Start (SS)
  - Over-Current Protection (OCP) in Hiccup Mode
  - Available in a QFN-17 (3mmx4mm) Package for MPQ4345 and a QFN-19 (3mmx4mm) Package for MPQ4345J with Wettable Flanks

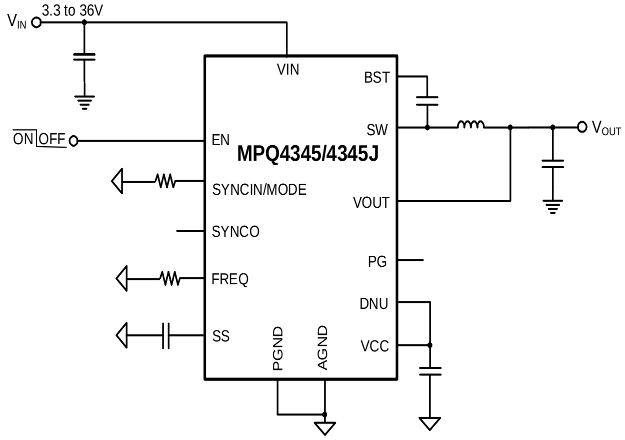
APPLICATIONS

- Automotive Clusters
- Automotive Infotainment
- Advanced Driver Assistance Systems (ADAS)
- Industrial Power Systems

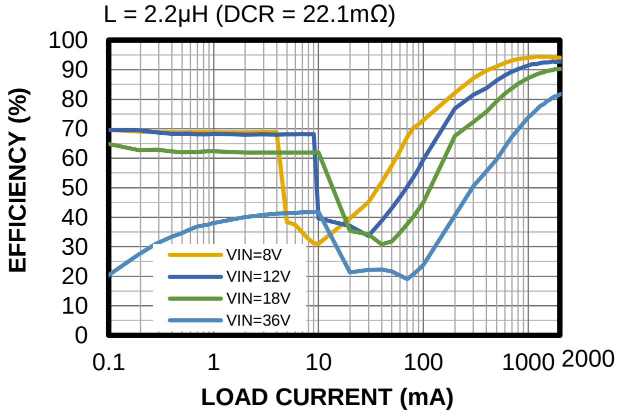
Note:

1) See the Ordering Information section on page 3 for the exact availability of each fixed output version. Additional output voltages may be available. Contact MPS for more details.

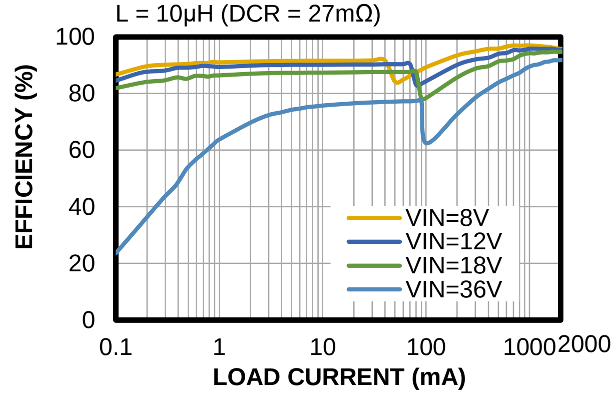
TYPICAL APPLICATION



Efficiency vs. Load Current
AAM mode, V_{OUT} = 5V, f_{SW} = 2.2MHz,
R_{FB1} = 14.67MΩ, R_{FB2} = 2MΩ,
L = 2.2µH (DCR = 22.1mΩ)



Efficiency vs. Load Current
AAM mode, V_{OUT} = 5V, f_{SW} = 410kHz,
R_{FB1} = 14.67MΩ, R_{FB2} = 2MΩ,
L = 10µH (DCR = 27mΩ)



ORDERING INFORMATION

Part Number (2) *	Output Voltage	Package	Top Marking	MSL Rating**
MPQ4345GLE-33-AEC1***	Fixed 3.3V	QFN-17 (3mmx4mm)	*See Below*	1
MPQ4345GLE-5-AEC1***	Fixed 5V	QFN-17 (3mmx4mm)	*See Below*	1
MPQ4345JGLE-33-AEC1***	Fixed 3.3V	QFN-19 (3mmx4mm)	*See Below*	1
MPQ4345JGLE-5-AEC1***	Fixed 5V	QFN-19 (3mmx4mm)	*See Below*	1

* For Tape & Reel, add suffix -Z (e.g. MPQ4345GLE-33-AEC1-Z).

** Moisture Sensitivity Level Rating

*** Wettable flank

Note:

2) Contact MPS for details on additional fixed output versions.

TOP MARKING

(MPQ4345GLE-33-AEC1 and MPQ4345GLE-5-AEC1)

MPYW
4345
LLL
E

MP: MPS prefix
Y: Year code
W: Week code
4345: Part number
LLL: Lot number
E: Wettable flank

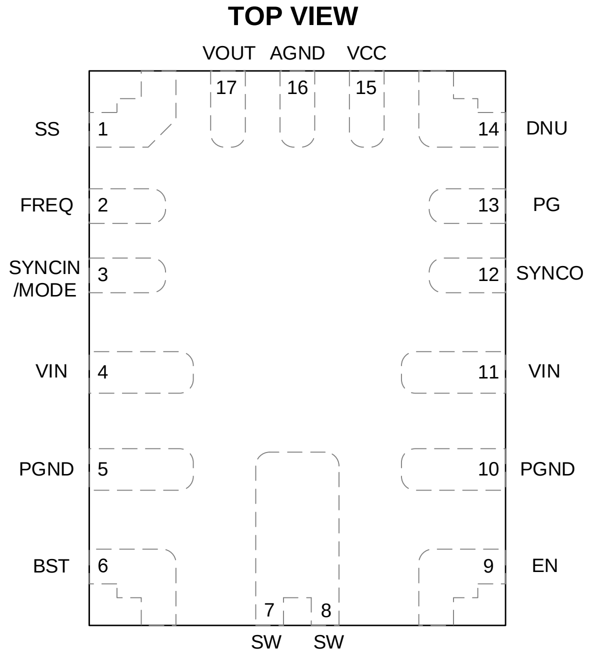
TOP MARKING

(MPQ4345JGLE-33-AEC1 and MPQ4345JGLE-5-AEC1)

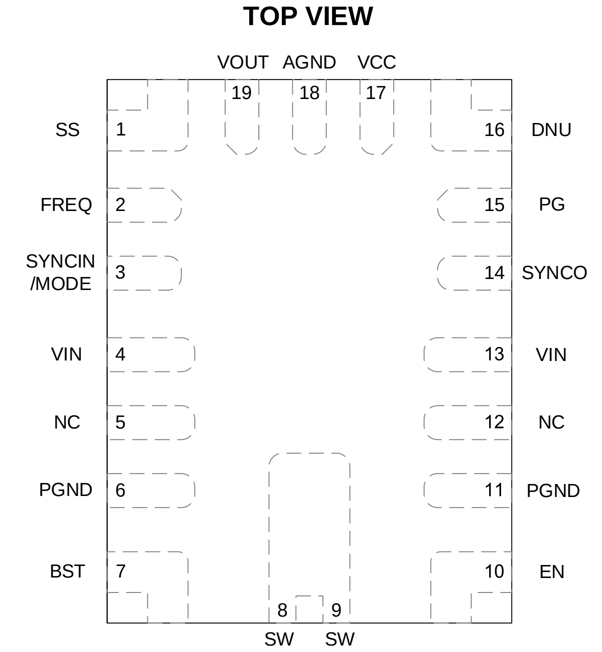
MPYW
4345
JLLL
E

MP: MPS prefix
Y: Year code
W: Week code
4345J: Part number
LLL: Lot number
E: Wettable flank

PACKAGE REFERENCE



QFN-17 (3mmx4mm)



QFN-19 (3mmx4mm)

PIN FUNCTIONS

Pin # QFN-19	Pin # QFN-17	Name	Description
1	1	SS	**Soft-start input.** Place a capacitor from the SS pin to ground to set the soft-start period. The MPQ4345/4345J sources 10µA from SS to the soft-start capacitor (C_{SS}) at start-up. As the SS voltage (V_{SS}) rises, the feedback reference voltage (V_{REF}) increases to limit inrush current during start-up. Do not float this pin.
2	2	FREQ	**Switching frequency configuration.** Connect a resistor from the FREQ pin to ground to set the switching frequency (f_{SW}).
3	3	SYNCIN/ MODE	**SYNC input and MODE selection.** Apply a clock signal to the SYNCIN/MODE pin to synchronize the internal oscillator frequency to the external clock. Use an external clock or pull this pin high to enter forced continuous conduction mode (FCCM). Pull this pin low to allow advanced asynchronous modulation (AAM) mode and pulse skipping under light loads. Do not float this pin.
4, 13	4, 11	VIN	**Input supply.** The VIN pin supplies power to all the internal control circuitry, as well as the power switch connected to SW. Place a decoupling capacitor from VIN to ground to minimize switching spikes. The capacitor should be placed close to VIN.
5, 12	-	NC	**No connection.** Float the NC pin.
6, 11	5, 10	PGND	**Power ground.**
7	6	BST	**Bootstrap.** The BST pin is the positive power supply for the high-side MOSFET (HS-FET) connected to SW. Connect a bypass capacitor between the BST and SW pins. See the Bootstrap Charging (BST, Pin 6) section on page 37 to calculate the size of this capacitor.
8, 9	7, 8	SW	**Switch node.** The SW pin is the internal power switch's output.
10	9	EN	**Enable.** Pull the EN pin below the specified threshold (0.85V) to shut down the chip. Pull EN above the specified threshold (1V) to enable the chip. Do not float this pin.
14	12	SYNCO	**SYNC output.** The SYNCO pin outputs a clock signal in phase with the internal oscillator signal, or the clock signal applied at the SYNCIN/MODE pin. This pin can be floated.
15	13	PG	**Power good output.** The PG pin's output is an open drain. If PG is used, it should be connected to a power source via a pull-up resistor. PG goes high if the output voltage (V_{OUT}) is within 94% to 106% of the nominal voltage. PG goes low if V_{OUT} is above 107% or below 93% of the nominal voltage. Float this pin if not used.
16	14	DNU	**Do not use.** Connect the DNU pin directly to VCC.
17	15	VCC	**Bias supply.** The VCC pin supplies 5V power to the internal control circuit and gate drivers. Place a decoupling capacitor from VCC to ground, and close to this pin. See the Setting the VCC Capacitor (VCC, Pin 15) section on page 39 to calculate the size of this capacitor.
18	16	AGND	**Analog ground.**
19	17	VOUT	**V_{OUT} regulation point.** Connect the VOUT pin directly to V_{OUT}.

ABSOLUTE MAXIMUM RATINGS [3]

VIN, EN……………………..............-0.3V to +42V
SW………………………. -0.3V to $V_{IN(MAX)}$ + 0.3V
BST………………………… .... V_{SW} +5.5V
All other pins…………… ....-0.3V to +6V
Continuous power dissipation (T_A = 25°C)
QFN-17 (3mmx4mm) [4] [8]…………………4.28W
QFN-19 (3mmx4mm) [4] [8]………………...4.13W
Operating junction temperature ....150°C
Lead temperature……………..................260°C
Storage temperature………….. -65°C to +150°C

ESD Ratings

Human body model (HBM)...................Class 2 [5]
Charged device model (CDM).........Class C2b [6]

Recommended Operating Conditions

Supply voltage (V_{IN})…… ....3.3V to 36V
Operating junction temp (T_J)…..-40°C to +150°C

Thermal Resistance

	θ_{JA}	θ_{JC}	
QFN-17 (3mmx4mm)			
JESD51-7	44.7	5.2	°C/W [7]
EVQ4345-L-00A	29.2		°C/W [8]
	Ψ_{JT}		
JESD51-7	1.2		°C/W [7]
EVQ4345-L-00A	6.1		°C/W [8]
QFN-19 (3mmx4mm)	θ_{JA}	θ_{JC}	
JESD51-7	43.6	5.4	°C/W [7]
EVQ4345J-L-00A	30.3		°C/W [8]
	Ψ_{JT}		
JESD51-7	0.9		°C/W [7]
EVQ4345J-L-00A	5.17		°C/W [8]

Notes:

3) Exceeding these ratings may damage the device.
4) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, which may cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
5) Per AEC-Q100-002.
6) Per AEC-Q100-011.
7) Measured on JESD51-7, a 4-layer PCB. The values given in this table are only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application. The θ_{JC} value shows the thermal resistance from junction-to-case bottom. The Ψ_{JT} value shows the characterization parameter from the junction-to-case top.
8) Measured on an MPS standard EVB, a 2oz copper thickness, 4-layer PCB (8.3cmx8.3cm). The Ψ_{JT} value shows the characterization parameter from the junction-to-case top.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to +150°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Supply						
Minimum operating input voltage (V_{IN})	V_{IN_MIN}				3.3	V
V_{IN} under-voltage lockout (UVLO) rising threshold	$V_{IN\_UVLO\_RISING}$		2.8	3	3.2	V
V_{IN} UVLO falling threshold	$V_{IN\_UVLO\_FALLING}$		2.6	2.8	3	V
V_{IN} UVLO hysteresis	$V_{IN\_UVLO\_HYS}$			200		mV
V_{IN} quiescent current (9)	I_Q	V_{OUT} = 1.05 x V_{SET}, no load (sleep mode), T_J = -40°C to +85°C	1.9	3	3.6	µA
		V_{OUT} = 1.05 x V_{SET}, no load (sleep mode), T_J = -40°C to +125°C	1.5		15	µA
V_{IN} switching quiescent current (9)	I_{Q_SLEEP}	SYNCIN/MODE = GND (AAM mode), switching, no load, T_J = -40°C to +85°C	2.4	3.5	4.5	µA
		SYNCIN/MODE = GND (AAM mode), switching, no load, T_J = -40°C to +125°C	2		16	µA
V_{IN} active current (no switching)	I_{Q_ACTIVE}	SYNCIN/MODE = VCC (FCCM), no switching		1200		µA
V_{IN} shutdown current	I_{SHDN}	EN = 0V, T_J = 25°C		1	3	µA
		EN = 0V			11	µA
V_{IN} over-voltage protection (OVP) threshold	$V_{IN\_OVP\_RISING}$		36	38	40	V
V_{IN} OVP hysteresis	$V_{IN\_OVP\_HYS}$			10		V
Enable (EN)						
EN rising threshold	V_{EN_RISING}		0.8	1	1.2	V
EN falling threshold	$V_{EN\_FALLING}$		0.65	0.85	1.05	V
EN hysteresis voltage	V_{EN_HYS}			150		mV
Switches and Frequency						
Switching frequency	f_{SW}	R_{FREQ} = 86.6kΩ	370	410	450	kHz
		R_{FREQ} = 33kΩ	950	1050	1150	kHz
		R_{FREQ} = 15kΩ	1980	2200	2420	kHz
Minimum on time	t_{ON_MIN}			20	35	ns
Minimum off time	t_{OFF_MIN}			120	140	ns
Switch leakage current	I_{SW_LKG}			0.01	5	µA
High-side MOSFET (HS-FET) on resistance	$R_{DS(ON)\_HS}$	V_{BST} - V_{SW} = 5V		60	110	mΩ
Low-side MOSFET(LS-FET) on resistance	$R_{DS(ON)\_LS}$	V_{CC} = 5V		35	60	mΩ

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to +150°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Bootstrap (BST)						
BST to SW refresh rising threshold	V_{BST-SW_RISING}			2.5	2.9	V
BST to SW refresh falling threshold	$V_{BST-SW\_FALLING}$			2.3	2.7	V
BST to SW refresh hysteresis	V_{BST-SW_HYS}			0.2		V
Soft Start (SS) and VCC						
VCC voltage	V_{CC}	I_{VCC} = 0	4.7	5	5.3	V
VCC regulation		I_{VCC} = 0mA and 30mA			1	%
VCC current limit	I_{LIMIT_VCC}	V_{CC} = 4V	50	100		mA
		V_{CC} = 0V		70		mA
Soft-start current	I_{SS}	V_{SS} = 0V		10		µA
Output and Regulation						
Output voltage (V_{OUT}) accuracy, 3.3V fixed output version	$V_{OUT\_ACC\_3.3}$	T_J = 25°C	3260	3300	3340	mV
		T_J = -40°C to +150°C	3230	3300	3370	mV
V_{OUT} accuracy, 5V fixed output version	$V_{OUT\_ACC\_5}$	T_J = 25°C	4940	5000	5060	mV
		T_J = -40°C to +150°C	4900	5000	5100	mV
V_{OUT} current	I_{VOUT}	V_{OUT} = V_{OUT_REG}		300		nA
V_{OUT} discharge	$I_{DISCHARGE}$	EN = 0V, V_{OUT} = 0.3V, V_{IN} = 3.3V to 36V	1.8			mA
Power Good (PG)						
PG rising threshold	PG_{VTH_RISING}	V_{OUT} rising	91	94	97	%
		V_{OUT} falling	103	106	109	
PG falling threshold	$PG_{VTH\_FALLING}$	V_{OUT} falling	90	93	96	%
		V_{OUT} rising	104	107	110	
PG trip threshold hysteresis	PG_{Vth_HYS}			1		%
PG low V_{OUT}	V_{PG_LOW}	I_{SINK} = 1mA		0.1	0.3	V
PG rising delay time	$t_{PG\_R\_DELAY}$			50		µs
PG falling delay time	$t_{PG\_F\_DELAY}$			50		µs
SYNCIN and SYNCO						
SYNCIN/MODE voltage rising threshold	V_{SYNC_RISING}		1.8			V
SYNCIN/MODE voltage falling threshold	$V_{SYNC\_FALLING}$				0.4	V
SYNCIN/MODE timeout	t_{MODE}	SYNCIN/MODE low to AAM mode		41		µs
SYNCIN clock range	f_{SYNC}	% of free-running frequency	90		115	%
SYNCO high voltage	V_{SYNCO_HIGH}	I_{SYNCO} = -1mA	3.3	5		V
SYNCO low voltage	V_{SYNCO_LOW}	I_{SYNCO} = 1mA			0.4	V

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to +150°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Protections						
High-side (HS) current limit	I_{LIMIT_HS}	Duty cycle = 30%	4.7	5.8	7.3	A
Low-side (LS) valley current limit (9)	I_{LIMIT_LS}		3	4.4	5.7	A
Zero-current detection (ZCD) current	I_{ZCD}	AAM mode	-0.05	+0.1	+0.25	A
LS reverse current limit	$I_{LIMIT\_REVERSE}$	FCCM		4		A
Thermal shutdown (9)	T_{SD}		150	170		°C
Thermal shutdown hysteresis(9)	T_{SD_HYS}			20		°C

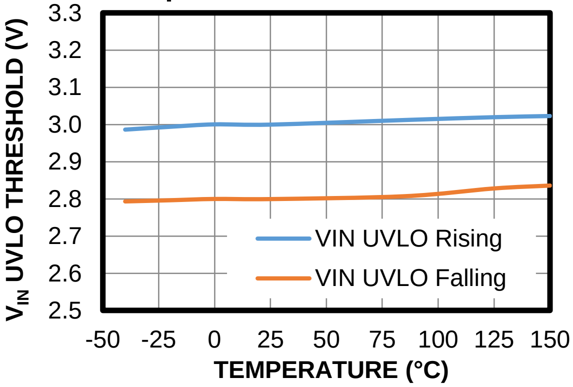
Note:

9) Guaranteed by design and characterization. Not tested in production.

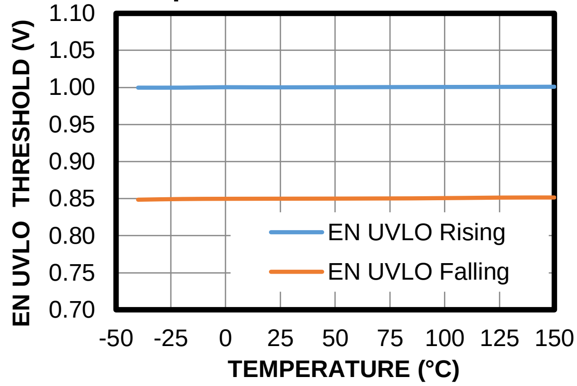
TYPICAL CHARACTERISTICS

V_{IN} = 12V, T_J = -40°C to +150°C, unless otherwise noted.

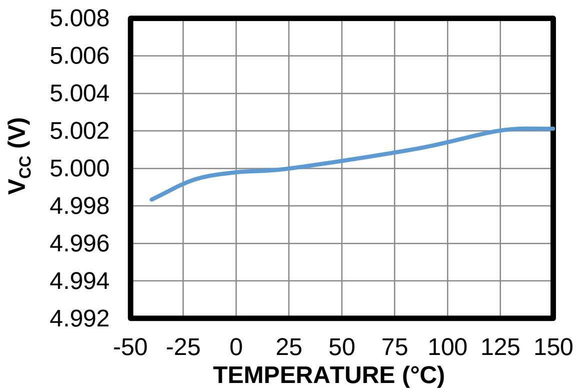
V_{IN} UVLO Threshold vs. Temperature



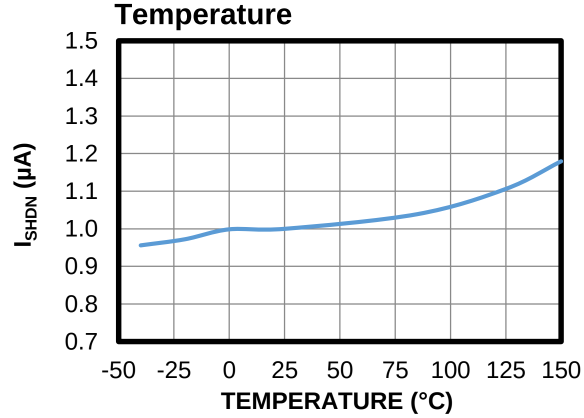
EN UVLO Threshold vs. Temperature



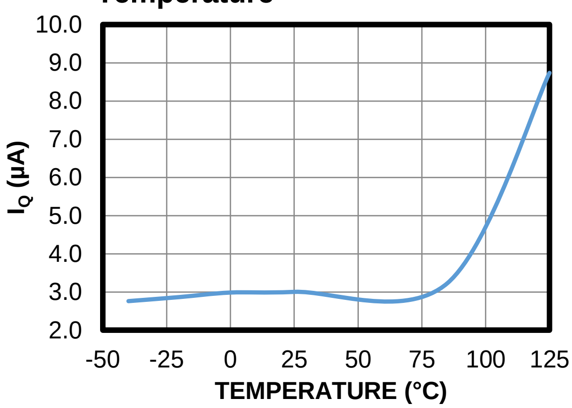
V_{CC} vs. Temperature



V_{IN} Shutdown Current vs. Temperature

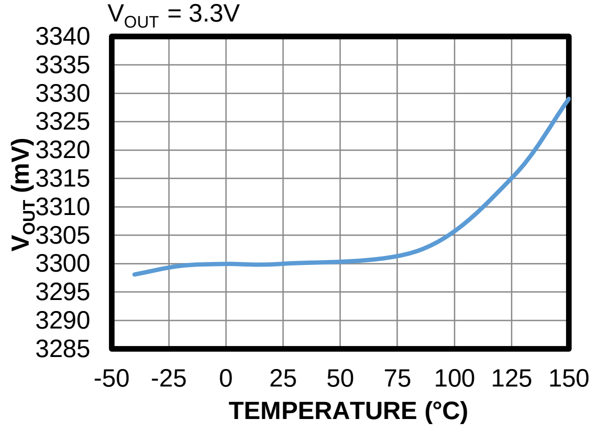


Quiescent Current vs. Temperature



V_{OUT} vs. Temperature

V_{OUT} = 3.3V

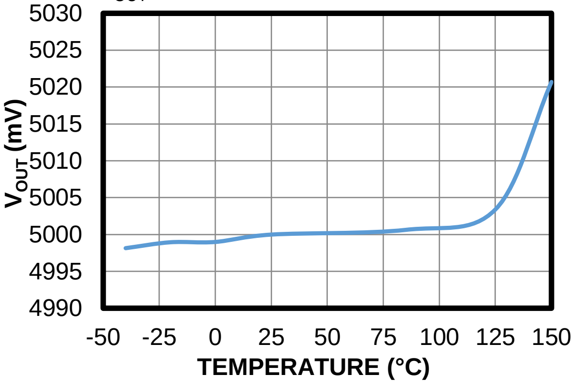


TYPICAL CHARACTERISTICS *(continued)*

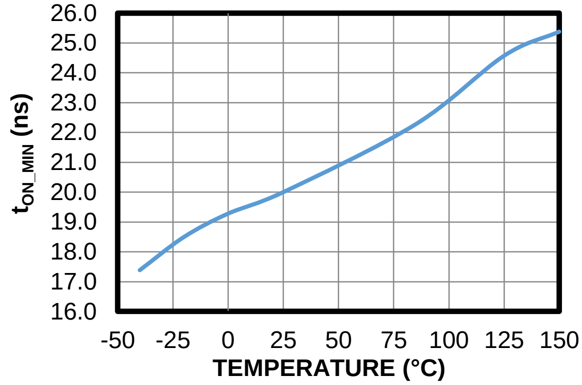
V_{IN} = 12V, T_J = -40°C to +150°C, unless otherwise noted.

V_{OUT} vs. Temperature

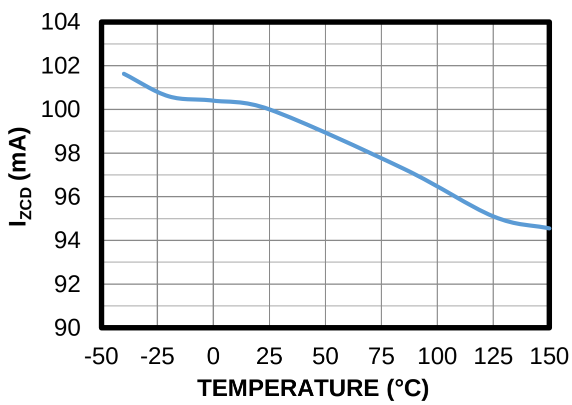
V_{OUT} = 5V



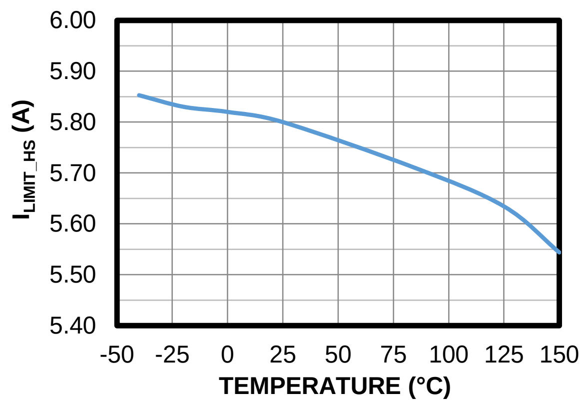
Minimum On Time vs. Temperature



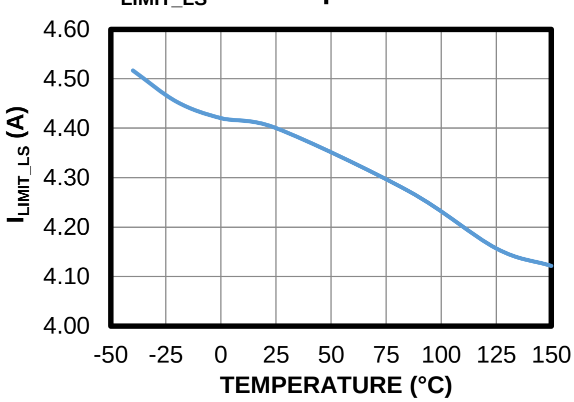
I_{ZCD} vs. Temperature



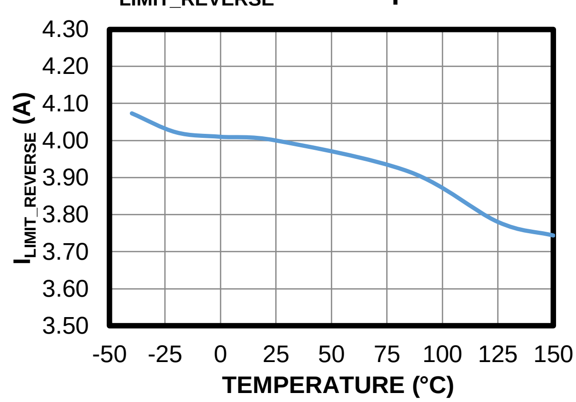
I_{LIMIT_HS} vs. Temperature



I_{LIMIT_LS} vs. Temperature

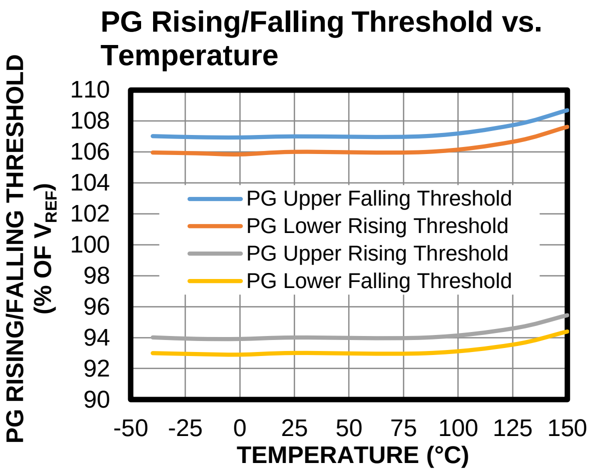


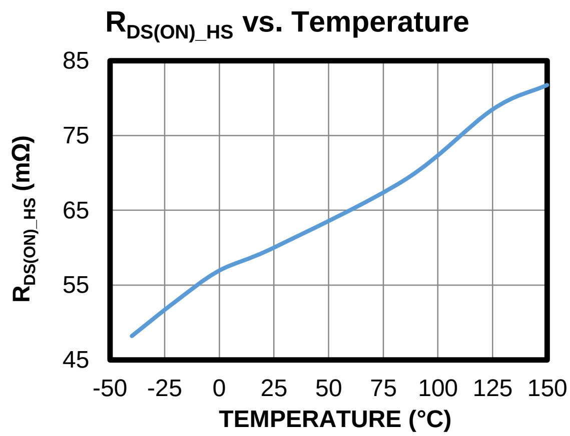
$I_{LIMIT\_REVERSE}$ vs. Temperature

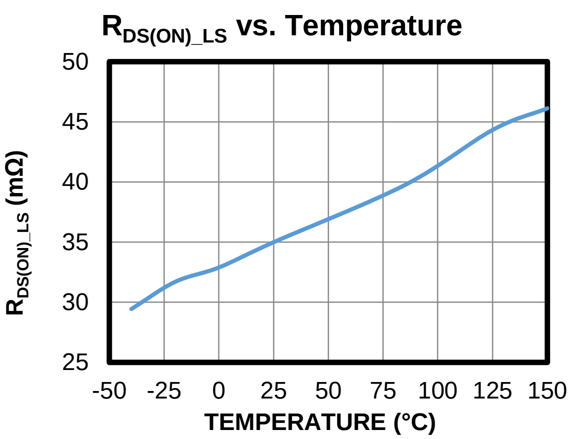


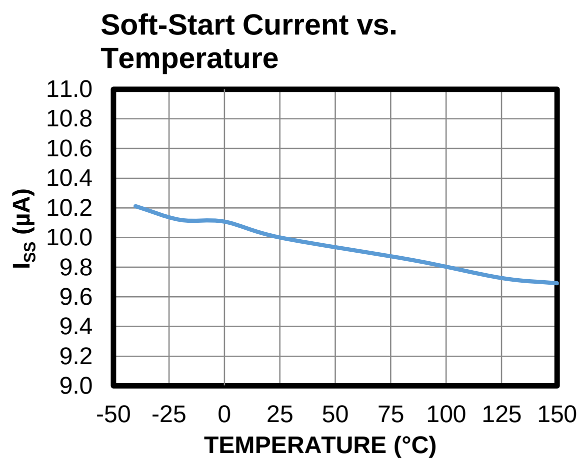
TYPICAL CHARACTERISTICS *(continued)*

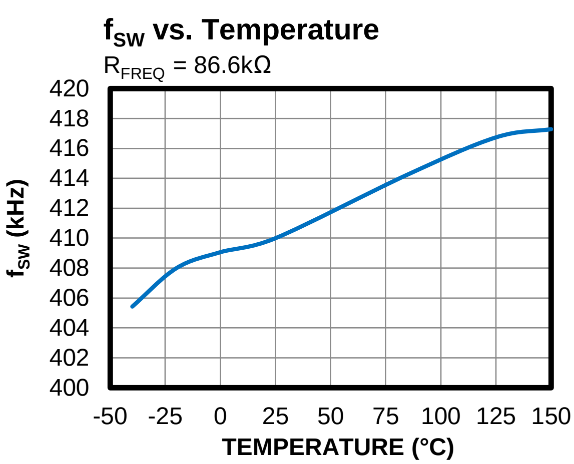
V_{IN} = 12V, T_J = -40°C to +150°C, unless otherwise noted.

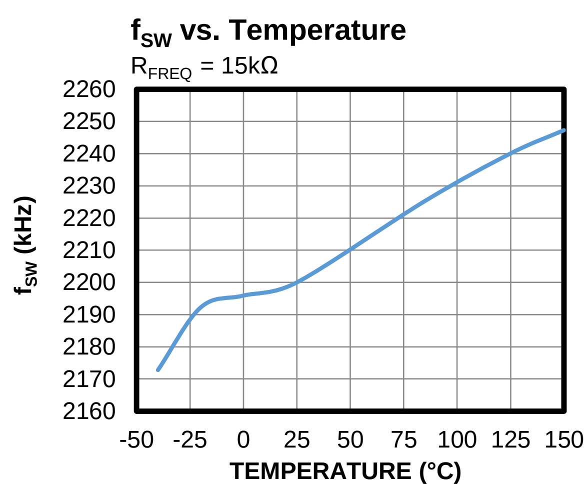








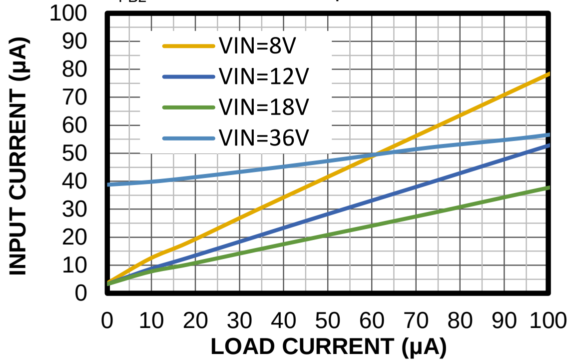




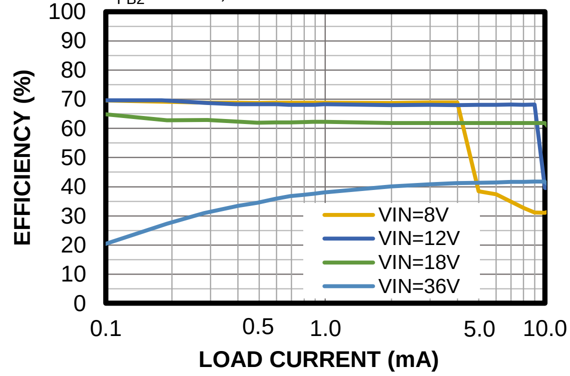
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 5V, L = 2.2µH (DCR = 22.1mΩ), f_{SW} = 2.2MHz, AAM mode, T_A = 25°C, unless otherwise noted.

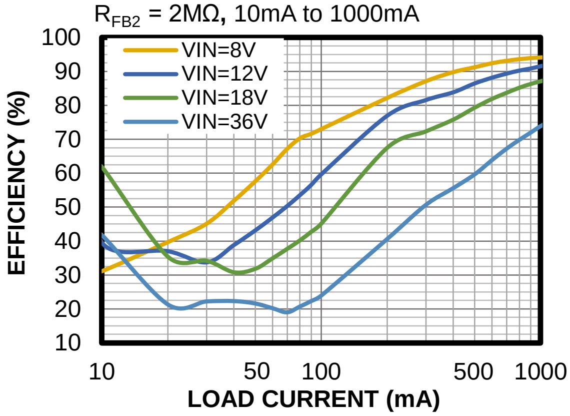
Input Current vs. Load Current
AAM mode, R_{FB1} = 14.67MΩ, R_{FB2} = 2MΩ, 0A to 100µA



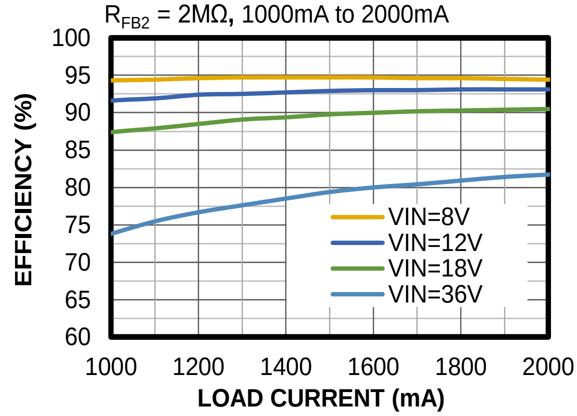
Efficiency vs. Load Current
AAM mode, R_{FB1} = 14.67MΩ, R_{FB2} = 2MΩ, 0.1mA to 10mA



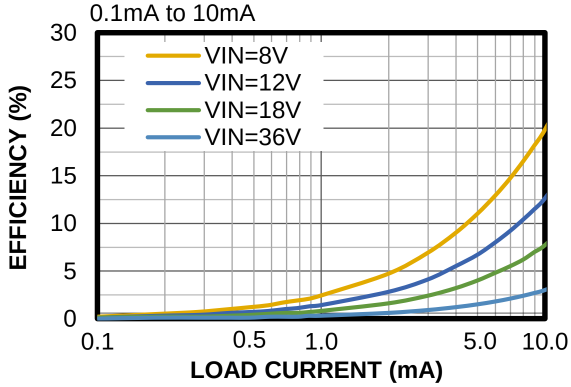
Efficiency vs. Load Current
AAM mode, R_{FB1} = 14.67MΩ, R_{FB2} = 2MΩ, 10mA to 1000mA



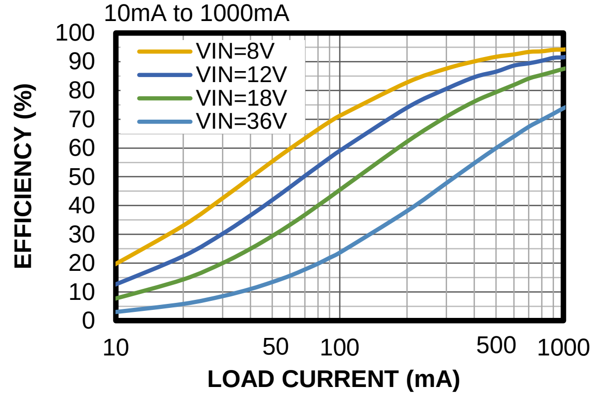
Efficiency vs. Load Current
AAM mode, R_{FB1} = 14.67MΩ, R_{FB2} = 2MΩ, 1000mA to 2000mA



Efficiency vs. Load Current
FCCM, R_{FB1} = 14.67MΩ, R_{FB2} = 2MΩ, 0.1mA to 10mA



Efficiency vs. Load Current
FCCM, R_{FB1} = 14.67MΩ, R_{FB2} = 2MΩ, 10mA to 1000mA

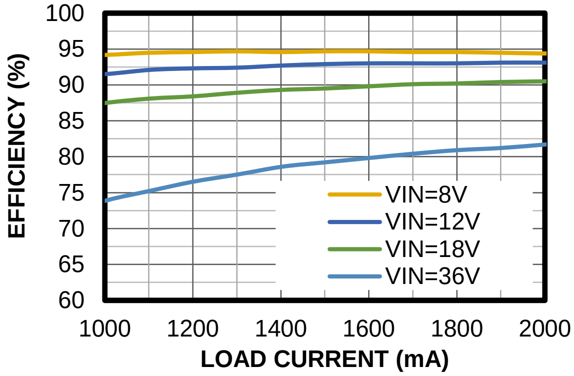


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 2.2µH (DCR = 22.1mΩ), f_{SW} = 2.2MHz, AAM mode, T_A = 25°C, unless otherwise noted.

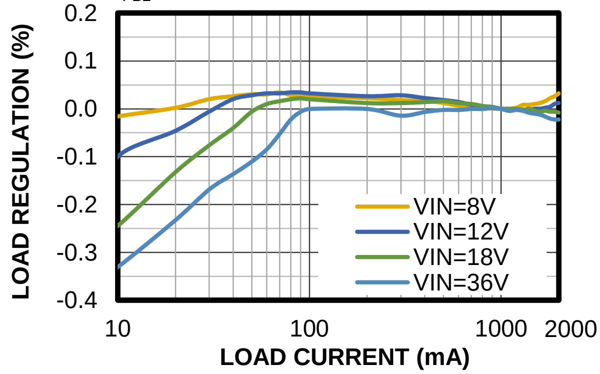
Efficiency vs. Load Current

FCCM, R_{FB1} = 14.67MΩ, R_{FB2} = 2MΩ, 1000mA to 2000mA



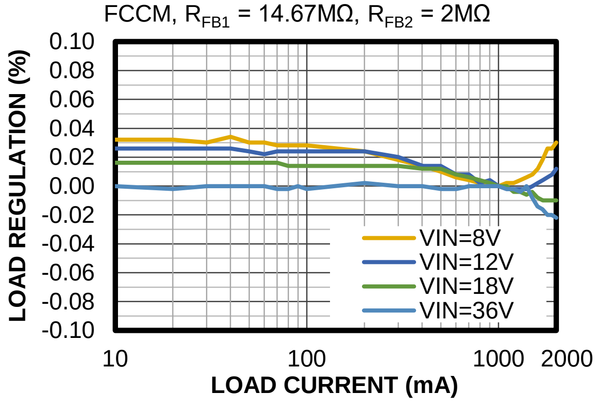
Load Regulation

AAM mode, R_{FB1} = 14.67MΩ, R_{FB2} = 2MΩ



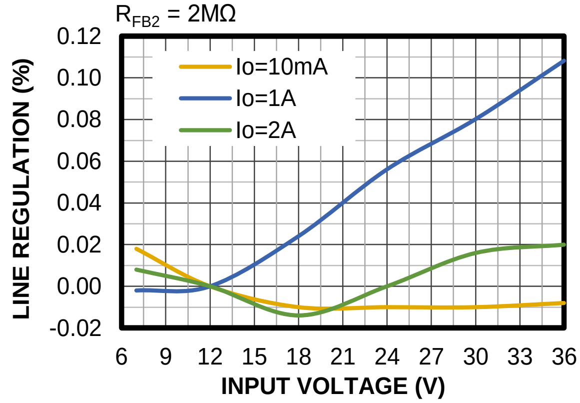
Load Regulation

FCCM, R_{FB1} = 14.67MΩ, R_{FB2} = 2MΩ



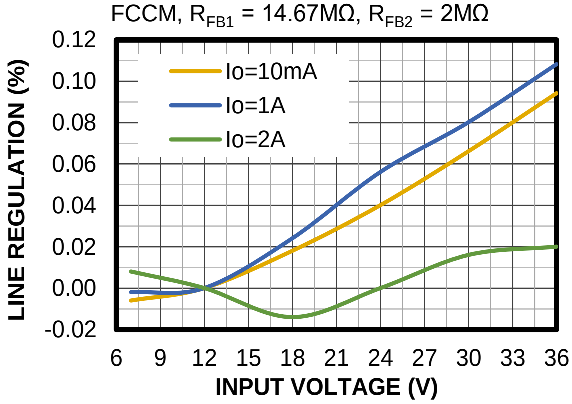
Line Regulation

AAM mode, R_{FB1} = 14.67MΩ, R_{FB2} = 2MΩ



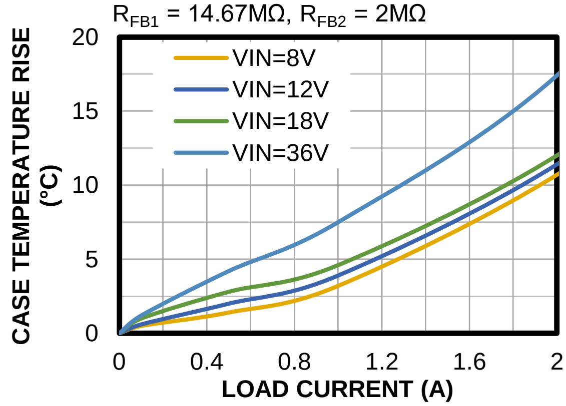
Line Regulation

FCCM, R_{FB1} = 14.67MΩ, R_{FB2} = 2MΩ



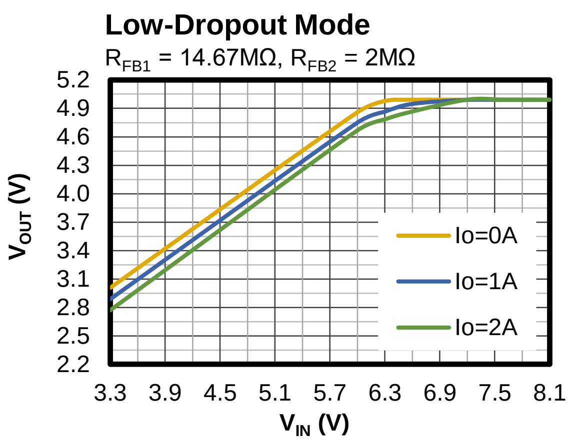
Case Temperature Rise

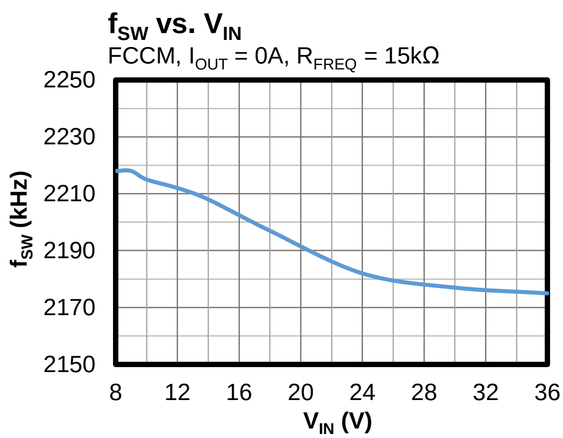
R_{FB1} = 14.67MΩ, R_{FB2} = 2MΩ



TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

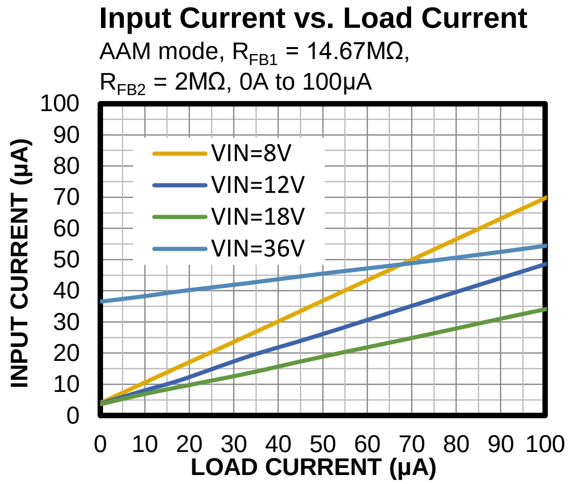
V_{IN} = 12V, V_{OUT} = 5V, L = 2.2µH (DCR = 22.1mΩ), f_{SW} = 2.2MHz, AAM mode, T_A = 25°C, unless otherwise noted.

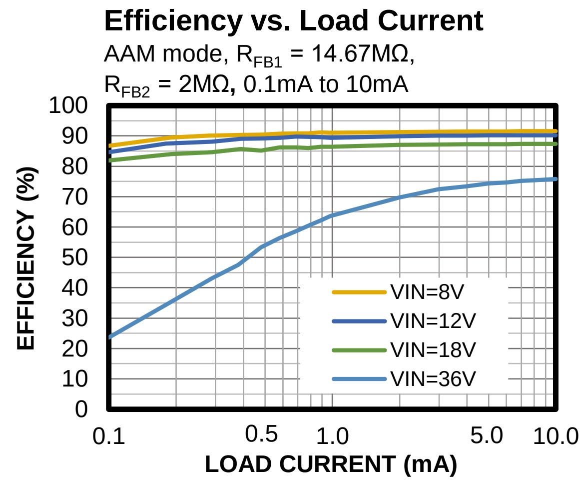


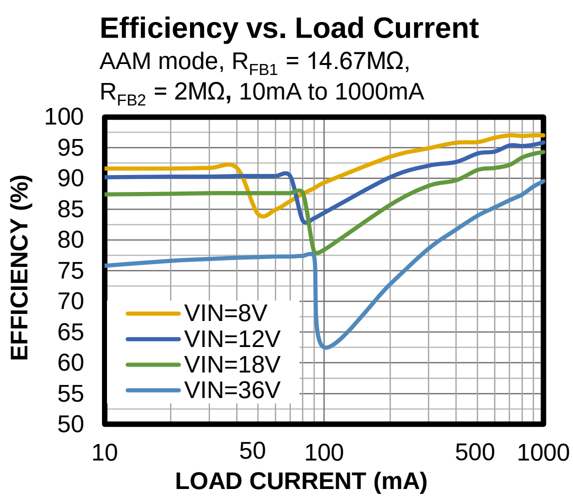


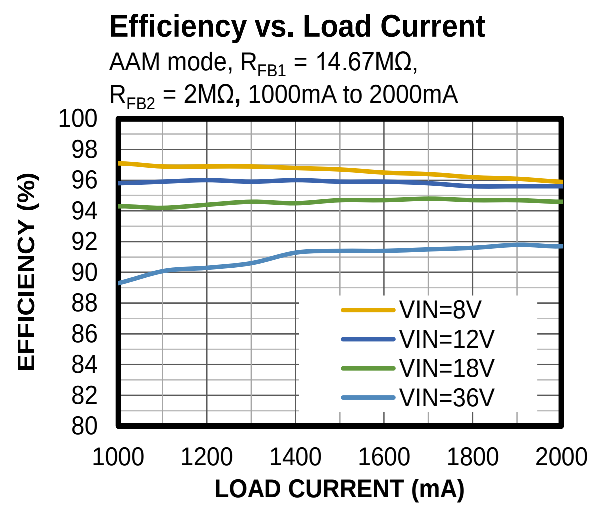
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

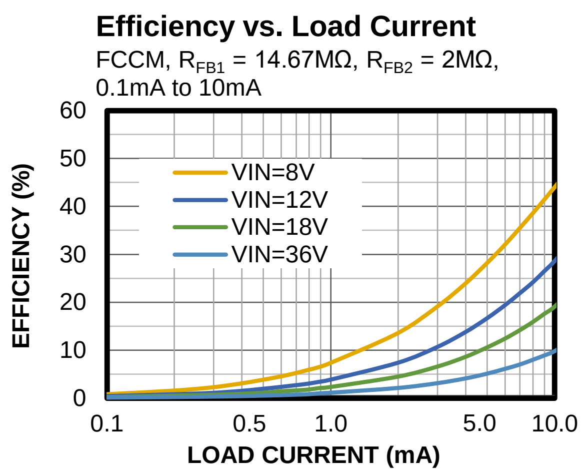
V_{IN} = 12V, V_{OUT} = 5V, L = 10μH (DCR = 27mΩ), f_{SW} = 410kHz, AAM mode, T_A = 25°C, unless otherwise noted.

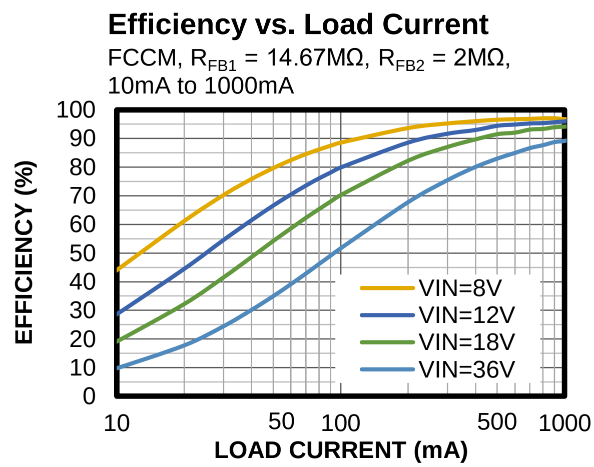










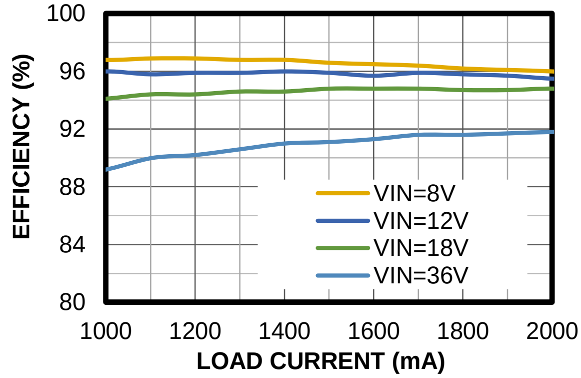


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 10µH (DCR = 27mΩ), f_{SW} = 410kHz, AAM mode, T_A = 25°C, unless otherwise noted.

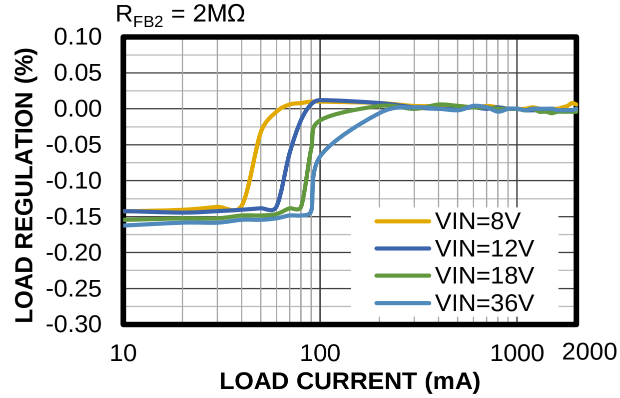
Efficiency vs. Load Current

FCCM, R_{FB1} = 14.67MΩ, R_{FB2} = 2MΩ, 1000mA to 2000mA



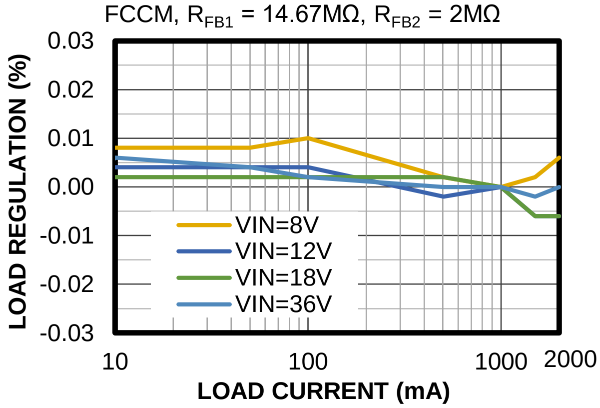
Load Regulation

AAM mode, R_{FB1} = 14.67MΩ, R_{FB2} = 2MΩ



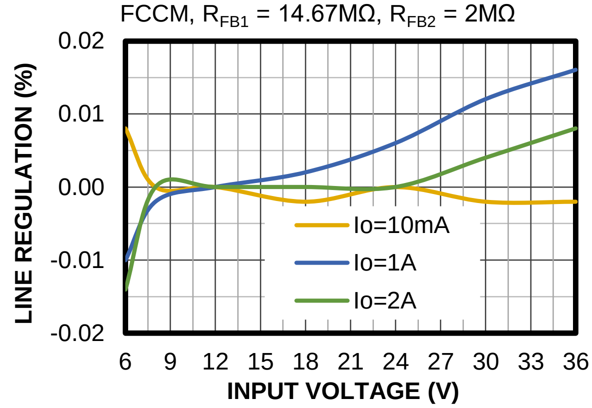
Load Regulation

FCCM, R_{FB1} = 14.67MΩ, R_{FB2} = 2MΩ



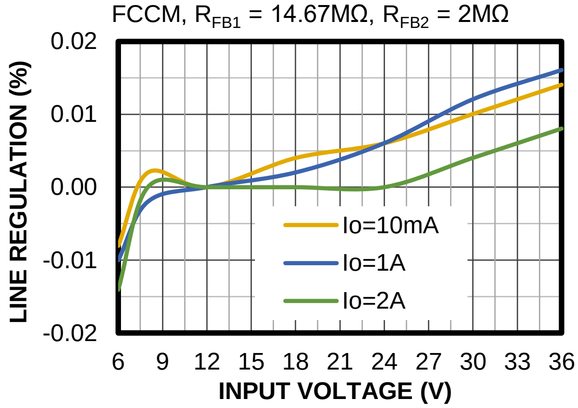
Line Regulation

FCCM, R_{FB1} = 14.67MΩ, R_{FB2} = 2MΩ



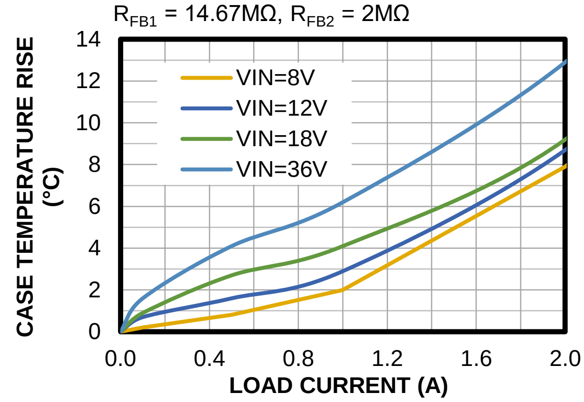
Line Regulation

FCCM, R_{FB1} = 14.67MΩ, R_{FB2} = 2MΩ



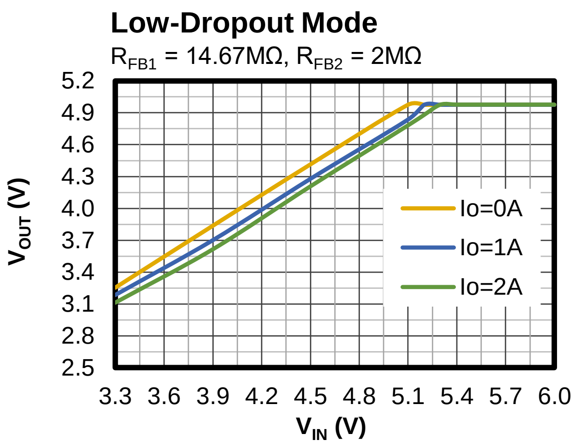
Case Temperature Rise

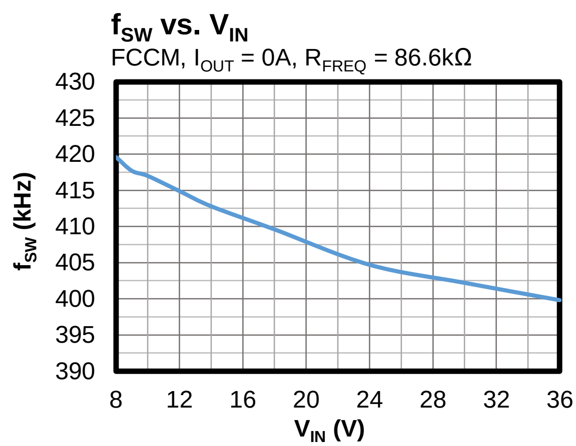
R_{FB1} = 14.67MΩ, R_{FB2} = 2MΩ



TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 10µH (DCR = 27mΩ), f_{SW} = 410kHz, AAM mode, T_A = 25°C, unless otherwise noted.

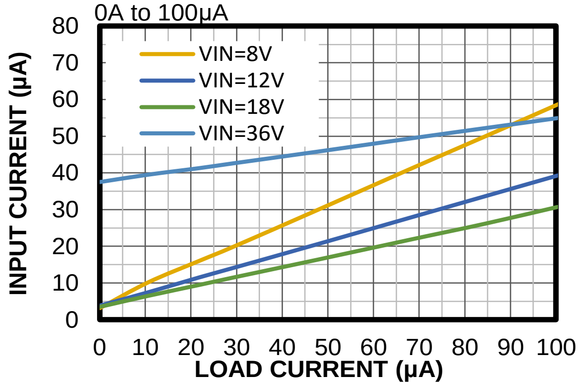




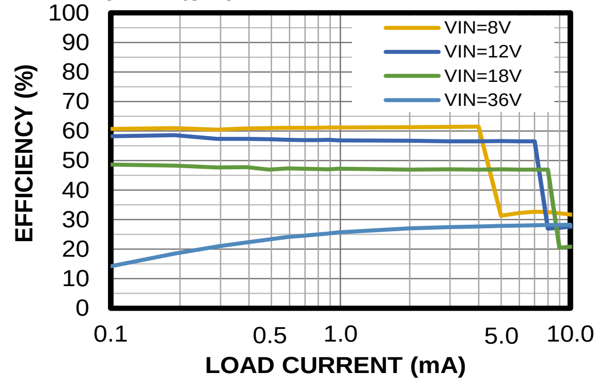
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 2.2µH (DCR = 22.1mΩ), f_{SW} = 2.2MHz, AAM mode, T_A = 25°C, unless otherwise noted.

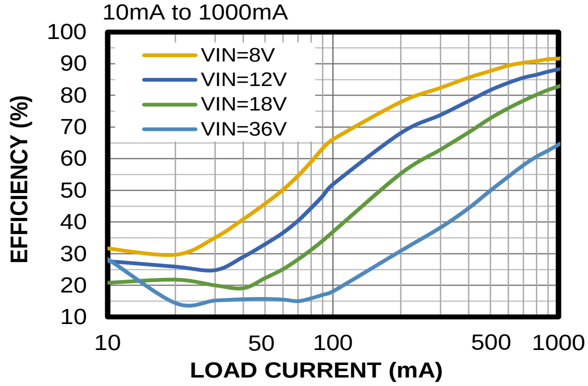
Input Current vs. Load Current
AAM mode, R_{FB1} = 9MΩ, R_{FB2} = 2MΩ,
0A to 100µA



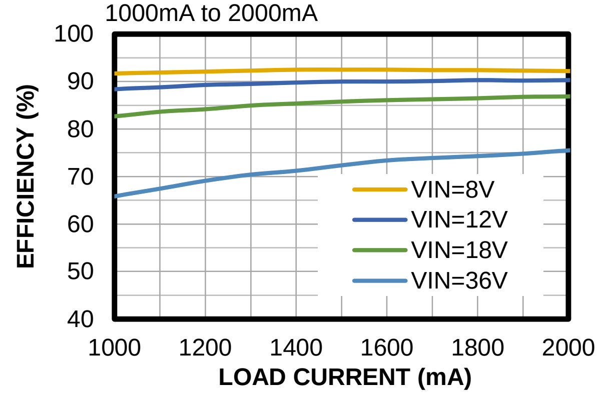
Efficiency vs. Load Current
AAM mode, R_{FB1} = 9MΩ, R_{FB2} = 2MΩ,
0.1mA to 10mA



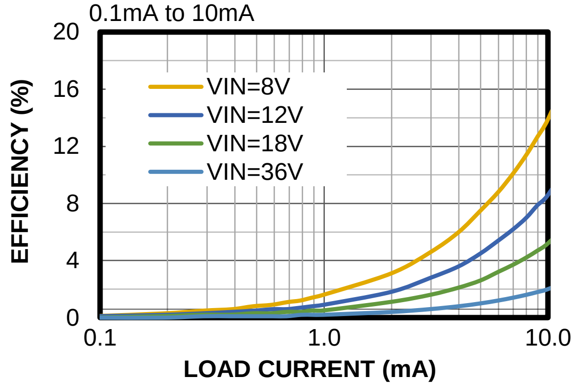
Efficiency vs. Load Current
AAM mode, R_{FB1} = 9MΩ, R_{FB2} = 2MΩ,
10mA to 1000mA



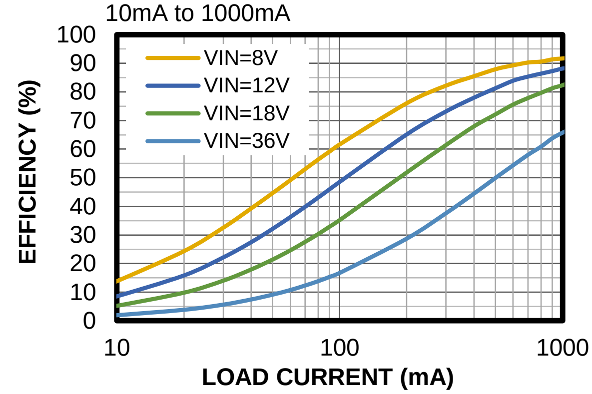
Efficiency vs. Load Current
AAM mode, R_{FB1} = 9MΩ, R_{FB2} = 2MΩ,
1000mA to 2000mA



Efficiency vs. Load Current
FCCM, R_{FB1} = 9MΩ, R_{FB2} = 2MΩ,
0.1mA to 10mA



Efficiency vs. Load Current
FCCM, R_{FB1} = 9MΩ, R_{FB2} = 2MΩ,
10mA to 1000mA

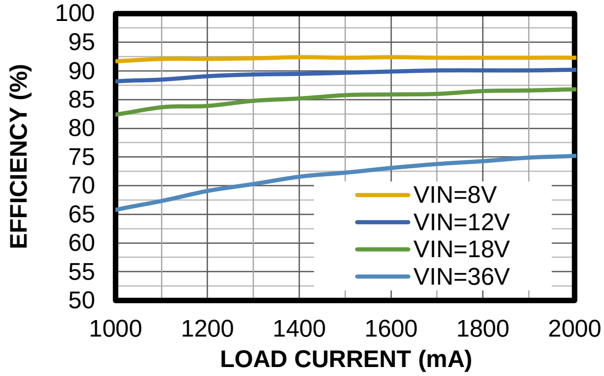


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 2.2µH (DCR = 22.1mΩ), f_{SW} = 2.2MHz, AAM mode, T_A = 25°C, unless otherwise noted.

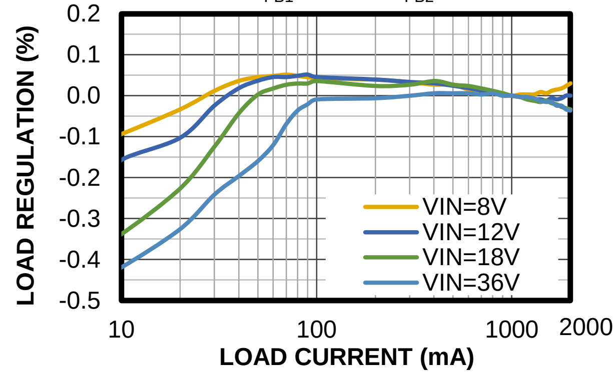
Efficiency vs. Load Current

FCCM, R_{FB1} = 9MΩ, R_{FB2} = 2MΩ, 1000mA to 2000mA



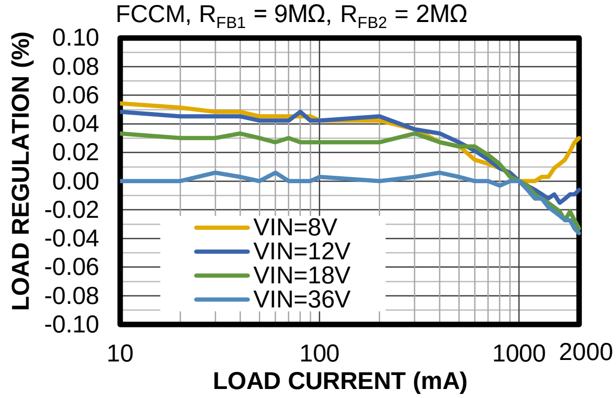
Load Regulation

AAM mode, R_{FB1} = 9MΩ, R_{FB2} = 2MΩ



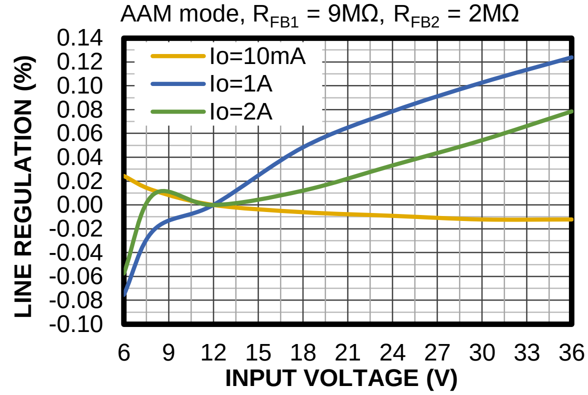
Load Regulation

FCCM, R_{FB1} = 9MΩ, R_{FB2} = 2MΩ



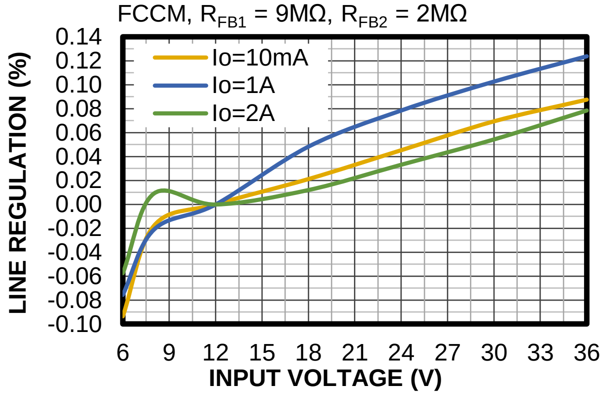
Line Regulation

AAM mode, R_{FB1} = 9MΩ, R_{FB2} = 2MΩ



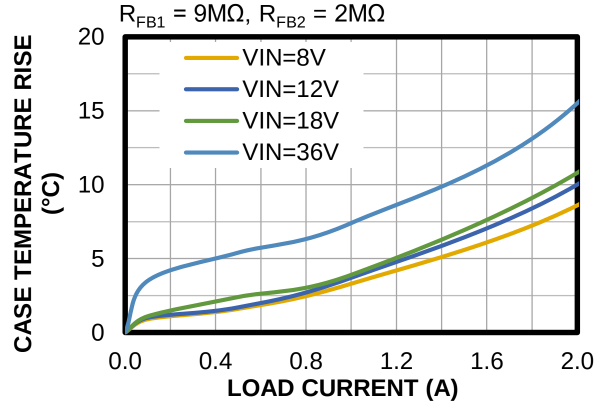
Line Regulation

FCCM, R_{FB1} = 9MΩ, R_{FB2} = 2MΩ



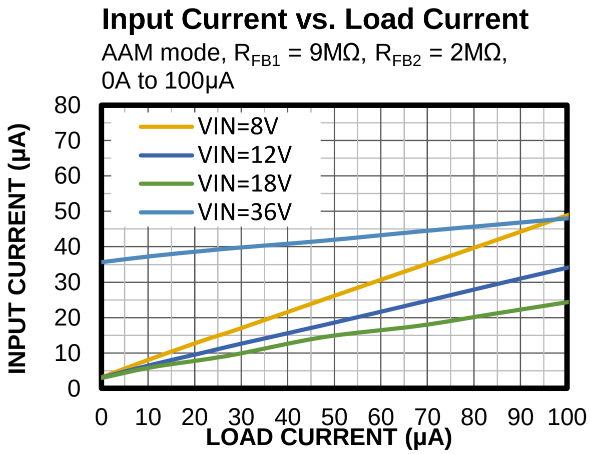
Case Temperature Rise

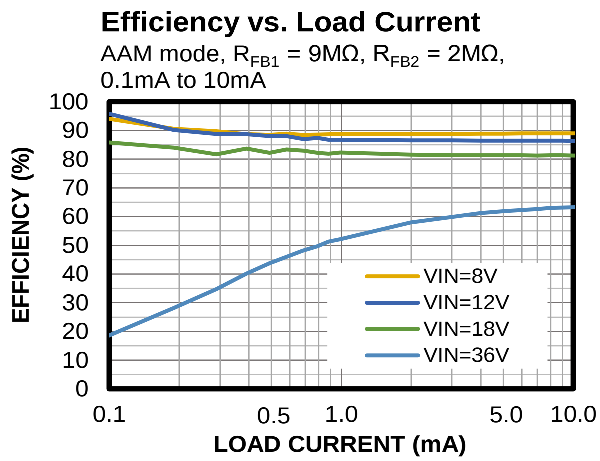
R_{FB1} = 9MΩ, R_{FB2} = 2MΩ

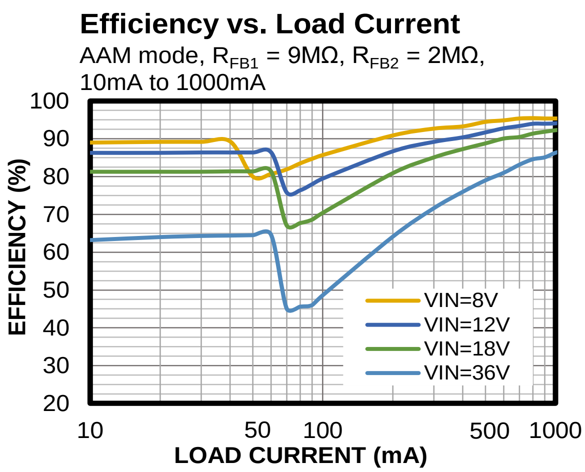


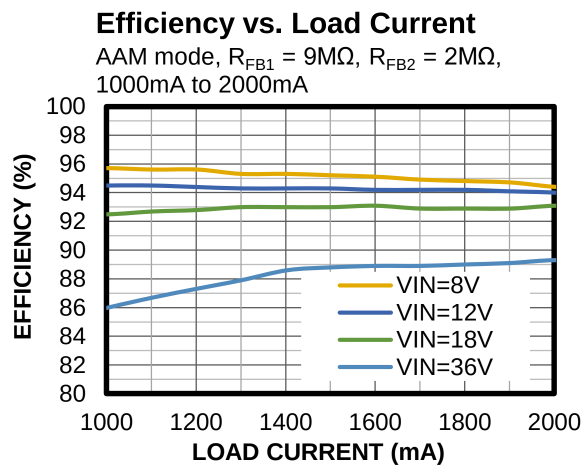
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

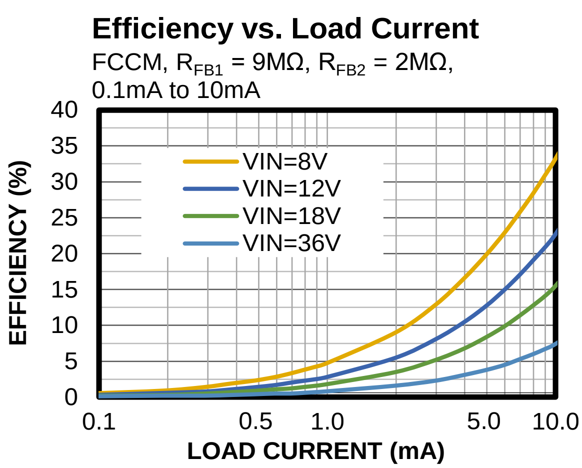
V_{IN} = 12V, V_{OUT} = 3.3V, L = 10µH (DCR = 27mΩ), f_{SW} = 410kHz, AAM mode, T_A = 25°C, unless otherwise noted.

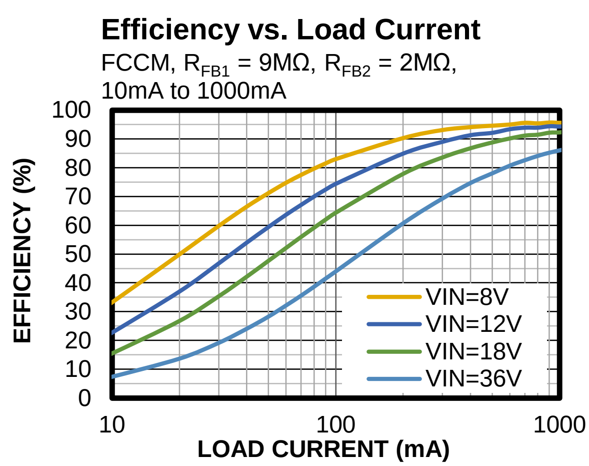










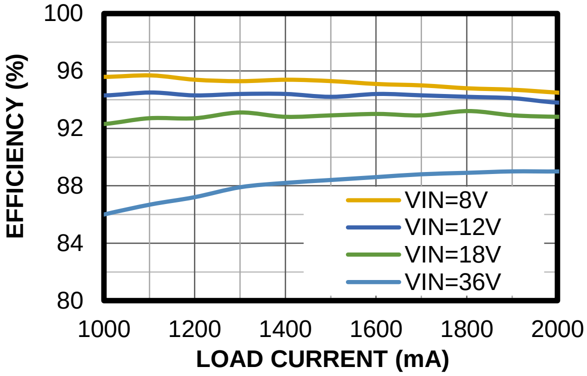


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 10µH (DCR = 27mΩ), f_{SW} = 410kHz, AAM mode, T_A = 25°C, unless otherwise noted.

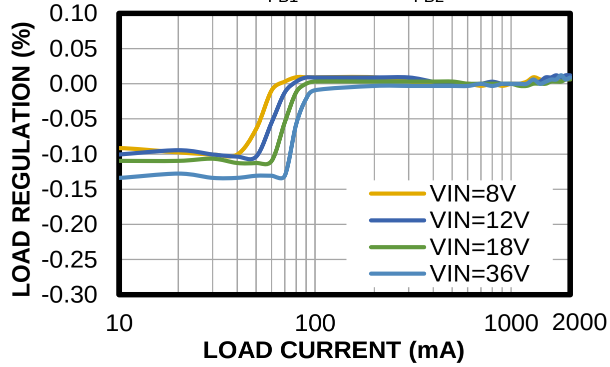
Efficiency vs. Load Current

FCCM, R_{FB1} = 9MΩ, R_{FB2} = 2MΩ, 1000mA to 2000mA



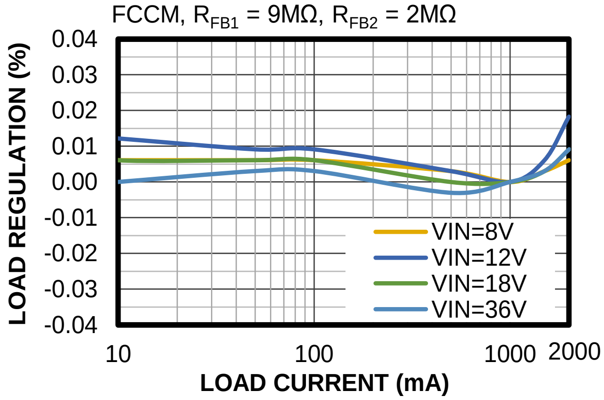
Load Regulation

AAM mode, R_{FB1} = 9MΩ, R_{FB2} = 2MΩ



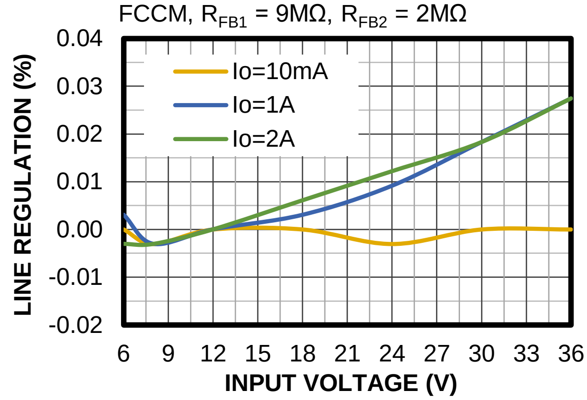
Load Regulation

FCCM, R_{FB1} = 9MΩ, R_{FB2} = 2MΩ



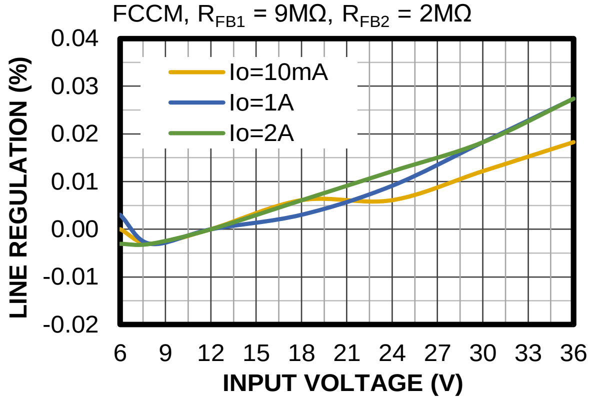
Line Regulation

FCCM, R_{FB1} = 9MΩ, R_{FB2} = 2MΩ



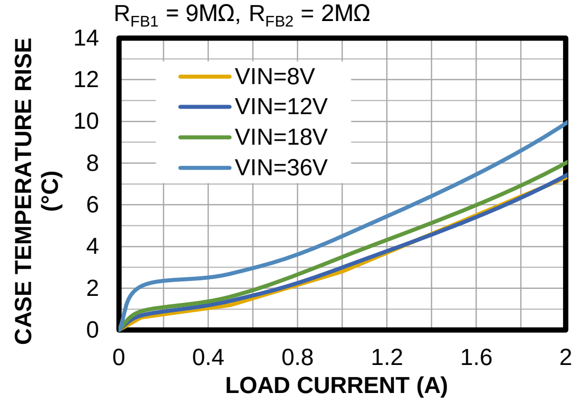
Line Regulation

FCCM, R_{FB1} = 9MΩ, R_{FB2} = 2MΩ



Case Temperature Rise

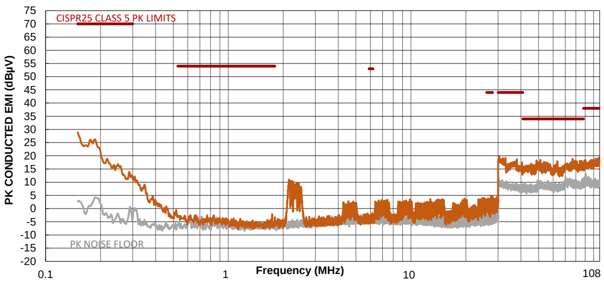
R_{FB1} = 9MΩ, R_{FB2} = 2MΩ



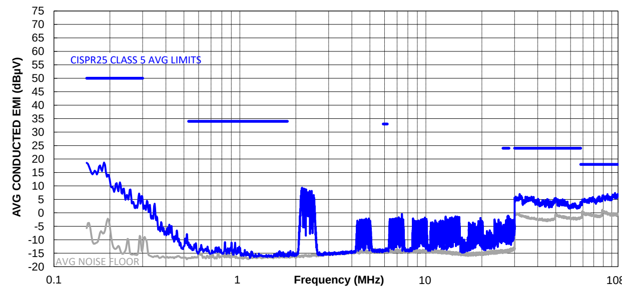
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L= 2.2µH [10], f_{SW} = 2.2MHz, AAM mode, T_A = 25°C, unless otherwise noted. [11]

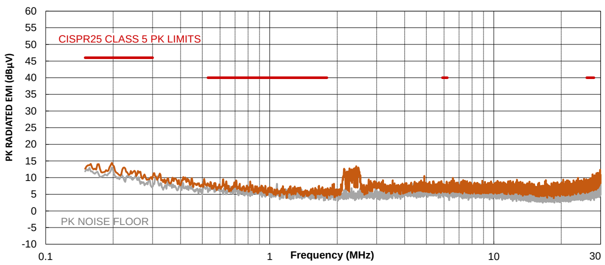
CISPR25 Class 5 Peak Conducted Emissions
150kHz to 108MHz



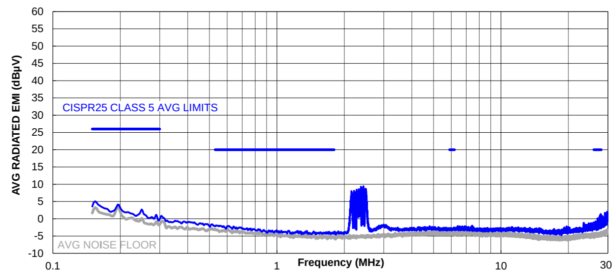
CISPR25 Class 5 Average Conducted Emissions
150kHz to 108MHz



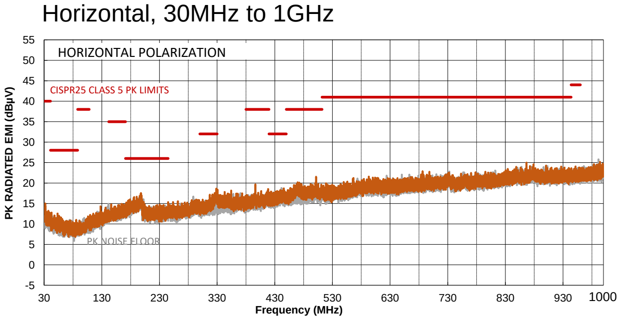
CISPR25 Class 5 Peak Radiated Emissions
150kHz to 30MHz



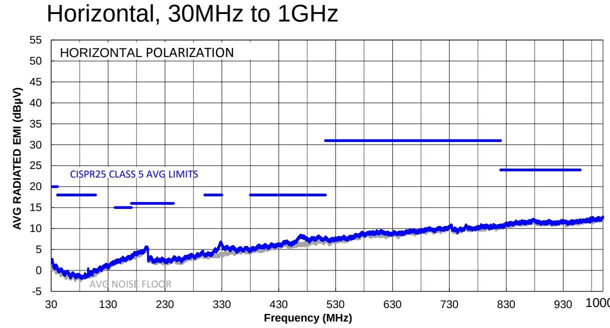
CISPR25 Class 5 Average Radiated Emissions
150kHz to 30MHz



CISPR25 Class 5 Peak Radiated Emissions
Horizontal, 30MHz to 1GHz



CISPR25 Class 5 Average Radiated Emissions
Horizontal, 30MHz to 1GHz

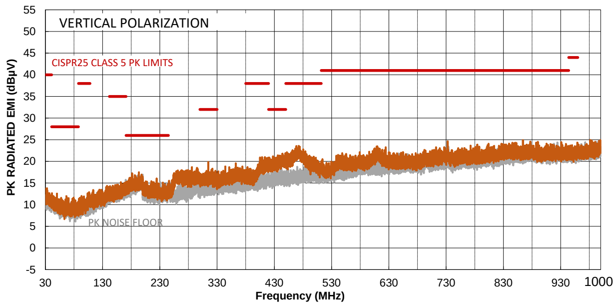


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L= 2.2µH (10), f_{SW} = 2.2MHz, AAM mode, T_A = 25°C, unless otherwise noted. (11)

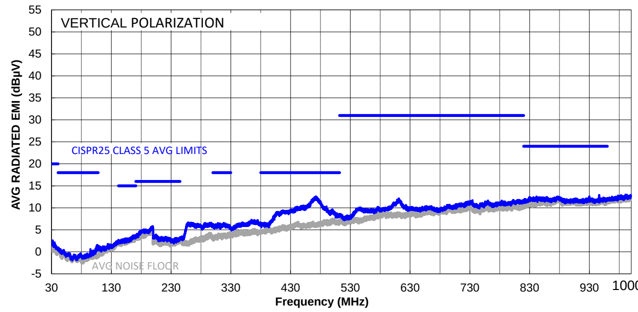
CISPR25 Class 5 Peak Radiated Emissions

Vertical, 30MHz to 1GHz



CISPR25 Class 5 Average Radiated Emissions

Vertical, 30MHz to 1GHz



Notes:

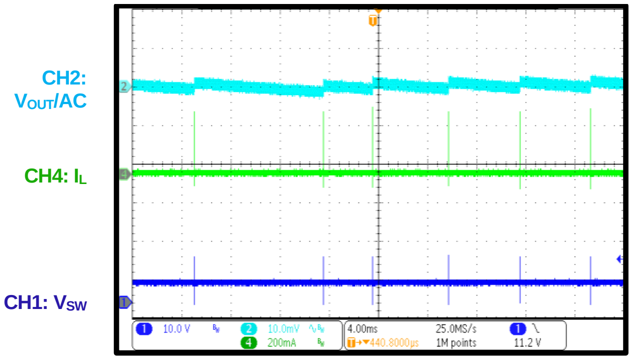
10) Inductor part number: XEL4030-222MEB/C. DCR = 22.1mΩ.
11) The EMC test results are based on the application circuit with EMI filters (see Figure 13 on page 43).

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 2.2µH, f_{SW} = 2.2MHz, AAM mode, T_A = 25°C, unless otherwise noted.

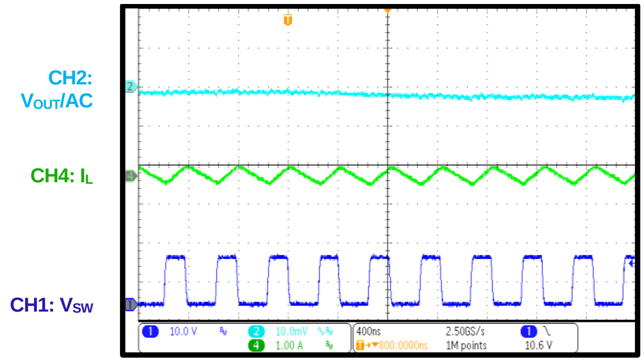
Steady State

I_{OUT} = 0A, AAM mode



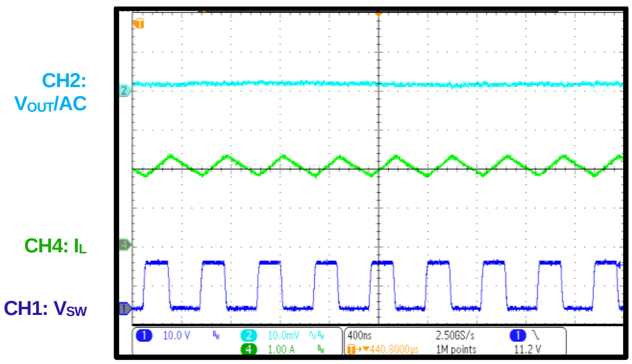
Steady State

I_{OUT} = 0A, FCCM



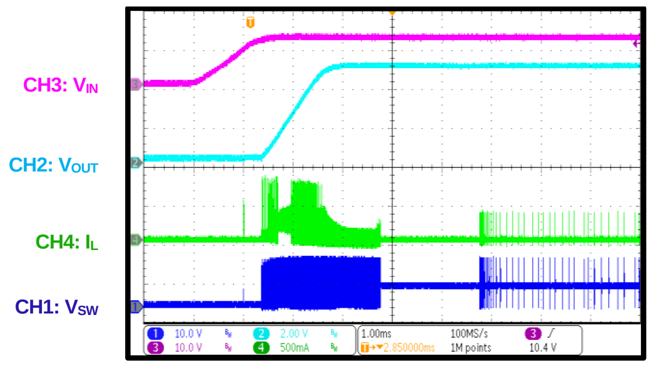
Steady State

I_{OUT} = 2A



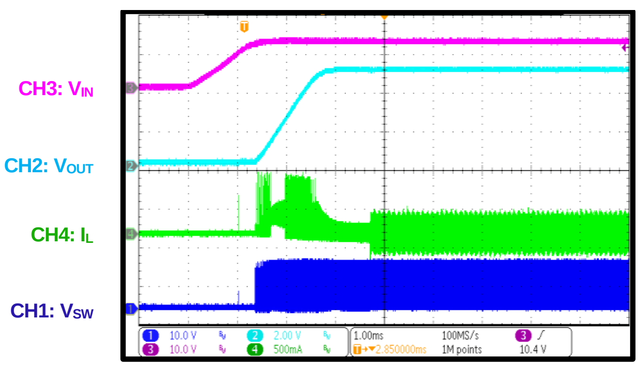
Start-Up through VIN

I_{OUT} = 0A, AAM mode



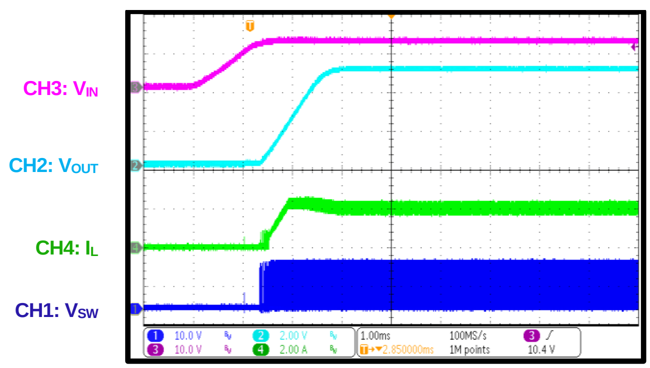
Start-Up through VIN

I_{OUT} = 0A, FCCM



Start-Up through VIN

I_{OUT} = 2A

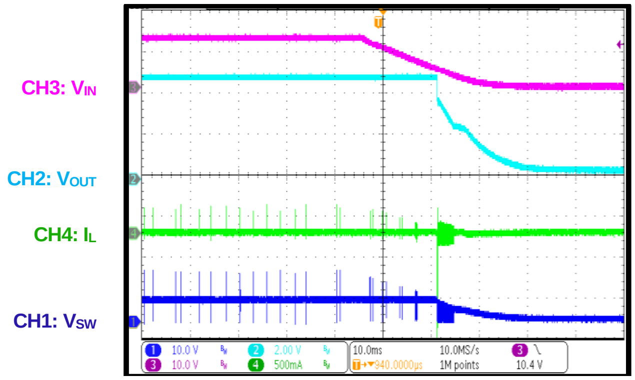


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 2.2µH, f_{SW} = 2.2MHz, AAM mode, T_A = 25°C, unless otherwise noted.

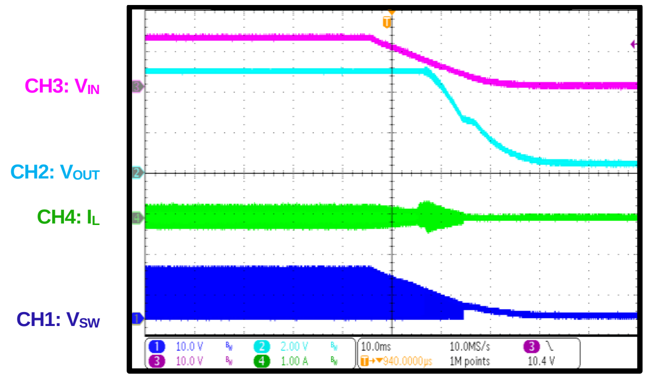
Shutdown through VIN

I_{OUT} = 0A, AAM mode



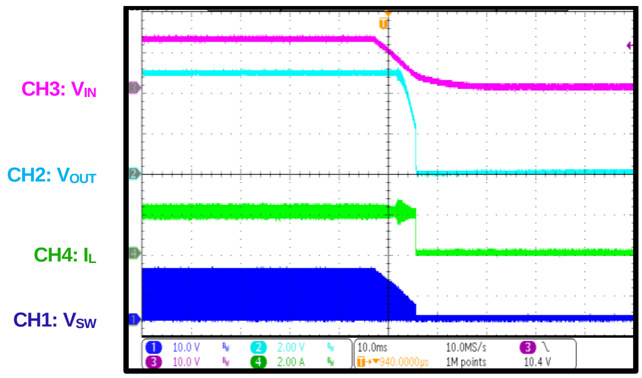
Shutdown through VIN

I_{OUT} = 0A, FCCM



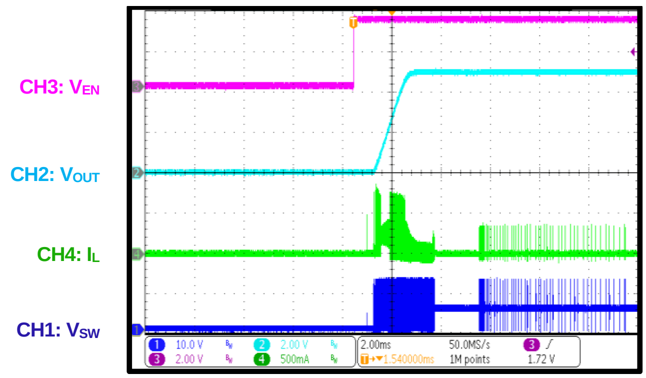
Shutdown through VIN

I_{OUT} = 2A



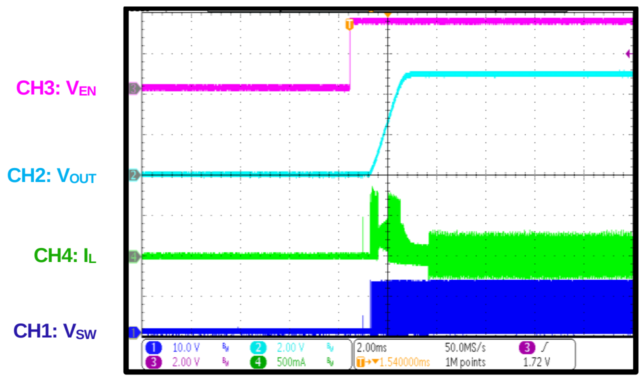
Start-Up through EN

I_{OUT} = 0A, AAM mode



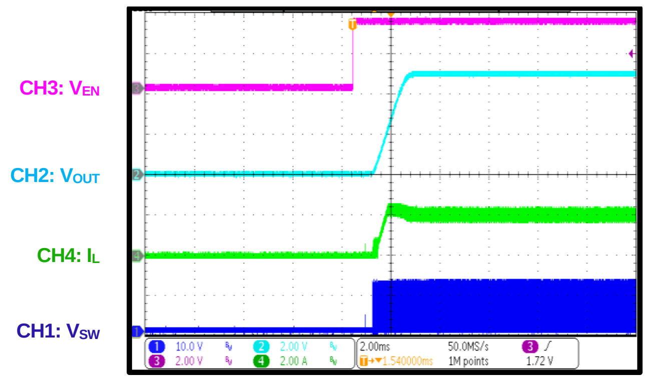
Start-Up through EN

I_{OUT} = 0A, FCCM



Start-Up through EN

I_{OUT} = 2A

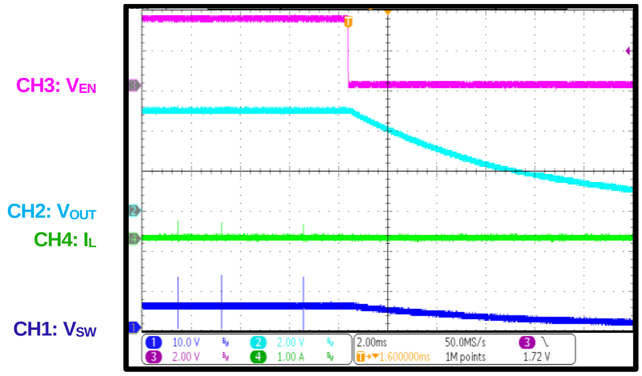


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 2.2µH, f_{SW} = 2.2MHz, AAM mode, T_A = 25°C, unless otherwise noted.

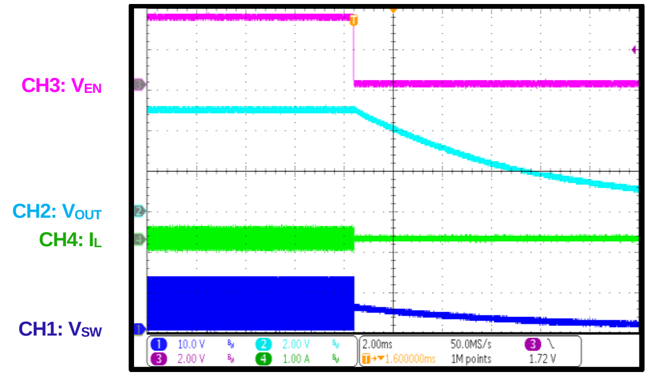
Shutdown through EN

I_{OUT} = 0A, AAM mode



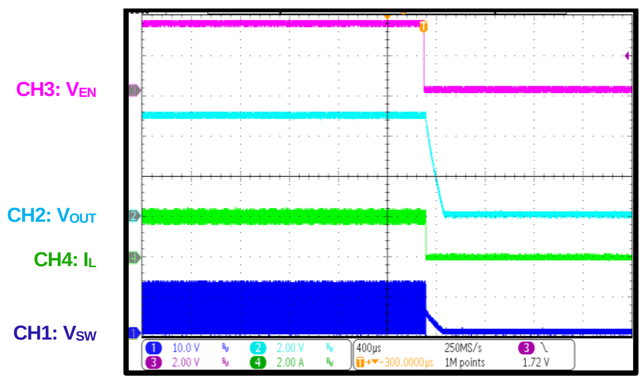
Shutdown through EN

I_{OUT} = 0A, FCCM



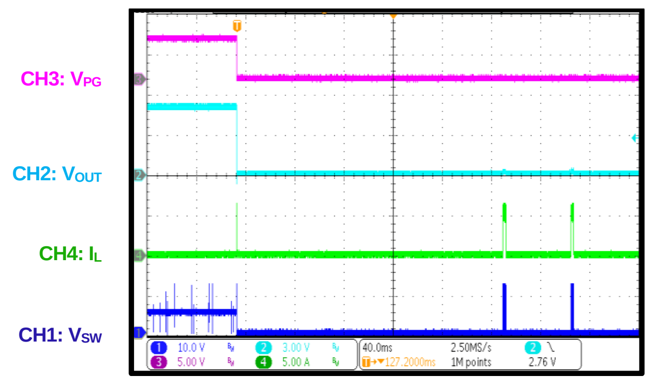
Shutdown through EN

I_{OUT} = 2A



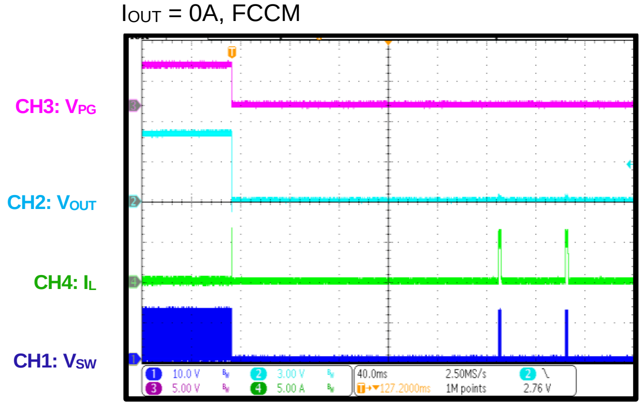
SCP Entry

I_{OUT} = 0A, AAM mode



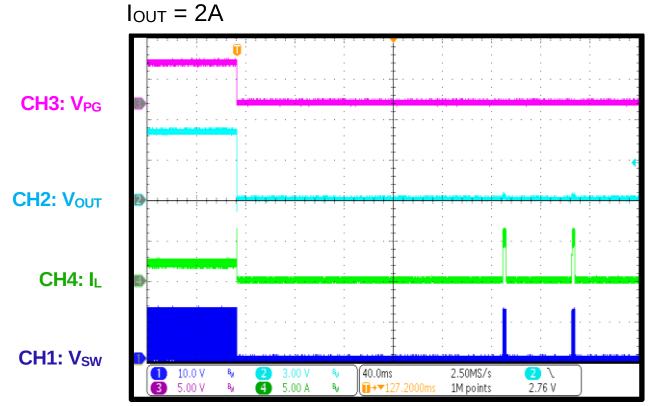
SCP Entry

I_{OUT} = 0A, FCCM



SCP Entry

I_{OUT} = 2A

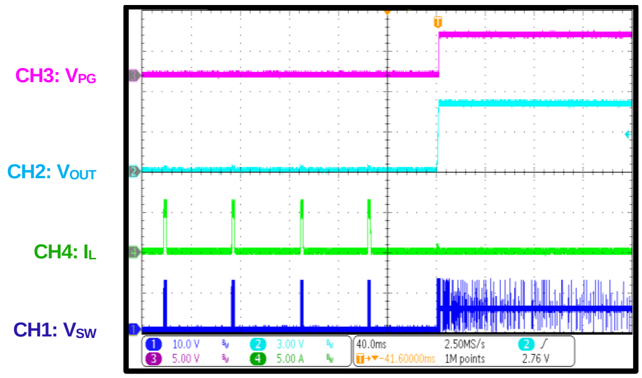


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 2.2µH, f_{SW} = 2.2MHz, AAM mode, T_A = 25°C, unless otherwise noted.

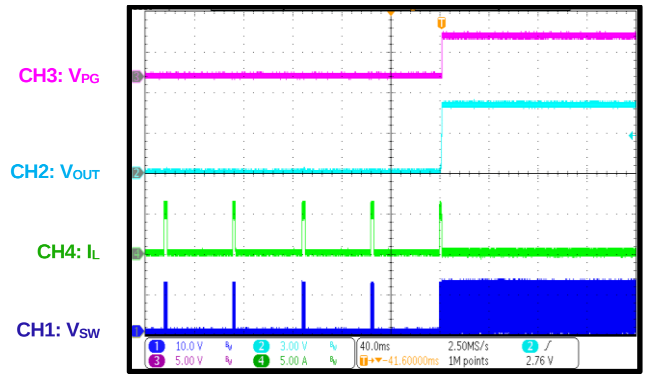
SCP Recovery

I_{OUT} = 0A, AAM mode



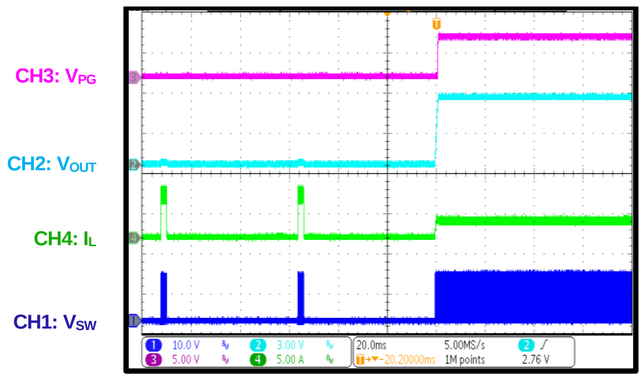
SCP Recovery

I_{OUT} = 0A, FCCM

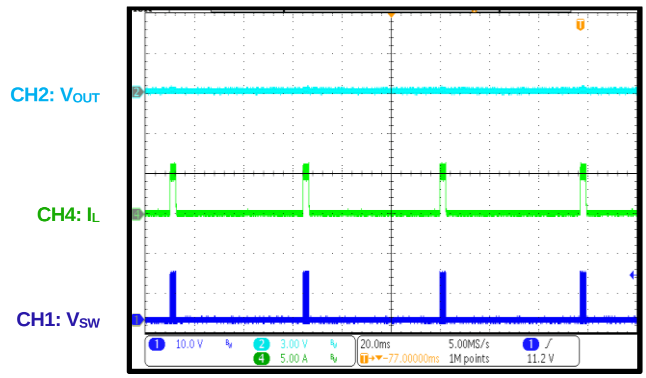


SCP Recovery

I_{OUT} = 2A

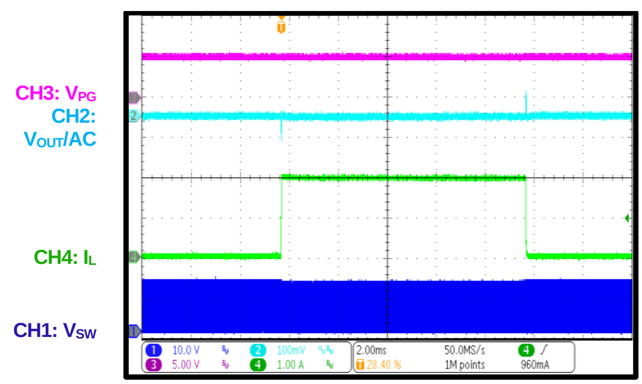


SCP Steady State



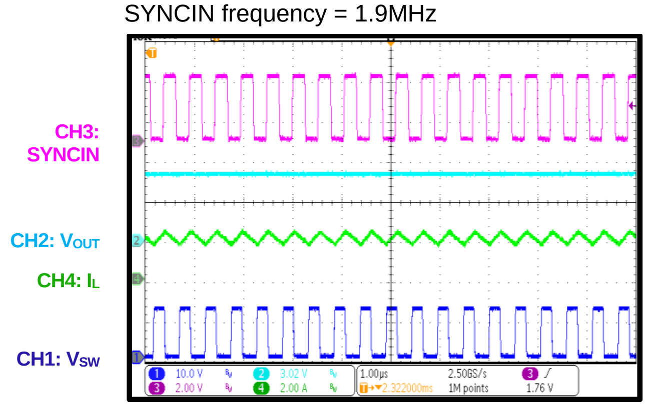
Load Transient

I_{OUT} = 0A to 2A, 1.6A/µs



SYNCIN Operation

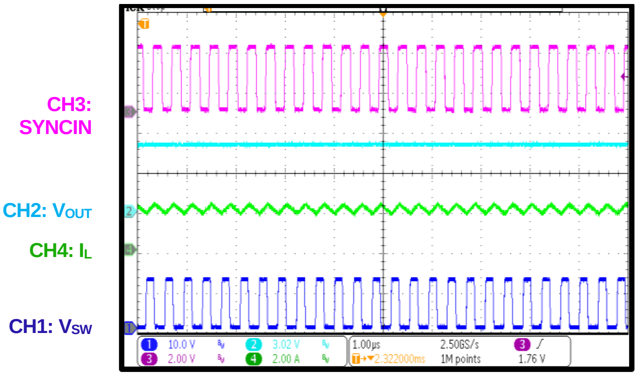
I_{OUT} = 2A, f_{SW} = 2.2MHz,
SYNCIN frequency = 1.9MHz



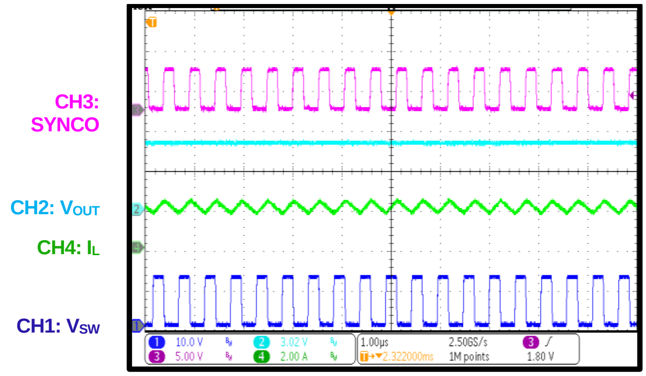
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 2.2µH, f_{SW} = 2.2MHz, AAM mode, T_A = 25°C, unless otherwise noted.

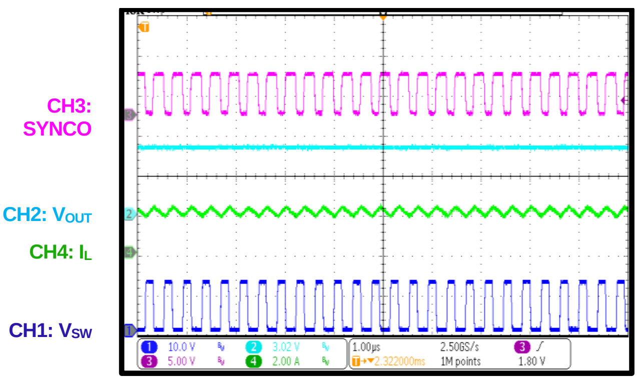
SYNCIN Operation
I_{OUT} = 2A, f_{SW} = 2.2MHz,
SYNCIN frequency = 2.6MHz



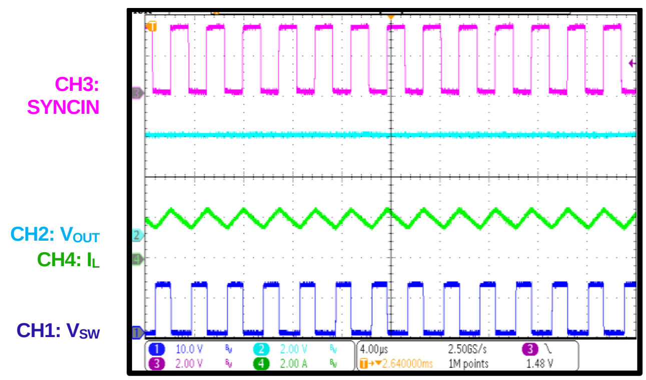
SYNCO Operation
I_{OUT} = 2A, f_{SW} = 2.2MHz,
SYNCIN frequency = 1.9MHz



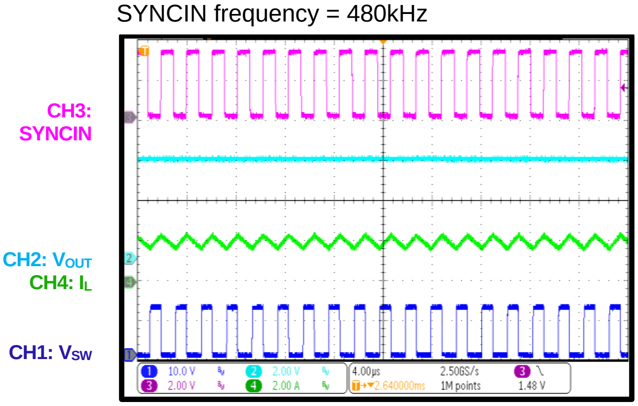
SYNCO Operation
I_{OUT} = 2A, f_{SW} = 2.2MHz,
SYNCIN frequency = 2.6MHz



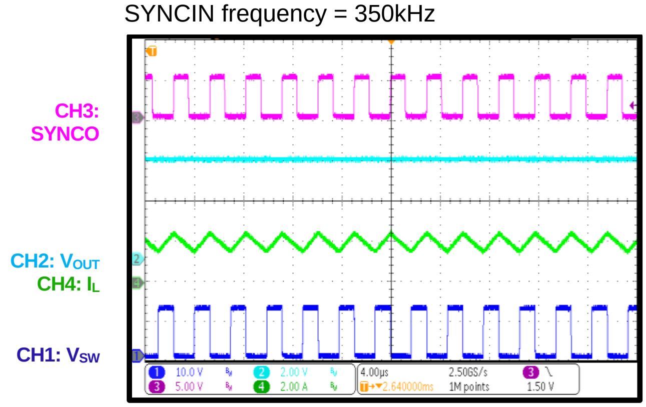
SYNCIN Operation
I_{OUT} = 2A, f_{SW} = 410kHz, L = 10µH,
SYNCIN frequency = 350kHz



SYNCIN Operation
I_{OUT} = 2A, f_{SW} = 410kHz, L = 10µH,
SYNCIN frequency = 480kHz



SYNCO Operation
I_{OUT} = 2A, f_{SW} = 410kHz, L = 10µH,
SYNCIN frequency = 350kHz

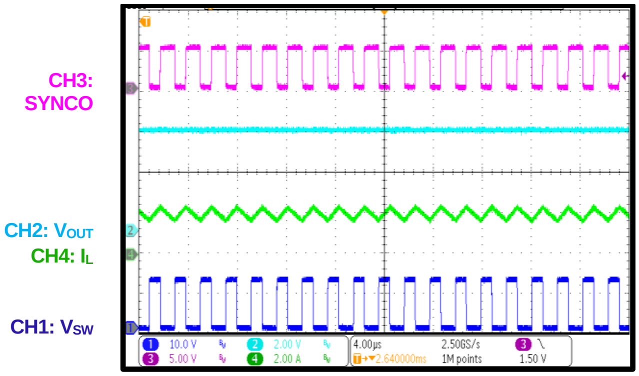


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 2.2µH, f_{SW} = 2.2MHz, AAM mode, T_A = 25°C, unless otherwise noted.

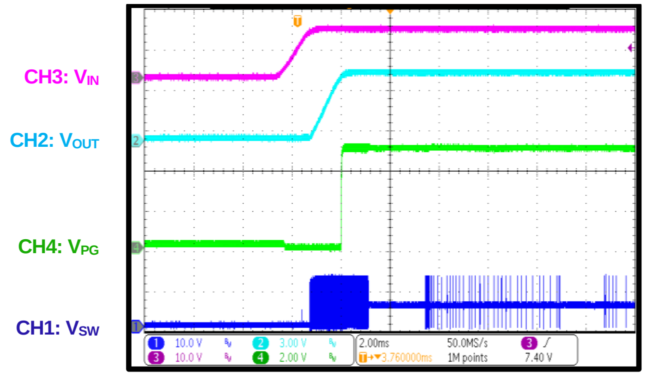
SYNCO Operation

I_{OUT} = 2A, f_{SW} = 410kHz, L = 10µH,
SYNCIN frequency = 480kHz



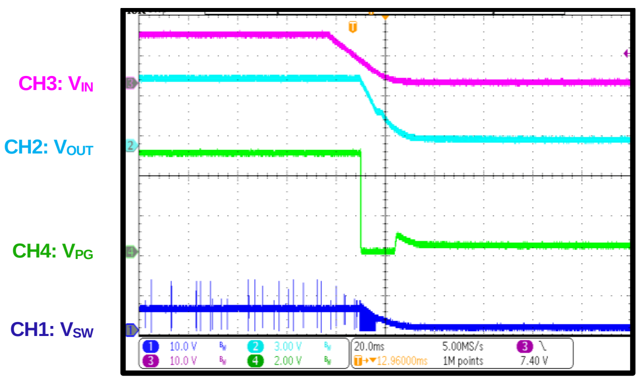
PG Start-Up through VIN

I_{OUT} = 0A, AAM mode



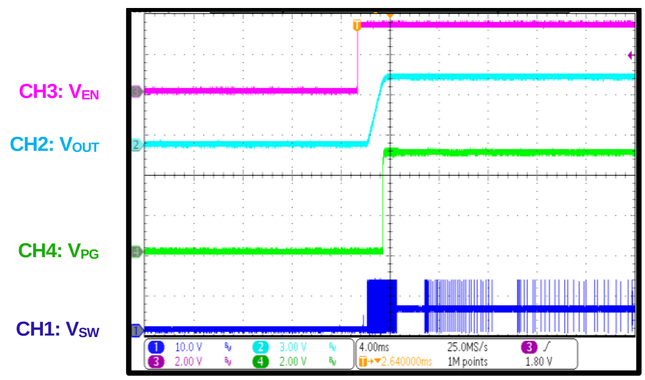
PG Shutdown through VIN

I_{OUT} = 0A, AAM mode



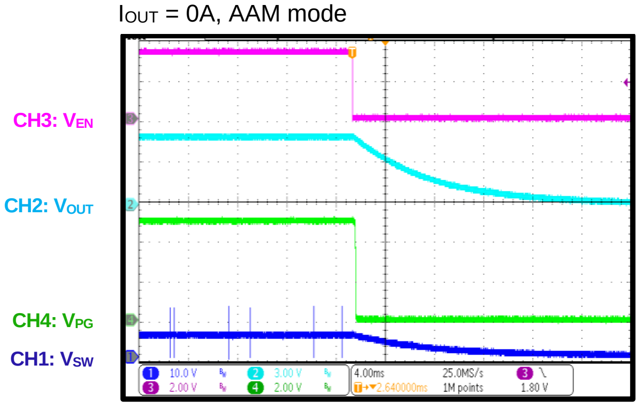
PG Start-Up through EN

I_{OUT} = 0A, AAM mode



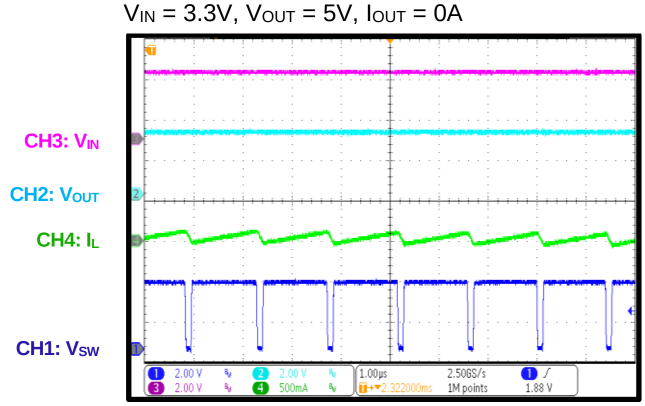
PG Shutdown through EN

I_{OUT} = 0A, AAM mode



Low-Dropout Mode

V_{IN} = 3.3V, V_{OUT} = 5V, I_{OUT} = 0A

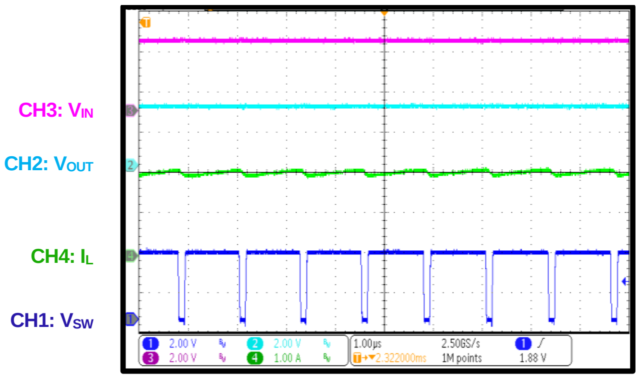


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 2.2µH, f_{SW} = 2.2MHz, AAM mode, T_A = 25°C, unless otherwise noted.

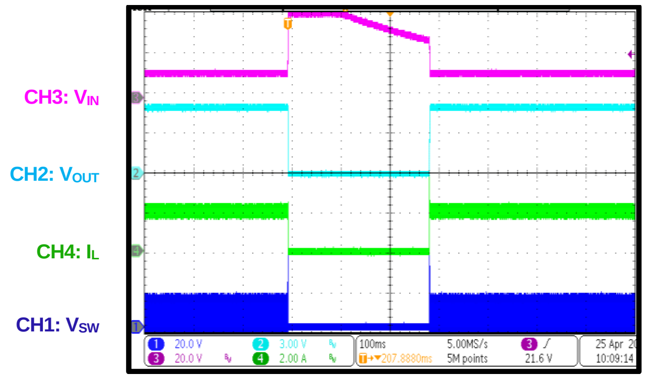
Low-Dropout Mode

V_{IN} = 3.3V, V_{OUT} = 5V, I_{OUT} = 2A



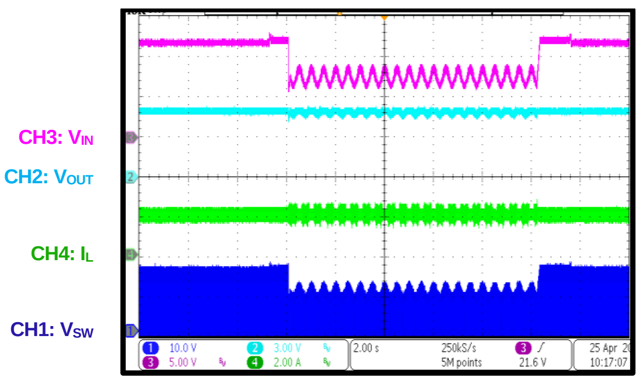
Load Dump

V_{IN} = 12V to 42V, I_{OUT} = 2A



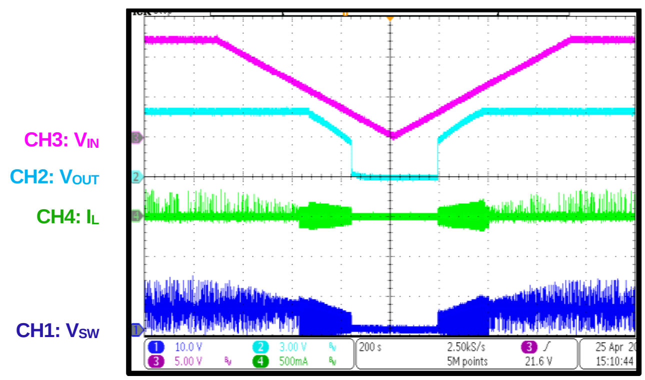
Cold Crank

I_{OUT} = 2A



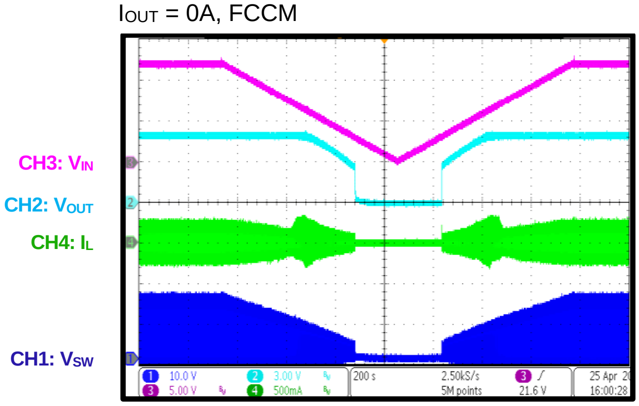
V_{IN} Ramping Up and Down

I_{OUT} = 0A, AAM mode



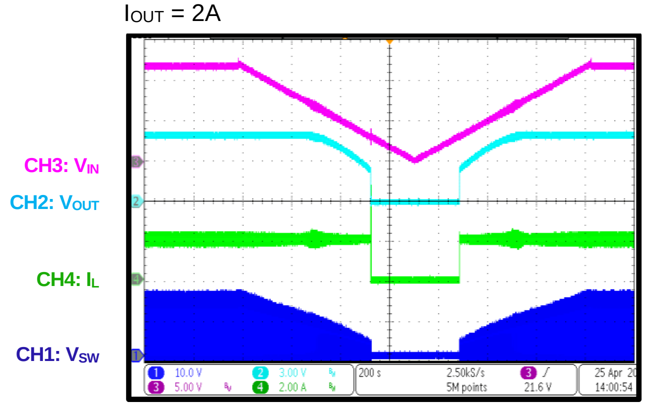
V_{IN} Ramping Up and Down

I_{OUT} = 0A, FCCM



V_{IN} Ramping Up and Down

I_{OUT} = 2A



FUNCTIONAL BLOCK DIAGRAM

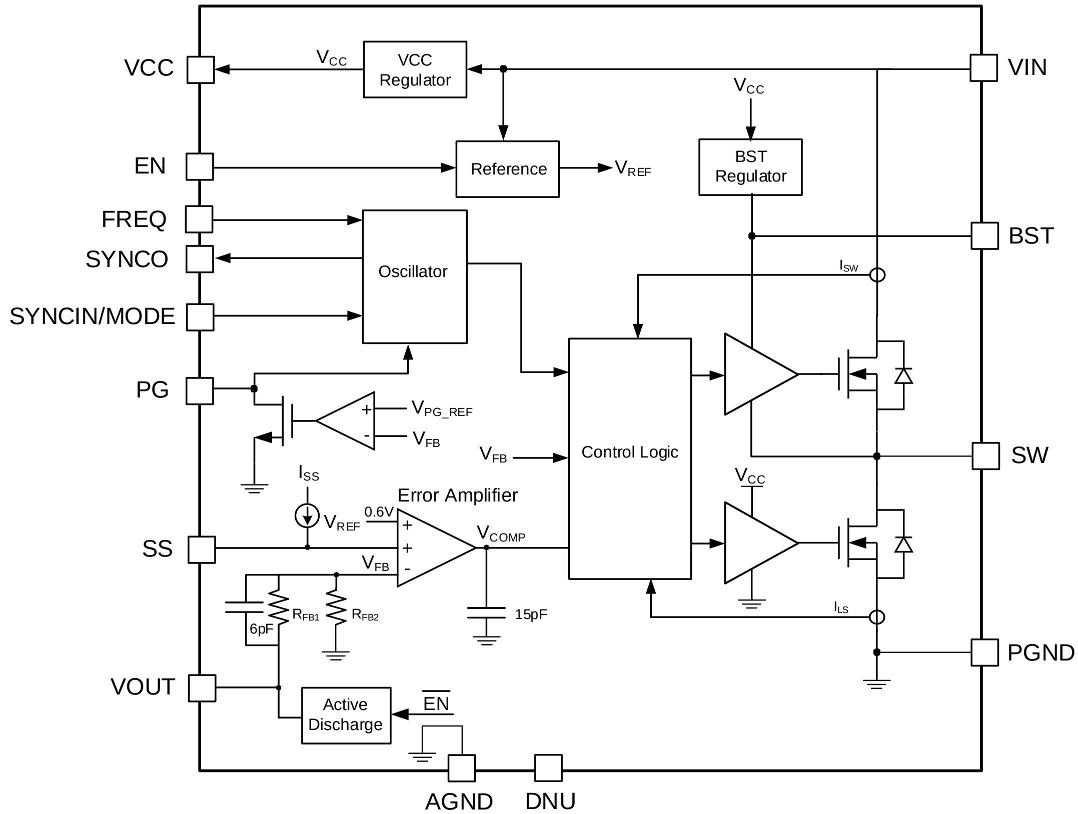


Figure 1: Functional Block Diagram

OPERATION

The MPQ4345/4345J is a synchronous, step-down switching regulator with an integrated internal high-side MOSFET (HS-FET) and low-side MOSFET (LS-FET). It provides up to 2A of highly efficient output current (I_{OUT}) with fixed-frequency, zero-delay pulse-width modulation (PWM) control.

The MPQ4345/4345J features a wide input voltage (V_{IN}) range, configurable 350kHz to 2.5MHz switching frequency (f_{SW}), external soft start (SS), and precision current limit. Its very low operational quiescent current (I_Q) makes the MPQ4345/4345J well-suited for battery-powered applications.

Zero-Delay Pulse-Width Modulation (PWM) Control

Automotive applications typically require fixed-frequency operation to reduce EMI, but traditional fixed-frequency control topologies have major limitations. Voltage mode is difficult to compensate for in automotive environments, while peak current mode control cannot always keep up with stringent, modern system-on-chip (SoC) transient requirements without excessive output capacitance. With these requirements in mind, the MPQ4345/4345J introduces fixed-frequency, zero-delay PWM control.

Zero-delay PWM control combines current information with hysteretic-style output voltage (V_{OUT}) control in a clocked system. This provides a near optimal transient response while maintaining a high phase margin across a wide variety of operating conditions and external component values. In addition, zero-delay PWM control maintains superior EMI performance. The improved transient response reduces output capacitor requirements and lowers the system cost. Trailing-edge modulation facilitates a narrow minimum on time (t_{ON_MIN}) for high conversion ratio applications.

At the beginning of the PWM cycle, the HS-FET turns off and the LS-FET turns on immediately, then remains on until the control signal reaches the COMP voltage (V_{COMP}). HS-FET remains off for at least 120ns at the beginning of the cycle.

Light-Load Operation

At moderate-to-high output currents, the MPQ4345/4345J operates at a fixed frequency. Under light-load conditions, the MPQ4345/4345J can work in two different operation modes by setting the state of the SYNCIN/MODE pin.

If the SYNCIN/MODE pin is pulled above 1.8V or an external clock is used, then the MPQ4345/4345J works in forced continuous conduction mode (FCCM). In FCCM, the device works with a fixed frequency from no-load to full-load conditions. The part has a -4A reverse current limit to prevent the negative current from dropping too low and potentially damaging the components. Once the negative inductor current (I_L) reaches the reverse current limit, the LS-FET immediately turns off and the HS-FET turns on. The advantage of FCCM is the constant frequency and lower output ripple under light loads.

If the SYNCIN/MODE pin is pulled below 0.4V, then the MPQ4345/4345J works in advanced asynchronous modulation (AAM) mode. The device cannot enter AAM mode until SS completes. AAM mode optimizes efficiency under light-load and no-load conditions.

During AAM mode, the LS-FET emulates a diode, and the HS-FET has a fixed one-shot on time to charge the inductor and regulate the output. As the load decreases, the interval between one-shots increases. When this interval exceeds 8µs, the part enters sleep mode, which turns off some internal circuits and extends the on time to achieve an ultra-low I_Q.

When the load increases, and the interval decreases to be shorter than 6µs, the part exits sleep mode and enters AAM mode again. In AAM mode, the device employs a zero-current detection (ZCD) circuit to turn off the LS-FET and prevent negative I_L flow under light loads. The device exits AAM mode if the MODE pin goes high. If a fault occurs in sleep mode, such as an over-voltage (OV) or over-temperature (OT) fault, the internal circuits are not disabled.

Frequency Spread Spectrum (FSS)

The MPQ4345/4345J uses a 12kHz modulation frequency with a fixed, 128-step triangular profile to spread the internal f_{SW} across a 20% (±10%) window. The absolute frequency step size varies proportionally with f_{SW} to maintain the ±10% frequency spread (see Figure 2).

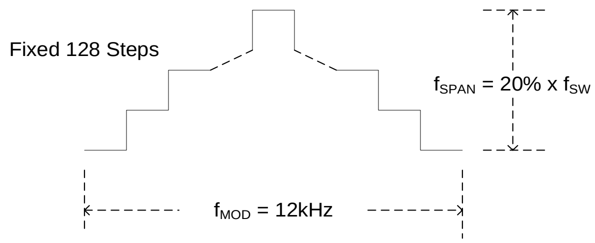


Figure 2: Frequency Spread Spectrum

Sidebands are created by modulating f_{SW} with the triangle modulation waveform. The emission power of the fundamental f_{SW} and its harmonics is distributed into smaller pieces. This significantly reduces peak EMI noise.

Low-Dropout (LDO) Mode

When V_{IN} drops to about 7V, the MPQ4345/4345J folds back the frequency. Once V_{IN} is almost equal to V_{OUT}, the device enters low-dropout (LDO) mode. This allows for a shorter off time to achieve higher duty cycle.

The effective duty cycle during the regulator's dropout period is mainly influenced by the voltage drops across the power MOSFET, the inductor resistance, the LS-FET diode, and the PCB resistance.

Start-Up and Shutdown

If both V_{IN} and EN exceed their respective thresholds, the device starts up. The reference block starts first, generating a stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries.

While the internal supply rail is up, an internal timer holds the power MOSFET off for about 50µs to blank any start-up glitches. When the SS block is enabled, it first holds its SS output low to ensure the remaining circuits are ready. Then the SS block slowly ramps up.

Three events shut down the chip: EN going low, V_{IN} going low, and thermal shutdown. During shutdown, the signaling path is blocked first to avoid any fault triggering. Then V_{COMP} and the internal supply rail are pulled down. The floating driver is not subject to this shutdown command, but its charging path is disabled.

SYNCIN and SYNCO

f_{SW} can be synchronized to the rising edge of a clock signal applied to the SYNCIN/MODE pin. The recommended SYNCIN frequency range is 90% to 115% of f_{SW}.

The SYNCO pin can output a clock signal in phase with the internal oscillator signal (inverter to switching clock) or the external SYNCIN frequency.

Thermal Shutdown

Thermal shutdown is implemented to prevent the chip from thermal runaway. If the silicon die temperature exceeds its upper 170°C threshold, the power MOSFETs shut down. Once the temperature drops below its lower threshold (150°C), the thermal shutdown condition is removed and the chip starts up again.

APPLICATION INFORMATION

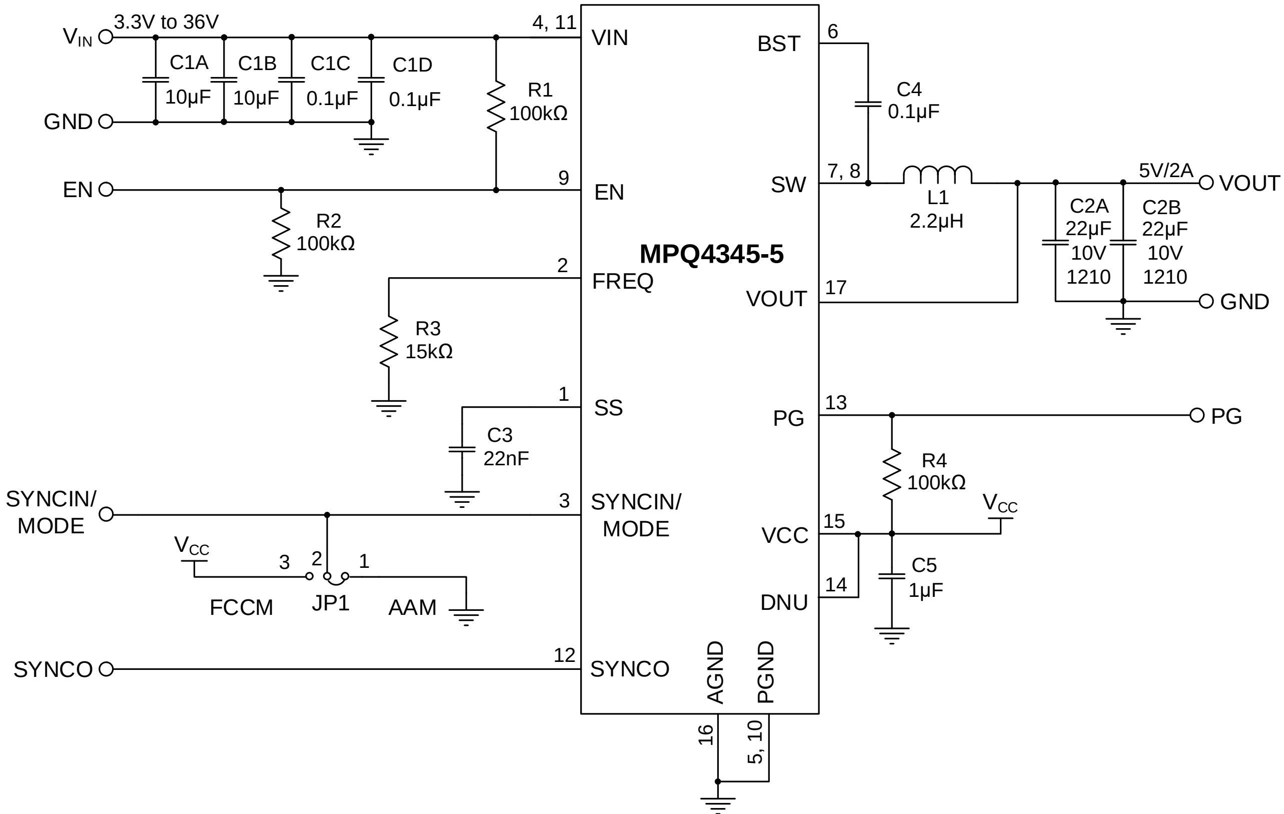


Figure 3: Typical Application Circuit for the MPQ4345GLE-5 (V_{OUT} = 5V, f_{SW} = 2.2MHz)

Table 1: Design Guide Index

Pin #	Pin Name	Component	Design Guide Index
1	SS	C3	Selecting the Soft-Start Capacitor (SS, Pin 1)
2	FREQ	R3	Setting the Switching Frequency (f_{SW}) (FREQ, Pin 2)
3	SYNCIN/MODE	-	SYNC Input and MODE Selection (SYNCIN/MODE, Pin 3)
4, 11	VIN	C1A, C1B, C1C, C1D	Selecting the Input Capacitors (VIN, Pins 4 and 11)
5, 10	PGND	-	Connection to GND (GND, Pins 5, 10, and 16)
6	BST	C4	Bootstrap Charging (BST, Pin 6)
7,8	SW	L1, C2A, C2B	Selecting the Inductor; Selecting the Output Capacitors (SW, Pins 7 and 8)
9	EN	R1, R2	Enable (EN, Pin 9) and V_{IN} Under-Voltage Lockout (UVLO)
12	SYNCO	-	SYNCO (Pin 12)
13	PG	R4	Power Good (PG) Indicator (PG, Pin 13)
14	DNU	-	DNU (Pin 14)
15	VCC	C5	Input Bias Supply (VCC, Pin 15)
16	AGND	-	Connection to GND (GND, Pins 5,10, and 16)
17	VOUT	-	VOUT (Pin 17)

Selecting the Soft-Start Capacitor (SS, Pin 1)

Soft start (SS) is implemented to prevent the converter's V_{OUT} from overshooting during start-up.

When SS begins, an internal current source begins charging the external SS capacitor (C_{SS}). When the SS voltage (V_{SS}) is below the internal reference voltage (V_{REF}), V_{SS} overrides V_{REF}, so the error amplifier (EA) uses V_{SS} as the reference. When V_{SS} exceeds V_{REF}, V_{REF} regains control.

C_{SS} can be calculated with Equation (1):

$$C_{SS}(nF) = \frac{t_{SS}(ms) \times I_{SS}(\mu A)}{V_{REF}(V)} = 16.6 \times t_{SS}(ms) \quad (1)$$

The SS pin can be used for tracking and sequencing.

Setting the Switching Frequency (f_{SW}) (FREQ, Pin 2)

f_{SW} can be configured by an external resistor connected from the FREQ pin to ground, placed as close to the device as possible.

The resistance that sets f_{SW} (R3) can be selected using the f_{SW} vs R_{FREQ} curves. Figure 4 shows the f_{SW} vs. R_{FREQ} curve when f_{SW} is between 1000kHz and 2500kHz.

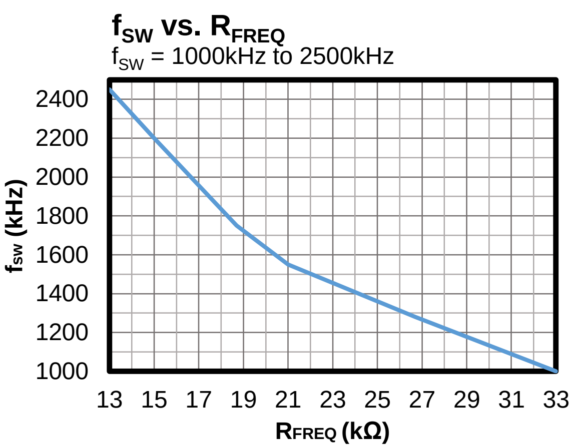


Figure 4: f_{SW} vs. R_{FREQ}

Figure 5 shows the f_{SW} vs. R_{FREQ} curve when f_{SW} is between 350kHz and 1000kHz.

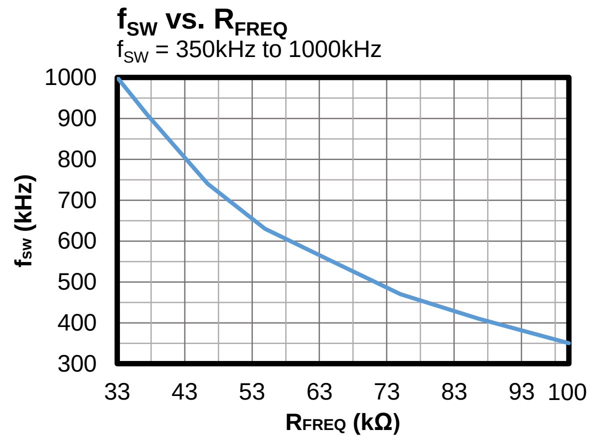


Figure 5: f_{SW} vs. R_{FREQ}

Table 2 shows some common f_{SW} and R_{FREQ} values when selecting f_{SW}.

Table 2: f_{SW} vs. R_{FREQ}

R_{FREQ} (kΩ)	f_{SW} (kHz)
100	350
86.6	410
75	470
64.9	550
54.9	630
46.4	740
37.4	910
33	1050
26.7	1280
21	1550
18.7	1750
15	2200
13	2450

SYNC Input and MODE Selection (SYNCIN/MODE, Pin 3)

When the SYNCIN/MODE pin is used as the SYNC input pin (SYNCIN), f_{SW} can be synchronized to the rising edge of a clock signal applied to SYNCIN/MODE. The recommended SYNCIN frequency range is 90% to 115% of f_{SW}.

When SYNCIN/MODE is used for mode selection (MODE), pulling this pin high allows the device to operate in FCCM, while pulling it low allows the device to operate in AAM mode (see Table 3 on page 37).

Table 3: Mode Selection

SYNCIN/MODE Input	Operation Mode
<0.4V	AAM mode
>1.8V	FCCM
External clock in	FCCM

Selecting the Input Capacitor (VIN, Pins 4 and 11)

The step-down converter has a discontinuous input current, and requires a capacitor to supply AC current to the converter while maintaining the DC V_{IN}. For the best performance, use low-ESR capacitors. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients.

For most applications, it is recommended to use a 4.7µF to 10µF capacitor. It is strongly recommended to use another, lower-value capacitor (e.g. 0.1µF) with a small package size (0603) to absorb high-frequency switching noise. Place the smaller capacitor as close to VIN and GND as possible.

Since the input capacitor (C_{IN}) absorbs the input switching current, it requires an adequate ripple current rating. The RMS current for C_{IN} (I_{CIN}) can be estimated with Equation (2):

$$I_{CIN} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (2)$$

The worst-case condition occurs at V_{IN} = 2 x V_{OUT}, which can be calculated with Equation (3):

$$I_{CIN} = \frac{I_{LOAD}}{2} \quad (3)$$

For simplification, choose C_{IN} with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality ceramic capacitor (e.g. 0.1µF) as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent excessive voltage ripple at the input.

The input voltage ripple (ΔV_{IN}) caused by the capacitance can be estimated with Equation (4):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (4)$$

V_{IN} Over-Voltage Protection (OVP)

The MPQ4345/4345J has a built-in V_{IN} over-voltage protection (OVP) circuit. V_{IN} OVP becomes active at 25V. When V_{IN} exceeds the OVP threshold (typically 38V), the LS-FET turns on until I_L is fully discharged, and then switching stops. When V_{IN} drops to the OV falling threshold (typically 28V), and the hiccup restart delay time expires, the device completes a soft-start cycle and resumes normal regulation.

Bootstrap Charging (BST, Pin 6)

The BST capacitor (C4) is recommended to be between 0.1µF and 0.22µF.

It is not recommended to place a resistor (R_{BST}) in series with the BST capacitor (C_{BST}) unless there is a strict EMI requirement. R_{BST} helps enhance EMI performance and reduce voltage stress at high input voltages, but it also increases power consumption and reduces efficiency. When R_{BST} is necessary, it should be below 10Ω.

C_{BST} is charged and regulated to about 5V by the dedicated internal bootstrap regulator. When the voltage between the BST and SW nodes is below its regulation, an N-channel MOSFET pass transistor connected from VCC to BST turns on to charge C_{BST}. The external circuit should provide sufficient voltage headroom to facilitate charging.

When the HS-FET is on, the BST voltage (V_{BST}) exceeds V_{CC}, so C_{BST} cannot be charged.

At higher duty cycles, the time available for bootstrap charging is shorter, so C_{BST} may not be sufficiently charged. If the external circuit has both insufficient voltage and time to charge C_{BST}, use additional external circuitry to ensure V_{BST} remains within the normal operation range.

Selecting the Output Capacitor (SW, Pins 7 and 8)

The output capacitor (C_{OUT}) maintains the DC V_{OUT}. Use ceramic, tantalum, or low-ESR electrolytic capacitors. For the best results, use low-ESR capacitors to keep the output voltage ripple (ΔV_{OUT}) low. ΔV_{OUT} can be estimated with Equation (5):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}) \quad (5)$$

Where L is the inductance, and R_{ESR} is the equivalent series resistance (ESR) value of C_{OUT}.

For ceramic capacitors, the capacitance dominates the impedance at f_{SW} and causes the majority of ΔV_{OUT}. For simplification, ΔV_{OUT} can be estimated with Equation (6):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (6)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at f_{SW}. For simplification, ΔV_{OUT} can be estimated with Equation (7):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (7)$$

The C_{OUT} characteristics also affect the stability of the regulation system. The part can be optimized for a wide range of capacitances and ESR values.

Selecting the Inductor

A 1µH to 10µH inductor with a DC current rating at least 25% greater than the maximum load current is recommended for most applications. For higher efficiency, choose an inductor with a lower DC resistance. A larger-value inductor results in less ripple current and a lower ΔV_{OUT}; however, it also has a larger physical size, higher series resistance, and lower saturation current. A good rule for determining the inductance is to allow the inductor ripple current to be approximately 30% of the maximum load current. The inductance (L) can be calculated with Equation (8):

$$L = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (8)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

Choose the inductor ripple current to be approximately 30% of the maximum load current. The maximum peak inductor current (I_{LP}) can be calculated with Equation (9):

$$I_{LP} = I_{LOAD} + \frac{V_{OUT}}{2 f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (9)$$

Peak and Valley Current Limit

Both the HS-FET and LS-FET have cycle-by-cycle current-limit protection. When I_L reaches the high-side peak current limit (typically 5.8A) or the rising edge of the internal clock is reached while the current is rising and the HS-FET is on, the HS-FET is forced off immediately to prevent the current from rising further. When the LS-FET is on, the valley current limit circuit blocks the PWM from turning on the HS-FET until I_L is below the low-side valley current limit (typically 4.4A). This current limit scheme prevents current runaway if an overload or short-circuit event occurs.

Short-Circuit Protection (SCP)

If the output is shorted to ground, V_{OUT} drops below 70% of its nominal output, and the LS-FET current exceeds the 4.4A valley current limit, then the device turns on the LS-FET until I_L is fully discharged. The device also begins slowly discharging C_{SS}. The device restarts with a full SS when C_{SS} is fully discharged. This hiccup process repeats until the fault is removed.

Output Over-Voltage Protection (OVP) and Discharge

There is an internal V_{OUT} OVP circuit. When the device is operating in discontinuous conduction mode (DCM) and V_{OUT} exceeds 106% of the target voltage, an output discharge path from VOUT to GND is activated to discharge V_{OUT}. The output discharge path remains activated until the device returns to regulation and switching resumes.

When the device is operating in FCCM and V_{OUT} exceeds 106% of the target voltage, the output discharge path turns on. If the negative current limit is triggered 265 times, the part enters hiccup mode and switching stops. Once V_{OUT} drops to or below 105% of the target value, a new SS cycle resumes. The V_{OUT} discharge path remains on until V_{OUT} reaches its regulated value, and the device begins switching.

Enable (EN, Pin 9) and V_{IN} Under-Voltage Lockout (UVLO)

EN is a digital control pin that turns the regulator on and off.

Enabled by External Logic High/Low Signal

When the EN voltage (V_{EN}) reaches about 0.7V, the VCC supply turns on. When V_{IN} exceeds 2.7V, it provides an accurate reference voltage for the EN threshold. Forcing EN above its 1V rising threshold turns on the device. Driving EN below 0.85V turns off the device.

Configurable V_{IN} Under-Voltage Lockout (UVLO)

When V_{IN} is sufficiently high, the chip can be enabled and disabled via the EN pin. An internal pull-down resistor in this circuit can generate a configurable V_{IN} under-voltage lockout (UVLO) and hysteresis.

The device requires a higher voltage (≥3.3V) for V_{IN} to directly start up. The part has an internal, fixed UVLO threshold. The rising threshold is 3V, while the falling threshold is about 2.8V. For applications that require a higher UVLO point, an external resistor divider placed between VIN and EN can raise the equivalent UVLO threshold (see Figure 6).

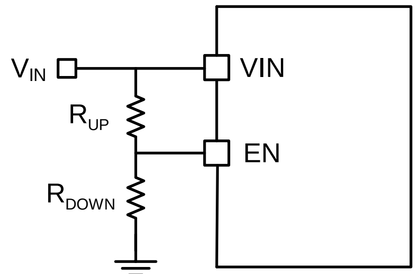


Figure 6: Adjustable UVLO Using EN Divider

The UVLO rising threshold ($V_{IN\_UVLO\_RISING}$) can be calculated with Equation (10):

$$V_{IN\_UVLO\_RISING} = (1 + \frac{R_{UP}}{R_{DOWN}}) \times V_{EN\_RISING} \quad (10)$$

The UVLO falling threshold ($V_{IN\_UVLO\_FALLING}$) can be calculated with Equation (11):

$$V_{IN\_UVLO\_FALLING} = (1 + \frac{R_{UP}}{R_{DOWN}}) \times V_{EN\_FALLING} \quad (11)$$

Where V_{EN_RISING} is 1V, and $V_{EN\_FALLING}$ is 0.85V.

SYNCO (Pin 12)

The SYNCO pin outputs a clock signal in phase with the internal oscillator signal or the external SYNCIN clock.

Power Good (PG, Pin 13)

The device includes an open-drain power good (PG) output that indicates whether the regulator's output is within its nominal output range. PG goes high if the V_{OUT} is within 94% to 106% of its nominal voltage; PG goes low if V_{OUT} exceeds 107% or is below 93% of its nominal voltage. Float PG if it is not used. The PG resistance (R_{PG}/R4) is recommended to be about 100kΩ.

DNU (Pin14)

Connect the DNU pin directly to the VCC pin.

Setting the VCC Capacitor (VCC, Pin 15)

Most of the internal circuitry is powered by the internal, 5V VCC regulator. This regulator uses V_{IN} as its input and operates across the full V_{IN} range. When V_{IN} exceeds 5V, V_{CC} is in full regulation. When V_{IN} is below 5V, the output V_{CC} degrades.

The VCC capacitor (C_{VCC}) should have a capacitance at least 10 times greater than the boost capacitor, and at least 1µF nominally. A C_{VCC} greater than 68µF nominal is not recommended.

VOUT (Pin 17)

Because the feedback resistor divider is integrated internally, connect the VOUT pin directly to the output (see Figure 7).

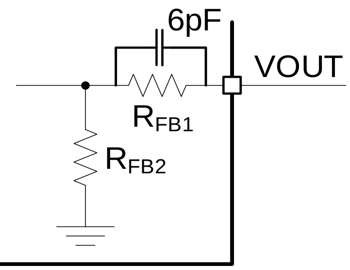


Figure 7: Feedback Divider Network of Fixed-Output Version

The selectable fixed-output options are as follows: 1V, 1.1V, 1.8V, 2.5V, 3V, 3.3V, 3.8V, and 5V.

Table 4 shows the relationship between the internal feedback resistor (R_{FB}) and V_{OUT}.

Table 4: R_{FB} vs. V_{OUT}

V_{OUT} (V)	R_{FB1} (MΩ)	R_{FB2} (MΩ)
1	1.33	2
1.1	1.67	2
1.8	4	2
2.5	6.33	2
3	8	2
3.3	9	2
3.8	10.67	2
5	14.67	2

Connection to GND (GND, Pins 5, 10, and 16)

See the PCB Layout Guidelines section below for more details.

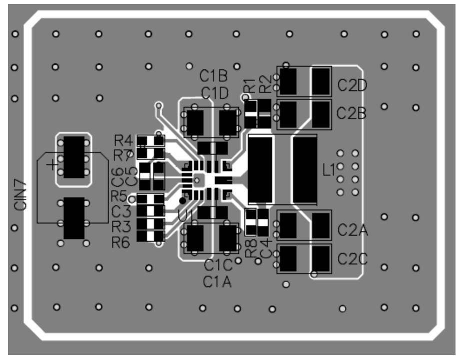
PCB Layout Guidelines [12]

Efficient PCB layout is critical for stable operation. A 4-layer layout is strongly recommended to achieve improved thermal performance. For the best results, refer to Figure 8 and follow the steps below:

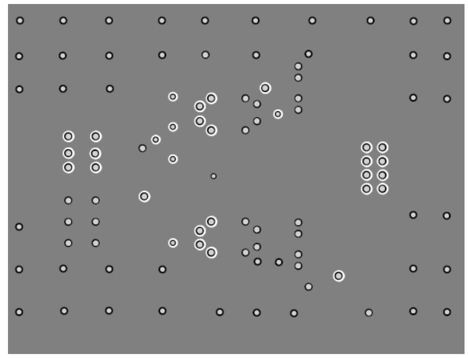
1. Place the symmetric C_{IN} as close to VIN and GND as possible.
2. Use a large ground plane to connect directly to PGND.
3. Add vias near PGND if the bottom layer is a ground plane.
4. Ensure that the high-current paths at GND and VIN have short, direct, and wide traces.
5. Place the ceramic C_{IN}, especially the small package size (0603) input bypass capacitor, as close to VIN and PGND as possible to minimize high-frequency noise.
6. Keep the connection between C_{IN} and VIN as short and wide as possible.
7. Place C_{VCC} as close to VCC and GND as possible.
8. Route SW and BST away from sensitive analog areas, such as FB.
9. Use multiple vias to connect the power planes to the internal layers.

Note:

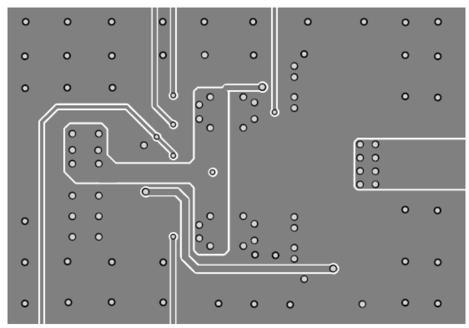
12) The recommended PCB layout is based on Figure 9 on page 41.



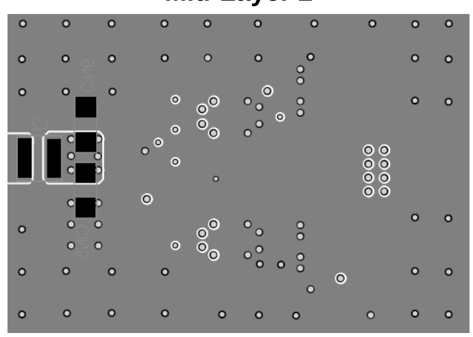
Top Layer



Mid-Layer 1



Mid-Layer 2



Bottom Layer

Figure 8: Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS

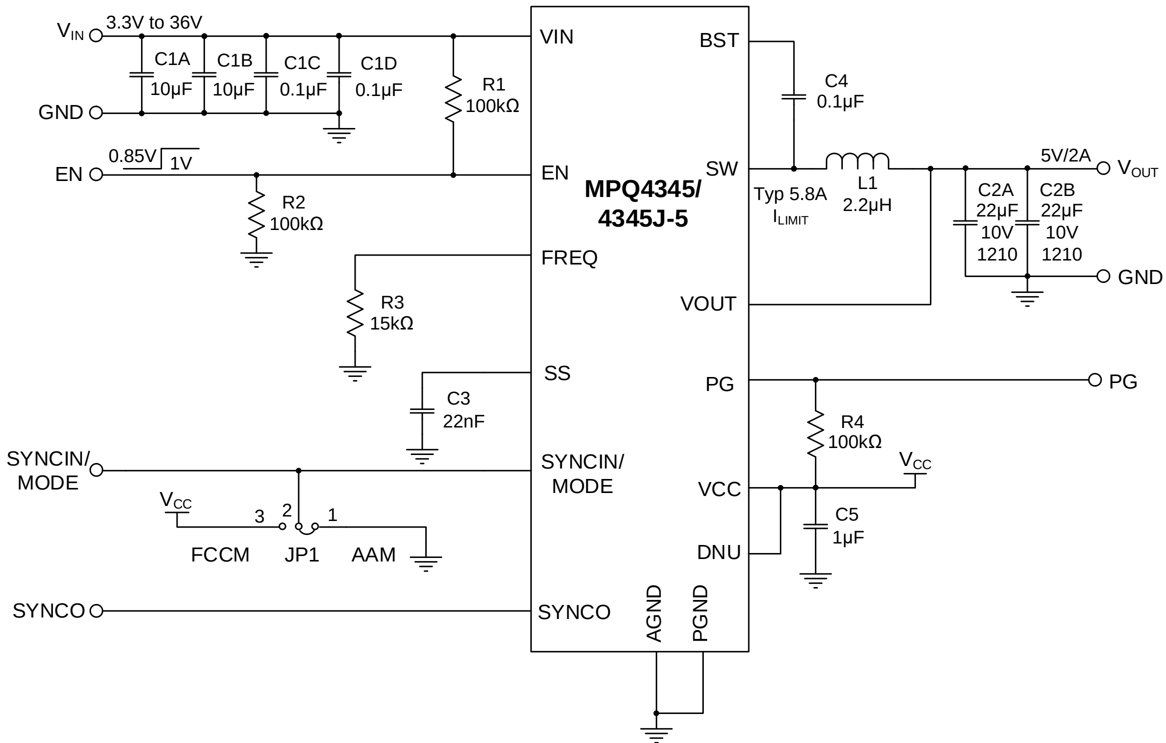


Figure 9: Typical Application Circuit (V_{OUT} = 5V, f_{SW} = 2.2MHz)

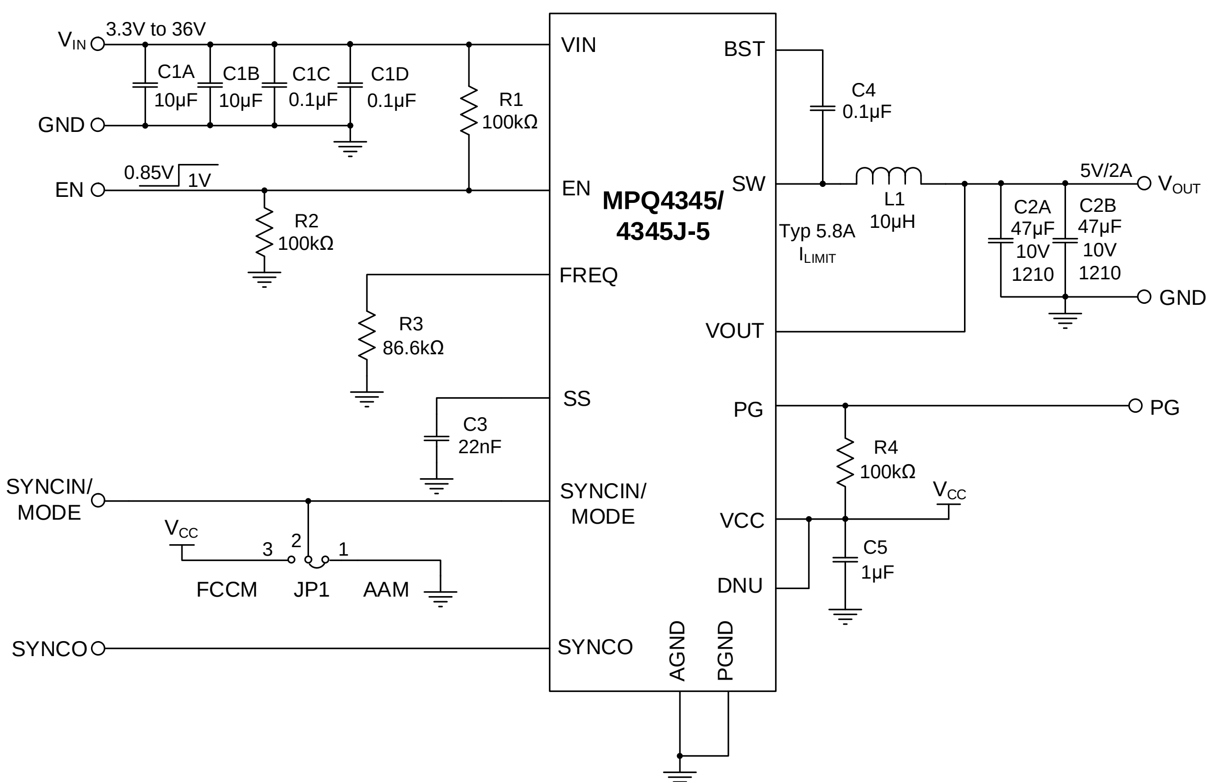


Figure 10: Typical Application Circuit (V_{OUT} = 5V, f_{SW} = 410kHz)

TYPICAL APPLICATION CIRCUITS *(continued)*

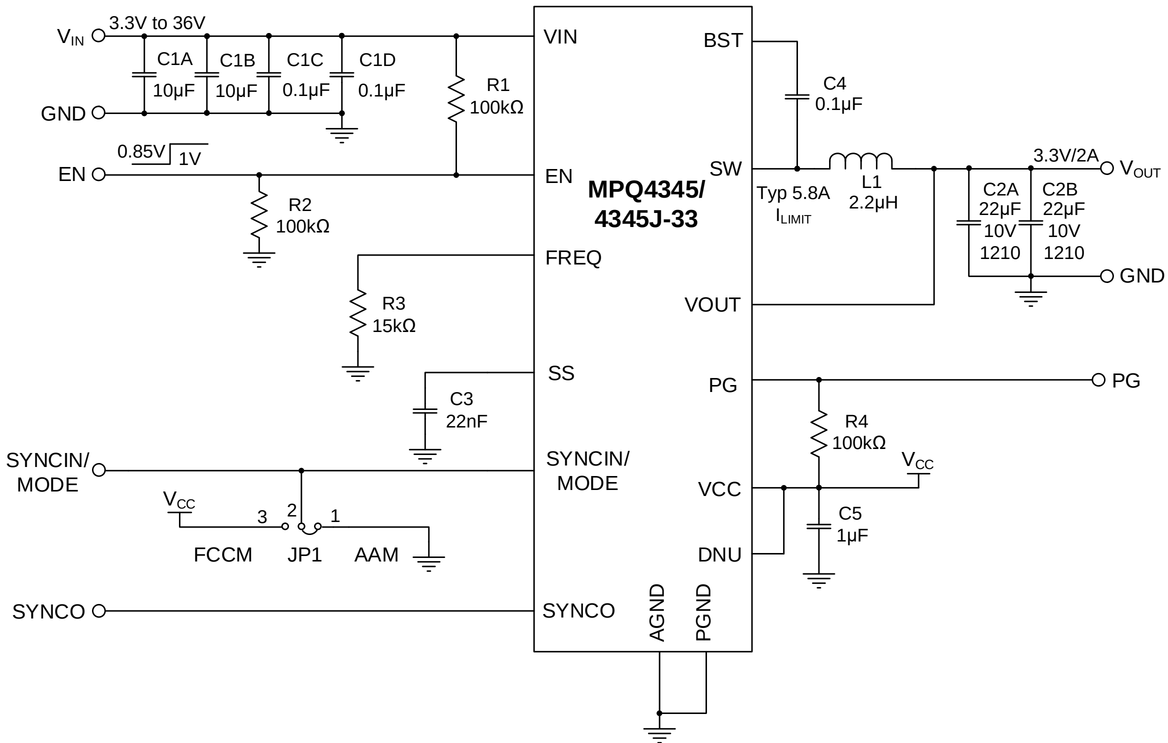


Figure 11: Typical Application Circuit (V_{OUT} = 3.3V, f_{SW} = 2.2MHz)

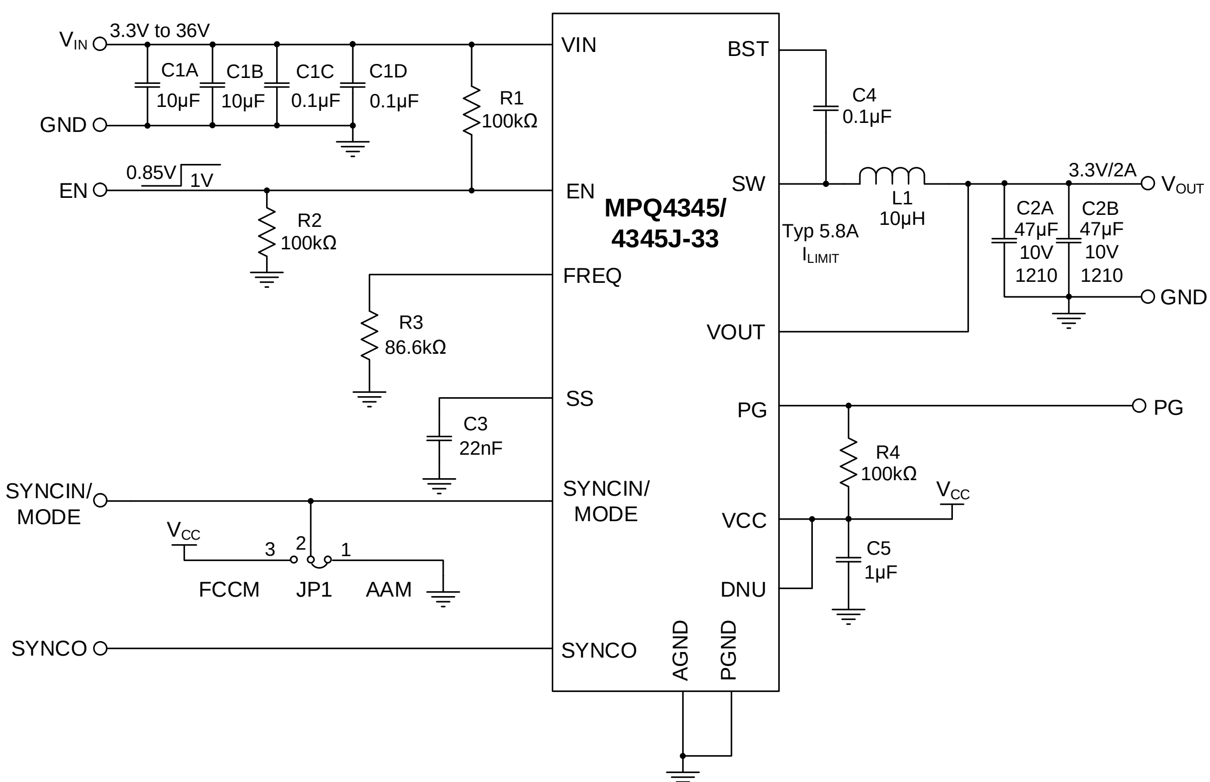


Figure 12: Typical Application Circuit (V_{OUT} = 3.3V, f_{SW} = 410kHz)

TYPICAL APPLICATION CIRCUITS *(continued)*

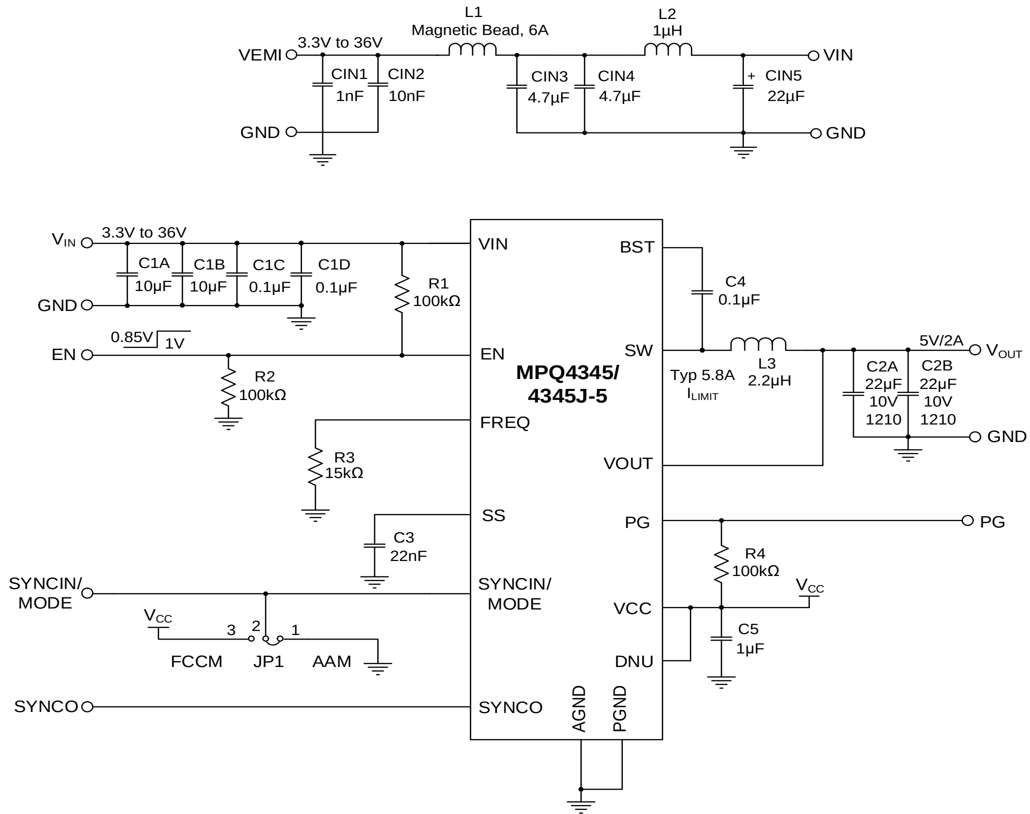


Figure 13: Typical Application Circuit (V_{OUT} = 5V, f_{SW} = 2.2MHz with EMI Filter)

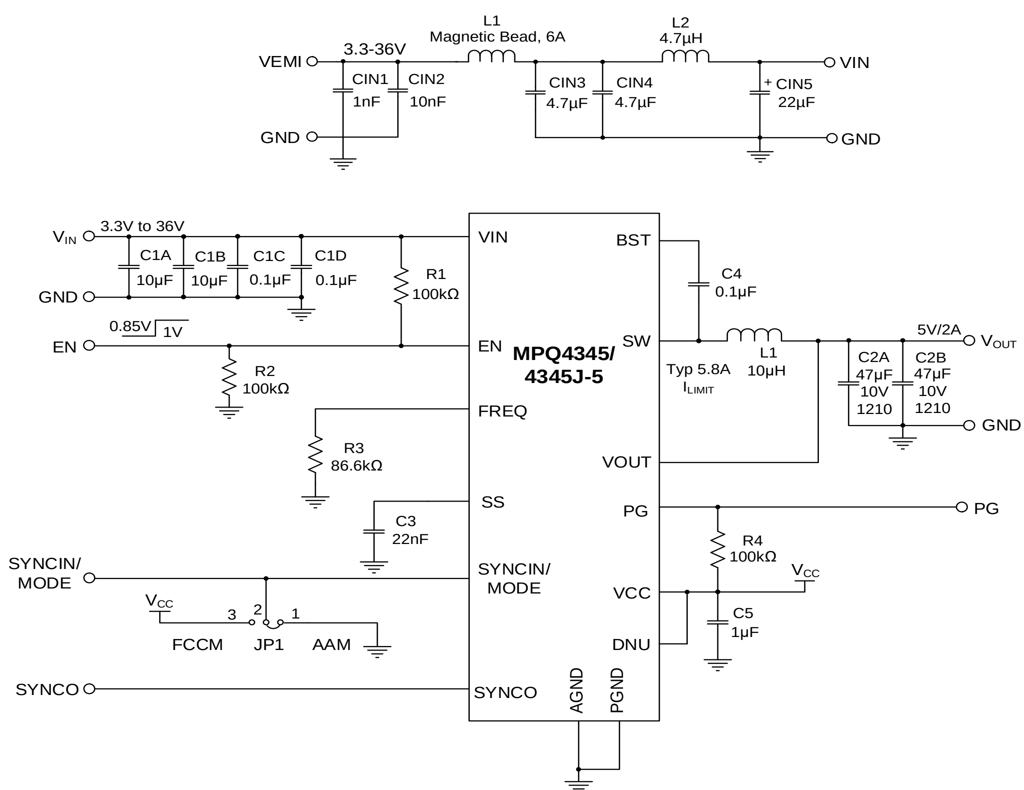
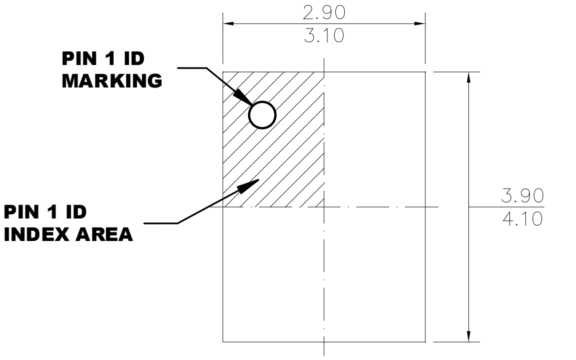


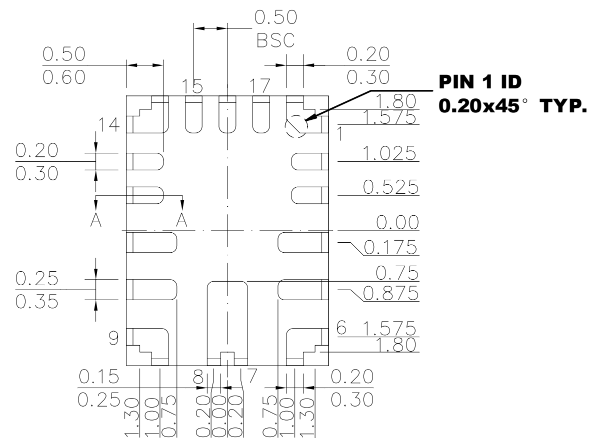
Figure 14: Typical Application Circuit (V_{OUT} = 5V, f_{SW} = 410kHz with EMI Filter)

PACKAGE INFORMATION

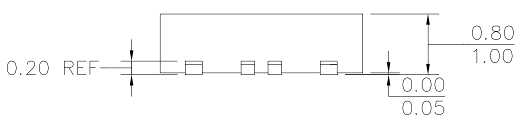
QFN-17 (3mmx4mm)
Wettable Flank



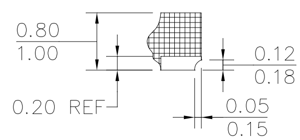
TOP VIEW



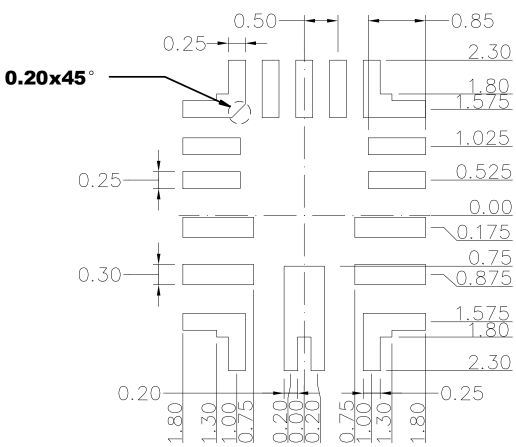
BOTTOM VIEW



SIDE VIEW



SECTION A-A



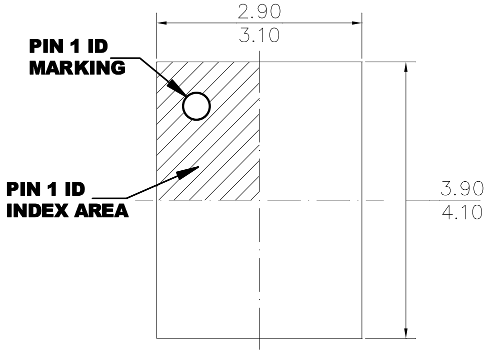
RECOMMENDED LAND PATTERN

NOTE:

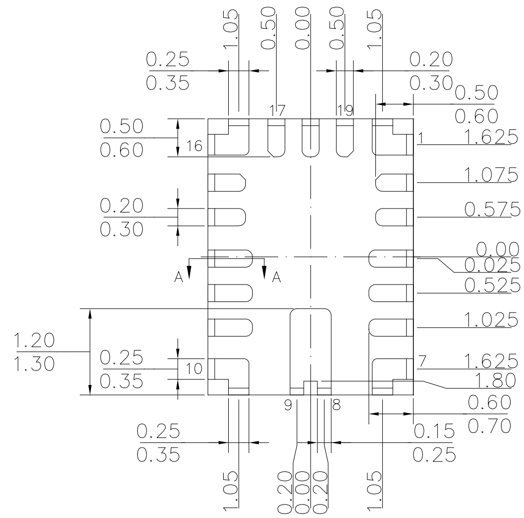
1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

PACKAGE INFORMATION *(continued)*

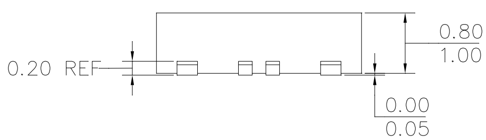
QFN-19 (3mmx4mm)
Wettable Flank



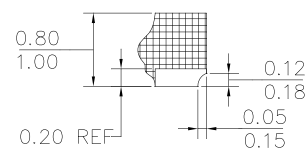
TOP VIEW



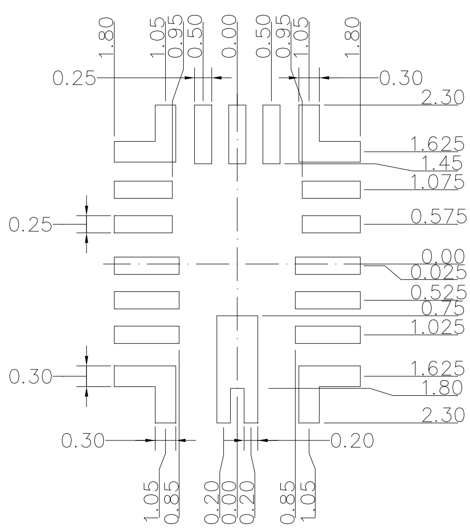
BOTTOM VIEW



SIDE VIEW



SECTION A-A



RECOMMENDED LAND PATTERN

NOTE:

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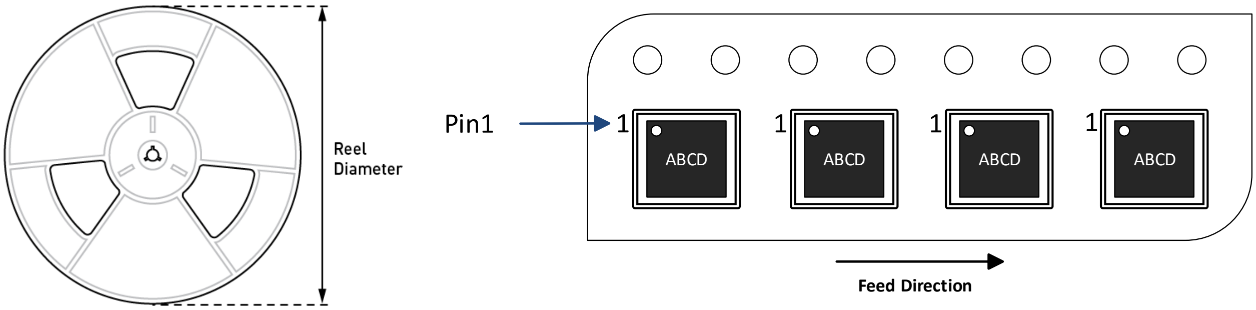
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity /Reel	Quantity /Tube (13)	Quantity /Tray (13)	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ4345GLE-33-AEC1-Z	QFN-17 (3mmx4mm)	5000	N/A	N/A	13in	12mm	8mm
MPQ4345GLE-5-AEC1-Z	QFN-17 (3mmx4mm)	5000	N/A	N/A	13in	12mm	8mm
MPQ4345JGLE-33-AEC1-Z	QFN-19 (3mmx4mm)	5000	N/A	N/A	13in	12mm	8mm
MPQ4345JGLE-5-AEC1-Z	QFN-19 (3mmx4mm)	5000	N/A	N/A	13in	12mm	8mm

Note:

13) N/A indicates "not available" in tubes. For 500-piece tape & reel prototype quantities, see factory. (Order code for 500-piece partial reel is "-P", tape & reel dimensions same as full reel.)

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	12/20/2022	Initial Release	-