Product Change Notification / NTDO-04AXQA020

Date:

04-Sep-2023

PCN Type:

Manufacturing Change

Notification Subject:

CCB 6547 Final Notice: Release of updated Libero SoC v2023.2 for selected products in the PolarFire FPGA, PolarFire SoC and RT PolarFire FPGA device family, including MPFxxx and RTPF device families.

Notification Text:

PCN Status: Final Notification

PCN Type: Manufacturing Change

Microchip Parts Affected: Please open one of the files found in the Affected CPNs section.
Note: For your convenience Microchip includes identical files in two formats (.pdf and .xls)

Description of Change: Release of updated Libero SoC v2023.2 for selected products in the PolarFire FPGA, PolarFire SoC and RT PolarFire FPGA device families, including MPFxxx and RTPF device families.
Refer to the PDF found in the Attachments section for additional details.

Notes:
Libero SoC v2023.2 released on Aug 17th, 2023 and is available for download on the webpage below:https://www.microchip.com/en-us/products/fpgas-and-plds/fpga-and-soc-design-tools/fpga/libero-software-later-versions#Download%20Software

Pre and Post Change Summary:

	Pre Change	Post Change
Software / Tool	Libero SoC Design Suite version 2023.1 or earlier.	Libero SoC Design Suite version 2023.2 or later.

Impacts to Data Sheet: None

Change Impact None

Reason for Change: The important updates in Libero SoC v2023.2 address issues in previous software versions that could result in either: High-Speed I/O Clock functional issues, device I/O performance outside the datasheet specifications, or registered I/O interface performance outside the user design's Static Timing Analysis results. Refer to the PDF attached to this PCN for additional details.

Change Implementation Status:
Complete

Estimated First Ship Date: August 18, 2023 (date code: 2333)

Note: Please be advised that after the estimated first ship date customers may receive pre and post change parts.

Time Table Summary:

	August 2023					September 2023			
Workweek	31	32	33	34	35	36	37	38	39
Final PCN Issue Date						x			
Estimated Implementation Date			x						

Method to Identify Change:
Not applicable. New software release is available as defined above.

Qualification Report:
Not applicable

Revision History:
September 4, 2023: Issued final notification.

The change described in this PCN does not alter Microchip's current regulatory compliance regarding the material content of the applicable products.

Attachments:

NTDO-04AXQA020_Affected_CPN_09042023.xlsx

NTDO-04AXQA020_Affected_CPN_09042023.pdf
MCHP_FPGA-BU_Libero_SoC_v2023p2_CN_Final.pdf

Please contact your local Microchip sales office with questions or concerns regarding this notification.

Terms and Conditions:

If you wish to receive Microchip PCNs via email please register for our PCN email service at our PCN home page select register then fill in the required fields. You will find instructions about registering for Microchips PCN email service in the PCN FAQ section.

If you wish to change your PCN profile, including opt out, please go to the PCN home page select login and sign into your myMicrochip account. Select a profile option from the left navigation bar and make the applicable selections.

NTDO-04AXQA020 - CCB 6547 Final Notice: Release of updated Libero SoC v2023.2 for selected products in the PolarFire FPGA, PolarFire SoC and RT PolarFire FPGA device family, including MPFxxx and RTPF device families.

Affected Catalog Part Numbers(CPN)
MPF300T-1FCVG484T2
MPF300T-FCVG484T2
MPF300T-1FCSG536T2
MPF300T-FCSG536T2
MPF300T-1FCG484I
MPF100T-1FCVG484T2
MPF100T-FCVG484T2
MPF100T-1FCSG325T2
MPF100T-FCSG325T2
MPF100T-1FCG484T2
MPF100T-FCG484T2
MPF200T-1FCVG484T2
MPF200T-FCVG484T2
MPF200T-1FCSG325T2
MPF200T-FCSG325T2
MPF200T-1FCSG536T2
MPF200T-FCSG536T2
MPF200T-1FCG484T2
MPF200T-FCG484T2
MPFS250T-1FCVG484T2
MPFS250T-FCVG484T2
MPFS250T-1FCVG784T2
MPFS250T-FCVG784T2
MPFS250T-1FCSG536T2
MPFS250T-FCSG536T2
MPF050T-1FCVG484T2
MPF050T-FCVG484T2
MPF050T-1FCSG325T2
MPF050T-FCSG325T2
MPF300TS-FC484M
MPF300T-FCG484X547
MPF300TS-FCV484M
MPF300TS-FC784M
MPF300TS-FCS536M
MPF300T-FC484M-B1
MPF300T-FC484M-B2
MPF300T-FC484M-B3
MPF300T-FC484M-B4
MPF300T-FCG484E-B1
MPF300XT-FCG484E-B1
MPF300T-FCG484E-B2
MPF300XT-FCG484E-B2
MPF300T-FCG484E-B3
MPF300XT-FCG484E-B3
MPF300T-FCG484E-B4
MPF300XT-FCG484E-B4
MPF300T-1FCG484E
MPF300T-FCG484EX52
MPF300T-FCG484E
MPF300T-FCG484I
MPF300TL-FCG484E
MPF300TL-FCG484I
MPF300TLS-FCG484I
MPF300TS-1FCG484I
MPF300TS-FCG484I
MPF300XT-1FCG484E
MPF300XT-1FCG484I
MPF300XT-FCG484E
MPF300XT-FCG484I
MPF300T-1FCG484IX548
MPF300T-1FCG484IS0322
MPF300T-FCV484M-B1
MPF300T-FCV484M-B2
MPF300T-FCV484M-B3
MPF300T-FCV484M-B4
MPF300T-FCVG484E-B1
MPF300T-FCVG484E-B2
MPF300T-FCVG484E-B3
MPF300T-FCVG484E-B4
MPF300T-1FCVG484E
MPF300T-1FCVG484I
MPF300T-FCVG484E
MPF300T-FCVG484I
MPF300TL-FCVG484E
MPF300TL-FCVG484I
MPF300TLS-FCVG484I
MPF300TS-1FCVG484I
MPF300TS-FCVG484I
MPF300T-FCVG484EX548
MPF300T-FCVG484T2-B1
MPF300T-FCVG484T2-B2
MPF300T-FCVG484T2-B3
MPF300T-FCVG484T2-B4
MPF300T-FC784M-B1
MPF300T-FC784M-B2
MPF300T-FC784M-B3
MPF300T-FC784M-B4
MPF300T-FCG784E-B1
MPF300XT-FCG784E-B1
MPF300T-FCG784E-B2

NTDO-04AXQA020 - CCB 6547 Final Notice: Release of updated Libero SoC v2023.2 for selected products in the PolarFire FPGA, PolarFire SoC and RT PolarFire FPGA device family, including MPFxxx and RTPF device families.

Affected Catalog Part Numbers(CPN)
MPF300XT-FCG784E-B2
MPF300T-FCG784E-B3
MPF300XT-FCG784E-B3
MPF300T-FCG784E-B4
MPF300XT-FCG784E-B4
MPF300T-1FCG784E
MPF300T-1FCG784I
MPF300T-FCG784E
MPF300T-FCG784I
MPF300TL-FCG784E
MPF300TL-FCG784I
MPF300TLS-FCG784I
MPF300TS-1FCG784I
MPF300TS-FCG784I
MPF300XT-1FCG784E
MPF300XT-1FCG784I
MPF300XT-FCG784E
MPF300XT-FCG784I
MPF300T-FCG784ES0317
MPF300T-FCG784ES0323
MPF300T-FCG784NE-B1
MPF300T-FCG784NE-B2
MPF300T-FCG784NE-B3
MPF300T-FCG784NE-B4
MPF300T-1FCG784NE
MPF300T-1FCG784NI
MPF300T-FCG784NE
MPF300T-FCG784NI
MPF300TS-1FCG784NI
MPF300TS-FCG784NI
MPF300T-FCG1152E-B1
MPF300XT-FCG1152E-B1
MPF300T-FCG1152E-B2
MPF300XT-FCG1152E-B2
MPF300T-FCG1152E-B3
MPF300XT-FCG1152E-B3
MPF300T-FCG1152E-B4
MPF300XT-FCG1152E-B4
MPF300T-1FCG1152EX3
MPF300T-1FCG1152E
MPF300T-1FCG1152I
MPF300T-FCG1152E
MPF300T-FCG1152I
MPF300TL-FCG1152E
MPF300TL-FCG1152I
MPF300TLS-FCG1152I
MPF300TS-1FCG1152I
MPF300TS-FCG1152I
MPF300XT-1FCG1152E
MPF300XT-1FCG1152I
MPF300XT-FCG1152E
MPF300XT-FCG1152I
MPF300T-1FCG1152IX45
MPF300T-FCG1152ES0311
MPF300T-FCG1152ES0324
MPF300T-FCS536M-B1
MPF300T-FCS536M-B2
MPF300T-FCS536M-B3
MPF300T-FCS536M-B4
MPF300T-FCSG536E-B1
MPF300T-FCSG536E-B2
MPF300T-FCSG536E-B3
MPF300T-FCSG536E-B4
MPF300T-1FCSG536E
MPF300T-1FCSG536I
MPF300T-FCSG536E
MPF300T-FCSG536I
MPF300TL-FCSG536E
MPF300TL-FCSG536I
MPF300TLS-FCSG536I
MPF300TS-1FCSG536I
MPF300TS-FCSG536I
MPF300T-FCSG536T2-B1
MPF300T-FCSG536T2-B2
MPF300T-FCSG536T2-B3
MPF300T-FCSG536T2-B4
MPF500TS-FC784M
MPF500TS-FC1152MX167
MPF500TS-FC1152M
MPF500TS-FC1152MX3
MPF500T-FC784M-B1
MPF500T-FC784M-B2
MPF500T-FC784M-B3
MPF500T-FC784M-B4
MPF500T-FCG784E-B1
MPF500T-FCG784E-B2
MPF500T-FCG784E-B3
MPF500T-FCG784E-B4
MPF500T-1FCG784E
MPF500T-1FCG784I

NTDO-04AXQA020 - CCB 6547 Final Notice: Release of updated Libero SoC v2023.2 for selected products in the PolarFire FPGA, PolarFire SoC and RT PolarFire FPGA device family, including MPFxxx and RTPF device families.

Affected Catalog Part Numbers(CPN)
MPF500T-FCG784E
MPF500T-FCG784I
MPF500TL-FCG784E
MPF500TL-FCG784I
MPF500TLS-FCG784I
MPF500TS-1FCG784I
MPF500TS-FCG784I
MPF500T-FC1152M-B1
MPF500T-FC1152M-B2
MPF500T-FC1152M-B3
MPF500T-FC1152M-B4
MPF500T-FCG1152E-B1
MPF500T-FCG1152E-B2
MPF500T-FCG1152E-B3
MPF500T-FCG1152E-B4
MPF500T-1FCG1152E
MPF500T-1FCG1152I
MPF500T-FCG1152E
MPF500T-FCG1152I
MPF500TL-FCG1152E
MPF500TL-FCG1152I
MPF500TLS-FCG1152I
MPF500TS-1FCG1152I
MPF500TS-FCG1152I
MPF500T-1FCG1152IX533
MPF100T-FCG484T2-B1
MPF100T-FCG484T2-B2
MPF100T-FCG484T2-B3
MPF100T-FCG484T2-B4
MPF100T-FCG484E-B1
MPF100T-FCG484E-B2
MPF100T-FCG484E-B3
MPF100T-FCG484E-B4
MPF100T-1FCG484E
MPF100T-1FCG484I
MPF100T-FCG484E
MPF100T-FCG484I
MPF100TL-FCG484E
MPF100TL-FCG484I
MPF100TLS-FCG484I
MPF100TS-1FCG484I
MPF100TS-FCG484I
MPF100T-FCVG484E-B1
MPF100T-FCVG484E-B2
MPF100T-FCVG484E-B3
MPF100T-FCVG484E-B4
MPF100T-1FCVG484E
MPF100T-1FCVG484I
MPF100T-FCVG484E
MPF100T-FCVG484I
MPF100TL-FCVG484E
MPF100TL-FCVG484I
MPF100TLS-FCVG484I
MPF100TS-1FCVG484I
MPF100TS-FCVG484I
MPF100T-FCVG484T2-B1
MPF100T-FCVG484T2-B2
MPF100T-FCVG484T2-B3
MPF100T-FCVG484T2-B4
MPF100T-FCSG325E-B1
MPF100T-FCSG325E-B2
MPF100T-FCSG325E-B3
MPF100T-FCSG325E-B4
MPF100T-1FCSG325E
MPF100T-1FCSG325I
MPF100T-FCSG325EX560
MPF100T-FCSG325E
MPF100T-FCSG325I
MPF100T-1FCSG325EX561
MPF100TL-FCSG325E
MPF100TL-FCSG325I
MPF100TLS-FCSG325I
MPF100TS-1FCSG325I
MPF100TS-FCSG325I
MPF100TL-FCSG325EQ347
MPF100T-FCSG325T2-B1
MPF100T-FCSG325T2-B2
MPF100T-FCSG325T2-B3
MPF100T-FCSG325T2-B4
MPF200T-FCG484T2-B1
MPF200T-FCG484T2-B2
MPF200T-FCG484T2-B3
MPF200T-FCG484T2-B4
MPF200TS-FCS325M
MPF200T-FCG484E-B1
MPF200T-FCG484E-B2
MPF200T-FCG484E-B3
MPF200T-FCG484E-B4
MPF200T-1FCG484E
MPF200T-1FCG484I

NTDO-04AXQA020 - CCB 6547 Final Notice: Release of updated Libero SoC v2023.2 for selected products in the PolarFire FPGA, PolarFire SoC and RT PolarFire FPGA device family, including MPFxxx and RTPF device families.

Affected Catalog Part Numbers(CPN)
MPF200T-FCG484E
MPF200T-FCG484I
MPF200TL-FCG484E
MPF200TL-FCG484I
MPF200TLS-FCG484I
MPF200TS-1FCG484I
MPF200TS-FCG484I
MPF200T-FCG484EZ330
MPF200T-FCG484ES0304
MPF200T-FCG484ES0305
MPF200T-FCG484ES0306
MPF200T-FCVG484E-B1
MPF200T-FCVG484E-B2
MPF200T-FCVG484E-B3
MPF200T-FCVG484E-B4
MPF200T-1FCVG484E
MPF200T-1FCVG484I
MPF200T-FCVG484E
MPF200T-FCVG484I
MPF200TL-FCVG484E
MPF200TL-FCVG484I
MPF200TLS-FCVG484I
MPF200TS-1FCVG484I
MPF200TS-FCVG484I
MPF200T-1FCVG484ES0302
MPF200T-FCVG484ES0307
MPF200T-FCVG484ES0308
MPF200T-FCVG484ES0309
MPF200T-FCVG484ES0010
MPF200T-FCVG484ES0314
MPF200T-FCVG484IS0315
MPF200T-FCVG484IS0316
MPF200T-FCVG484ES0319
MPF200T-FCVG484ES0318
MPF200T-FCVG484ES0320
MPF200T-FCVG484IS0321
MPF200T-FCVG484ES0327
MPF200T-FCVG484ES0328
MPF200T-FCVG484ES0329
MPF200T-FCVG484T2-B1
MPF200T-FCVG484T2-B2
MPF200T-FCVG484T2-B3
MPF200T-FCVG484T2-B4
MPF200T-FCG784E-B1
MPF200T-FCG784E-B2
MPF200T-FCG784E-B3
MPF200T-FCG784E-B4
MPF200T-1FCG784E
MPF200T-1FCG784I
MPF200T-FCG784E
MPF200T-FCG784I
MPF200TL-FCG784E
MPF200TL-FCG784I
MPF200TLS-FCG784I
MPF200TS-1FCG784I
MPF200TS-FCG784I
MPF200T-FCG784EH701
MPF200T-FCG784ES0301
MPF200T-FCG784IS0303
MPF200T-FCG784ES0039
MPF200T-FCG784ES0312
MPF200T-FCG784IS0313
MPF200T-FCG784IS0325
MPF200T-FCG784IS0326
MPF200T-FCS325M-B1
MPF200T-FCS325M-B2
MPF200T-FCS325M-B3
MPF200T-FCS325M-B4
MPF200T-FCSG325E-B1
MPF200T-FCSG325E-B2
MPF200T-FCSG325E-B3
MPF200T-FCSG325E-B4
MPF200T-1FCSG325E
MPF200T-1FCSG325I
MPF200T-FCSG325E
MPF200T-FCSG325I
MPF200TL-FCSG325E
MPF200TL-FCSG325I
MPF200TLS-FCSG325I
MPF200TS-1FCSG325I
MPF200TS-FCSG325I
MPF200T-FCSG325T2-B1
MPF200T-FCSG325T2-B2
MPF200T-FCSG325T2-B3
MPF200T-FCSG325T2-B4
MPF200T-FCSG536E-B1
MPF200T-FCSG536E-B2
MPF200T-FCSG536E-B3
MPF200T-FCSG536E-B4
MPF200T-1FCSG536E

NTDO-04AXQA020 - CCB 6547 Final Notice: Release of updated Libero SoC v2023.2 for selected products in the PolarFire FPGA, PolarFire SoC and RT PolarFire FPGA device family, including MPFxxx and RTPF device families.

Affected Catalog Part Numbers(CPN)
MPF200T-1FCSG536I
MPF200T-FCSG536E
MPF200T-FCSG536I
MPF200TL-FCSG536E
MPF200TL-FCSG536I
MPF200TLS-FCSG536I
MPF200TS-1FCSG536IQ302
MPF200TS-1FCSG536I
MPF200TS-FCSG536I
MPF200T-FCSG536T2-B1
MPF200T-FCSG536T2-B2
MPF200T-FCSG536T2-B3
MPF200T-FCSG536T2-B4
MPFS250TS-FCV484M
MPFS250TS-FCV784M
MPFS250TS-FC1152M
MPFS250TS-FCS536M
MPFS250T-FCV484M-B1
MPFS250T-FCV484M-B2
MPFS250T-FCV484M-B3
MPFS250T-FCV484M-B4
MPFS250T-FCVG484E-B1
MPFS250T-FCVG484E-B2
MPFS250T-FCVG484E-B3
MPFS250T-FCVG484E-B4
MPFS250T-FCVG484I
MPFS250T-1FCVG484IPP
MPFS250T-FCVG484IPP
MPFS250T-1FCVG484EPP
MPFS250T-FCVG484EPP
MPFS250T-1FCVG484I
MPFS250TL-FCVG484I
MPFS250TLS-FCVG484I
MPFS250TS-1FCVG484I
MPFS250TS-FCVG484I
MPFS250T-1FCVG484E
MPFS250T-FCVG484E
MPFS250TL-FCVG484E
MPFS250T-FCVG484T2-B1
MPFS250T-FCVG484T2-B2
MPFS250T-FCVG484T2-B3
MPFS250T-FCVG484T2-B4
MPFS250T-FCVG784E-B1
MPFS250T-FCVG784E-B2
MPFS250T-FCVG784E-B3
MPFS250T-FCVG784E-B4
MPFS250T-1FCVG784I
MPFS250T-FCVG784I
MPFS250TL-FCVG784I
MPFS250TLS-FCVG784I
MPFS250TS-1FCVG784I
MPFS250TS-FCVG784I
MPFS250T-1FCVG784E
MPFS250T-FCVG784E
MPFS250TL-FCVG784E
MPFS250T-FCVG784T2-B1
MPFS250T-FCVG784T2-B2
MPFS250T-FCVG784T2-B3
MPFS250T-FCVG784T2-B4
MPFS250T-FCV784M-B1
MPFS250T-FCV784M-B2
MPFS250T-FCV784M-B3
MPFS250T-FCV784M-B4
MPFS250T-FC1152M-B1
MPFS250T-FC1152M-B2
MPFS250T-FC1152M-B3
MPFS250T-FC1152M-B4
MPFS250T-FCG1152E-B1
MPFS250T-FCG1152E-B2
MPFS250T-FCG1152E-B3
MPFS250T-FCG1152E-B4
MPFS250T-1FCG1152IPP
MPFS250T-FCG1152IPP
MPFS250T-FCG1152I
MPFS250T-1FCG1152EPP
MPFS250T-FCG1152EPP
MPFS250T-1FCG1152I
MPFS250TL-FCG1152I
MPFS250TLS-FCG1152I
MPFS250TS-1FCG1152I
MPFS250TS-FCG1152I
MPFS250T-1FCG1152E
MPFS250T-FCG1152E
MPFS250TL-FCG1152E
MPFS250TS-1FCG1152IPP
MPFS250T-1FCG1152IX259
MPFS250T-FCS536M-B1
MPFS250T-FCS536M-B2
MPFS250T-FCS536M-B3
MPFS250T-FCS536M-B4

NTDO-04AXQA020 - CCB 6547 Final Notice: Release of updated Libero SoC v2023.2 for selected products in the PolarFire FPGA, PolarFire SoC and RT PolarFire FPGA device family, including MPFxxx and RTPF device families.

Affected Catalog Part Numbers(CPN)
MPFS250T-FCSG536E-B1
MPFS250T-FCSG536E-B2
MPFS250T-FCSG536E-B3
MPFS250T-FCSG536E-B4
MPFS250T-1FCSG536I
MPFS250T-FCSG536I
MPFS250TL-FCSG536I
MPFS250TLS-FCSG536I
MPFS250TS-1FCSG536I
MPFS250TS-FCSG536I
MPFS250T-1FCSG536E
MPFS250T-FCSG536E
MPFS250TL-FCSG536E
MPFS250T-FCSG536IPP
MPFS250T-FCSG536T2-B1
MPFS250T-FCSG536T2-B2
MPFS250T-FCSG536T2-B3
MPFS250T-FCSG536T2-B4
MPFS025T-FCVG484E-A-B1
MPFS025T-FCVG484E-A-B2
MPFS025T-FCVG484E-A-B3
MPFS025T-FCVG484E-A-B4
MPFS025T-FCVG484E-B1
MPFS025T-FCVG484E-B2
MPFS025T-FCVG484E-B3
MPFS025T-FCVG484E-B4
MPFS025T-1FCVG484E
MPFS025T-1FCVG484I
MPFS025T-FCVG484E
MPFS025T-FCVG484I
MPFS025TL-FCVG484E
MPFS025TL-FCVG484I
MPFS025TLS-FCVG484I
MPFS025TS-1FCVG484I
MPFS025TS-FCVG484I
MPFS025T-FCSG325E-A-B1
MPFS025T-FCSG325E-A-B2
MPFS025T-FCSG325E-A-B3
MPFS025T-FCSG325E-A-B4
MPFS025T-FCSG325E-B1
MPFS025T-FCSG325E-B2
MPFS025T-FCSG325E-B3
MPFS025T-FCSG325E-B4
MPFS025T-1FCSG325E
MPFS025T-1FCSG325I
MPFS025T-FCSG325E
MPFS025T-FCSG325I
MPFS025TL-FCSG325E
MPFS025TL-FCSG325I
MPFS025TLS-FCSG325I
MPFS025TS-1FCSG325I
MPFS025TS-FCSG325I
MPFS095T-FCS325M-B1
MPFS095T-FCS325M-B2
MPFS095T-FCS325M-B3
MPFS095T-FCS325M-B4
MPFS095T-FCSG325E-B1
MPFS095T-FCSG325E-B2
MPFS095T-FCSG325E-B3
MPFS095T-FCSG325E-B4
MPFS095T-1FCSG325E
MPFS095T-1FCSG325I
MPFS095T-FCSG325E
MPFS095T-FCSG325I
MPFS095TL-FCSG325E
MPFS095TL-FCSG325I
MPFS095TLS-FCSG325I
MPFS095TS-1FCSG325I
MPFS095TS-FCSG325I
MPFS095T-FCVG484E-B1
MPFS095T-FCVG484E-B2
MPFS095T-FCVG484E-B3
MPFS095T-FCVG484E-B4
MPFS095T-1FCVG484E
MPFS095T-1FCVG484I
MPFS095T-FCVG484E
MPFS095T-FCVG484I
MPFS095TL-FCVG484E
MPFS095TL-FCVG484I
MPFS095TLS-FCVG484I
MPFS095TS-1FCVG484I
MPFS095TS-FCVG484I
MPFS095T-FCVG784E-B1
MPFS095T-FCVG784E-B2
MPFS095T-FCVG784E-B3
MPFS095T-FCVG784E-B4
MPFS095T-1FCVG784E
MPFS095T-1FCVG784I
MPFS095T-FCVG784E
MPFS095T-FCVG784I

NTDO-04AXQA020 - CCB 6547 Final Notice: Release of updated Libero SoC v2023.2 for selected products in the PolarFire FPGA, PolarFire SoC and RT PolarFire FPGA device family, including MPFxxx and RTPF device families.

Affected Catalog Part Numbers(CPN)
MPFS095TL-FCVG784E
MPFS095TL-FCVG784I
MPFS095TLS-FCVG784I
MPFS095TS-1FCVG784I
MPFS095TS-FCVG784I
MPFS095T-FCSG536E-B1
MPFS095T-FCSG536E-B2
MPFS095T-FCSG536E-B3
MPFS095T-FCSG536E-B4
MPFS095T-1FCSG536E
MPFS095T-1FCSG536I
MPFS095T-FCSG536E
MPFS095T-FCSG536I
MPFS095TL-FCSG536E
MPFS095TL-FCSG536I
MPFS095TLS-FCSG536I
MPFS095TS-1FCSG536I
MPFS095TS-FCSG536I
MPF050T-FCVG484E-B1
MPF050T-FCVG484E-B2
MPF050T-FCVG484E-B3
MPF050T-FCVG484E-B4
MPF050T-1FCVG484E
MPF050T-1FCVG484I
MPF050T-FCVG484E
MPF050T-FCVG484I
MPF050TL-FCVG484E
MPF050TL-FCVG484I
MPF050TS-1FCVG484I
MPF050TS-FCVG484I
MPF050TLS-FCVG484I
MPF050T-FCVG484T2-B1
MPF050T-FCVG484T2-B2
MPF050T-FCVG484T2-B3
MPF050T-FCVG484T2-B4
MPF050T-FCSG325E-B1
MPF050T-FCSG325E-B2
MPF050T-FCSG325E-B3
MPF050T-FCSG325E-B4
MPF050T-1FCSG325E
MPF050T-1FCSG325I
MPF050T-FCSG325E
MPF050T-FCSG325I
MPF050TL-FCSG325E
MPF050TL-FCSG325I
MPF050TS-1FCSG325I
MPF050TS-FCSG325I
MPF050TLS-FCSG325I
MPF050T-FCSG325T2-B1
MPF050T-FCSG325T2-B2
MPF050T-FCSG325T2-B3
MPF050T-FCSG325T2-B4
MPFS160T-FCVG484E-B1
MPFS160T-FCVG484E-B2
MPFS160T-FCVG484E-B3
MPFS160T-FCVG484E-B4
MPFS160T-1FCVG484E
MPFS160T-1FCVG484I
MPFS160T-FCVG484E
MPFS160T-FCVG484I
MPFS160TL-FCVG484E
MPFS160TL-FCVG484I
MPFS160TLS-FCVG484I
MPFS160TS-1FCVG484I
MPFS160TS-FCVG484I
MPFS160T-FCVG484T2-B1
MPFS160T-FCVG484T2-B2
MPFS160T-FCVG484T2-B3
MPFS160T-FCVG484T2-B4
MPFS160T-FCVG784E-B1
MPFS160T-FCVG784E-B2
MPFS160T-FCVG784E-B3
MPFS160T-FCVG784E-B4
MPFS160T-1FCVG784E
MPFS160T-1FCVG784I
MPFS160T-FCVG784E
MPFS160T-FCVG784I
MPFS160TL-FCVG784E
MPFS160TL-FCVG784I
MPFS160TLS-FCVG784I
MPFS160TS-1FCVG784I
MPFS160TS-FCVG784I
MPFS160T-FCVG784T2-B1
MPFS160T-FCVG784T2-B2
MPFS160T-FCVG784T2-B3
MPFS160T-FCVG784T2-B4
MPFS160T-FCSG536E-B1
MPFS160T-FCSG536E-B2
MPFS160T-FCSG536E-B3
MPFS160T-FCSG536E-B4

NTDO-04AXQA020 - CCB 6547 Final Notice: Release of updated Libero SoC v2023.2 for selected products in the PolarFire FPGA, PolarFire SoC and RT PolarFire FPGA device family, including MPFxxx and RTPF device families.

Affected Catalog Part Numbers(CPN)

MPFS160T-1FCSG536E
MPFS160T-1FCSG536I
MPFS160T-FCSG536E
MPFS160T-FCSG536I
MPFS160TL-FCSG536E
MPFS160TL-FCSG536I
MPFS160TLS-FCSG536I
MPFS160TS-1FCSG536I
MPFS160TS-FCSG536I
MPFS160T-FCSG536T2-B1
MPFS160T-FCSG536T2-B2
MPFS160T-FCSG536T2-B3
MPFS160T-FCSG536T2-B4
MPF300TS-WAFER
MPF500TS-WAFER
MPF100TS-WAFER
MPF100TS-WAFER-PROCESSED
MPF200TS-WAFER
MPFS160TS-WAFERLOT
RTPF500T-1CB1509MS
RTPF500T-1CB1509PROTO
RTPF500T-1CG1509EX259
RTPF500T-1CG1509EX3
RTPF500T-1CG1509MS
RTPF500T-1CG1509PROTO
RTPF500T-1LG1509MS
RTPF500T-1LG1509PROTO
RTPF500T-CB1509PROTO
RTPF500T-CG1509PROTO
RTPF500T-LG1509PROTO
RTPF500TL-CB1509ES
RTPF500TL-CB1509PROTO
RTPF500TL-CG1509E
RTPF500TL-CG1509EX519
RTPF500TL-CG1509PROTO
RTPF500TL-LG1509ES
RTPF500TL-LG1509PROTO
RTPF500TLS-CB1509ES
RTPF500TLS-CB1509PROTO
RTPF500TLS-CG1509PROTO
RTPF500TLS-LG1509ES
RTPF500TLS-LG1509PROTO
RTPF500TS-1CB1509ES
RTPF500TS-1CB1509PROTO
RTPF500TS-1CG1509BX3
RTPF500TS-1CG1509EX155
RTPF500TS-1CG1509PROTO
RTPF500TS-1LG1509ES
RTPF500TS-1LG1509PROTO
RTPF500TS-CB1509PROTO
RTPF500TS-CG1509PROTO
RTPF500TS-LG1509ES
RTPF500TS-LG1509PROTO
RTPF500ZT-1CB1509MS
RTPF500ZT-1CB1509PROTO
RTPF500ZT-1CG1509MS
RTPF500ZT-1CG1509PROTO
RTPF500ZT-1LG1509MS
RTPF500ZT-1LG1509PROTO
RTPF500ZT-CB1509PROTO
RTPF500ZT-CG1509PROTO
RTPF500ZT-LG1509B
RTPF500ZT-LG1509ES
RTPF500ZT-LG1509PROTO
RTPF500ZTL-CB1509MS
RTPF500ZTL-CG1509MS
RTPF500ZTL-LG1509E
RTPF500ZTL-LG1509MS
RTPF500ZTLS-CB1509PROTO
RTPF500ZTLS-CG1509PROTO
RTPF500ZTLS-LG1509ES
RTPF500ZTLS-LG1509PROTO
RTPF500ZTS-1CB1509ES
RTPF500ZTS-1CB1509PROTO
RTPF500ZTS-1CG1509PROTO
RTPF500ZTS-1LG1509ES
RTPF500ZTS-1LG1509PROTO
RTPF500ZTS-CB1509PROTO
RTPF500ZTS-CG1509PROTO
RTPF500ZTS-LG1509ES
RTPF500ZTS-LG1509PROTO

Customer Notification (CN)

Subject: Important Updates in Libero SoC v2023.2 for PolarFire® FPGA, PolarFire SoC, and RT PolarFire FPGA

August 2023

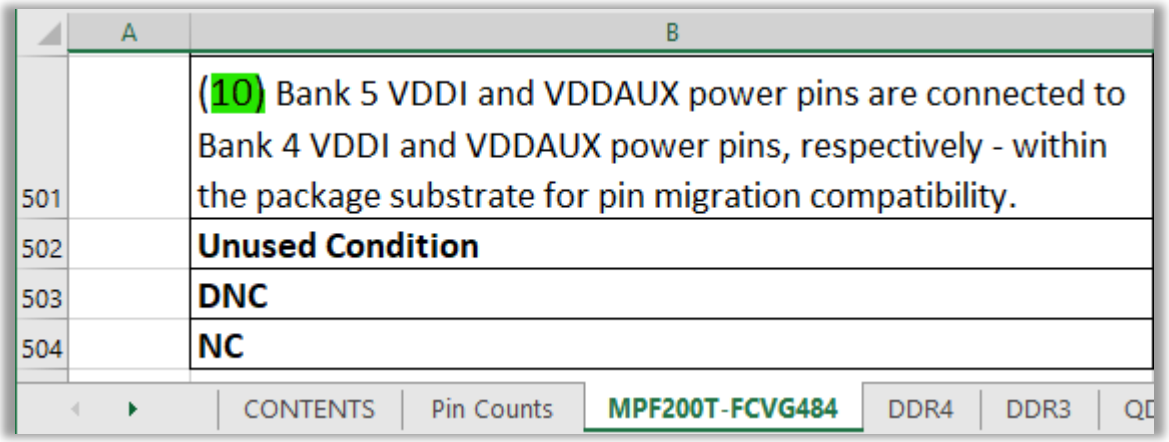
This notification highlights some of the important updates contained in the v2023.2 release of Libero SoC Design Suite affecting PolarFire FPGA, PolarFire SoC, and RT PolarFire FPGA devices.

Table of Contents:

PolarFire FPGA MPF200Txx-FCVG484 I/O Bank 4 and 5 DRC Update

Description:

This customer notification applies to PolarFire MPF200Txx FPGAs in the FCVG484 package. Device I/O banks 4 and 5 on the FCVG484 package of MPF200T/TS/TL/TLS devices are connected to a single VDDI I/O voltage supply, as stated in the device Package Pin Assignment Table (PPAT), per the figure below.



	A	B
501		(10) Bank 5 VDDI and VDDAUX power pins are connected to Bank 4 VDDI and VDDAUX power pins, respectively - within the package substrate for pin migration compatibility.
502		**Unused Condition**
503		**DNC**
504		**NC**

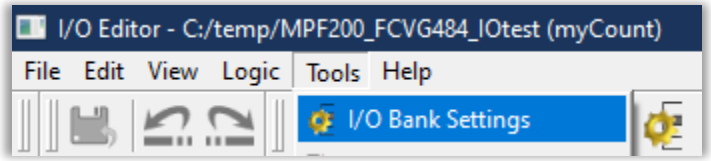
CONTENTS | Pin Counts | MPF200T-FCVG484 | DDR4 | DDR3 | QD

In other words, there is no VDDI5 nor VDDAUX5 package pin on this device die and package combination. Similarly, the Libero SoC design specific pin reports do not contain separate I/O voltage supply pins for I/O banks 4 and 5.

Prior to Libero SoC v2023.2, it was possible for the user to assign different VDDI bank voltages to the two I/O banks in a Libero SoC design targeting this device. Libero SoC v2023.2 has been updated to flag this erroneous user selection and to enforce a Design Rule Check (DRC) on the VDDI assignments to the two I/O banks.

Reason for Change:

With Libero SoC v2023.1 or earlier, a user design could have selected different I/O bank voltage levels for I/O banks 4 and 5 of the MPF200T/TS/TL/TLS device in the FCVG484 package. This selection could have been entered in the Libero SoC Constraints Manager, I/O Editor tool via the I/O Bank Settings window in the Tools menu, or via a user PDC constraint file, per the figures below.



OR

```
set_iobank -bank_name Bank4   \
    -vcci 3.30                \
    -fixed true               \
    -update_iostd true

set_iobank -bank_name Bank5   \
    -vcci 2.50                \
    -fixed true               \
    -update_iostd true
```

Alternatively, the user might have assigned incompatible I/O standards to the I/Os placed in bank 4 vs. bank 5, as shown in the figure below.

```
------------------------------------------------------------------
-Pin Report - Date: Thu Jul  6 14:38:33 2023
-Product: Designer
-Release: v2023.1
-Version: 2023.1.0.6
-Design Name: myCount
-Family: PolarFire
-Die: MPF200T
-Package: FCVG484
------------------------------------------------------------------

Port       |Pin |Fixed |Function                                |Bank     |I/O Std   |Direction |
-----------|----|------|----------------------------------------|---------|----------|----------|
clear       F2   Yes    GPIO172PB5/CCC_SW_PLL0_OUT1             Bank5     LVCMOS25   Input
clk         G4   Yes    GPIO174PB5/CLKIN_W_1/CCC_SW_CLKIN_W_1   Bank5     LVCMOS25   Input
count[0]    J1   Yes    GPIO149NB4                              Bank4     LVTTL      Output
                                                  .
                                                  .
                                                  .
count[14]   K9   Yes    GPIO145PB4/DQS                          Bank4     LVTTL      Output
count[15]   F1   Yes    GPIO173NB5                              Bank5     LVCMOS25   Output
enable      G2   Yes    GPIO172NB5                              Bank5     LVCMOS25   Input
```

If this discrepancy between the user design settings versus the board layout pin reports and PPAT remained unnoticed, the potential exists for 1 of the 2 banks to be powered at a voltage level different from that specified in the Libero design. In this scenario, where the board I/O supply doesn't match

the design's I/O bank voltage selection, it could result in 1 of the 2 I/O banks performing outside of the datasheet specifications.

Libero SoC v2023.2, or later, will perform a DRC and issue an error if the user design attempts to assign different VDDI voltages to I/O banks 4 and 5.

Application Impact:

The following design configurations are NOT impacted:

- Designs that didn't place any I/O in bank 4 are not impacted.
- Designs that didn't place any I/O in bank 5 are not impacted.
- Designs where all I/Os placed in banks 4 and 5 have the same VDDI are not impacted.
- Designs where all I/Os placed in banks 4 and 5 are I/O standard compatible are not impacted.

Designs where I/Os placed in banks 4 and 5 have incompatible I/O standards selected, requiring different VDDI levels, could experience I/O performance outside of the device datasheet specifications and device timing models, for the respective bank whose Libero VDDI bank voltage doesn't match the board I/O supply voltage.

Required Action:

Existing, ongoing, or completed designs targeting the MPF200T/TS/TL/TLS device in the FCVG484 package that are affected by the issue described above must update the I/O bank VDDI settings or I/O standard settings to ensure that:

- All I/Os assigned to banks 4 and 5 use compatible I/O standards powered by the same I/O supply voltage level.
- The I/O bank voltage set in the Libero design matches the board design's VDDI4 supply voltage.
- Mixed voltage receivers adhere to the VDDI / VDDAUX recommended operating conditions, and the compatibility rules in the PolarFire FPGA I/O User Guide, section 7.2.2 - Mixed I/O in VDDI Banks, describing the compatible input standards for a given VDDI and VDDAUX supply.

After updating the design, re-run Place and Route, Verify Timing, and all subsequent design flow steps.

When a pre-existing design containing this issue is opened in Libero SoC v2023.2, the design's Place & Route state will be invalidated, and the message below will be printed in the Libero log window:

> *Error: The I/O banks 'Bank4 Bank5' must have the same VDDI for this package which is not the case in this design. Please make sure to fix the bank setting before running Place and Route.*
> *Info: Converted design '<ROOT>' to pre-Place and Route state.*

PolarFire FPGA MPF050Txx and PolarFire SoC MPFS025Txx High-Speed I/O Clock Connectivity Update

Description:

This customer notification applies to PolarFire MPF050T/TS/TL/TLS FPGAs and MPFS025T/TS/TL/TLS SoC devices. Prior to Libero SoC v2023.2, designs targeting these two devices could have placed High-Speed I/O Bank Clock (HS_IO_CLK) instances at locations that are not routable. Libero SoC v2023.2 has been updated to fix this issue and prevent usage of HS_IO_CLK instances in locations that are not routable on these two devices.

Reason for Change:

Prior to Libero SoC v2023.2, designs targeting these two devices could have placed High-Speed I/O Clock (HS_IO_CLK) instances at locations that are not routable. The design would successfully complete the Libero SoC design flow, however, when programmed with the design bitstream, the related HS_IO_CLK signal would not function, causing a time-zero issue on the user I/O interface requiring the HS_IO_CLK.

Libero SoC v2023.2 fixes this issue by including updated HS_IO_CLK connectivity rules for these two devices to ensure that HS_IO_CLK instance placement and routing satisfies the device-specific periphery connection rules.

Application Impact:

The following design configurations are NOT impacted:

- Designs that don't contain any HS_IO_CLK post-layout macro are not impacted.

Designs where HS_IO_CLK instances are placed in non-routable locations of PolarFire MPF050T/TS/TL/TLS FPGAs and MPFS025T/TS/TL/TLS SoC devices would see time-zero functional issues on the user I/O interface requiring the HS_IO_CLK.

Required Action:

No action is required for MPF050T/TS/TL/TLS FPGA and MPFS025T/TS/TL/TLS SoC designs that have successfully completed full functional system testing over the full operating conditions range, including the user I/O interfaces using High-Speed I/O Bank Clock (HS_IO_CLK) instances.

For new or ongoing MPF050T/TS/TL/TLS FPGA and MPFS025T/TS/TL/TLS SoC designs, Microchip recommends upgrading to Libero SoC v2023.2, or later, and re-running Place and Route to ensure that HS_IO_CLK instances are placed and routed using the updated device-specific HS_IO_CLK connectivity rules.

Existing MPF050T/TS/TL/TLS FPGA and MPFS025T/TS/TL/TLS SoC designs opened in Libero SoC v2023.2 that contain HS_IO_CLK instances placed in non-routable locations will have the Place and Route design state invalidated, with the following message in the Libero log window:

Info: This design contains HS_IO_CLK instances placed in an invalid location for this device. Place and Route will be invalidated. Please refer to the Libero SoC v2023.2 Release Notes for more information.
Info: Converted design '<ROOT>' to pre-Place and Route state

PolarFire, PolarFire SoC, and RT PolarFire Programmable I/O Delay Update on Ports using Combined I/O Registers

Description:

This notification applies to PolarFire FPGA, PolarFire SoC, and RT PolarFire FPGA designs using programmable I/O delay along with I/O registers that have been combined from fabric Flip-Flops. The I/Os in these devices support programmable input and output delays to assist with timing closure on external interfaces. These delays can be applied automatically through Timing Driven Place and Route (TDPR) Min-Delay Repair (MDR) or manually through a user setting in the I/O Editor or I/O PDC constraints. Each I/O path also supports "I/O Register Combining" where a directly connected fabric flip-flop is combined into the I/O input, output or output-enable register (IOFF). I/O register combining can occur automatically during TDPR, if enabled, or manually through a user set_ioff directive in an NDC constraint file.

Libero SoC v2023.2 fixes an issue where any specified programmable I/O delays occurring in the path of a combined IOFF were disabled.

Reason for Change:

Prior to Libero SoC v2023.2, a design containing programmable I/O delays in the path of a combined IOFF would have the programmable I/O delays disabled in the programming bitstream. However, the Static Timing Analysis (STA) would have included the programmable delays in the setup and hold calculations. Therefore, a device programmed with such a design bitstream would experience a mismatch in FPGA I/O timing on hardware compared to the design's STA timing reports.

Libero SoC v2023.2 fixes the issue so that programmable I/O delay settings in the path of a combined IOFF are honored in the programming bitstream.

Application Impact:

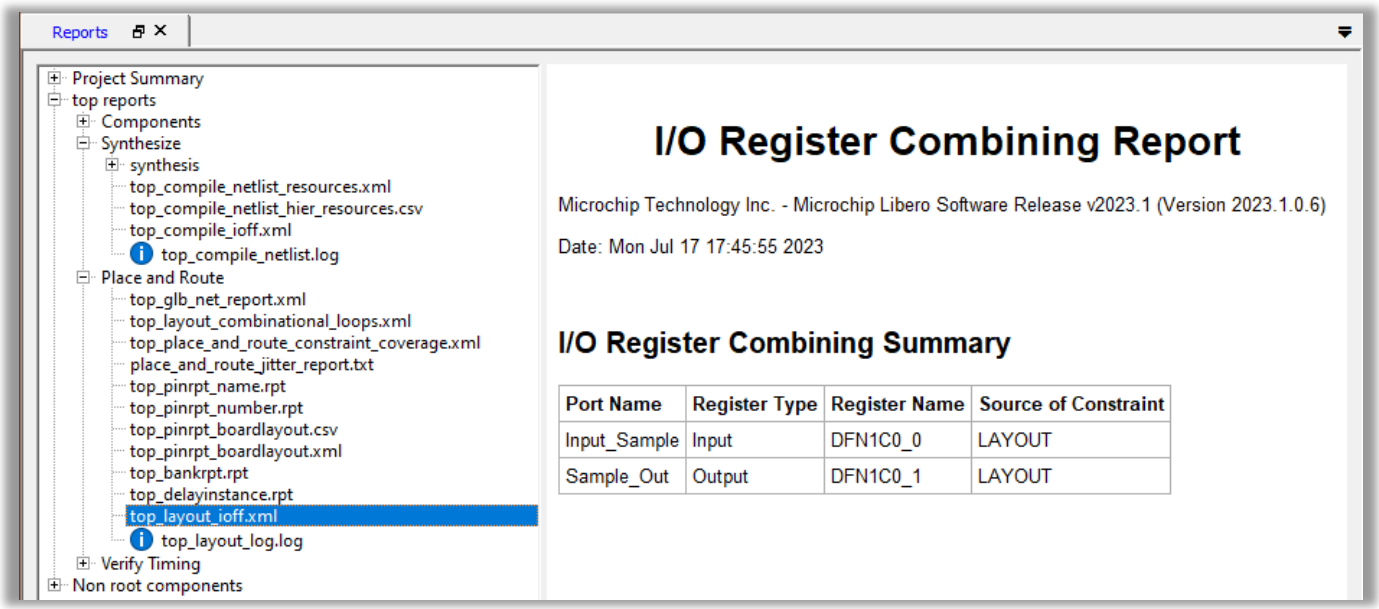
The following design configurations are NOT impacted:

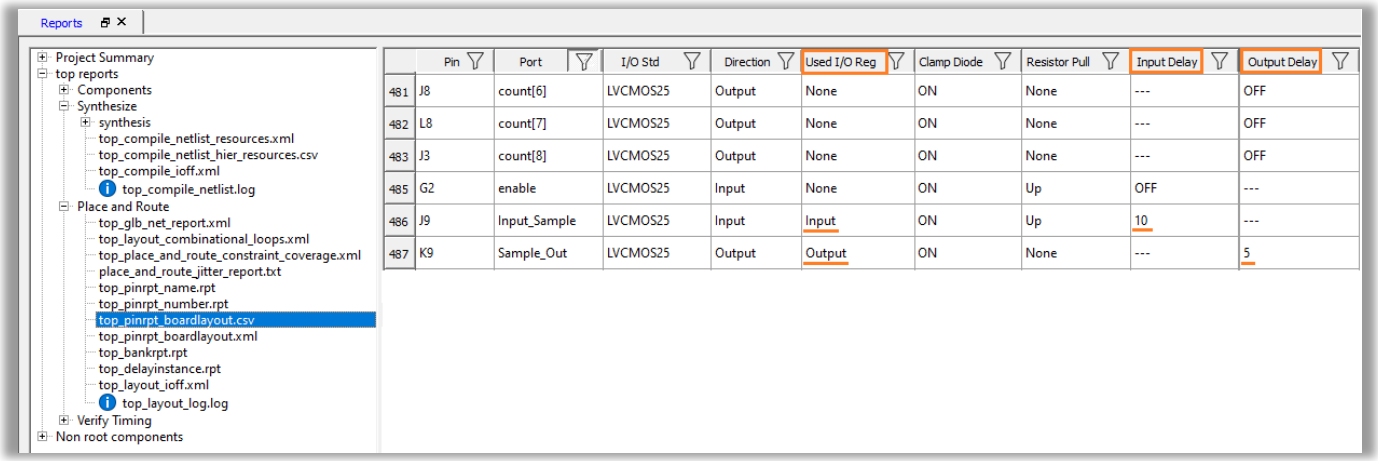
- Designs that don't contain any programmable I/O delay taps are not impacted.
    - The design pin report (<root>_pinrpt*) Input Delay and Output Delay columns will contain "OFF" if I/O delays are not used for an I/O
- Designs that don't contain any combined IOFF registers are not impacted.

- Refer to the <root>_layout_ioff.xml report for a list of fabric FFs that have been combined into I/O Registers.

The following figures show the Libero SoC reports that can be used to identify whether programable I/O delays are used in the path of an I/O that also used I/O Registers (also known as I/O Flip-Flops, or IOFFs).

- The first figure shows an example I/O Register Combining report, <root>_layout_ioff.xml, listing the fabric FFs that have been combined into I/O Registers.
- The second figure shows an example Pin Report with the “Used I/O Reg”, “Input Delay”, and “Output Delay” columns highlighted, indicated that this example does indeed use programmable I/O delays in the path of combined IOFFs.





	Pin	Port	I/O Std	Direction	Used I/O Reg	Clamp Diode	Resistor Pull	Input Delay	Output Delay
481	J8	count[6]	LVCMOS25	Output	None	ON	None	---	OFF
482	L8	count[7]	LVCMOS25	Output	None	ON	None	---	OFF
483	J3	count[8]	LVCMOS25	Output	None	ON	None	---	OFF
485	G2	enable	LVCMOS25	Input	None	ON	Up	OFF	---
486	J9	Input_Sample	LVCMOS25	Input	Input	ON	Up	10	---
487	K9	Sample_Out	LVCMOS25	Output	Output	ON	None	---	5

Designs using Libero SoC v2023.1, or earlier, that do contain programmable I/O delays in the path of a combined IOFF would not have the programmable I/O delays reflected in the programmed device. If the programmable I/O delay was required for correct interface functionality in hardware, then communication issues could be observed. Furthermore, the Libero SoC STA results would have been performed with the inclusion of the programmable I/O delays, however the STA result would not match the programmed device I/O timing in HW.

Required Action:

No action is required for designs that don't enable programable I/O delay in the path of an I/O that also used I/O register combining of a fabric FF into an IOFF.

<u>For designs that use both programmable I/O delay and I/O register combining:</u>

Open the design in Libero SoC v2023.2 and observe whether the state of the "Generate FPGA Array Data" design flow step is invalidated and the following message is printed in the Libero log window:

Warning: Design '<ROOT>' uses programmable I/O delay settings in the path of a combined IOFF. The Generate FPGA Array Data state has been invalidated. Please re-run Generate FPGA Array Data and subsequent design flow steps. For more information, refer to the Libero SoC v2023.2 release notes.

Use Libero SoC v2023.2 to re-run the "Generate FPGA Array Data" design flow step, and subsequent design flow steps to obtain a programming bitstream that will honor the programmable I/O delay settings in a programmed device.

Download Libero SoC Design Suite

The latest version of Libero SoC Design Suite can be downloaded from the following webpage:
https://www.microchip.com/en-us/products/fpgas-and-plds/fpga-and-soc-design-tools/fpga/libero-software-later-versions#Download%20Software

Contact Information

For any questions about this subject, contact Microchip FPGA-BU Technical Support at the web portal below:
http://www.microchip.com/support

Regards,

Microsemi Corporation, a wholly owned subsidiary of Microchip Technology Inc.