

Preliminary Specification

PRODUCT NAME : 1.3" 128X96 White OLED

PRODUCT NO.: PMO14201

APPROVED BY
DATE:

PACER	PLC.	APPROVED

REVISION RECORD

REV.	REVISION DESCRIPTION	REV. DATE	REMARK
X01	INITIAL RELEASE	2006. 01. 12	
X02	<ul style="list-style-type: none">▪ Add the operating conditions for different luminance▪ Add the panel electrical specification▪ Modify the CIE specification▪ Add the application circuit	2006. 03. 01	Page 6, 7, 8 & 17

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1. SCOPE

The purpose of this specification is to define the general provisions and quality requirements that apply to the supply of display cells manufactured by RiTdisplay. This document, together with the Module Ass'y Drawing, is the highest-level specification for this product. It describes the product, identifies supporting documents and contains specifications.

2. WARRANTY

Pacer PLC warrants that the products delivered pursuant to this specification (or order) will conform to the agreed specifications for twelve (12) months from the shipping date ("Warranty Period"). Pacer PLC is obligated to repair or replace the products which are found to be defective or inconsistent with the specifications during the Warranty Period without charge, on condition that the products are stored or used as the conditions specified in the specifications. Nevertheless, Pacer PLC is not obligated to repair or replace the products without charge if the defects or inconsistency are caused by the force majeure or the reckless behaviors of the customer.

After the Warranty Period, all repairs or replacements of the products are subject to charge.

3. FEATURES

- Small Molecular Passive Organic Light Emission Diode.
- Color : White
- Panel matrix : 128*96
- Driver IC : SSD1329U2
- Excellent Quick response time : 10 μ s
- Extremely thin thickness for best mechanism design : 1.65mm.
- High contrast : 500:1
- Wide viewing angle : 160°
- 8-bit 6800-series Parallel Interface, 8-bit 8080-series Parallel Interface, Serial Peripheral Interface.
- Wide range operating temperature : -40 to 70 °C

4. MECHANICAL DATA

NO	ITEM	SPECIFICATION	UNIT
1	Dot Matrix	128 (W) x 96 (H)	dot
2	Dot Size	0.19 (W) x 0.19 (H)	mm ²
3	Dot Pitch	0.21 (W) x 0.21 (H)	mm ²
4	Aperture Rate	82	%
5	Active Area	26.86 (W) x 20.14 (H)	mm ²
6	Panel Size	33 (W) x 26.8 (H)	mm ²
7	Panel Thickness	1.65	mm
8	Module Size	33 (W) x 41.6 (H) x 1.65 (T)	mm ³
9	Diagonal A/A size	1.3	inch
10	Module Weight	TBD	gram

5. MAXIMUM RATINGS

ITEM	MIN	MAX	UNIT	Condition	Remark
Supply Voltage (V_{DD})	-0.3	3.5	V	Ta = 25°C	
Supply Voltage (V_{CC})	8	16	V	Ta = 25°C	
Operating Temp.	-40	70	°C		
Storage Temp	-40	85	°C		
Humidity		85	%		
Operating Life Time	8,000	-	Hrs	120 cd/m ² , 50% checkerboard	Note (1)
Operating Life Time	10,000	-	Hrs	100 cd/m ² , 50% checkerboard	Note (2)
Operating Life Time	12,500	-	Hrs	80 cd/m ² , 50% checkerboard	Note (3)

Note:

(A) Under $V_{CC} = 15V$, Ta = 25°C, 50% RH.

(B) Life time is defined the amount of time when the luminance has decayed to less than 50% of the initial measured luminance.

(1) Setting of 120cd/m² :

- Contrast setting : **0xEC**
- Frame rate : 85Hz
- Duty setting : 1/96

(2) Setting of 100cd/m² :

- Contrast setting : **0xB7**
- Frame rate : 85Hz
- Duty setting : 1/96

(3) Setting of 80cd/m² :

- Contrast setting : **0x82**
- Frame rate : 85Hz
- Duty setting : 1/96

6. ELECTRICAL CHARACTERISTICS

6.1 D.C ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETERS	TEST CONDITION	MIN	TYP	MAX	UNIT
V _{CC}	Driver power supply (for OLED panel)	Ta=-20°C to +70°C	14.5	15	15.5	V
V _{DD}	Logic operating voltage	Ta=-20°C to +70°C	2.4	2.7	3.5	V
V _{OH}	Hi logic output level	I _{out} =100 uA, 3.3MHz	0.9* V _{DD}	-	V _{DD}	V
V _{OL}	Low logic output level	I _{out} =100uA, 3.3MHZ	0	-	0.1* V _{DD}	V
V _{IH}	Hi logic input level	I _{out} =100uA, 3.3MHZ	0.8* V _{DD}	-	V _{DD}	V
V _{IL}	Low logic output level	I _{out} =100uA, 3.3MHZ	0	-	0.2* V _{DD}	V
I _{CC}	Operating current for V _{CC}	Contrast=7F	-	750	850	uA
I _{DD}	Operating current for V _{DD}	Contrast=7F	-	72	200	uA
I _{SEG}	Segment output current	Contrast=7F	250	300	370	uA
		Contrast=5F	-	225	-	uA
		Contrast=3F	-	150	-	uA
		Contrast=1F	50	75	100	uA

Note : V_{DD}=2.7 V □ V_{CC}= 15 V □ Frame rate= 85 Hz □ No panel attached.

6.2 ELECTRO-OPTICAL CHARACTERISTICS

PANEL ELECTRICAL SPECIFICATIONS

PARAMETER	MIN	TYP.	MAX	UNITS	COMMENTS
Normal mode current	-	24		mA	All pixels on (1)
Standby mode current		1		mA	Standby mode 10% pixels on (2)
Normal mode power consumption	-	360		mW	All pixels on (1)
Standby mode power consumption		15		mW	Standby mode 10% pixels on (2)
Normal mode Luminance	80	100		cd/m ²	Display Average
Standby mode Luminance		10		cd/m ²	Display Average
CIE _x (White)	0.24	0.28	0.32		x, y (CIE 1931)
CIE _y (White)	0.30	0.34	0.38		
Dark Room Contrast	500:1				
Viewing Angle	160			degree	
Response Time		10		μs	

(1) Normal mode condition :

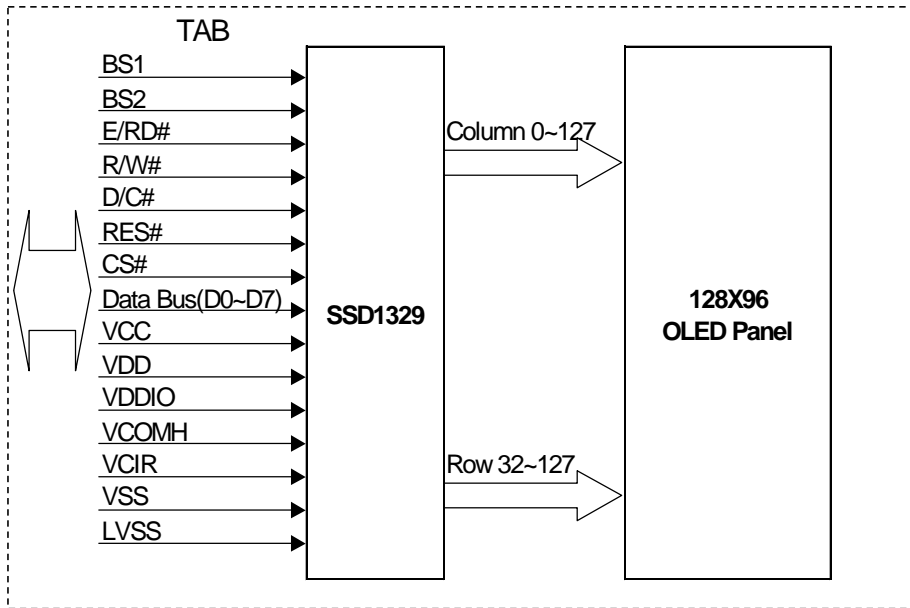
- Driving Voltage : 15V
- Contrast setting : 0xB7
- Frame rate : 85Hz
- Duty setting : 1/96

(2) Standby mode condition :

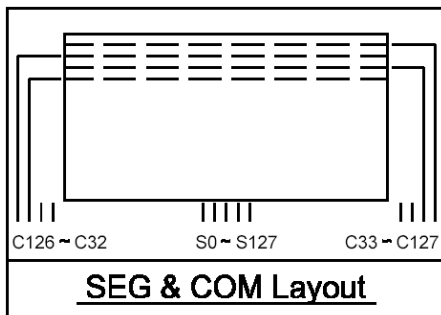
- Driving Voltage : 15V
- Contrast setting : 0x00
- Frame rate : 85Hz
- Duty setting : 1/96

7. INTERFACE

7.1 FUNCTION BLOCK DIAGRAM



7.2 PANEL LAYOUT DIAGRAM



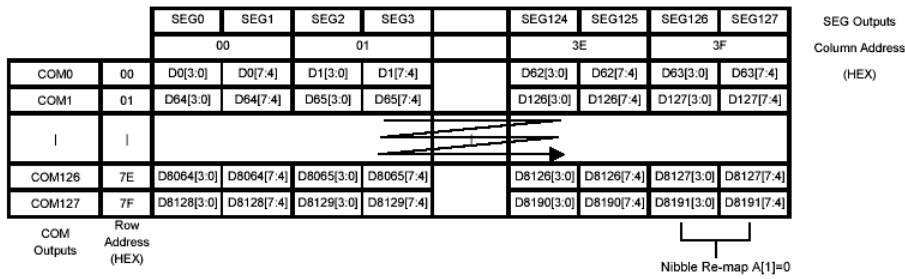
7.3 PIN ASSIGNMENTS

PIN NAME	PIN NO	DESCRIPTION												
NC	1	No connection.												
VCIR	2	No connection and left float.												
VCOMH	3	Com Voltage Output. A capacitor should be connected between this pin and V _{SS} .												
LVSS	4	Ground.												
VSS	5	Ground.												
BS1	6	MCU parallel interface selection input. <table border="1" style="margin-left: 20px;"> <thead> <tr> <th></th> <th>6800-parallel interface</th> <th>8080-parallel interface</th> <th>Serial interface</th> </tr> </thead> <tbody> <tr> <td>BS1</td> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>BS2</td> <td>1</td> <td>1</td> <td>0</td> </tr> </tbody> </table>		6800-parallel interface	8080-parallel interface	Serial interface	BS1	0	1	0	BS2	1	1	0
	6800-parallel interface	8080-parallel interface	Serial interface											
BS1	0	1	0											
BS2	1	1	0											
BS2	7													
IREF	8	Reference current input pin. A resistor should be connected between this pin and V _{SS} .												
CS#	9	Chip select input.												
RES#	10	Reset signal input. When it's low, initialization of SSD1329 is executed.												
D/C#	11	Data/ Command control. Pull high for write/read display data. Pull low for write command or read status.												
R/W#	12	MCU interface input. Data write operation is initiated when it's pull low. MCU interface input. Data read operation is initiated when it's pull low.												
E	13													
D0	14	Data bus(for parallel interface)												
D1	15	Data bus(for parallel interface)												
D2	16	Data bus(for parallel interface)												
D3	17	Data bus(for parallel interface)												
D4	18	Data bus(for parallel interface)												
D5	19	Data bus(for parallel interface)												
D6	20	Data bus(for parallel interface)												
D7	21	Data bus(for parallel interface)												
VDDIO	22	This pin is a power supply pin of I/O buffer.												
VDD	23	Power supply for logic.												
VCC	24	Power supply for analog circuit.												
NC	25	No connection.												

7.4 GRAPHIC DISPLAY DATA RAM ADDRESS MAP

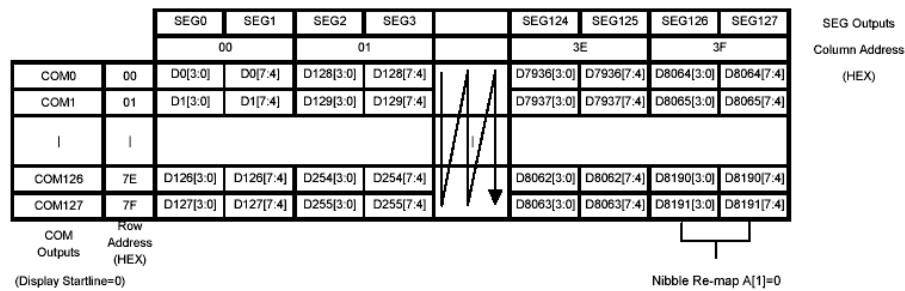
GDDRAM Address Map - Horizontal Address Increment A[2]=0, Column Address Re-map A[0]=0, Nibble Re-map

A[1]=0, COM Re-map A[4]=0, Display Start Line=00H (Data byte sequence: D0, D1, D2 ... D8191)



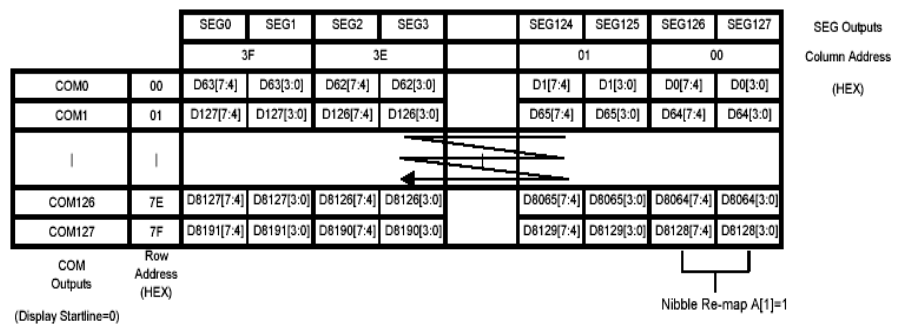
GDDRAM Address Map - Vertical Address Increment A[2]=1, Column Address Re-map A[0]=0, Nibble Re-map

A[1]=0, COM Re-map A[4]=0, Display Start Line=00H (Data byte sequence: D0, D1, D2 ... D8191)



GDDRAM Address Map - Horizontal Address Increment A[2]=0, Column Address Re-map A[0]=1, Nibble Re-map

A[1]=1, COM Re-map A[4]=0, Display Start line=00H (Data byte sequence: D0, D1, D2 ... D8191)



GDDRAM Address Map - Horizontal Address Increment A[2]=0, Column Address Re-map A[0]=0, Nibble Re-map A[1]=0, COM Re-map A[4]=1, Display Start Line=78H (Data byte sequence: D0, D1, D2 ... D8191)

		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127		
		00		01			3E		3F			
COM119	00	D0[3:0]	D0[7:4]	D1[3:0]	D1[7:4]		D62[3:0]	D62[7:4]	D63[3:0]	D63[7:4]	SEG Outputs Column Address (HEX)	
COM118	01	D1[3:0]	D84[7:4]	D65[3:0]	D65[7:4]		D126[3:0]	D126[7:4]	D127[3:0]	D127[7:4]		
COM121	7E	D126[3:0]	D8064[7:4]	D8065[3:0]	D8065[7:4]		D8126[3:0]	D8126[7:4]	D8127[3:0]	D8127[7:4]		
COM120	7F	D127[3:0]	D8128[7:4]	D8129[3:0]	D8129[7:4]		D8190[3:0]	D8190[7:4]	D8191[3:0]	D8191[7:4]		

COM Outputs Row Address (HEX)
(Display Startline=78H)

GDDRAM Address Map - Horizontal Address Increment A[2]=0, Column Address Re-map A[0]=0, Nibble Re-map A[1]=0, COM Re-map A[4]=0, Display Start Line=00H (Data byte sequence: D0, D1, D2 ... D7811), Column Start Address = 01H, Column End Address = 3EH, Row Start Address = 01H, Row End Address = 7EH

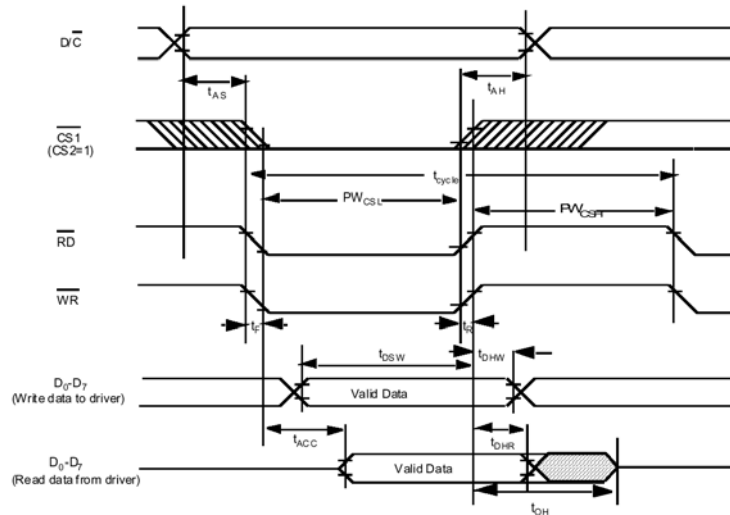
		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127		
		00		01			3E		3F			
COM0	00										SEG Outputs Column Address (HEX)	
COM1	01			D0[3:0]	D0[7:4]		D61[3:0]	D61[7:4]				
COM126	7E			D7750[3:0]	D7750[7:4]		D7811[3:0]	D7811[7:4]				
COM127	7F											

COM Outputs Row Address (HEX)
(Display Startline=0)

7.5 INTERFACE TIMING CHART

8080-Series MPU Parallel Interface Timing Characteristics ($V_{DD}-V_{SS} = 2.4$ to $3.5V$, $T_A = -30$ to $85^\circ C$)

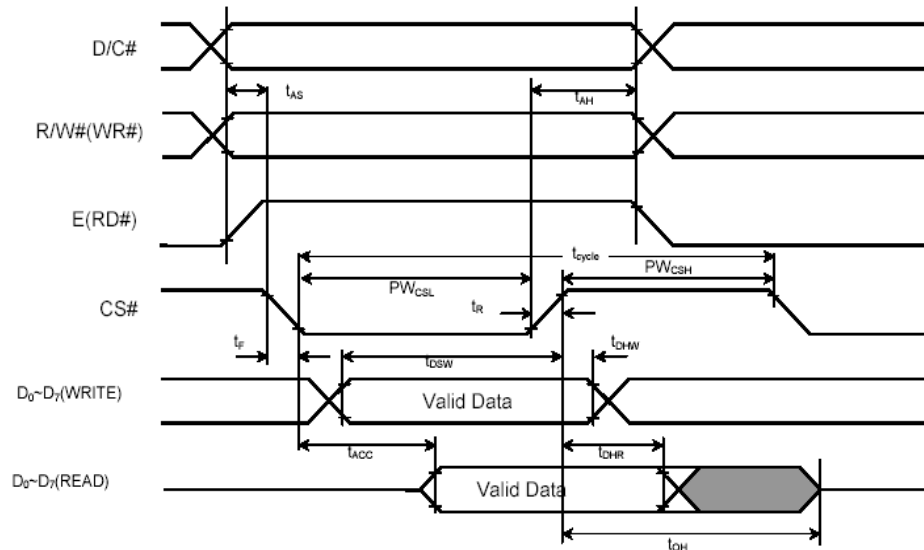
Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns



8080-series MPU Parallel Interface Characteristics

6800-Series MPU Parallel Interface Timing Characteristics ($V_{DD} - V_{SS} = 2.4$ to $3.5V$, $T_A = 25^\circ C$)

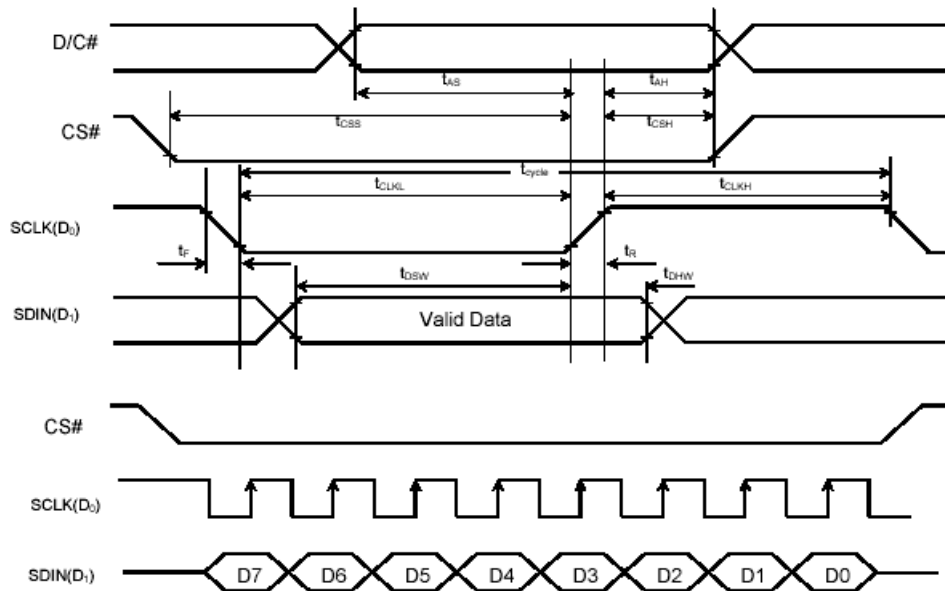
Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns



6800-series MPU Parallel Interface Characteristics

Serial Interface Timing Characteristics ($V_{DD} - V_{SS} = 2.4$ to $3.5V$, $T_A = 25^\circ C$)

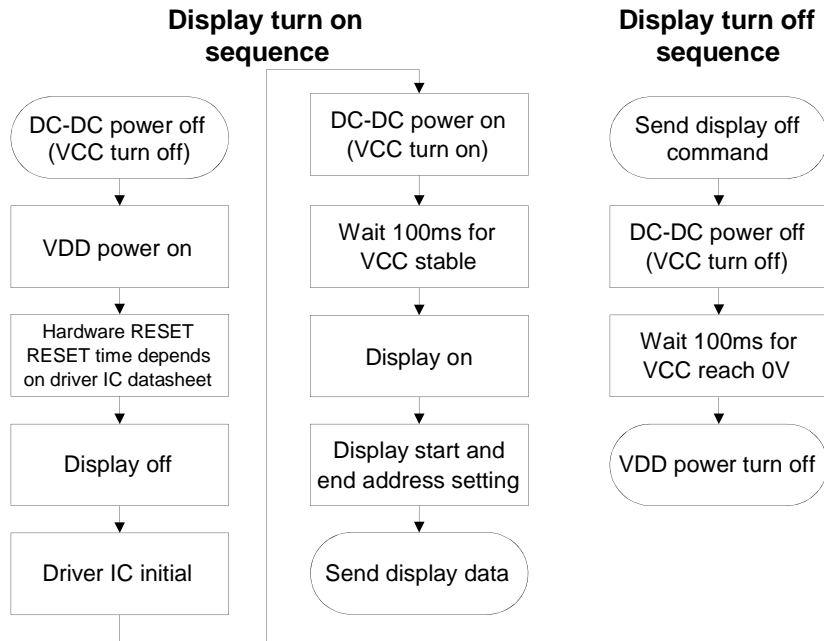
Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	250	-	-	ns
t_{AS}	Address Setup Time	150	-	-	ns
t_{AH}	Address Hold Time	150	-	-	ns
t_{CSS}	Chip Select Setup Time	120	-	-	ns
t_{CSH}	Chip Select Hold Time	60	-	-	ns
t_{DSW}	Write Data Setup Time	100	-	-	ns
t_{DHW}	Write Data Hold Time	100	-	-	ns
t_{CLKL}	Clock Low Time	100	-	-	ns
t_{CLKH}	Clock High Time	100	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns



Serial Interface Characteristics

8. POWER ON / OFF SEQUENCE & APPLICATION CIRCUIT

8.1 POWER ON / OFF SEQUENCE



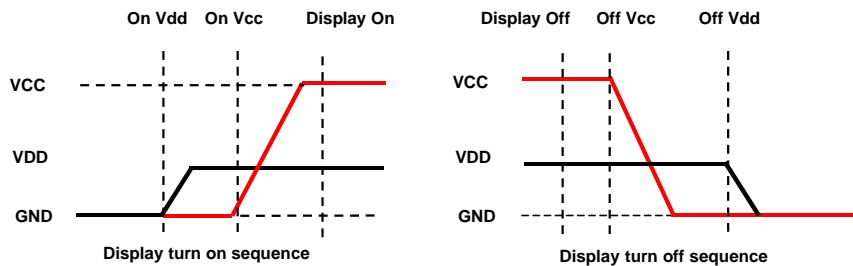
To protect OLED panel and extend the panel lifetime, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources turn on/off.

Power up Sequence:

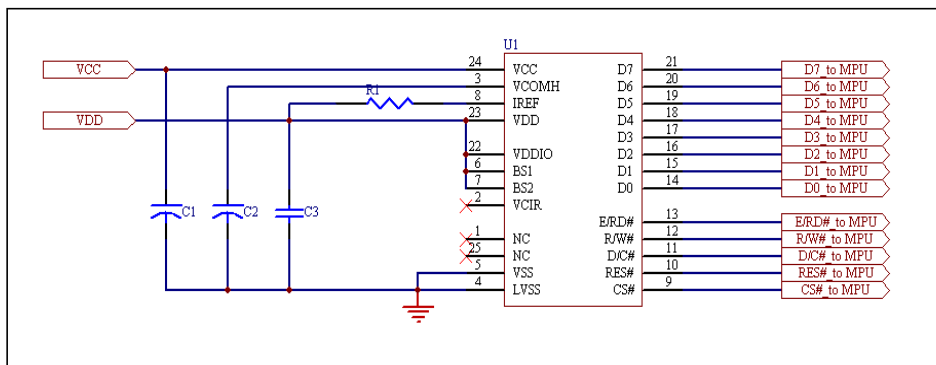
1. Power up Vdd
2. Hardware RESET
3. Send display off command
4. Power up Vcc
5. Delay 100ms (when Vcc is stable)
6. Send Display on command

Power down Sequence:

1. Send Display off command
2. Power down Vcc
3. Delay 100ms (When Vcc is reach 0 and panel is completely discharges)
4. Power down Vdd



8.2 APPLICATION CIRCUIT



- U1: 128x96 OLED module
- C1: 4.7uF, tantalum type
- C2: 1uF, tantalum type
- C3: 0.1uF
- R1: 200 K ohm, tolerance 1%

8.3 COMMAND TABLE

Refer to IC Spec.: SSD1329

9. RELIABILITY TEST CONDITIONS

No.	Items	Specification	Quantity
1	High temp. (Non-operation)	85°C, 240hrs	5
2	High temp. (Operation)	70°C, 120hrs	5
3	Low temp. (Operation)	-40°C, 120hrs	5
4	High temp. / High humidity (Operation)	65°C, 90%RH, 120hrs	5
5	Thermal shock (Non-operation)	-40°C ~85°C (-40°C /30min; transit /3min; 85°C /30min; transit /3min) 1cycle: 66min, 100 cycles	5
6	Vibration	Frequency : 5~50HZ, 0.5G Scan rate : 1 oct/min Time : 2 hrs/axis Test axis : X, Y, Z	1 Carton
7	Drop	Height: 120cm Sequence : 1 angle □ 3 edges and 6 faces Cycles: 1	1 Carton
8	ESD (Non-operation)	Air discharge model, ±8kV, 10 times	5

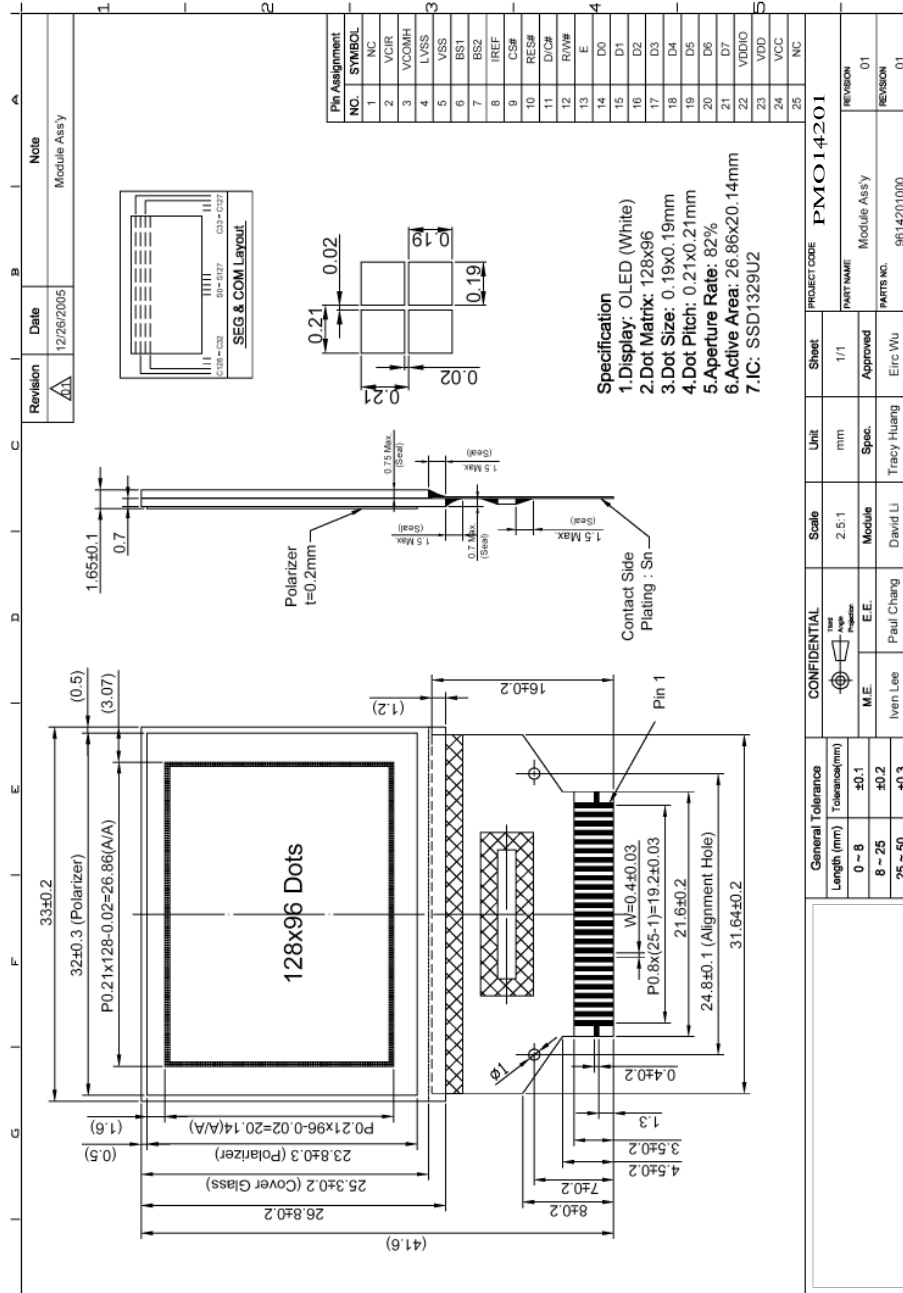
Test and measurement conditions

1. All measurements shall not be started until the specimens attain to temperature stability.
2. All-pixels-on is used as operation test pattern.
3. The degradation of Polarizer are ignored for item 1 & 4.

Evaluation criteria

1. The function test is OK.
2. No observable defects.
3. Luminance: > 50% of initial value.
4. Current consumption: within ± 50% of initial value.

10. EXTERNAL DIMENSION



11. PACKING SPECIFICATION

TBD

12. APPENDIXES

APPENDIX 1: DEFINITIONS

A. DEFINITION OF CHROMATICITY COORDINATE

The chromaticity coordinate is defined as the coordinate value on the CIE 1931 color chart for R, G, B, W.

B. DEFINITION OF CONTRAST RATIO

The contrast ratio is defined as the following formula:

$$\text{Contrast Ratio} = \frac{\text{Luminance of all pixels on measurement}}{\text{Luminance of all pixels off measurement}}$$

C. DEFINITION OF RESPONSE TIME

The definition of turn-on response time T_r is the time interval between a pixel reaching 10% of steady state luminance and 90% of steady state luminance. The definition of turn-off response time T_f is the time interval between a pixel reaching 90% of steady state luminance and 10% of steady state luminance. It is shown in Figure 2.

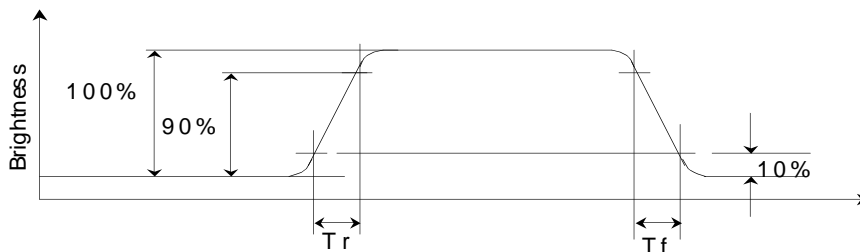


Figure 2 Response time

D. DEFINITION OF VIEWING ANGLE

The viewing angle is defined as Figure 3. Horizontal and vertical (H & V) angles are determined for viewing directions where luminance varies by 50% of the perpendicular value.

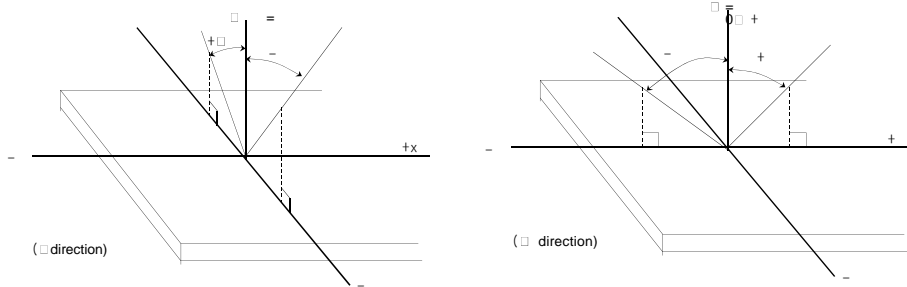
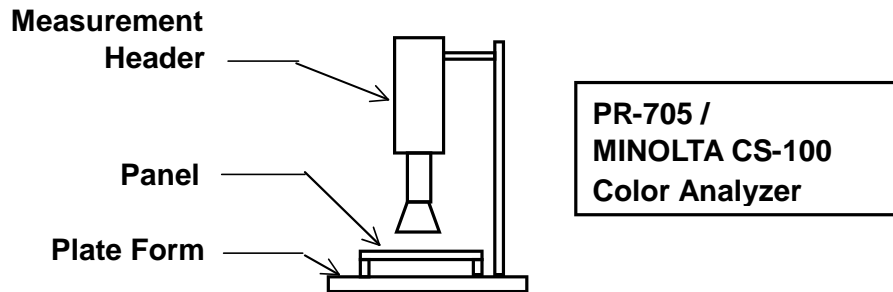


Figure 3 Viewing angle

APPENDIX 2: MEASUREMENT APPARATUS

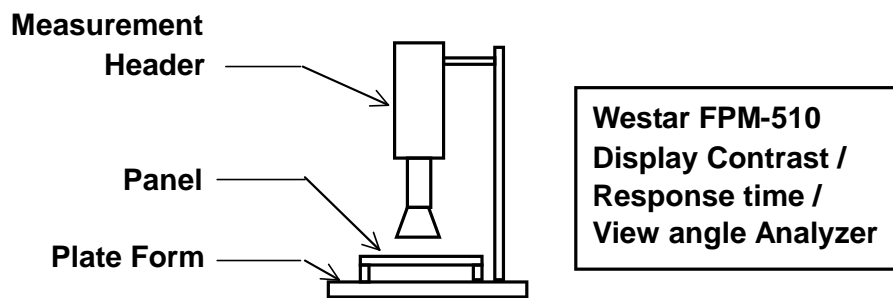
A. LUMINANCE/COLOR COORDINATE

PHOTO RESEARCH PR-705, MINOLTA CS-100

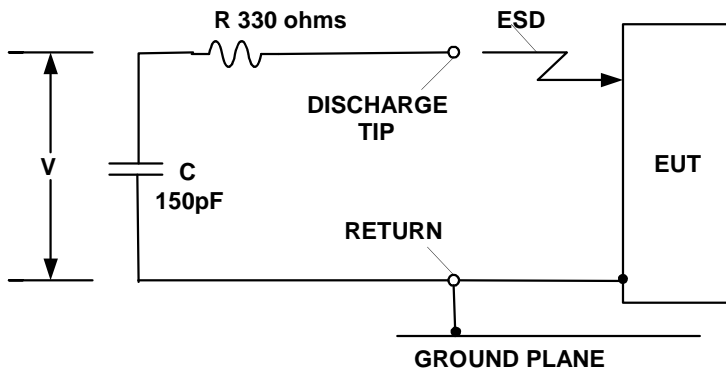


B. CONTRAST / RESPONSE TIME / VIEW ANGLE

WESTAR CORPORATION FPM-510



C. ESD ON AIR DISCHARGE MODE



APPENDIX 3: PRECAUTIONS

A. RESIDUE IMAGE

Because the pixels are lighted in different time, the luminance of active pixels may reduce or differ from inactive pixels. Therefore, the residue image will occur. To avoid the residue image, every pixel needs to be lighted up uniformly.