Evaluating the ADF4378 Microwave Wideband Synthesizer with Integrated VCO and Deterministic General-Purpose Pulse Retimer

FEATURES

- Self-contained board, including ADF4378 frequency synthesizer with integrated VCO, loop filter, USB interface, on-board reference oscillator, propagation delay calibration paths, and voltage regulators
- Windows®-based software allows control of synthesizer functions from a PC
- Externally powered by 6 V

EVALUATION BOARD CONTENTS

- EV-ADF4378SD1Z evaluation board

EQUIPMENT NEEDED

- Windows-based PC with USB port for evaluation software
- System demonstration platform, serial only (SDP-S) EVAL-SDP-CS1Z controller board
- Power supply (6 V)
- Spectrum analyzer or phase noise analyzer, oscilloscope or digital communication analyzer (DCA)
- 50 Ω terminators
- Low noise REFIN source (optional)
- SYSREF clock

DOCUMENTS NEEDED

- ADF4378 data sheet

SOFTWARE REQUIRED

- ACE software, Version 1.26 or newer
- ADF4378 plugin, Version 1.2022.48100 or newer

GENERAL DESCRIPTION

The EV-ADF4378SD1Z evaluates the performance of the ADF4378 frequency synthesizer with an integrated voltage controlled oscillator (VCO) for phase-locked loops (PLLs). A photograph of the EV-ADF4378SD1Z is shown in Figure 1. The EV-ADF4378SD1Z contains the ADF4378 frequency synthesizer with an integrated VCO, a USB interface, power supply connectors, on-board reference oscillator, propagation delay calibration paths, and Subminiature Version A (SMA) connectors. The outputs are AC-coupled with 50 Ω transmission lines, which make the outputs suitable to drive 50 Ω impedance instruments. The EV-ADF4378SD1Z requires an SDP-S board (not supplied with the kit). The SDP-S allows software programming of the EV-ADF4378SD1Z with ACE software.

Full specifications on the ADF4378 frequency synthesizer are available in the ADF4378 data sheet available from Analog Devices, Inc., and must be consulted with this user guide when using the EV-ADF4378SD1Z evaluation board.

EVALUATION BOARD PHOTOGRAPH

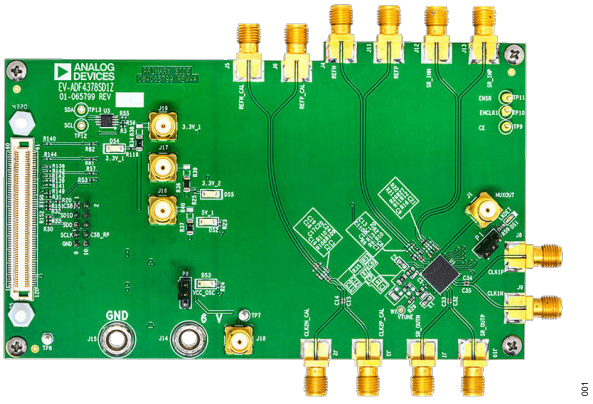


Figure 1. EV-ADF4378SD1Z Evaluation Board Photograph

TABLE OF CONTENTS

REVISION HISTORY

12/2023—Revision 0: Initial Version

GETTING STARTED

SOFTWARE INSTALLATION PROCEDURES

To install the ACE software and ADF4378 plugin, do the following steps:

1. Install the latest version of the ACE software platform.
2. If the ADF4378 plugin appears automatically, proceed to Step 4.
3. Double-click the ADF4378 plugin file, **Board.ADF4378.1.2022.48100.acezip**.
4. Check that the ADF4378 plugin appears when the EV-ADF4378SD1Z is attached through the system demonstration platform (SDP) connector to the PC, as shown in Figure 3.

EVALUATION BOARD SETUP PROCEDURES

The EV-ADF4378SD1Z setup diagram is shown in Figure 2. The EV-ADF4378SD1Z uses a single 6 V power supply with J14 and J15 banana plugs or a J12 SMA connector by default. On-board low noise and low dropout (LDO) regulators are used to generate nominal 3.3 V and 5 V supplies.

For more details on the power supply circuitry, see the Power Supplies section.

To power-up the EV-ADF4378SD1Z, do the following steps:

1. Set the voltage of the power supply to 6 V and the current limit to 1 A.
2. Connect power cables to J14 and J15 (two banana cables) or to J18 (single SMA cable).
3. Turn on the power.

To run the software, do the following steps:

1. Select **Start** > **All Programs** > **Analog Devices** > **ACE**.
2. On the **Select Device and Connection** tab, choose **ADF4378** and the EV-ADF4378SD1Z appears as shown in Figure 3 under **Attached Hardware**.
3. When connecting the EV-ADF4378SD1Z, allow 5 sec to 10 sec for the label on the status bar to change.

EVALUATION BOARD HARDWARE

The EV-ADF4378SD1Z requires the SDP-S platform that uses the EVAL-SDP-CS1Z.

The EV-ADF4378SD1Z schematics are shown in Figure 8, Figure 9, Figure 10, and Figure 11.

POWER SUPPLIES

The EV-ADF4378SD1Z is powered by a 6 V power supply connected to the J12 SMA, or the banana plug, J14, and GND to the banana plug, J15.

The power supply circuitry has three LT3045 and one LT3042 high performance, low noise, and LDO regulators.

One LT3045 is used to generate 5 V to drive the VCO supply pins. The other two LT3045 provide 3.3 V supplies for Supply Group 1 and Supply Group 2.

Component placement for single 6 V supply is shown in Table 1. The EV-ADF4378SD1Z provides the flexibility to use external 3.3 V and 5 V supplies with component placement changes shown in Table 2.

Table 1. Component Placement for Power Supplies for Single 6 V Supply

	3.3 V Supply Group 1		3.3 V Supply Group 2		5 V Supply Group 1	
6 V	**R34**	**R38**	**R36**	**R39**	**R37**	**R40**
Component	0 Ω	Do not install (DNI)	0 Ω	DNI	0 Ω	DNI
Connector	J14 and J15 banana plug or J12 SMA connector					

Table 2. Component Placement for Power Supplies for External Supplies

	3.3 V Supply Group 1		3.3 V Supply Group 2		5 V Supply Group 1	
External Supply	**R34**	**R38**	**R36**	**R39**	**R37**	**R40**
Component	DNI	0 Ω	DNI	0 Ω	DNI	0 Ω
Connector	J19		J17		J16	

The LT3042 is used to generate 5 V to drive the on-board ultra-low phase noise sine wave oscillator.

REFERENCE INPUT

The EV-ADF4378SD1Z has an on-board 125 MHz ultra-low phase noise sine wave oscillator to drive the ADF4378 reference input. The single-ended oscillator output is connected to the REFP pin, and the REFN pin is AC grounded.

The Y2 reference footprint supports 5 mm x 7.5 mm and 14 mm x 9 mm packages in the 4-pin or 6-pin format. The R87 and R91 resistors can be populated if there is a need to set the control voltage of an alternative voltage controlled crystal oscillator (VCXO).

The default oscillator supply voltage is set to 5 V. If an alternative oscillator requires a different supply voltage, the resistor of the LT3042, R17, can be changed to provide the required supply voltage.

The reference input can also be driven externally via a pair of SMA connectors, REFN (J4), and REFP (J11). The on-board oscillator supply must be disabled when using an external reference.

Table 3 provides the required EV-ADF4378SD1Z modifications for the external reference clock.

The ADF4378 has a configurable reference input buffer whose performance can be optimized for different reference slew rates, amplitudes, and frequencies. For more information on the REF_SEL bit, BST_REF bit, and FILT_REF bit, refer to the ADF4378 data sheet.

For detailed reference buffer amplitude and frequency considerations, refer to the ADF4378 data sheet.

Table 3. Component Placement for Different Reference Sources

	Default On-Board Oscillator	Single-Ended External Reference	Differential External Reference	
Component			**CML/LVPECL**	**LVDS**
P8	Short Pin 1 and Pin 2	Short Pin 2 and Pin 3	Short Pin 2 and Pin 3	Short Pin 2 and Pin 3
C120	1 µF	Remove C120	Remove C120	Remove C120
C13	DNI	1 µF	1 µF	1 µF
C110	DNI	DNI	1 µF	1 µF
R9	0 Ω	0 Ω	Remove R9	Remove R9
R10	49.9 Ω	49.9 Ω	Remove R10	Remove R10
R13	DNI	DNI	100 Ω	100 Ω

SYSREF INPUT/OUTPUT

The EV-ADF4378SD1Z has differential SYSREF clock input through J12 and J13 SMA connectors, which can be used to retime SYSREF clocks with respect to reference clock. Retimed output clock is available on J7 and J10 SMA connectors. SYSREF output buffer is disabled with the default register settings. To enable it, in the **POWER-DOWN** area, clear the **PD_SYSREFOUT** box, as shown in Figure 6.

SYSREF input buffer can be configured to interface CML/LVPECL or LVDS signal levels using SR_SEL bit field. SR_SEL bit field sets the input common-mode voltage of the buffer to 1.85 for CML / LVPECL signals and 1.3 V for LVDS signals.

SYSREF monitor is used to determine whether SYSREF signal has valid setup and hold time with respect to reference input. If the setup and hold time of SYSREF clock is valid, SR_OK bit field returns 1. RST_SR_MON bit field should be toggled to reset the SYSREF monitor status before checking the SR_OK status.

INV_SR bit field is used to change the retiming edge of output clock. It is set to 0 by default. When IV_SR is set to 1, SYSREF output is delayed by half output clock cycle. If additional delay is required on the SYSREF output, SR_SEL bit field can be set to add additional delay to SYSREF output.

EVALUATION BOARD HARDWARE

CLOCK OUTPUT

The EV-ADF4378SD1Z has two SMA connectors for the CLKP/CLKN a differential clock outputs.

The output power of clock output channel can be adjusted by the software.

The clock output channel can be powered-down by the software or hardware.

If only one port of a differential pair is used, terminate the complementary port with an equal load terminator (in general, a 50 Ω terminator). For more information on output termination examples, refer to the ADF4378 data sheet.

CALIBRATION PATH

The EV-ADF4378SD1Z calibration path has two pairs of SMA connectors, which are labeled REFN_CAL/REFP_CAL and CLK2P_CAL/CLK2N_CAL. The calibration path is used to measure and calibrate out the EV-ADF4378SD1Z effect on reference to output delay.

LOOP FILTER

The loop filter schematic is included in Figure 8. The fifth order loop filter on the EV-ADF4378SD1Z is optimized for the ADF4378 low noise amplifier (LNA) reference amplifier, a 6 dBm sine wave reference frequency of 125 MHz, a phase frequency detector (PFD) frequency of 250 MHz, and an 11.1 mA charge-pump current. A fourth order loop filter may be used with faster slew-rate reference signals that allow for use of the delay matched amplifier (DMA) reference amplifier of the ADF4378. For more information on loop filter design, refer to the ADF4378 data sheet.

SERIAL PERIPHERAL INTERFACE (SPI)

Connector P5 interfaces with the SDP-S to evaluate the ADF4378 using the ACE graphical user interface (GUI) software. A second connector, P2, is provided for software development. The P2 connector allows for a common open source hardware (OSH) board, such as a peripheral module (Pmod™), Raspberry Pi, and SDP-K1, to interface directly with the EV-ADF4378SD1Z.

DEFAULT CONFIGURATION

All components necessary for local oscillator (LO) generation are installed on the EV-ADF4378SD1Z. The EV-ADF4378SD1Z is shipped with an 125 MHz crystal oscillator (XO), the ADF4378 synthesizer with an integrated VCO, and a 650 kHz loop filter (charge-pump current (I_{CP}) = 11.1 mA) at 10 GHz. When the EV-ADF4378SD1Z is powered-up and connected to the ACE software, click the **LoadDefault** and **Write All Registers/ Initialize** buttons, as shown in Figure 5, which provides a 10 GHz output clock on both clock output channels.

EVALUATION BOARD HARDWARE

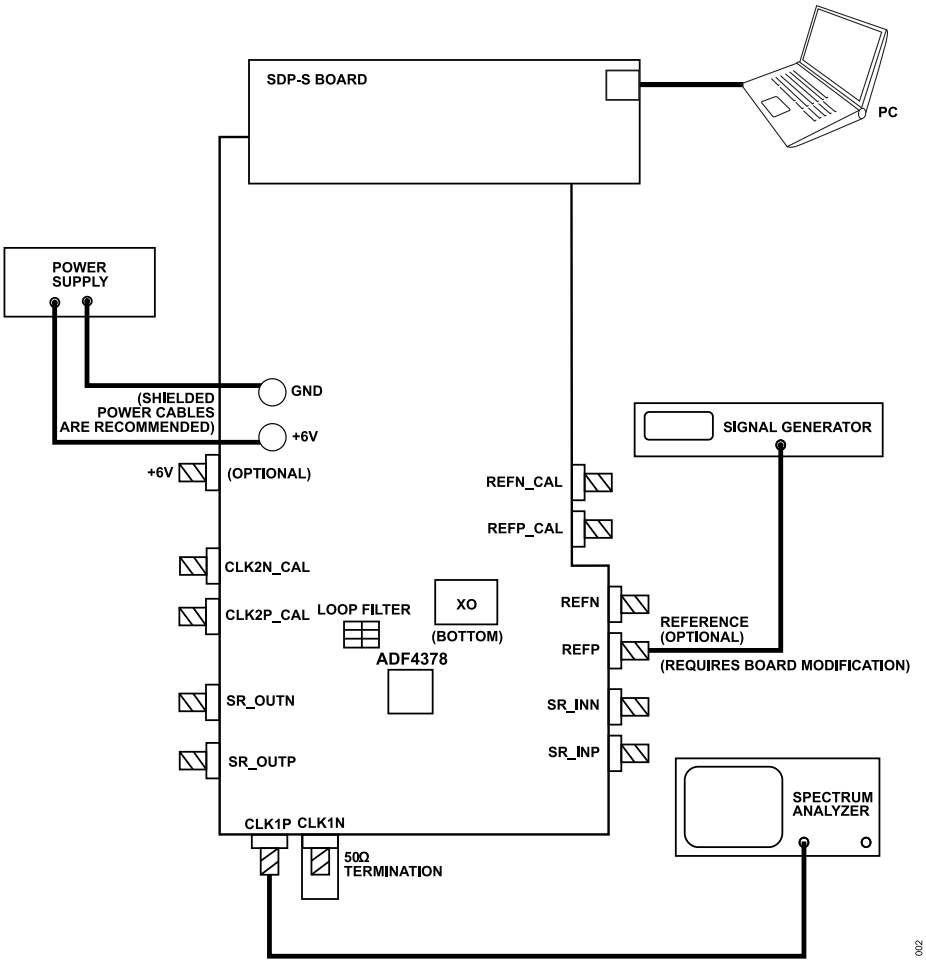


Figure 2. EV-ADF4378SD1Z Setup Diagram

EVALUATION BOARD SOFTWARE

The ACE software is the main platform that is used to control the EV-ADF4378SD1Z. The ADF4378 plugin includes user interfaces that relate to the ADF4378 and allow evaluation of the device. Do the following steps to open the main control window for the ADF4378:

1. Launch the ACE application. With the SDP-S board connected to the EV-ADF4378SD1Z, the attached hardware appears in the GUI, as shown in Figure 3.
2. Double-click the **ADF4378 Board** button, and the **ADF4378 Board** tab appears, as shown in Figure 4.
3. Double-click the **ADF4378** button that appears in Figure 4 to open the main control window, as shown in Figure 5.

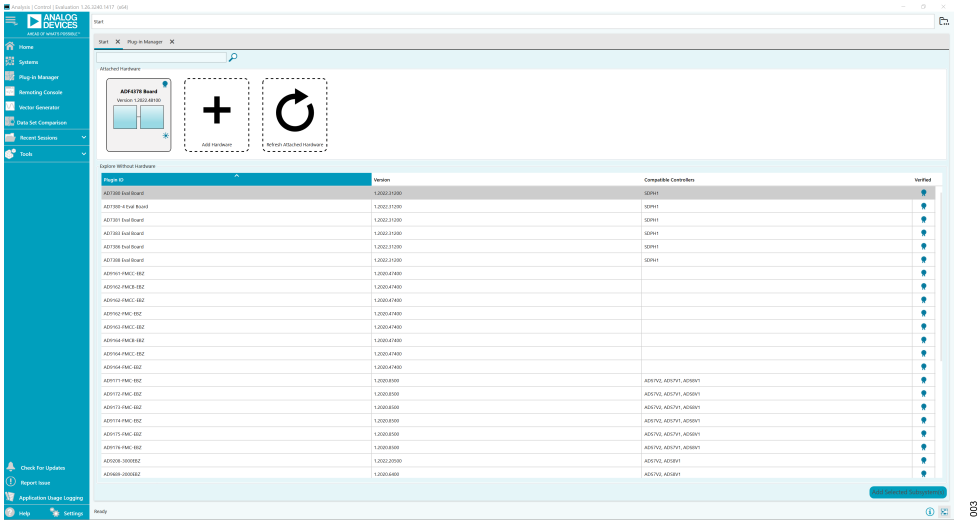


Figure 3. ACE Start Page, Attached Hardware (ADF4378 Board Button)

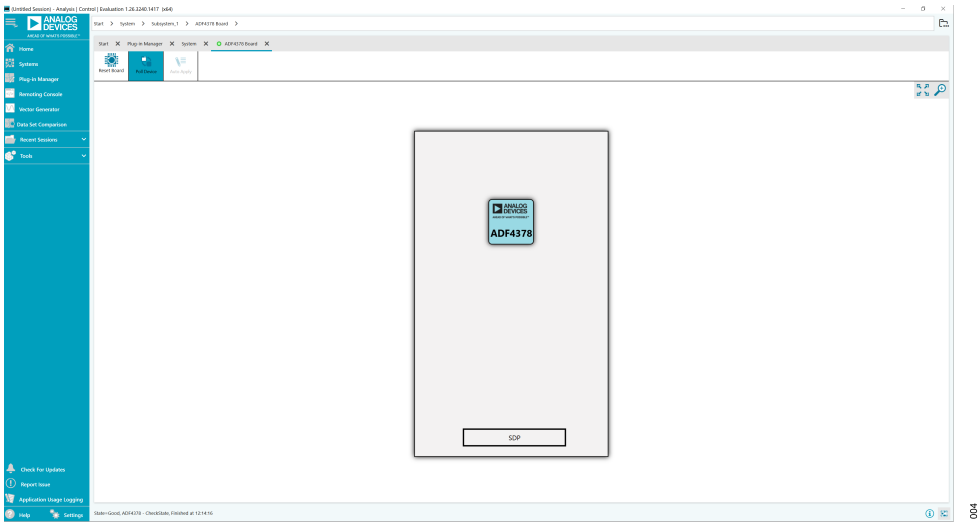


Figure 4. ACE Board Page, Device Selection

EVALUATION BOARD SOFTWARE

MAIN CONTROLS

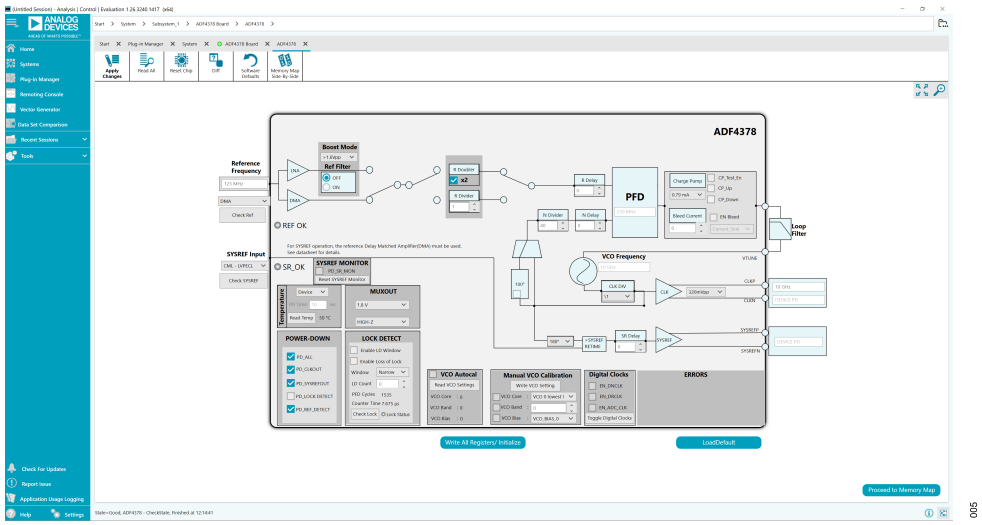
The main controls are available in the high-level register map, as shown in Figure 5. To modify registers, do the following steps:

1. ACE plug-in is opened with power-on reset register values. The **LoadDefault** button must be clicked to load the suggested register settings for initialization.
2. After clicking **LoadDefault**, any changes to the configuration can be made before writing to device.
3. Click **Write All Registers/ Initialize** to load all registers and initialize the device.
4. Modify the registers as required.

Click **Apply Changes** to load modified settings to the device. This action loads the updated registers only. All registers can be reloaded using the **Write All Registers/ Initialize** button.

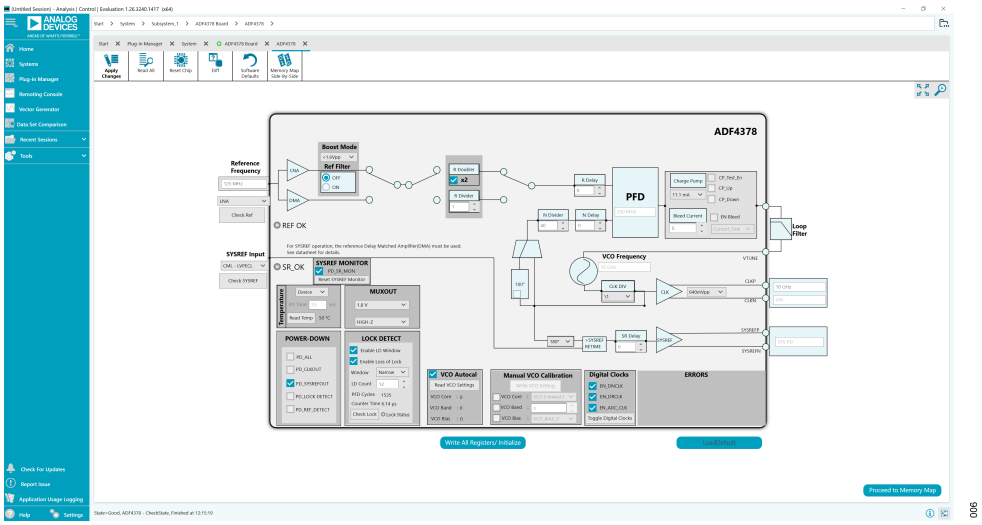
The following list provides some miscellaneous tips to aid in executed common task:

- If VCO frequency or output frequency is outside of the operational range, an error message appears under the **ERRORS** box of the window.
- To power-down specific ADF4378 blocks, see the **POWER-DOWN** list in the window.
- To save a specific ADF4378 register configuration, click **Memory Map Side-By-Side** and then click **Export**. This exports the register values to a .csv file.



005

Figure 5. Main Page



006

Figure 6. Main Page After Loading Suggested Register Settings

EVALUATION AND TEST

To evaluate and test the performance of the ADF4378, prepare the hardware and software setup as explained in the Evaluation Board Hardware and the Evaluation Board Software sections.

Run the software and follow the steps shown in the Evaluation Board Software section to open the main page, as shown in Figure 5.

Click the **LoadDefault** and **Write All Registers/ Initialize** buttons, respectively, which provide an 10 GHz clock at the CLKP/CLKN output. Measure the output spectrum and single-sideband phase noise on a spectrum analyzer.

Figure 7 shows a phase noise plot of the SMA CLKP output equal to 10 GHz with an on-board ultra-low noise sine wave oscillator (250 MHz PFD frequency).

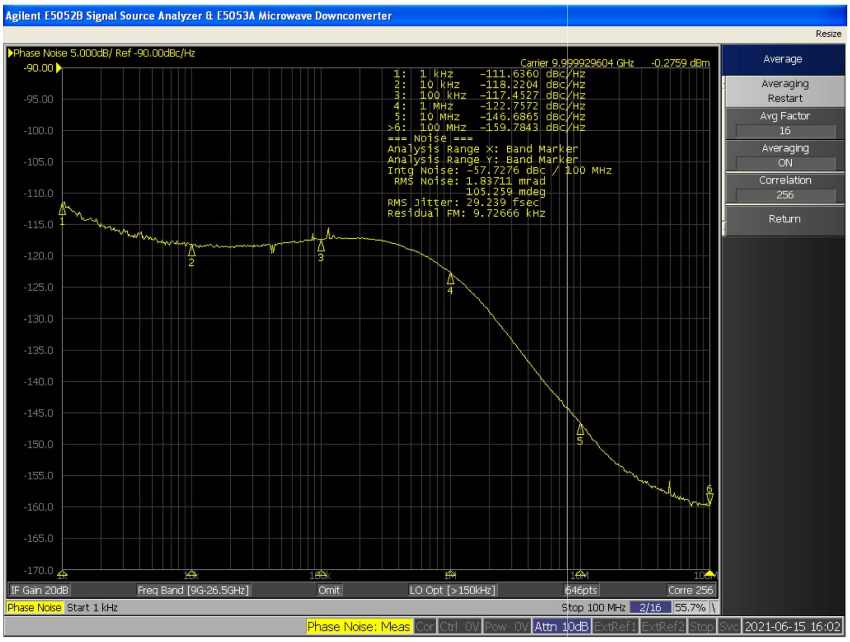


Figure 7. Single-Sideband Phase Noise of 10 GHz Output with On-Board 125 MHz Oscillator

EVALUATION BOARD SCHEMATIC AND ARTWORK

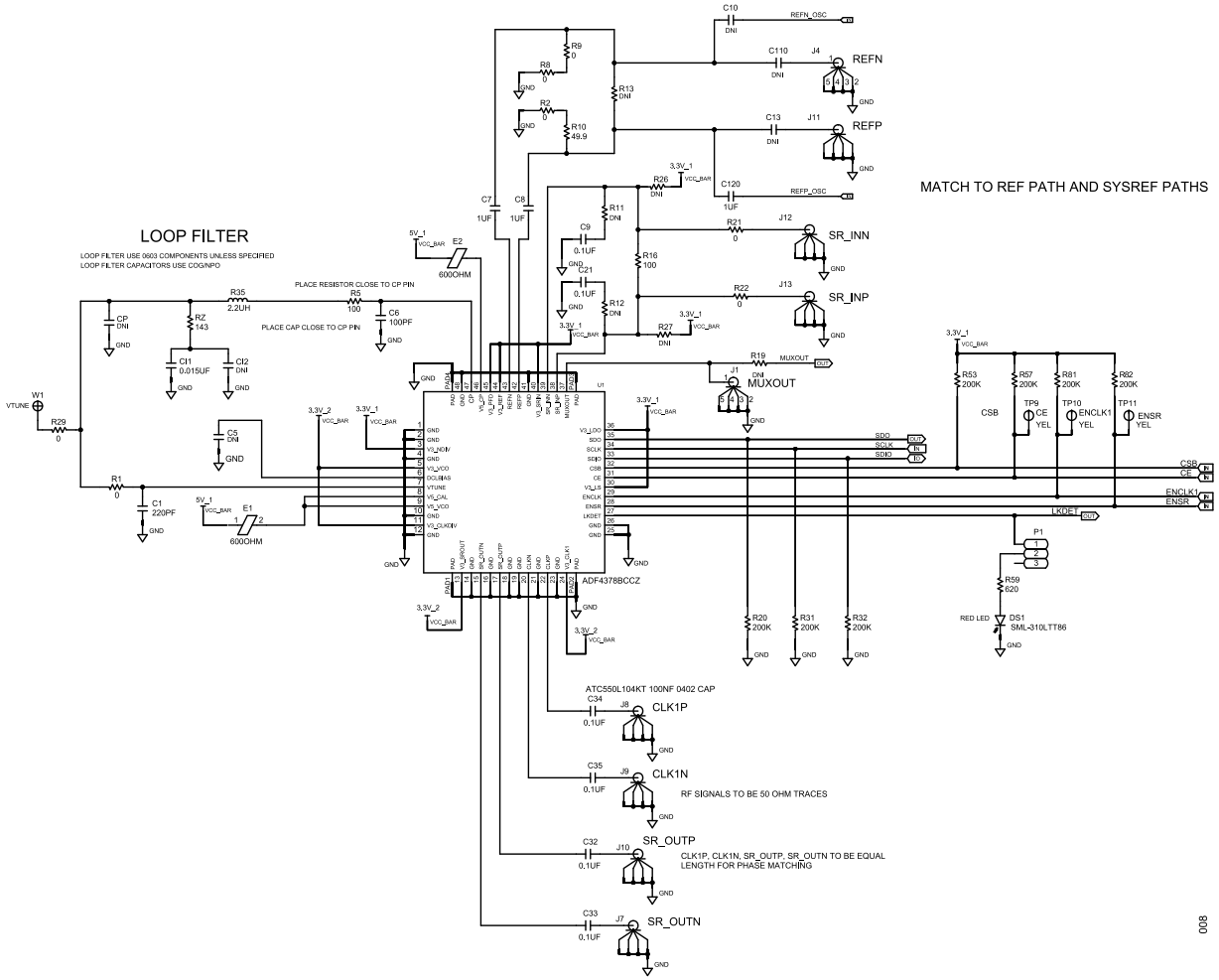


Figure 8. EV-ADF4378SD1Z Schematic, ADF4378 Connections and Loop Filter

EVALUATION BOARD SCHEMATIC AND ARTWORK

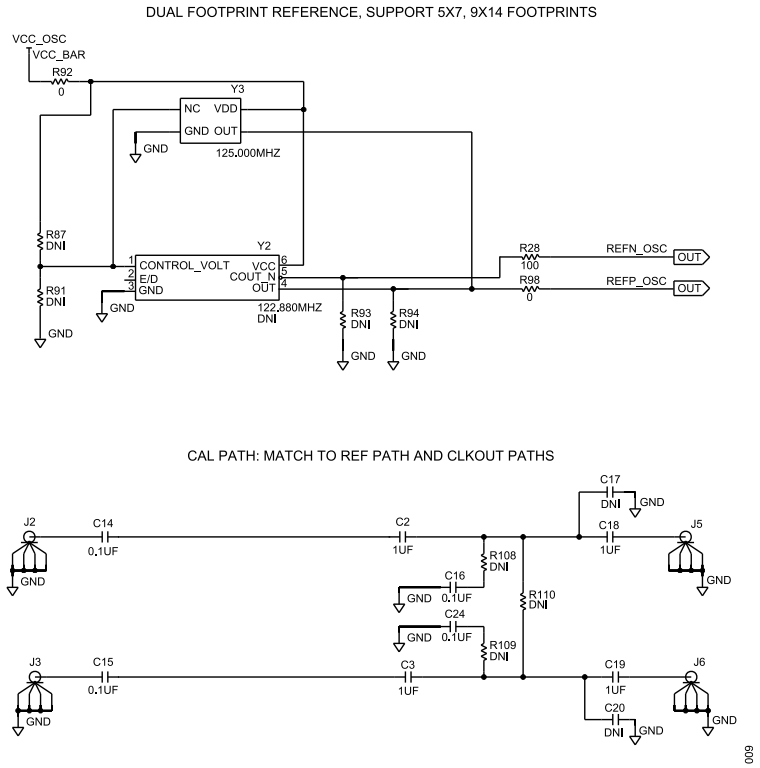


Figure 9. EV-ADF4378SD1Z Schematic, On-Board Ultra-Low Noise Oscillator and Calibration Path

EVALUATION BOARD SCHEMATIC AND ARTWORK

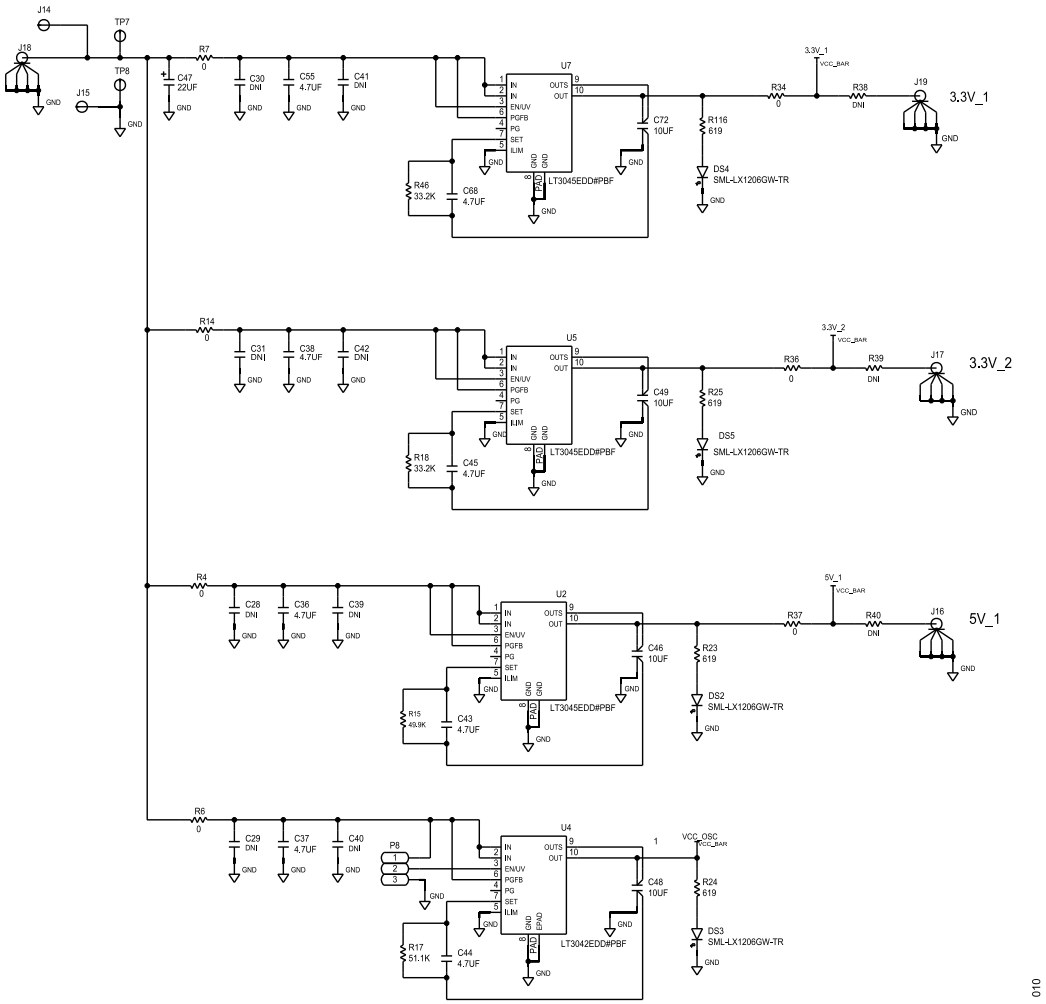


Figure 10. EV-ADF4378SD1Z Schematic, LDO Regulators

EVALUATION BOARD SCHEMATIC AND ARTWORK

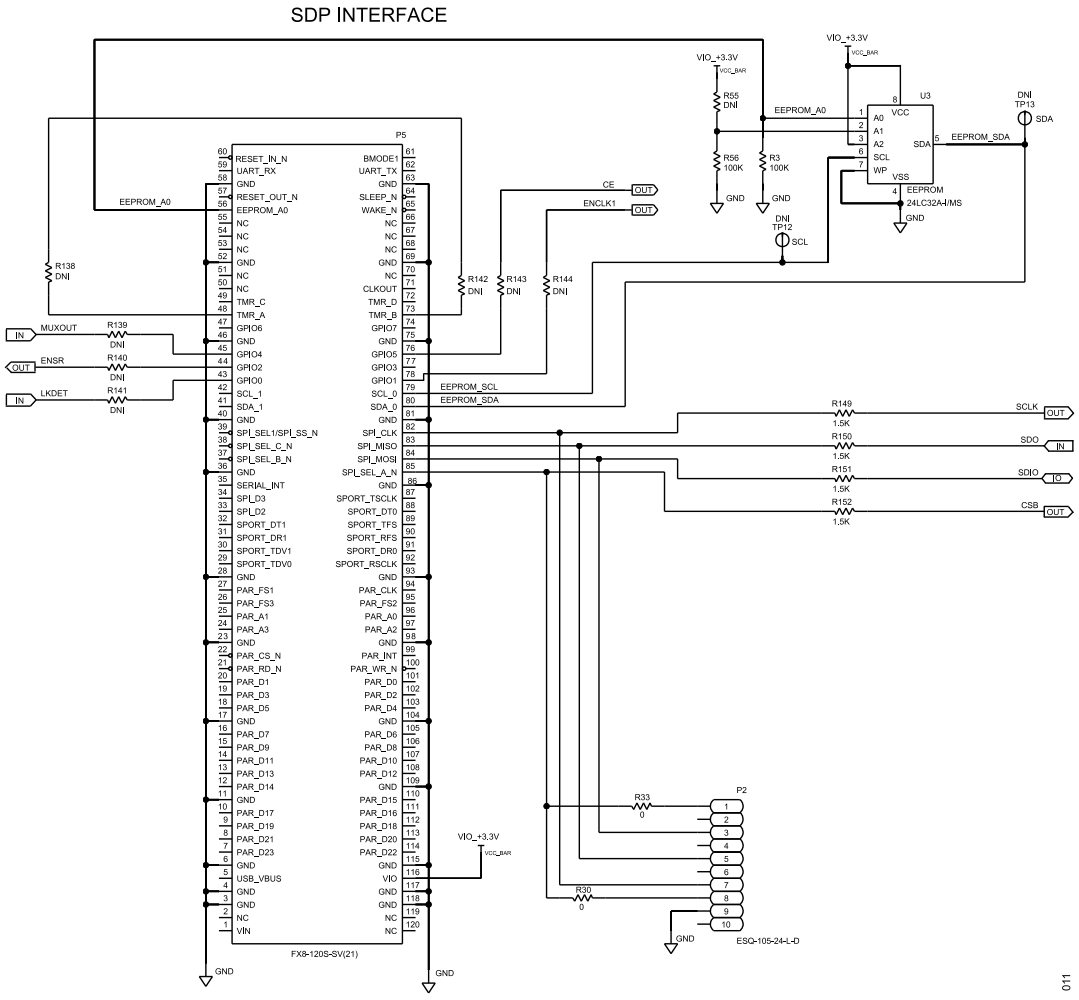


Figure 11. EV-ADF4378SD1Z Schematic, SDP Interface

EVALUATION BOARD SCHEMATIC AND ARTWORK

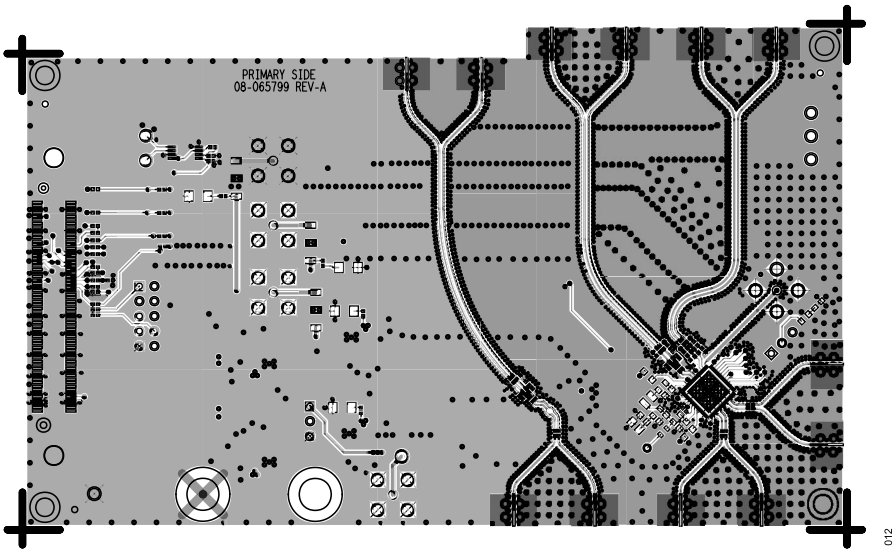


Figure 12. EV-ADF4378SD1Z Layer 1, Primary

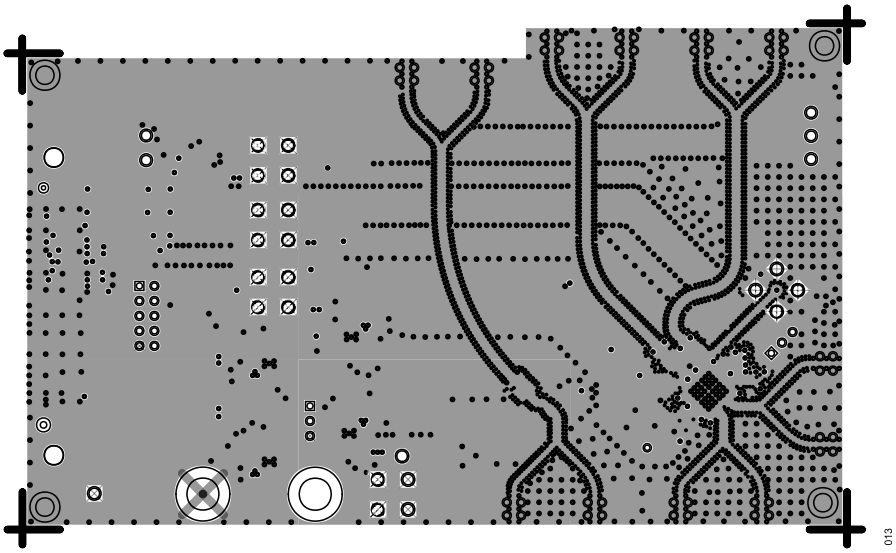


Figure 13. EV-ADF4378SD1Z Layer 2, Ground

EVALUATION BOARD SCHEMATIC AND ARTWORK

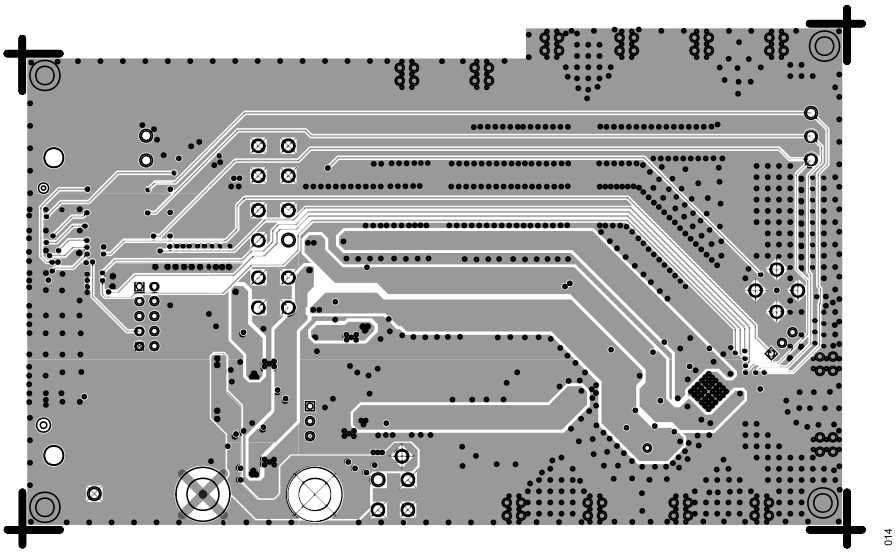


Figure 14. EV-ADF4378SD1Z Layer 3, Power

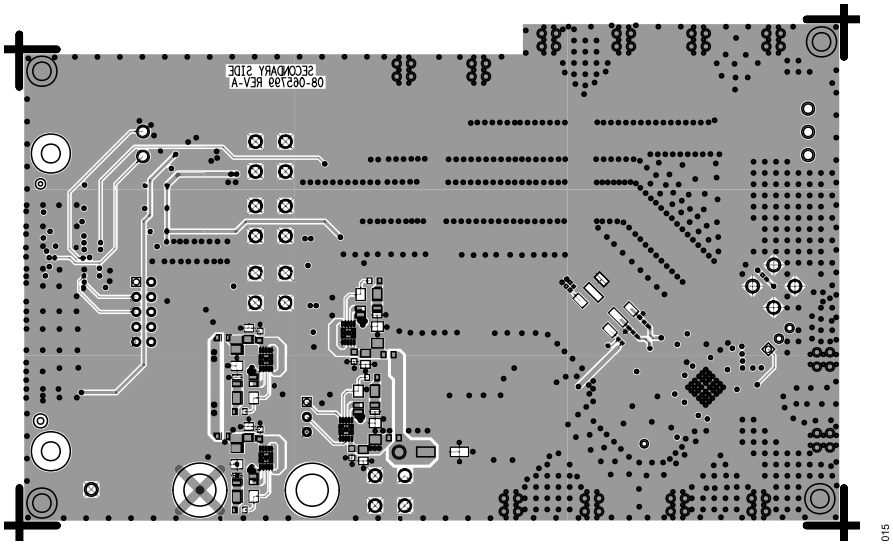


Figure 15. EV-ADF4378SD1Z Layer 4, Secondary

EVALUATION BOARD SCHEMATIC AND ARTWORK

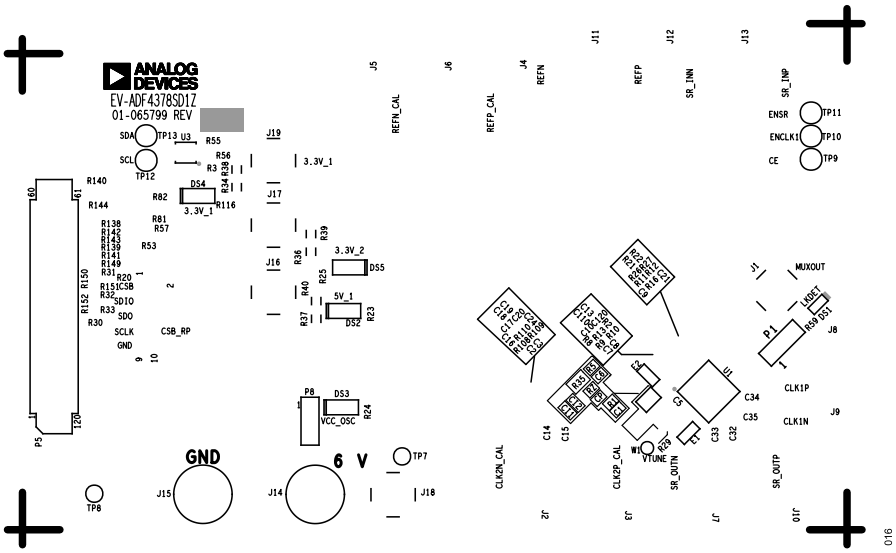


Figure 16. EV-ADF4378SD1Z Silkscreen, Top Side

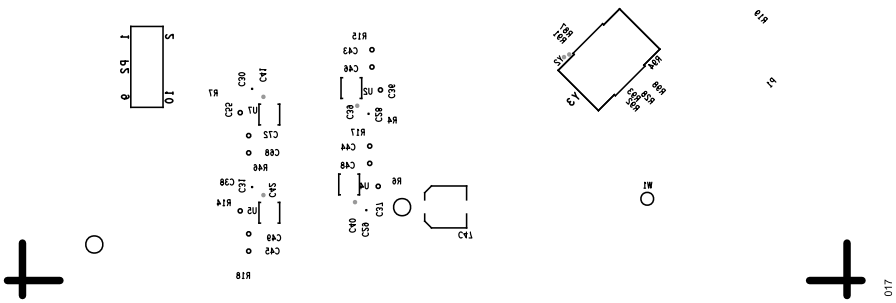


Figure 17. EV-ADF4378SD1Z Silkscreen, Bottom Side

ORDERING INFORMATION

BILL OF MATERIALS

Table 4. Bill of Materials for EV-ADF4378SD1Z

Quantity	Reference Designator	Description	Manufacturer	Part Number
1	C1	Capacitor, 220 pF, 100 V, 5%, C0G, 0603	Kemet	C0603C221J1GACTU
7	C2, C3, C7, C8, C18, C19, C120	Capacitors, 1 µF, 6.3 V, 10%, X7R, 0402	Murata	GRM155R70J105KA12D
10	C9, C14, C15, C16, C21, C24, C32, C33, C34, C35	Capacitors, 0.1 µF, 16 V, 10%, X7R, 0402	Kemet	C0402C104K4RACTU
8	C36, C37, C38, C43, C44, C45, C55, C68	Capacitors, 4.7 µF, 25 V, 10%, X7R, 1206	Kemet	C1206C475K3RACTU
4	C46, C48, C49, C72	Capacitors, X7R, 4-pins footprint	Taiyo Yuden	GMK316AB7106KL-TR
1	C47	Aluminum electrolytic capacitor, 22 µF, 63 V, 20%, 6.3 mm × 7.7 mm, AEC-Q200	Sun Electronic Ind. Corp.	63CE22BSA
1	C6	Capacitor, 100 pF, 50 V, 5%, C0G, 0603, AEC-Q200, low ESR	TDK	CGA3E2C0G1H101J080AA
1	CI1	Capacitor, 0.015 µF, 50 V, 5%, C0G, 0805	Murata	GRM2195C1H153JA01D
1	DS1	LED red surface mount	Rohm	SML-310LTT86
4	DS2, DS3, DS4, DS5	LED green surface mounts	Lumex	SML-LX1206GW-TR
2	E1, E2	Ferrite beads	Taiyo Yuden	FBMH1608HL601-T
5	J1, J16, J17, J18, J19	SMA jacks, 50 Ω, contact center surface mount with thru hole legs	Amphenol RF	132134-15
12	J2, J3, J4, J5, J6, J7, J8, J9, J10, J11, J12, J13	SMA edge mounts	Emerson Network Power	142-0761-811
2	J14, J15	Banana jacks	Keystone Electronics	575-4
2	P1, P8	3-position male headers, 2.54 mm pitch	Samtec Inc.	TSW-103-08-T-S
1	P2	10-position female header, 2.54 mm pitch	Samtec Inc.	ESQ-105-24-L-D
1	P5	SDP-S connector	Hirose Electric Co. Ltd.	FX8-120S-SV(21)
6	R1, R4, R6, R7, R14, R29	Resistors, 0 Ω jumper, 1/10 W, 0603, AEC-Q200	Panasonic	ERJ-3GEY0R00V
1	R10	Resistor, 49.9 Ω, 1%, 1/10 W, 0402, AEC-Q200	Panasonic	ERJ-2RKF49R9X
3	R34, R36, R37	Resistors, 0 Ω, 5%, 1/4 W, 1206, AEC-Q200	Vishay	CRCW12060000Z0EA
4	R23, R24, R25, R116	Resistors, 619 Ω, 1%, 1/10 W, 0402, AEC-Q200	Panasonic	ERJ-2RKF6190X
4	R149, R150, R151, R152	Resistors, 1.5 kΩ, 1%, 1/16 W, 0402, AEC-Q200	Stackpole Electronics, Inc.	RMCF0402FT1K50
1	R15	Resistor, 49.9 kΩ, 1%, 1/10 W, 0603, AEC-Q200	Panasonic	ERJ-3EKF4992V
1	R17	Resistor, 51.1 kΩ, 1%, 1/10 W, 0603, AEC-Q200	Panasonic	ERJ-3EKF5112V
2	R18, R46	Resistors, 33.2 kΩ, 1%, 1/10 W, 0603, AEC-Q200	Panasonic	ERJ-3EKF3322V
9	R2, R8, R9, R21, R22, R30, R33, R92, R98	Resistors, 0 Ω jumper, 1/10 W, 0402, AEC-Q200	Panasonic	ERJ-2GE0R00X
7	R20, R31, R32, R53, R57, R81, R82	Resistors, 200 kΩ, 1%, 1/10 W, 0402, AEC-Q200	Panasonic	ERJ-2RKF2003X
2	R16, R28	Resistors, 100 Ω, 1%, 1/10 W, 0402, AEC-Q200	Panasonic	ERJ-2RKF1000X
2	R3, R56	Resistors, 100 kΩ, 1%, 1/10 W, 0402, AEC-Q200	Panasonic	ERJ-2RKF1003X
1	R35	Inductor unshielded wirewound, 2.2 µH, 5%, 7.9 MHz, 0.365 A, 1.28 Ω, 0805, AEC-Q200	Coilcraft Inc.	0805LS-222XJLB
1	R5	Resistor, 100 Ω, 1%, 1/10 W, 0603, AEC-Q200	Panasonic	ERJ-3EKF1000V
1	R59	Resistor, 620 Ω, 1%, 1/10 W, 0603, AEC-Q200	Panasonic	ERJ-3EKF6200V
1	RZ	Resistor, 143 Ω, 1%, 1/10 W, 0603, AEC-Q200	Panasonic	ERJ-3EKF1430V
3	TP9, TP10, TP11	Test points, yellow	Components Corporation	TP-104-01-04
2	TP7, TP8	Solder terminal turrets for clip leads	Mill-Max	2308-2-00-80-00-00-07-0
1	U1	Microwave wideband synthesizer with integrated VCO	Analog Devices, Inc.	ADF4378BCCZ
3	U2, U5, U7	20 V, 500 mA, ultra-low noise, ultra-high power supply rejection ratio (PSRR) linear regulator	Linear Technology	LT3045EDD#PBF
1	U3	IC 32 kb serial electronically erasable programmable read-only memory (EEPROM)	Microchip Technology	24LC32A-I/MS

ORDERING INFORMATION

Table 4. Bill of Materials for EV-ADF4378SD1Z (Continued)

Quantity	Reference Designator	Description	Manufacturer	Part Number
1	U4	20 V, 200 mA, ultra-low noise, ultra-high PSRR RF linear regulator	Analog Devices, Inc.	LT3042EDD#PBF
1	Y3	Crystal oscillator, ultra-low noise sine wave clock oscillator	Crystek Corp.	CCSS-945X-25-125.000

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.