Revision in SQJ422EP Datasheet from Rev. A to Rev. B

For further information, please contact your regional Vishay office.

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Description of Change: As part of Vishay Siliconix commitment to Quality, we would like to extend to you a courtesy advisory notification of a datasheet revision for SQJ422EP (Doc #63989 Rev B attached). There is no change to the materials or processes used in the manufacture of this part.

The changes per this Advisory reflect updates as follows:

1) Removed: superscript “c” from AEC-Q101 Qualified; “-T1-GE3” from Ordering Information; and “c. Parametric verification ongoing” from Notes.

2) Renamed: superscript “d, e” of Soldering Recommendation (Peak Temperature) to “c, d”; and Notes “d, e” to “c, d”.

3) Updated: Ciss/Coss/Crss Typ values from 3730pF/553pF/223pF to 4616pF/420pF/182pF; Ciss Max value from 4660pF to 5000pF; and Capacitance chart.

4) Corrected typo for: td(on)/tf/td(off)/tf Rg from “6” to “1”; VSD “VGS=0” to “VGS=0V”; and RthJA chart label from 68 oC/W to 65 oC/W.

Reason for Change: Datasheet Revision

Expected Influence on Quality/Reliability/Performance: None

Part Numbers/Series/Families Affected: SQJ422EP-T1_GE3, SQJ422EP-T1_BE3,

Vishay Brand(S): Vishay Siliconix

Time Schedule:

Start Shipment Date: Wed Feb 14, 2024

Sample Availability: This is a datasheet revision only. There is no change to the materials or processes used in the manufacture of this part.

Product Identification: SQJ422EP-T1_GE3, SQJ422EP-T1_BE3

Qualification Data: N/A

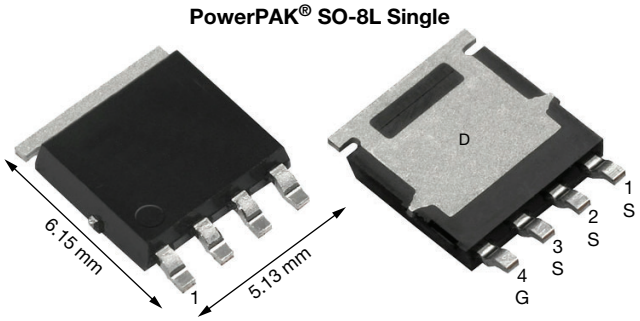
Product Information Notification

Product Group: SIL/Wed Feb 14, 2024/PIN-SIL-008-2024-REV-0

Issued By: Lance Gurrola, automostechsupport@vishay.com

Automotive N-Channel 40 V (D-S) 175 °C MOSFET

PowerPAK® SO-8L Single



Top View Bottom View

FEATURES

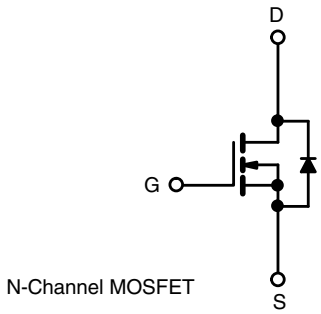
- TrenchFET® power MOSFET
- 100 % R_g and UIS tested
- AEC-Q101 qualified
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

AUTOMOTIVE GRADE

Pb-free

RoHS COMPLIANT

HALOGEN FREE



N-Channel MOSFET

PRODUCT SUMMARY	
V_{DS} (V)	40
$R_{DS(on)}$ (Ω) at V_{GS} = 10 V	0.0034
$R_{DS(on)}$ (Ω) at V_{GS} = 4.5 V	0.0043
I_D (A)	75
Configuration	Single
Package	PowerPAK SO-8L

ORDERING INFORMATION	
Package	PowerPAK® SO-8L
Lead (Pb)-free and halogen-free	SQJ422EP (for detailed order number please see www.vishay.com/doc?79776)

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		V_{DS}	40	V
Gate-source voltage		V_{GS}	± 20	
Continuous drain current	T_C = 25 °C	I_D	75	A
	T_C = 125 °C		62	
Continuous source current (diode conduction)		I_S	75	
Pulsed drain current [a]		I_{DM}	300	
Single pulse avalanche current	L = 0.1 mH	I_{AS}	46	
Single pulse avalanche energy		E_{AS}	105	mJ
Maximum power dissipation	T_C = 25 °C	P_D	83	W
	T_C = 125 °C		27	
Operating junction and storage temperature range		T_J, T_{stg}	-55 to +175	°C
Soldering recommendations (peak temperature) [c, d]			260	

THERMAL RESISTANCE RATINGS

PARAMETER		SYMBOL	LIMIT	UNIT
Junction-to-ambient	PCB mount [b]	R_{thJA}	65	°C/W
Junction-to-case (drain)		R_{thJC}	1.8	

Notes

a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %

b. When mounted on 1" square PCB (FR4 material)

c. See solder profile *(www.vishay.com/doc?73257)*. The PowerPAK SO-8L is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection

d. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components

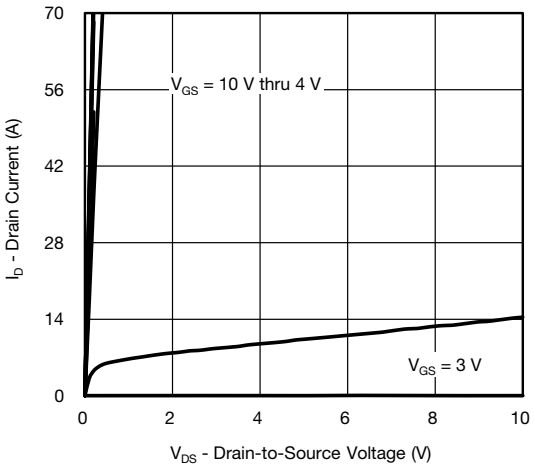
SPECIFICATIONS (T_C = 25 °C, unless otherwise noted)							
PARAMETER	**SYMBOL**	**TEST CONDITIONS**		**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static							
Drain-source breakdown voltage	V_{DS}	V_{GS} = 0, I_D = 250 µA		40	-	-	V
Gate-source threshold voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA		1.5	2.0	2.5	
Gate-source leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V		-	-	± 100	nA
Zero gate voltage drain current	I_{DSS}	V_{GS} = 0 V	V_{DS} = 40 V	-	-	1	µA
		V_{GS} = 0 V	V_{DS} = 40 V, T_J = 125 °C	-	-	50	
		V_{GS} = 0 V	V_{DS} = 40 V, T_J = 175 °C	-	-	150	
On-state drain current [a]	$I_{D(on)}$	V_{GS} = 10 V	V_{DS} ≥ 5 V	30	-	-	A
Drain-source on-state resistance [a]	$R_{DS(on)}$	V_{GS} = 10 V	I_D = 18 A	-	0.0028	0.0034	Ω
		V_{GS} = 4.5 V	I_D = 16 A	-	0.0035	0.0043	
		V_{GS} = 10 V	I_D = 18 A, T_J = 125 °C	-	-	0.0071	
		V_{GS} = 10 V	I_D = 18 A, T_J = 175 °C	-	-	0.0089	
Forward transconductance [b]	g_{fs}	V_{DS} = 15 V, I_D = 18 A		-	117	-	S
Dynamic [b]							
Input capacitance	C_{iss}	V_{GS} = 0 V	V_{DS} = 20 V, f = 1 MHz	-	4616	5000	pF
Output capacitance	C_{oss}			-	420	691	
Reverse transfer capacitance	C_{rss}			-	182	278	
Total gate charge [c]	Q_g	V_{GS} = 10 V	V_{DS} = 20 V, I_D = 10 A	-	67	100	nC
Gate-source charge [c]	Q_{gs}			-	11.25	-	
Gate-drain charge [c]	Q_{gd}			-	10.31	-	
Gate resistance	R_g	f = 1 MHz		0.3	0.63	1.1	Ω
Turn-on delay time [c]	$t_{d(on)}$	V_{DD} = 20 V, R_L = 20 Ω I_D ≅ 10 A, V_{GEN} = 10 V, R_g = 1 Ω		-	13	19	ns
Rise time [c]	t_r			-	10	15	
Turn-off delay time [c]	$t_{d(off)}$			-	29	44	
Fall time [c]	t_f			-	8	12	
Source-Drain Diode Ratings and Characteristics [b]							
Pulsed current [a]	I_{SM}			-	-	300	A
Forward voltage	V_{SD}	I_F = 12 A, V_{GS} = 0 V		-	0.75	1.1	V

Notes

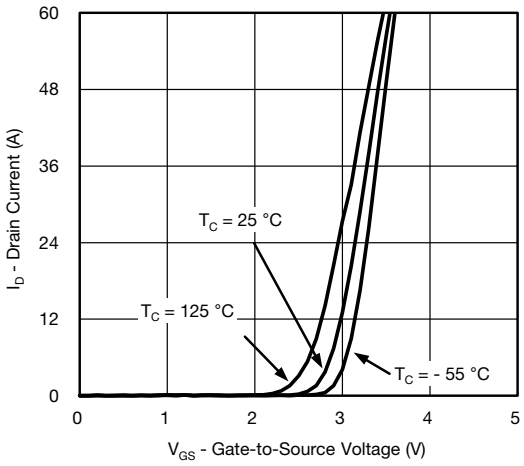
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %
b. Guaranteed by design, not subject to production testing
c. Independent of operating temperature

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

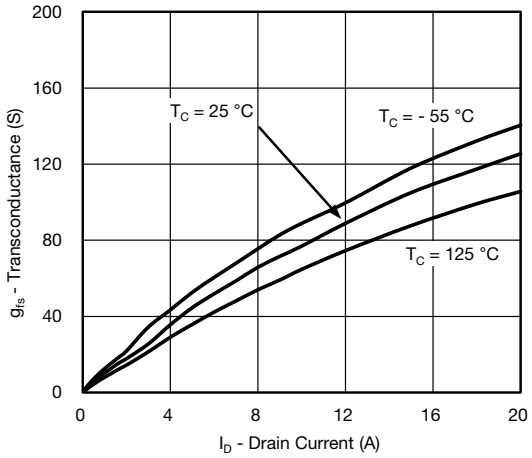
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



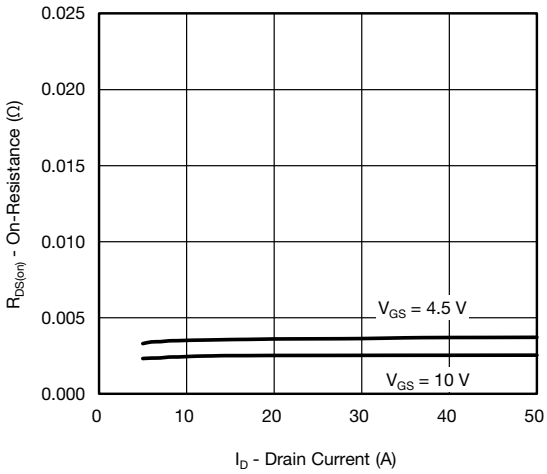
Output Characteristics



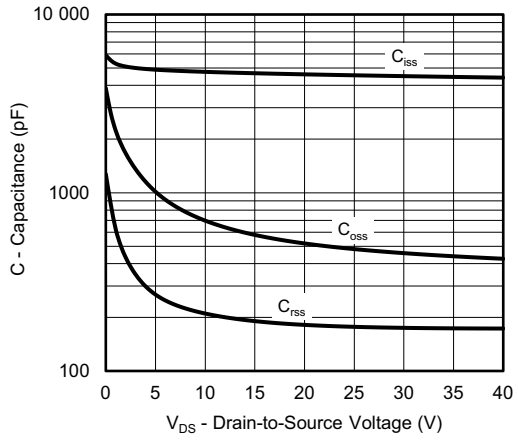
Transfer Characteristics



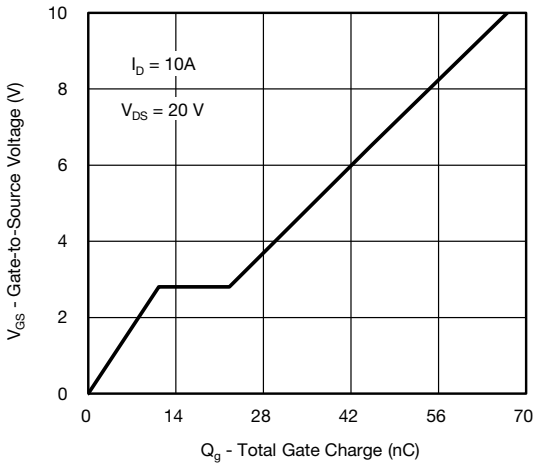
Transconductance



On-Resistance vs. Drain Current

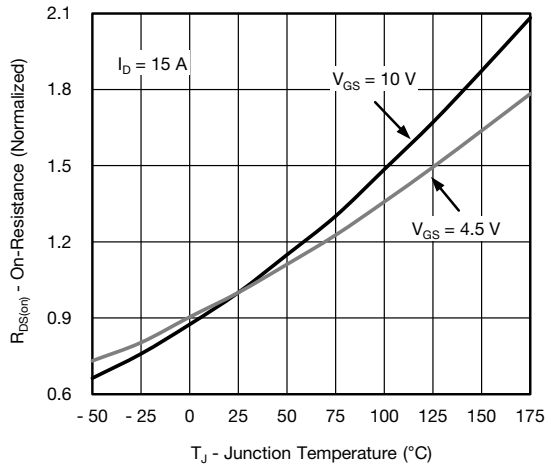


Capacitance

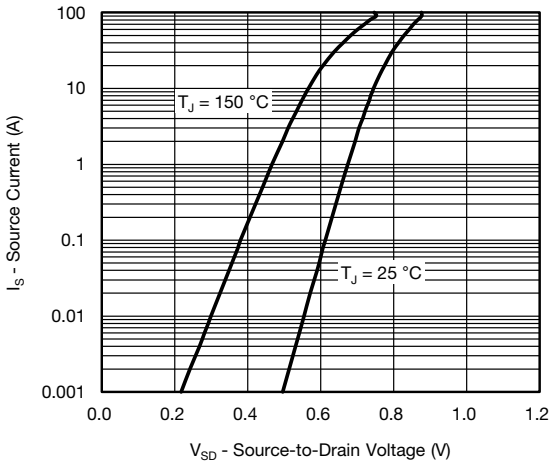


Gate Charge

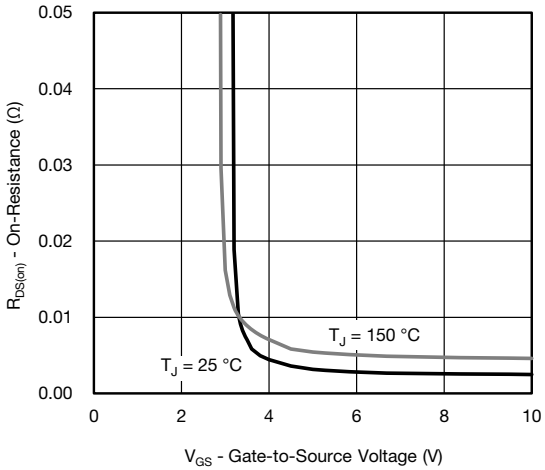
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



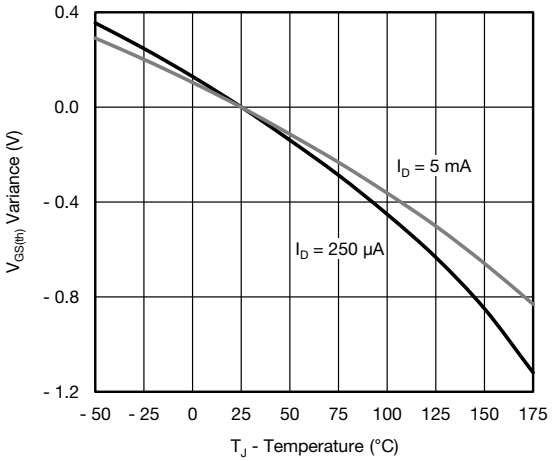
On-Resistance vs. Junction Temperature



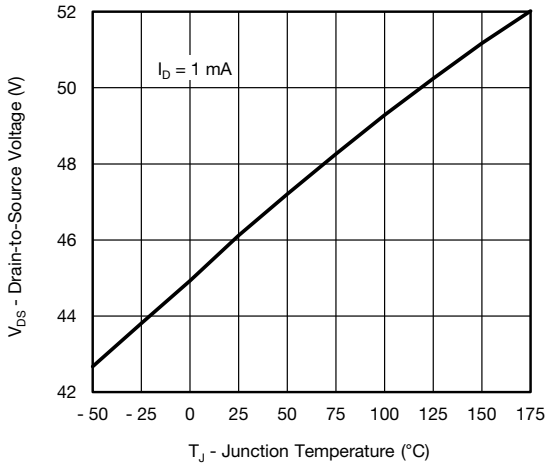
Source Drain Diode Forward Voltage



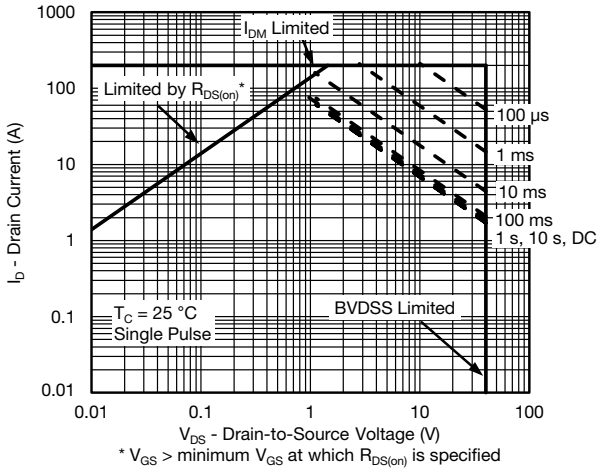
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

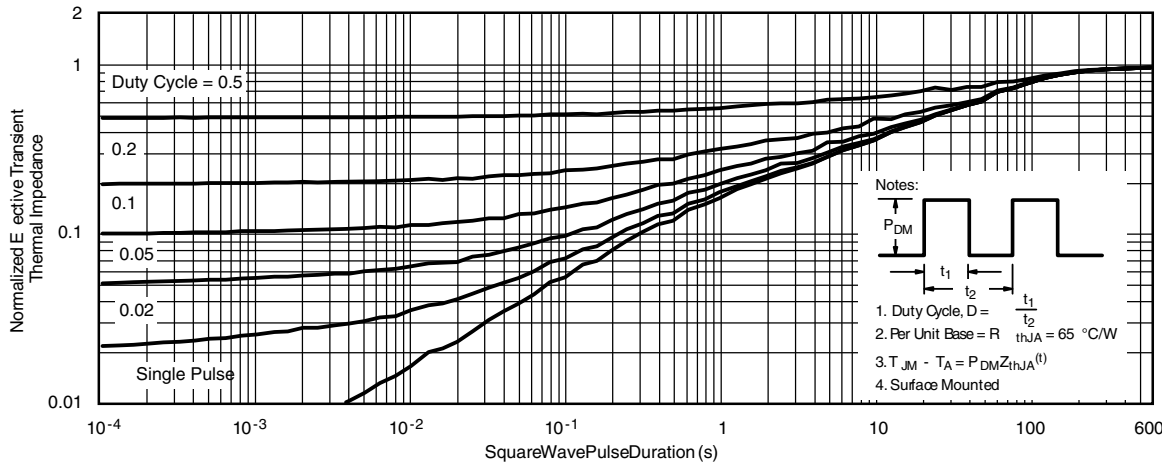


Drain Source Breakdown vs. Junction Temperature

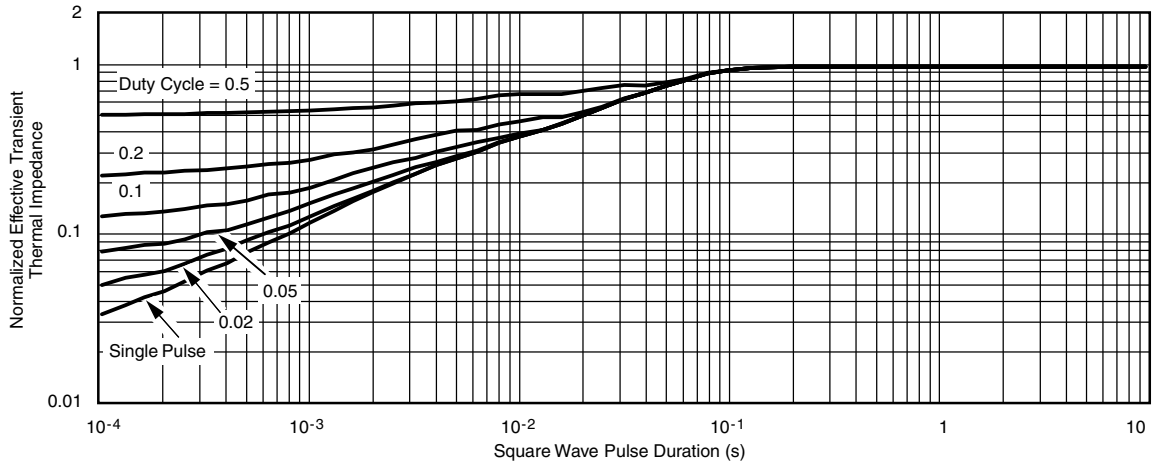


Safe Operating Area

THERMAL RATINGS (T_A = 25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

Note

- The characteristics shown in the two graphs
  - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
  - Normalized Transient Thermal Impedance Junction-to-Case (25 °C)

  are given for general guidelines only to enable the user to get a “ball park” indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?63989.