56F8037

Evaluation Module User Manual

56F8000
16-bit Digital Signal Controllers

MC56F8037EVMUM
Rev. 0
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Preface

This manual describes the hardware on the 56F8037EVM in detail.

Audience

This document is intended for application developers who are creating software for devices using the Freescale 56F8037 part or a member of the 56F8000 family that is compatible with this part.

Organization

This manual is organized into two chapters and two appendices.

- Chapter 1, Introduction, provides an overview of the Evaluation Module and its features.
- Chapter 2, Technical Summary, describes the 56F8037EVM hardware in detail.
- Appendix A, 56F8037EVM Schematics, contains the schematics of the 56F8037EVM.
- Appendix B, 56F8037EVM Bill of Material, provides a list of the materials used on the 56F8037EVM.

Suggested Reading

More documentation on the 56F8037EVM and the MC56F8037EVM kit may be found at URL:

www. freescale.com

Notation Conventions

This manual uses the following notational conventions:

Term or Value	Symbol	Examples	Exceptions
Active High Signals (Logic One)	No special symbol attached to the signal name	A0 CLKO	
Active Low Signals (Logic Zero)	Noted with an overbar in text and in most figures	$\overline{WE}$ $\overline{OE}$	In schematic drawings, Active Low Signals may be noted by a backslash: /WE
Hexadecimal Values	Begin with a “$” symbol	$0FF0 $80	
Decimal Values	No special symbol attached to the number	10 34	
Binary Values	Begin with the letter “b” attached to the number	b1010 b0011	
Numbers	Considered positive unless specifically noted as a negative value	5 -10	Voltage is often shown as positive: +3.3V
Blue Text	Linkable on-line	...refer to Chapter 7, License	
Bold	Reference sources, paths, emphasis	...see: **http://www.freescale.com/**	

Definitions, Acronyms, and Abbreviations

Definitions, acronyms and abbreviations for terms used in this document are defined below for reference.

56F8037	Digital signal controller with motor control peripherals
A/D	Analog-to-Digital; a method of converting Analog signals to Digital values
ADC	Analog-to-Digital Converter; a peripheral on the 56F8037 part
D/A	Digital-to-Analog; a method of converting Digital values to Analog signals
DAC	Digital-to-Analog Converter; a peripheral on the 56F8037 part
EOnCE	Enhanced On-Chip Emulation; a debug bus and port which enables a designer to create a low-cost hardware interface for a professional-quality debug environment
EVM	Evaluation Module; a hardware platform which allows a customer to evaluate the silicon and develop his application
GPIO	General Purpose Input and Output port on Freescale's family of digital signal controllers; does not share pin functionality with any other peripheral on the chip and can only be set as an input, an output, or a level-sensitive interrupt input
IC	Integrated Circuit
JTAG	Joint Test Action Group; a bus protocol/interface used for test and debug
LED	Light Emitting Diode
LQFP	Low-profile Quad Flat Package
OnCE™	On-Chip Emulation, a debug bus and port created to allow a means for low-cost hardware to provide a professional-quality debug environment
PCB	Printed Circuit Board
PWM	Pulse Width Modulation
SCI	Serial Communications Interface; a peripheral on Freescale's family of digital signal controllers
SPI	Serial Peripheral Interface; a peripheral on Freescale's family of digital signal controllers

References

The following sources were referenced to produce this manual:

[1] *DSP56800E Reference Manual*, DSP56800ERM, Freescale Semiconductor, Inc.

[2] *56F802X and 56F803X Peripheral Reference Manual*, MC56F80XXRM, Freescale Semiconductor, Inc.

[3] *56F8037 Technical Data*, MC56F8037, Freescale Semiconductor, Inc.

Chapter 1
Introduction

The 56F8037EVM is used to demonstrate the abilities of the 56F8037 digital signal controller and to provide a hardware tool allowing the development of applications.

The 56F8037EVM is an evaluation module board that includes a 56F8037 part, USB interface, user LEDs, user pushbutton switches and a daughter card connector. The daughter card connector allows signal monitoring and expandability of user features.

The 56F8037EVM is designed for the following purposes:

- Allowing new users to become familiar with the features of the 56800E architecture. The tools and examples provided with the 56F8037EVM facilitate evaluation of the feature set and the benefits of the family.
- Serving as a platform for real-time software development. The tool suite enables the user to develop and simulate routines, download the software to on-chip memory, run it, and debug it using a debugger via the JTAG/Enhanced OnCE (EOnCE) port. The breakpoint features of the EOnCE port enable the user to easily specify complex break conditions and to execute user-developed software at full speed until the break conditions are satisfied. The ability to examine and modify all user-accessible registers, memory and peripherals through the EOnCE port greatly facilitates the task of the developer.
- Serving as a platform for hardware development. The hardware platform enables the user to connect external hardware peripherals. The on-board peripherals can be disabled, providing the user with the ability to reassign any and all of the processor's peripherals. The EOnCE port's unobtrusive design means that all memory on the board and on the processor is available to the user.

1.1 56F8037EVM Architecture

The 56F8037EVM facilitates the evaluation of various features present in the 56F8037 part. The 56F8037EVM can be used to develop real-time software and hardware products. The 56F8037EVM provides the features necessary for a user to write and debug software,

demonstrate the functionality of that software and interface with the user's application-specific device(s). The 56F8037EVM is flexible enough to allow a user to fully exploit the 56F8037's features to optimize the performance of his product, as shown in **Figure 1-1**.

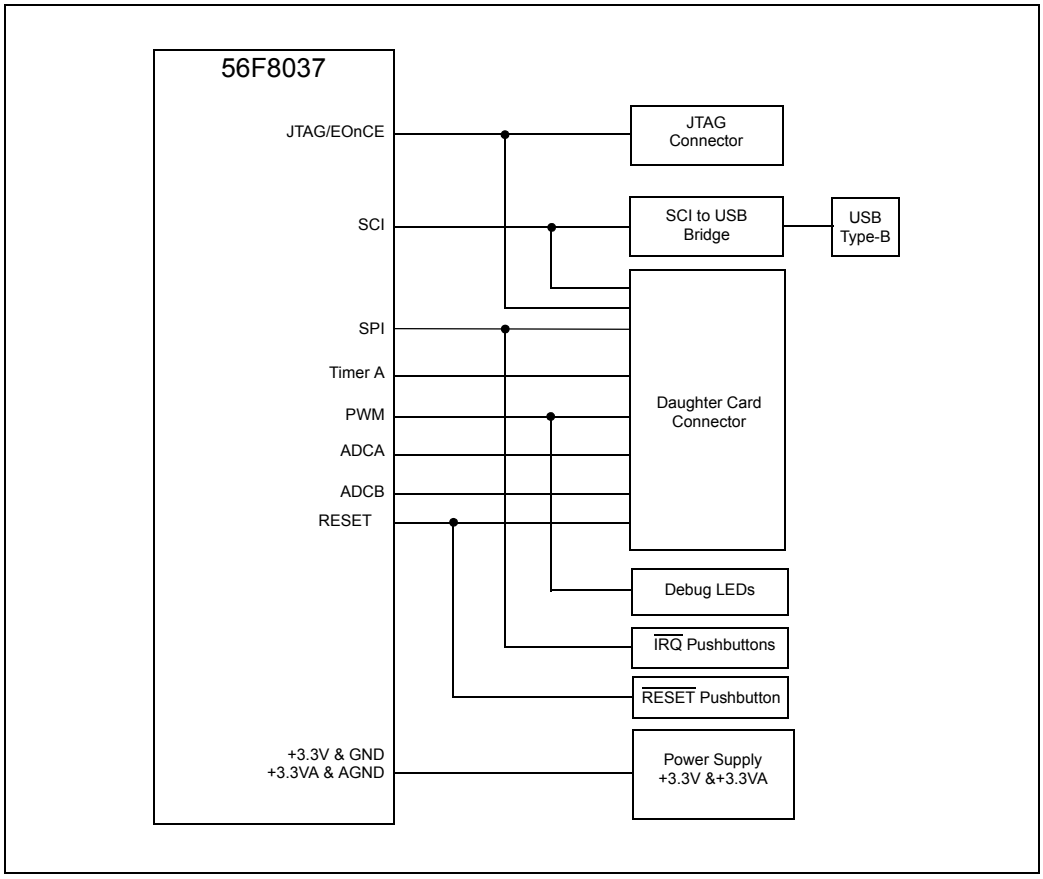

Figure 1-1. Block Diagram of the 56F8037EVM

1.2 56F8037EVM Connections

There are several power connection arrangements supported by the 56F8037EVM. Power can be provided to the 56F8037EVM by using a USB connector, P2, attached to a PC or USB hub. Power can be provided to the 56F8037EVM by an external +9.0V DC power supply using the 2.1mm power jack, P1, or via the Daughter Card connector, P3. However, the debug interconnect is always the same using the JTAG connector, J1.

1.2.1 USB Power Connection

An interconnection diagram is shown in **Figure 1-2** for connecting the JTAG Debug and USB between a PC and the 56F8037EVM.

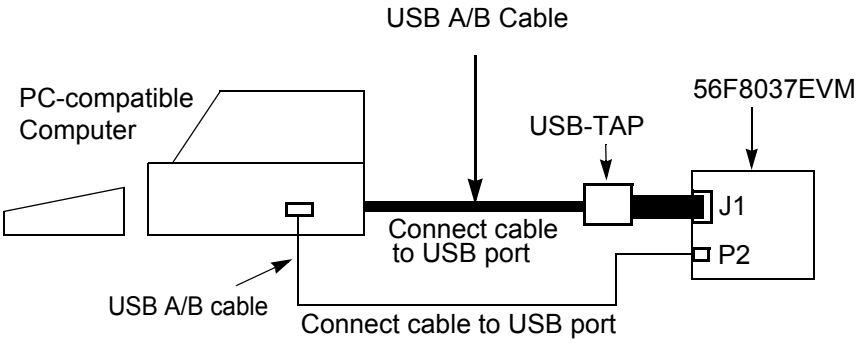

Figure 1-2. 56F8037EVM Cabling for USB Power

Perform the following steps for USB power connection:

1. Connect the USB-TAP's USB cable to a USB port on the host computer.
2. Connect the other end of the USB-TAP cable to the USB-TAP module. Connect the ribbon cable from the USB-TAP module to J1 on the 56F8037EVM, shown in **Figure 1-2**. This provides the connection which allows the host computer to control the debug functions on the 56F8037EVM board.
3. Connect the second USB cable to another USB port on the host computer or a USB hub.
4. Connect the other end of the second USB cable to the USB connector, P2, on the 56F8037EVM board, shown in **Figure 1-2**. The green Power-ON LED, LED7, will illuminate when power is correctly applied.

1.2.2 External +9.0V DC Power Connection

An interconnection diagram is shown in **Figure 1-3** for connecting the PC and a user-supplied external +9.0V DC power supply to the 56F8037EVM.

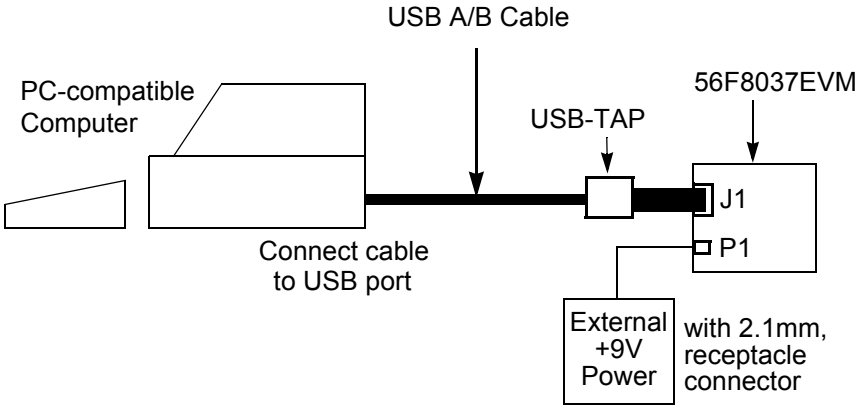

Figure 1-3. 56F8037EVM Cabling for External +9V Power

Perform the following steps for +9.0V DC power connection:

1. Connect the USB-TAP's USB cable to a USB port on the host computer.
2. Connect the other end of the USB-TAP cable to the USB-TAP module. Connect the ribbon cable from the USB-TAP module to J1 on the 56F8037EVM, shown in **Figure 1-3**. This provides the connection which allows the host computer to control the board.
3. Make sure that the external +9V DC, 450mA power supply is not plugged into any AC power source.
4. Connect the 2.1mm output power plug from the external power supply into P1 on the 56F8037EVM, shown in **Figure 1-3**.
5. Apply power to the external power supply. The green Power-ON LED, LED7, will illuminate when po wer is correctly applied.

1.2.3 External +3.3V DC Power Connection

An interconnection diagram is shown in **Figure 1-4** for connecting the PC and a user-supplied Daughter Card providing +3.3V DC to the 56F8037EVM.

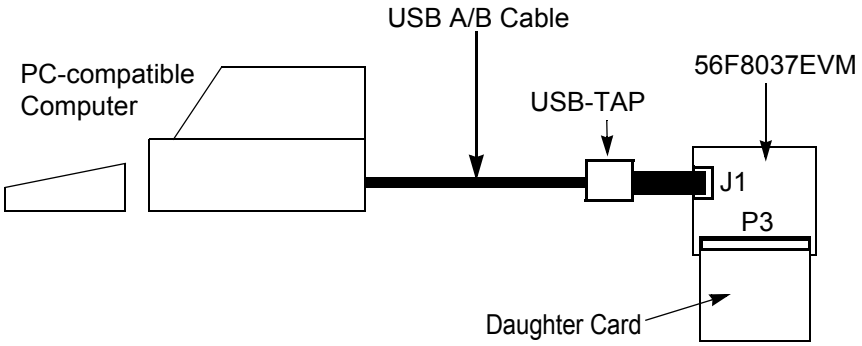

Figure 1-4. 56F8037EVM Cabling for External +3.3V Power

Perform the following steps to provide +3.3V DC power from a Daughter Card:

1. Connect the USB-TAP's USB cable to a USB port on the host computer.
2. Connect the other end of the USB-TAP cable to the USB-TAP module. Connect the ribbon cable from the USB-TAP module to J1 on the 56F8037EVM, shown in **Figure 1-4**. This provides the connection which allows the host computer to control the board.
3. Make sure the power supply on the Daughter Card is turned OFF.
4. Connect the Daughter Card to P3 on the 56F8037EVM, shown in **Figure 1-4**.
5. Apply power to the Daughter Card. The green Power-ON LED, LED7, will illuminate when power is correctly applied.

Chapter 2
Technical Summary

The 56F8037EVM is designed as a versatile development card using the 56F8037 processor, allowing the creation of real-time software and hardware products to support a new generation of applications in servo and motor control, digital and wireless messaging, digital answering machines, feature phones, modems, and digital cameras. The power of the 16-bit 56F8037 processor, combined with the on-board USB interface and daughter card connector, makes the 56F8037EVM ideal for developing and implementing many motor control algorithms, as well as for learning the architecture and instruction set of the 56F8037 processor.

The main features of the 56F8037EVM, with board and schematic reference designators, include:

- 56F8037, a 16-bit +3.3V digital signal controller operating at 60MHz [U1]
- Joint Test Action Group (JTAG) port interface connector, for an external debug Host Target Interface [J1]
- USB interface, for easy connection to a host processor [U2 and P2]
- Daughter Card connector, to allow the user to connect his own PWM, ADC, DAC, SCI, SPI or GPIO-compatible peripheral to the digital signal controller [P3]
- On-board power regulation provided from an external +9V DC-supplied power input [P1]
- Light Emitting Diode (LED) power indicator [LED7]
- Six on-board real-time user debugging LEDs [LED1-6]
- Manual RESET pushbutton [S1]
- Manual interrupt #1 pushbutton [S2]
- Manual interrupt #2 pushbutton [S3]

2.1 56F8037

The 56F8037EVM uses a Freescale 56F8037 part, designated as U1 on the board and in the schematics. This part will operate at a maximum external bus speed of 60MHz. A full description of the 56F8037, including functionality and user information, is provided in these documents:

- 56F8037 *Technical Data Sheet*, (MC56F8037)**:** Electrical and timing specifications, pin descriptions, device specific peripheral information and package descriptions
- *56F802X and 56F803X Peripheral Reference Manual*, (MC56F80XXRM): Detailed description of peripherals of the 56F802x and 56F803x devices
- *DSP56800E Reference Manual*, (DSP56800ERM): Detailed description of the 56800E family architecture, 16-bit core processor, and the instruction set

Refer to these documents for detailed information about chip functionality and operation. They can be found on this URL:

www.freescale.com

2.2 USB Serial Communications

The 56F8037EVM provides an RS-232 to USB bridge interface by the use of an USB bridge part, Silicon Labs CP2102, designated as U2. Refer to the USB schematic details in **Appendix A**. The USB bridge handles all the USB 2.0 protocol interactions and transitions the SCI port's +3.3V signal levels to USB-compatible signal levels and connects to the host's USB port via connector P2. The SCI ports signals, GPIOB6 and GPIOB7, or GPIOC12 and GPIOC8, can be disconnected from the USB bridge by pulling the jumpers at JG3, RxD, and JG4, TxD, on the board. The jumper options available on JG3 and JG4 for the SCI port are shown in **Table 2-1** and **Table 2-2**.

Table 2-1. SCI RxD Signal Options

JG3		
Pin #	**Signal**	**Description**
1	GPIO Port B, Bit 6	RXD0
2	RxD	From CP2102
3	GPIO Port C, Bit 12	RXD1

Table 2-2. SCI TxD Signal Options

JG4		
Pin #	**Signal**	**Description**
1	GPIO Port B, Bit 7	TXD0
2	TxD	To CP2102
3	GPIO Port C, Bit 8	TXD1

2.3 Debug LEDs

Six on-board Light-Emitting Diodes, (LEDs), are provided to allow real-time debugging for user programs. These LEDs will allow the programmer to monitor program execution without having to stop the program during debugging; refer to **Figure 2-1**. **Table 2-3** describes the control of each LED.

Setting GPIOA0, GPIOA1, GPIOA2, GPIOA3, GPIOA4, or GPIOA5 to a Logic One value will turn on the associated LED.

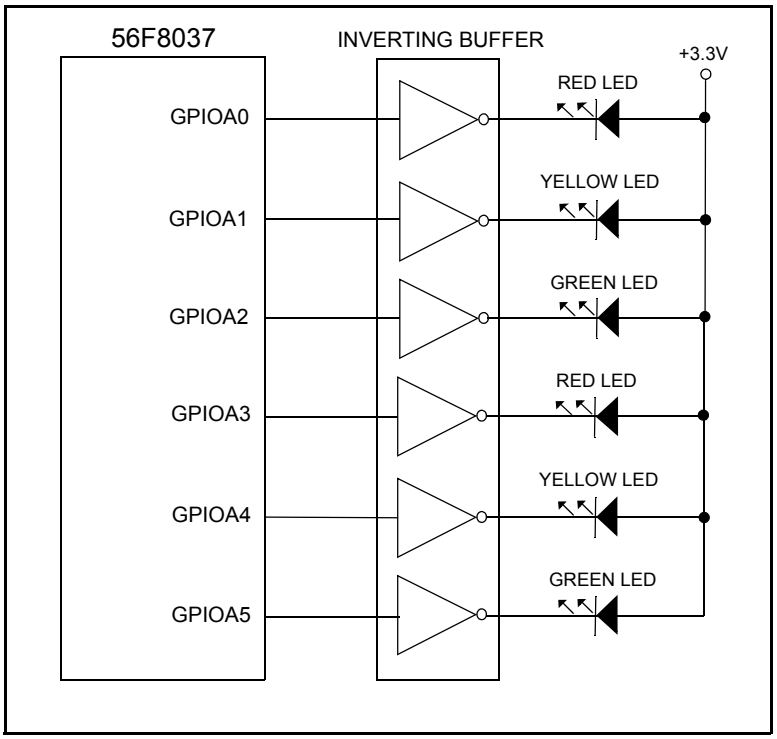

Figure 2-1. Diagram of the Debug LED Interface

Table 2-3. LED Control

	Controlled by	
User LED	**Color**	**Signal**
LED1	RED	GPIO Port A, Bit 0
LED2	YELLOW	GPIO Port A, Bit 1
LED3	GREEN	GPIO Port A, Bit 2
LED4	RED	GPIO Port A, Bit 3
LED5	YELLOW	GPIO Port A, Bit 4
LED6	GREEN	GPIO Port A, Bit 5

2.4 Debug Support

A JTAG connector, J1, on the 56F8037EVM allows the connection of an external Host Target Interface for downloading programs and working with the 56F8037's registers. This connector is used to communicate with an external Host Target Interface, which passes information and data back and forth with a host processor running a debugger program. **Table 2-4** shows the pin-out for this connector.

Table 2-4. JTAG Connector

J1			
Pin #	**Signal**	**Pin #**	**Description**
1	TDI	2	GND
3	TDO	4	GND
5	TCK	6	GND
7	N/C	8	KEY
9	$\overline{\text{RESET}}$	10	TMS
11	+3.3V DC	12	N/C
13	N/C	14	N/C

2.5 External Interrupts

Two on-board pushbutton switches are provided for external interrupt generation, as shown in **Figure 2-2**. S2 allows the user to generate a hardware interrupt, IRQ #1, using GPIO Port B, Bit 2. S3 allows the user to generate a hardware interrupt, IRQ #2, using GPIO Port B, Bit 3. These two switches allow the user to generate interrupts for their user-specific programs. Alternately, the user can use GPIO Port B, Bit 4, for IRQ #1. To accomplish this, remove the jumper at JP5, pins 1 and 2, and place the jumper between JP5 pins 2 and 3. Also, the user can use GPIO Port B, Bit 5, for IRQ #2. To accomplish this, remove the jumper at JP6, pins 1 and 2, and place the jumper between JP6 pins 2 and 3.

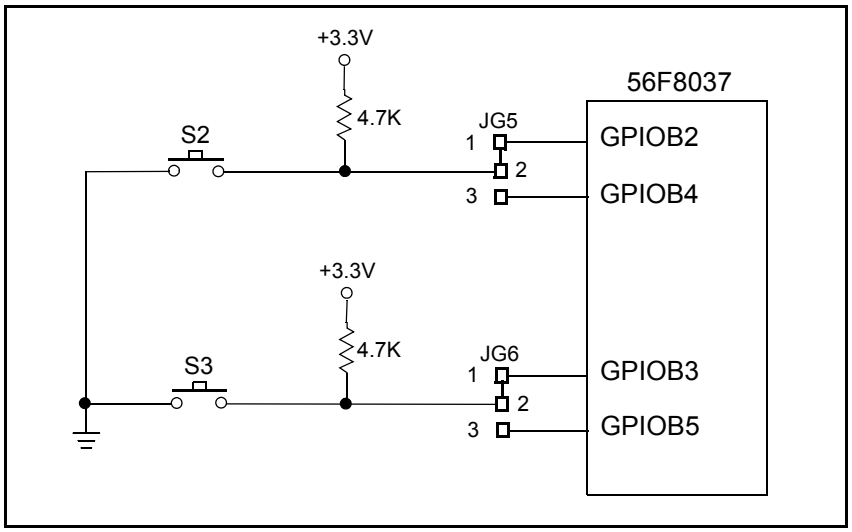

Figure 2-2. Schematic Diagram of the User Interrupt Interface

2.6 Reset

Logic is provided on the 56F8037 to generate an internal Power-On RESET. Additional reset logic is provided to support the RESET signal from the JTAG connector and the user RESET pushbutton, S1; refer to the schematics in **Appendix A**.

2.7 Power Supply

The 56F8037EVM supports the option of power being provided from three different sources. Since only one power supply source can be active at one time, the selection of the active power supply source is made by the jumper group formed by JG1 and JG2. **Table 2-5** depicts the jumper options for selecting each power supply source. Jumpering JG2, pins 2 and 3, the default selection, selects the USB power supply source. Jumpering JG2, pins 1 and 2, selects the external power supply source. Jumpering JG1 to JG2, pin 2, uses the Daughter Card power source.

Table 2-5. Power Source Selector

JG1		JG2	
Pin #	**Description**	**Pin #**	**Description**
		1	External Power Supply Source
1	Daughter Card Source	2	Power to 56F8037EVM
		3	USB Power Supply Source

2.7.1 USB Power Source

The main power source for the 56F8037EVM is through the USB connector, P2. This +5.0V USB bus input power goes to the USB bridge device which creates a regulated +3.3V output voltage. The USB bus power input is restricted to 450mA maximum for a high power device. However, the USB bridge regulator output is limited to 350mA. This +3.3V DC voltage regulation is used by the 56F8037 processor, ADC, LEDs, JTAG interface and supporting logic; refer to schematics in **Appendix A**. When power is applied to the 56F8037EVM board, the Power-ON LED, referenced as LED7, will illuminate.

2.7.2 External +9V DC Power Source

The optional external +9V DC power input to the 56F8037EVM is through the 2.1mm coax power jack, P1. This input power passes through a reverse power-blocking diode to provide a DC supply input for the +3.3V voltage regulator, U4, and the +5.0V voltage regulator, U5. A 450mA external power supply is sufficient to power the 56F8037EVM. However, less than 300mA is required by the 56F8037EVM board. The remaining current is available for custom control applications when connected to the Daughter Card connector. The 56F8037EVM provides +5.0V DC regulation for the CAN transceiver and, +3.3V DC voltage regulation for the processor, ADC, JTAG interface and supporting logic; refer to schematics in **Appendix A**. When power is applied to the 56F8037EVM board, the Power-ON LED, referenced as LED7, will illuminate.

2.7.3 Daughter Card Power Source

The optional Daughter Card power input to the 56F8037EVM is through the Daughter Card connector, P3. Regulated +3.3V voltage is provided on P3, pin 1. The Daughter Card power supply ground reference is provided on P3, pin 3. At least 300mA should be provided to power the 56F8037EVM board. This input +3.3V DC voltage will power the processor, ADC, DAC, LEDs, JTAG interface and supporting logic; refer to schematics in **Appendix A**. When power is applied to the 56F8037EVM board, the Power-ON LED, referenced as LED7, will illumate.

2.8 Daughter Card Connector

The 56F8037EVM contains a Daughter Card connector, P3, which contains the processor's peripheral port signals. The daughter card connector is used to connect a Daughter Card or a user-specific Daughter Card to the processor's peripheral port signals. The Daughter Card connector is a 60-pin 0.1" pitch connector with signals for RESET, SPI, SCI, PWM, ADC, DAC and GPIO ports. **Table 2-6** shows the Daughter Card connector's signal-to-pin assignments.

Table 2-6. Daughter Card Connector Description

P3			
Pin #	**Signal**	**Pin #**	**Signal**
1	+3.3V	2	GPIOA10 / CINA2 / TB2
3	GND	4	GPIOA7 / $\overline{\text{RESET}}$ / V_{PP}
5	GPIOB7 / TXD0 / SCL	6	GPIOD4 / EXTAL
7	GPIOB6 / RXD0 / SDA / CLKIN	8	GPIOD5 / XTAL / CLKIN
9	GPIOA0 / PWM0	10	GPIOC0 / ANA0 / CINA3
11	GPIOA1 / PWM1	12	GPIOC1 / ANA1
13	GPIOB4 / TA0 / CLKO / SS1 / TB0 / SCR2	14	GPIOC2 / ANA2 / V_{REFH}
15	GPIOB5 / TA1 / FAULT3 / CLKIN	16	GPIOC3 / ANA3 / V_{REFL}
17	GPIOB3 / MOSI0 / T3 / PSRC1	18	GPIOC4 / ANB0 / CINB3
19	GPIOB2 / MISO0 / TA2 / PSRC0	20	GPIOC5 / ANB1
21	GPIOB0 / SCLK0 / SCL	22	GPIOC6 / ANB2 / V_{REFH}
23	GPIOB1 / $\overline{\text{SS0}}$ / SDA	24	GPIOC7 / ANB3 / V_{REFL}
25	GPIOD0 / TDI	26	GPIOB1 / $\overline{\text{SS0}}$ / SDA
27	GPIOD1 / TDO	28	GPIOB0 / SCLK0 / SCL
29	GPIOD2 / TCK	30	GPIOA2 / PWM2
31	GPIOD3 / TMS	32	GPIOA3 / PWM3
33	GPIOA6 / FAULT0 / TA0	34	GPIOA4 / PWM4
35	GPIOA11 / CINB2 / TB3	36	GPIOA5 / PWM5
37	GPIOA12 / TB1 / SCLK1 / TA1	38	CINA1 / FAULT1 / TA2
39	GPIOA13 / TB2 / MISO1 / TA2	40	FAULT2 / TA3 / CINB1

Table 2-6. Daughter Card Connector Description (Continued)

P3			
Pin #	**Signal**	**Pin #**	**Signal**
41	GPIOA14 / TB3 / MOSI1 / TA3	42	N/C
43	GPIOB8 / SCL / CANTX	44	GPIOC8 / ANA4 / TXD1
45	GPIOB9 / SDA / CANRX	46	GPIOC9 / ANA5
47	GPIOB10 / COUTA / TB0	48	GPIOC10 / ANA6
49	GPIOB11 / COUTB / TB1	50	GPIOC11 / ANA7
51	GPIOB12 / CANTX	52	GPIOC12 / ANB4 / RXD1
53	GPIOB13 / CANRX	54	GPIOC13 / ANB5
55	N/C	56	GPIOC14 / ANB6
57	GPIOD6 / DAC0	58	GPIOC15 / ANB7
59	GPIOD7 / DAC1	60	GNDA

2.9 Test Points

The 56F8037EVM board has two test points:

- +3.3V, TP1
- Digital Ground (GND), TP2

Appendix A
56F8037EVM Schematics

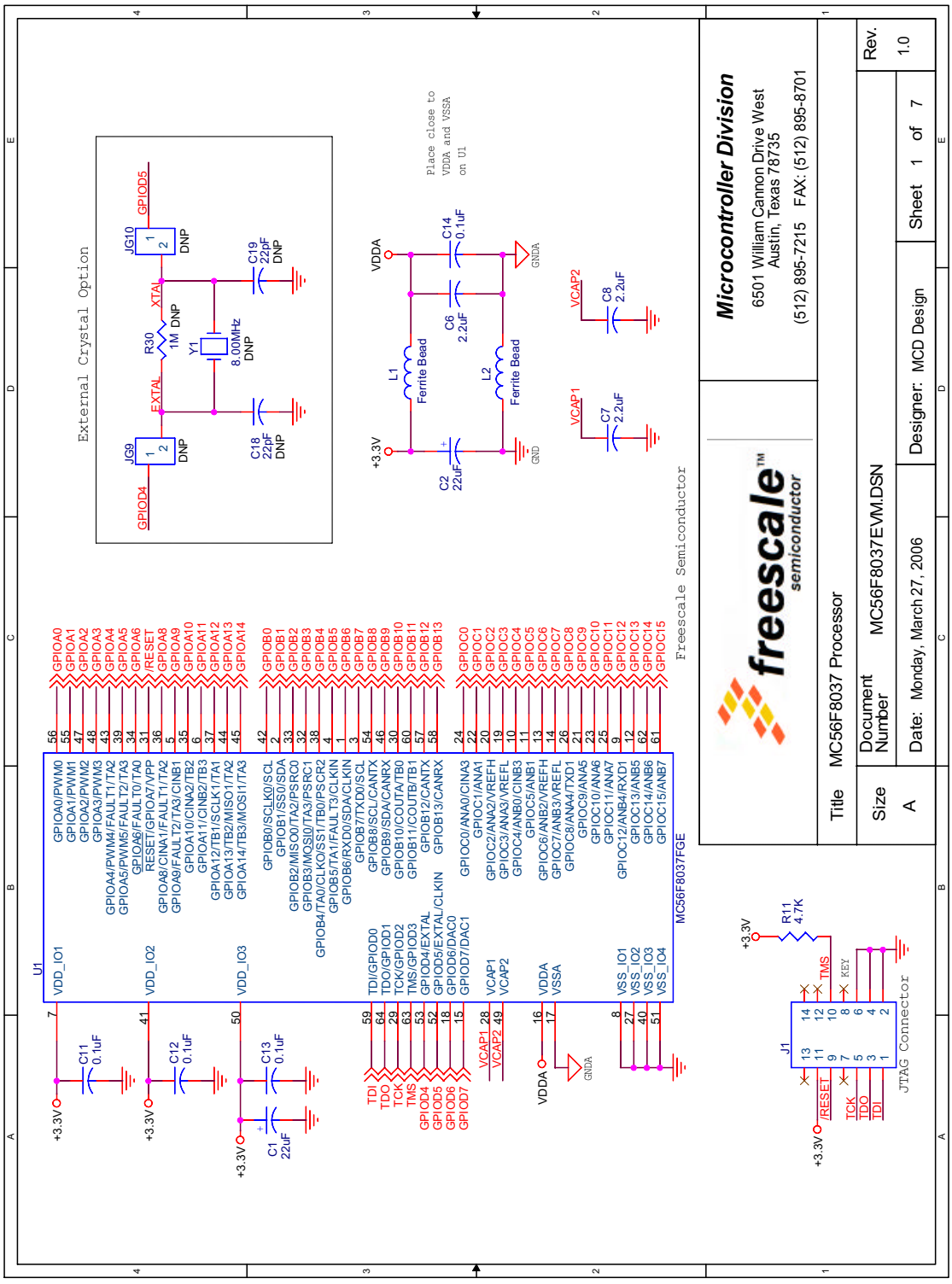

Figure A-1. MC56F8037 Processor

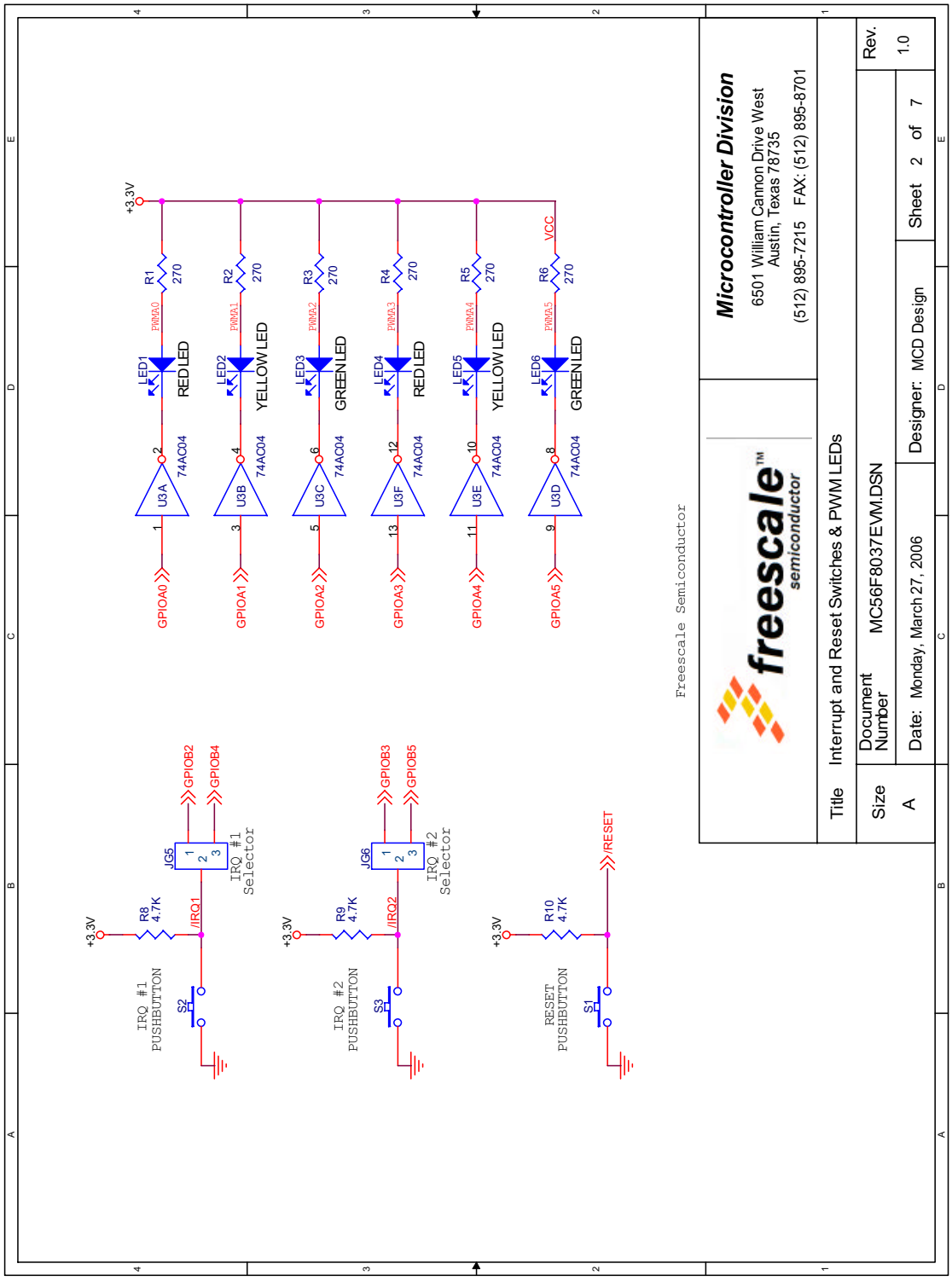

Figure A-2. Interrupt and Reset Switches and PWM LEDs

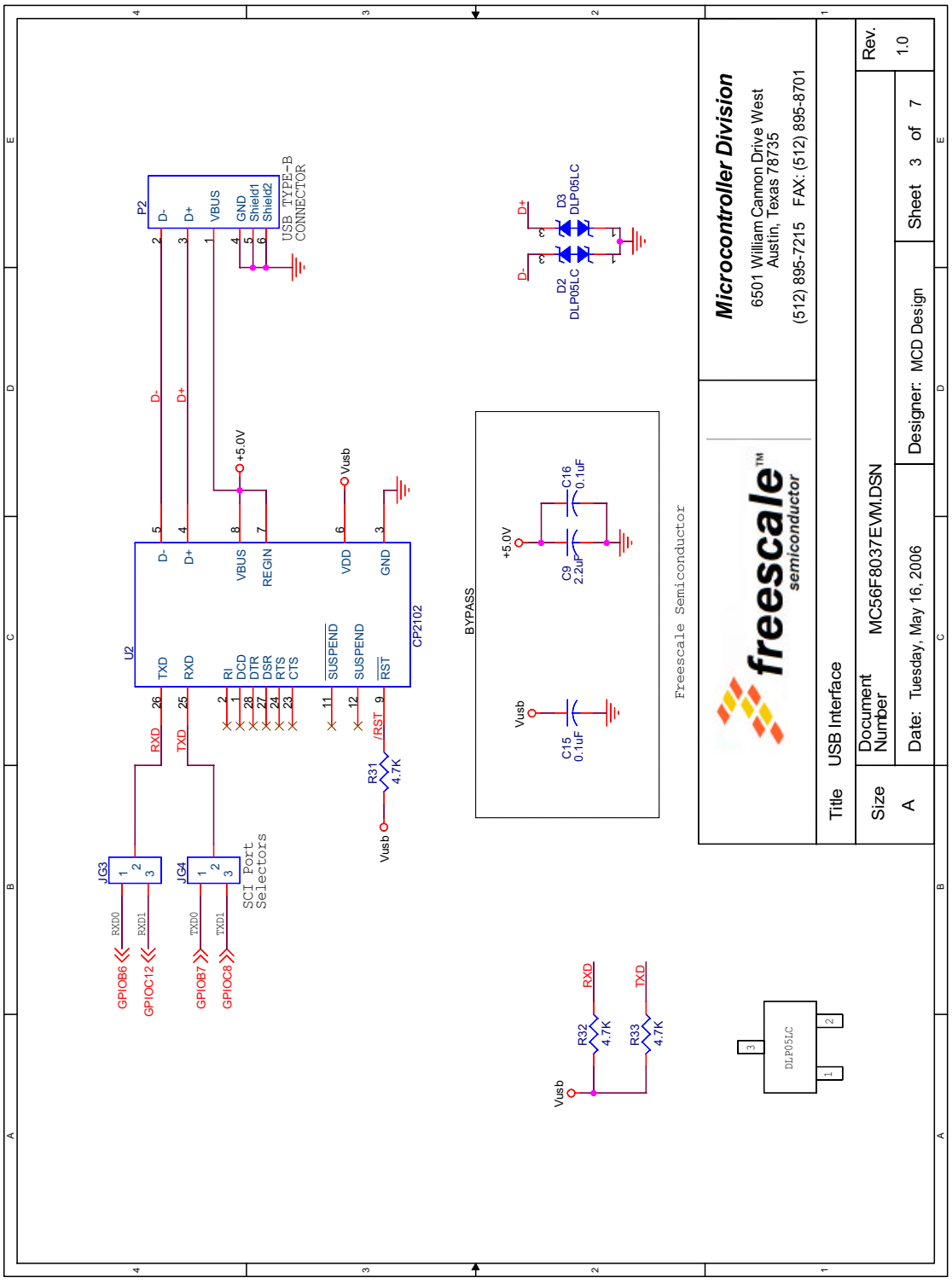

Figure A-3. USB Interface

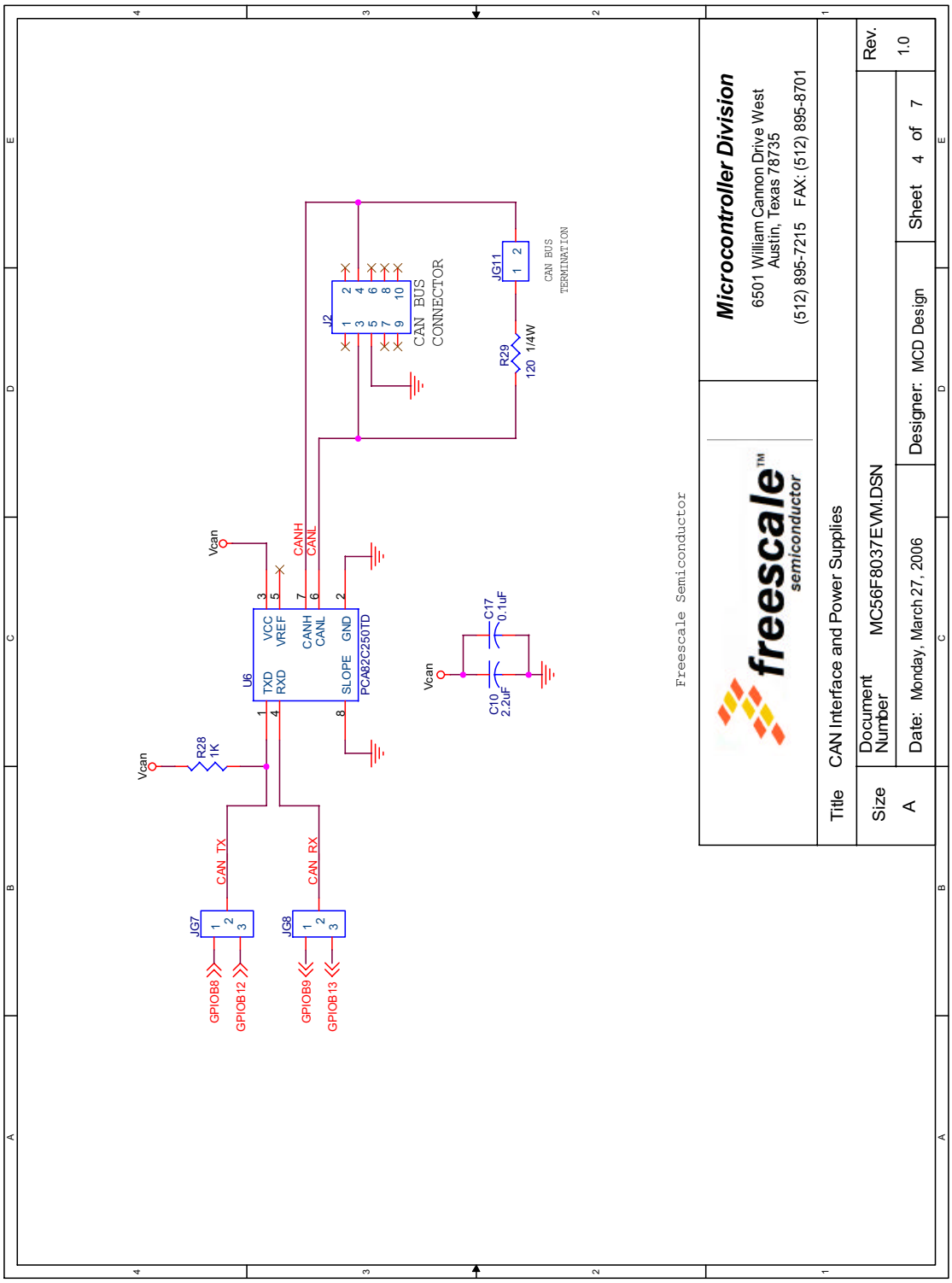

Figure A-4. CAN Interface and Power Supplies

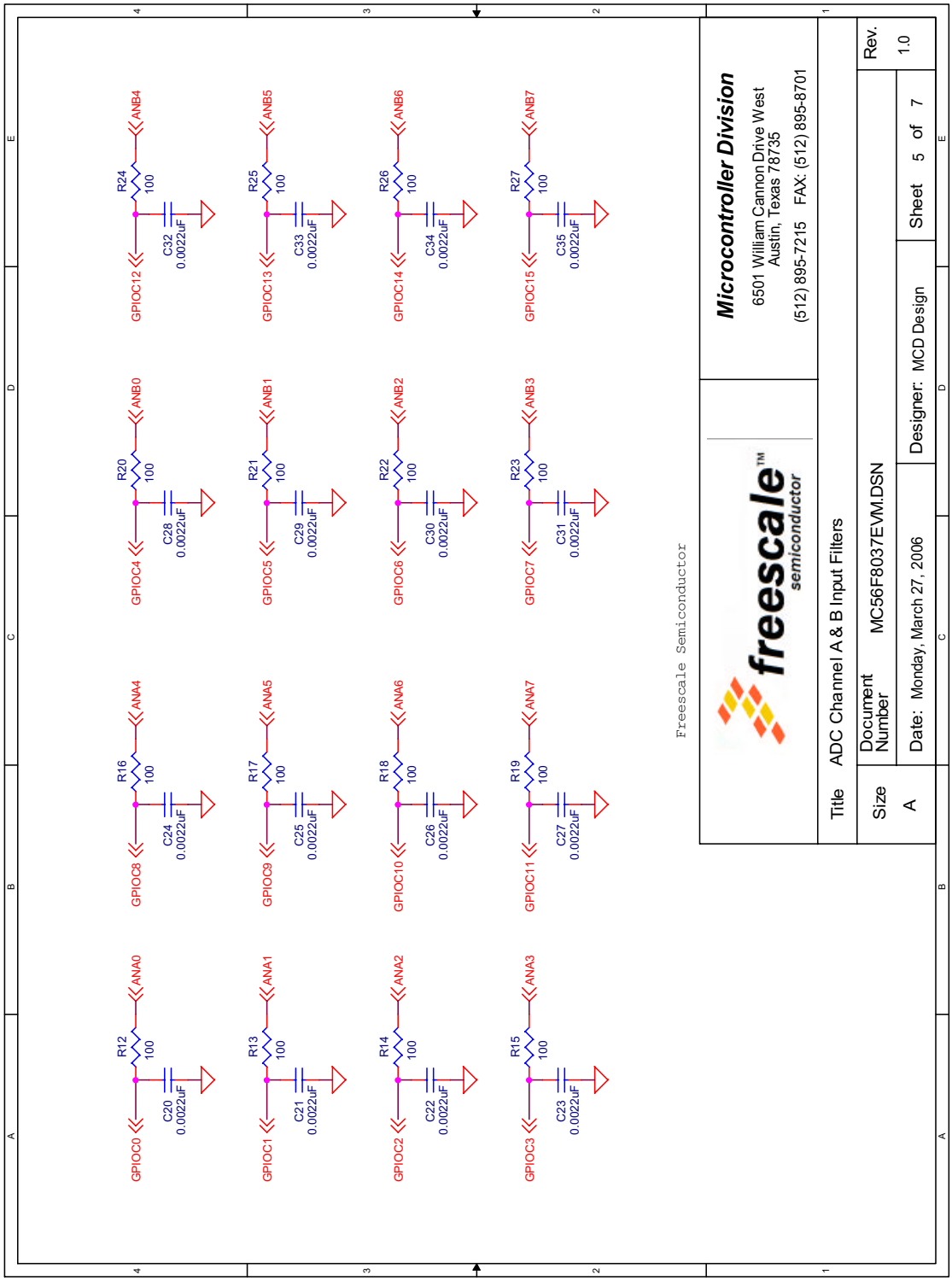

Figure A-5. ADC Channel A and B Input Filters

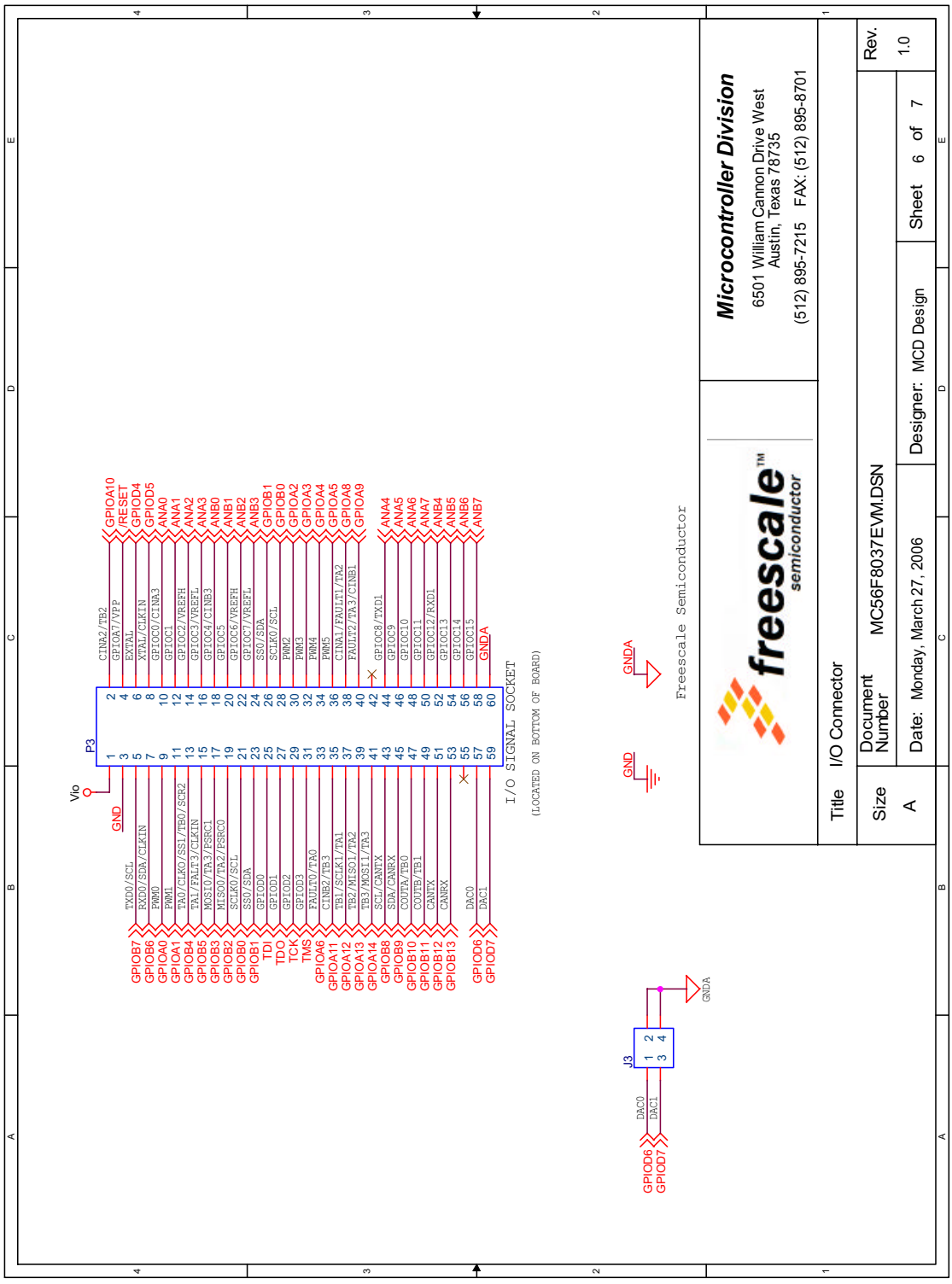

Figure A-6. I/O Connector

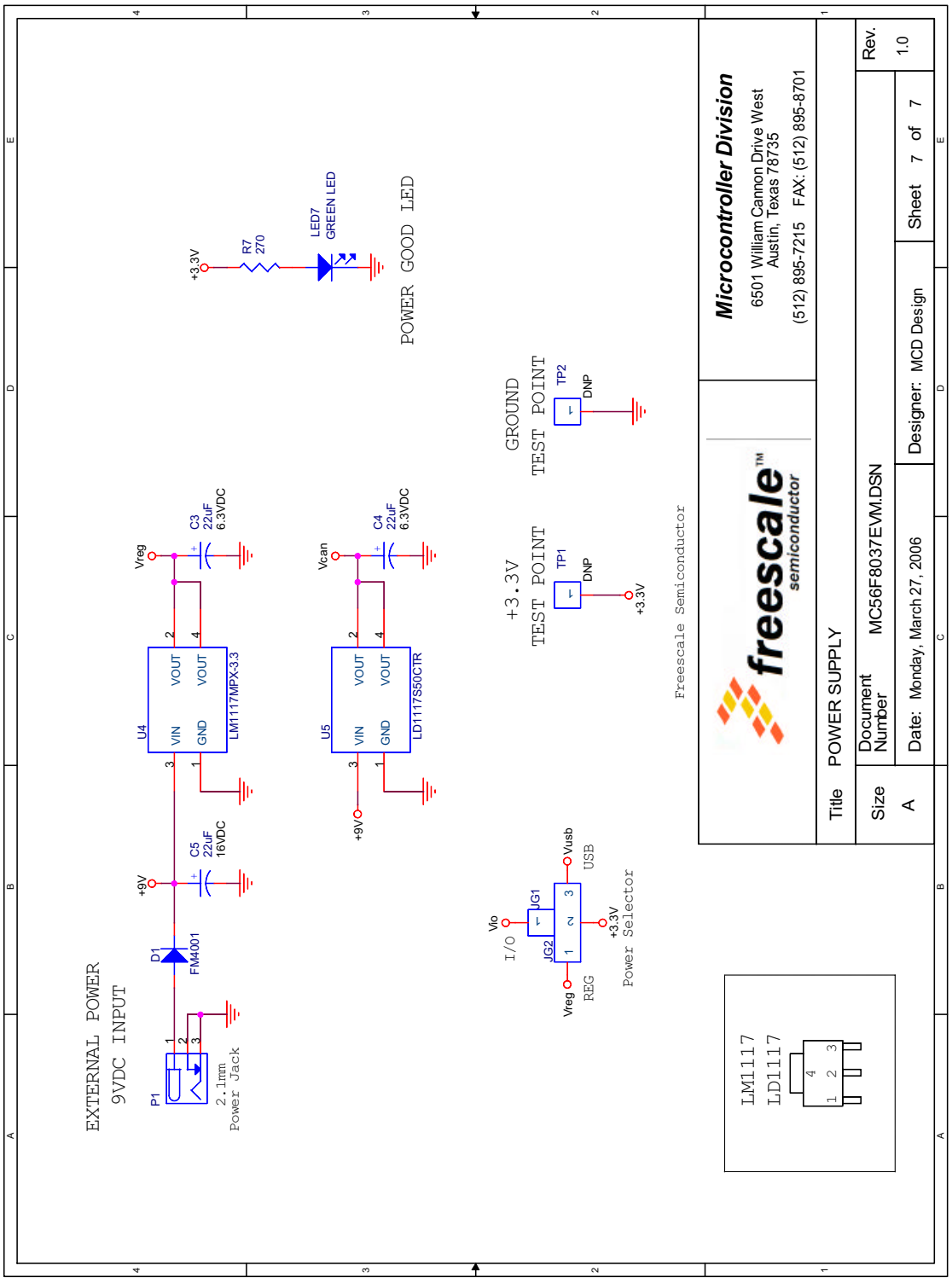

Figure A-7. Power Supply

Appendix B
56F8037EVM
Bill of Material

Qty	Description	Ref. Designators	Vendor Part #
Integrated Circuits			
1	MC56F8037	U1	Freescale, MC56F8037VFBE
1	SCI to USB Bridge	U2	Silicon Lab, CP2102-GM
1	74AC04	U3	ON Semiconductor, MC74AC04DG
1	+3.3V Voltage Regulator	U4	National Semiconductor, LM1117MPX-3.3/NOPB
1	+5.0V Voltage Regulator	U5	STMicroelectronics, LD1117S50CTR
1	CAN Transceiver	U6	Philips Semiconductor, PCA82C250TD
Resistors			
7	270 Ω, 0603	R1—R7	SMEC, RC73L2X271JTF
7	4.7 KΩ, 0603	R8-R11, R31-R33	SMEC, RC73L2X472JTF
16	100 Ω, 0603	R12—R27	SMEC, RC73L2X101JTF
1	1K Ω, 0603	R28	SMEC, RC73L2X102JTF
1	120 Ω, 1/4W	R29	YAGEO, CFR-25JB-120R
0	1.0M Ω, 0603	R30 (Optional)	SMEC, RC73L2X105JTF
Inductors			
2	Ferrite Bead, 0603	L1—L2	SMEC, FCB0603-1000HNTF
LEDs			
2	Red LED, 0805	LED1, LED4	Lite-ON, LTST-C171CKT
2	Yellow LED, 0805	LED2, LED5	Lite-ON, LTST-C171YKT
3	Green LED, 0805	LED3, LED6, LED7	Lite-ON, LTST-C171GKT

56F8037EVM Bill of Material, Rev. 0

Qty	Description	Ref. Designators	Vendor Part #
Diode			
1	1N4003, SMA	D1	ON Semiconductor, MRA4003T3G
2	TVS, SOT-23	D2, D3	Diodes Electronics, DLP05LC-7-F
Capacitors			
4	22µF, +6.3V DC, EIA-A	C1—C4	SMEC, ESR900-22K6.3AF
1	22µF, +16V DC, EIA-B	C5	SMEC, ESR600-22K16BF
5	2.2µF, 0805	C6—C10	SMEC, MCCB225M2NRTF
7	0.1µF, 0603	C11—C17	SMEC, MCCA104K1NRTF
2	22pF, 0603	C18 , C19 (Optional)	SMEC, MCCA220K1NRTF
16	0.0022µF, 0603	C20—C35	SMEC, MCCA222K1NRTF
Test Points			
0	+3.3V Test Point	TP1 (Optional)	KEYSTONE, 5000, RED
0	GND Test Point	TP2 (Optional)	KEYSTONE, 5001, BLACK
Connectors			
1	2.1mm Power Jack	P1	CUI, PJ-102A
1	USB Type-B Connector	P2	MOLEX, 67068-8000
1	Daughter Card Connector	P3	SAMTEC, SSM-130-L-DV-LC
1	1x1 Header	JG1	SAMTEC, TSW-101-07-G-S
7	3x1 Header	JG2—JG8	SAMTEC, TSW-103-07-G-S
2	2x1 Header	JG9, JG10 (Optional)	SAMTEC, TSW-102-07-G-S
1	2x1 Header	JG11	SAMTEC, TSW-102-07-G-S
1	7x2 JTAG Header	J1	SAMTEC, TSW-107-07-G-D
1	5x2 Header	J2	SAMTEC, TSW-105-07-G-D
1	2x2 Header	J3	SAMTEC, TSW-102-07-G-D
Switches			
3	SPST Pushbutton	S1—S3	OMRON,B3F-1022

Qty	Description	Ref. Designators	Vendor Part #
Crystals			
1	8.000MHz Crystal	Y1 (Optional)	CITIZEN CRYSTAL, HCM49-8.000MABJ-UT
Miscellaneous			
2	Rubber Feet, 0.4”		3M, SJ-5007 (BLACK)
8	0.1” Shunt Jumpers		SULLINS, SPC02SYAN

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