Product Change Notification / SYST-24YPYI186

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Product Category:

Motor Control Sips

PCN Type:

Document Change

Notification Subject:

dsPIC33EDV64MC205 Family Silicon Errata and Data Sheet Clarification

Affected CPNs:

SYST-24YPYI186_Affected_CPN_06032024.pdf
SYST-24YPYI186_Affected_CPN_06032024.csv

Notification Text:

SYST-24YPYI186

Microchip has released a new Document for the dsPIC33EDV64MC205 Family Silicon Errata and Data Sheet Clarification of devices. If you are using one of these devices please read the document located at dsPIC33EDV64MC205 Family Silicon Errata and Data Sheet Clarification.

Notification Status: Final

Description of Change:

Added silicon issue 30 (MOSFET Gate Driver).

Impacts to Data Sheet: None

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 03 June 2024

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices::N/A

Attachments:

dsPIC33EDV64MC205 Family Silicon Errata and Data Sheet Clarification

Please contact your local Microchip sales office with questions or concerns regarding this notification.

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Affected Catalog Part Numbers (CPN)

DSPIC33EDV64MC205-E/M7
DSPIC33EDV64MC205-E/M7VAO
DSPIC33EDV64MC205-I/M7
DSPIC33EDV64MC205T-H/M7
DSPIC33EDV64MC205T-H/M7V02
DSPIC33EDV64MC205T-H/M7VAO
DSPIC33EDV64MC205-H/M7
DSPIC33EDV64MC205-H/M7VAO
DSPIC33EDV64MC205T-I/M7
DSPIC33EDV64MC205T-E/M7
DSPIC33EDV64MC205T-E/M7V01
DSPIC33EDV64MC205T-E/M7VAO

dsPIC33EDV64MC205
Silicon Errata and Data Sheet Clarification

The dsPIC33EDV64MC205 device that you have received conforms functionally to the current Device Data Sheet (DS70005292**F**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the dsPIC33EDV64MC205 silicon.

> **Note:** This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**D2**).

Data Sheet clarifications and corrections start on page 17, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers and emulation tools, which are available at the Microchip corporate website (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
   a) For MPLAB IDE 8, select *Programmer > Reconnect*.
   b) For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

> **Note:** If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various dsPIC33EDV64MC205 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision	
		D1	D2
dsPIC33EDV64MC205	1DA3h	4006h	4007h

Note 1: The Device IDs (DEVID and DEVREV) are located at the last two implemented addresses of configuration memory space. They are shown in hexadecimal in the format "DEVID DEVREV".

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions	
				D1	D2
CPU	`div.sd` Instruction	1.	When using the `div.sd` instruction, the Overflow bit is not getting set when an overflow occurs.	X	X
CPU	`DO` Loop	2.	PSV access, including table reads or writes in the first or last instruction of a `DO` loop, is not allowed.	X	X
CPU	Program Memory	3.	Address error trap may occur while accessing certain program memory locations.	X	X
Power System	Flash Regulator	4.	The VREGSF (RCON[11]) bit always reads back as '0'.	X	X
Flash	Flash Programming	5.	The Stall mechanism may not function properly when erasing or programming Flash memory.	X	X
SPI	Frame Sync Pulse	6.	Frame Sync pulse is not generated in Host mode when FRMPOL = 0.	X	X
SPI	Frame Sync Pulse	7.	When in SPI Client mode, with the Frame Sync pulse set as an input, the FRMDLY bit must be set to '0'.	X	X
UART	TX Interrupt	8.	A Transmit (TX) interrupt may occur before the data transmission is complete.	X	X
PTG	Strobe Output	9.	Strobe output pulse width is incorrectly dependent on the PTGPWD[3:0] (PTGCON[7:4]) bits setting.	X	X
PWM	Dead-Time Compensation	10.	Dead-time compensation is not enabled for Center-Aligned PWM mode.	X	X
PWM	Master Time Base Mode	11.	In Master Time Base mode, writing to the period register and any other timing parameter of the PWMx module will cause the update of the other timing parameter to take effect one PWM cycle after the period update is effective.	X	X
PWM	Immediate Update	12.	Dead time is not asserted when PDCx is updated to cause an immediate transition on the PWMxH and PWMxL outputs.	X	X
PWM	Complementary Mode	13.	With dead time greater than zero, 0% and 100% duty cycle cannot be obtained on PWMxL and PWMxH outputs.	X	X
PWM	Center-Aligned Mode	14.	Under certain conditions, PWMxH and PWMxL are deasserted.	X	X
PWM	PWM Override	15.	Glitch on PWMxH or PWMxL pins when override is turned off.	X	X
PWM	Edge-Aligned Mode	16.	Missing dead time under certain conditions.	X	X
PWM	Output Modes	17.	Output glitch pulse.	X	X
PWM	Complementary Output Mode	18.	Missing dead time between complementary outputs under certain conditions.	X	X
PWM	PWM SWAP	19.	In Center-Aligned mode, there is missing dead time when SWAP is disabled.	X	X
PWM	Center-Aligned Mode	20.	Updates to the PHASEx registers occur only at the middle of the Center-Aligned PWM cycle.	X	X
QEI	Index Counter	21.	The QEI Index Counter does not count correctly in Quadrature Detector mode.	X	X
QEI	Modulo Mode	22.	Modulo mode functionality is incorrect when the count polarity bit is set.	X	X
QEI	Velocity Counter	23.	Under certain circumstances, the Velocity Counter 1 register (VEL1CNT) misses count pulses.	X	X

TABLE 2: SILICON ISSUE SUMMARY (CONTINUED)

Module	Feature	Item Number	Issue Summary	Affected Revisions	
				D1	D2
ADC	Channel Scan	24.	Channel scanning is limited to AN0 through AN15.	X	X
CTMU	ADC Operation	25.	CTMU does not work with the ADC Converter in 12-bit mode.	X	X
Input Capture	External Synchronization	26.	Input capture and output compare modules cannot be synchronized.	X	X
Output Compare	Interrupt	27.	Under certain circumstances, an output compare match may cause the Output Compare x Interrupt Flag (OCxIF) bit to become set prior to the Change-of-State (COS) of the OCx pin.	X	X
Op Amp/ Comparator	External Reference	28.	Op amp/comparator voltage reference fails when the voltage on VREF+ is less than 1.33V.	X	X
MOSFET Gate Driver	Sleep Mode	29.	The MOSFET gate driver may not function as expected if Sleep mode is enabled.	X	
MOSFET Gate Driver	XUVLO Fault Detection	30.	After any device Reset, when the high-side driver is enabled for the first time, an erroneous XUVLO (External MOSFET Undervoltage Lock Out) FAULT may be triggered. This will disable the HSx outputs. This issue affects only the XUVLO fault on high-side gate drivers.	X	X

Silicon Errata Issues

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**D2**).

1. Module: CPU

When using the Signed 32-by-16-bit Division instruction, `div.sd`, the Overflow bit does not always get set when an overflow occurs.

Work around

Test for and handle overflow conditions outside of the `div.sd` instruction.

Affected Silicon Revisions

D1	D2						
X	X						

2. Module: CPU

Table write (`TBLWTL`, `TBLWTH`) instructions cannot be the first or last instruction of a `DO` loop.

Work around

None.

Affected Silicon Revisions

D1	D2						
X	X						

3. Module: CPU

An unexpected address error trap may occur during accesses to program memory addresses, 0x001 through 0x200. This has been observed when one or more interrupt requests are asserted, while reading or writing program memory addresses, using `TBLRDx`, `TBLWTx` or PSV-based instructions.

Work around

Before executing instructions that read or write program memory addresses, 0x001 through 0x200, disable interrupts using the `DISI` instruction.

Affected Silicon Revisions

D1	D2						
X	X						

4. Module: Power System

The VREGSF bit functions as documented but will always read back as '`0`'. Because of the Read-Modify-Write process, any `BSET` or `BCLR` instruction of the RCON register will also write a '`0`' to the VREGSF bit.

Work around

If the VREGSF bit is intended to be set to '`1`', the user software must also write a '`1`' to the VREGSF bit when setting or clearing any other bit in the RCON register.

Affected Silicon Revisions

D1	D2						
X	X						

5. Module: Flash

The Stall mechanism may not function properly when erasing or programming Flash memory.

Work around

Disable interrupts until the erase or programming operation is complete. Test for completion by inserting a bit test operation of the Write Control (WR) bit.

Code is provided in Example 1 that can be used to disable interrupts during RTSP erase/program operations.

EXAMPLE 1: WORK AROUND CODE

```
; Load write latches if programming
    …
; Setup NVMCON register to erase or program
  as required
    …
; Disable interrupts
    PUSH    SR
    MOV     #0x00E0, W0
    IOR     SR
; Write the KEY sequence
    MOV     #0x55, W0
    MOV     W0, NVMKEY
    MOV     #0xAA, W0
    MOV     W0, NVMKEY
; Start the programming sequence
    BSET    NVMCON, #15
; Insert two NOPs after programming
    NOP
    NOP
; Wait for operation to completeprog_wait:
    BTSC    NVMCON, #15
    BRA     prog_wait
; Re-enable interrupts,
    POP     SR
```

Affected Silicon Revisions

D1	D2						
X	X						

6. Module: SPI

When using the Frame Sync pulse output feature (FRMEN bit (SPIxCON2[15]) = 1) in Host mode (SPIFSD bit (SPIxCON2[14]) = 0), the Frame Sync pulse is not being generated with an active-low pulse (FRMPOL bit (SPIxCON2[13]) = 0).

Work around

The $\overline{SSx}$ pin is used as the Frame Sync pulse when the Frame Sync pulse output feature is used. Mapping the $\overline{SSx}$ input function and output function to the same pad by using the Peripheral Pin Select (PPS) feature resolves this issue.

Affected Silicon Revisions

D1	D2						
X	X						

7. Module: SPI

When in SPI Client mode (MSTEN bit (SPIxCON1[5]) = 0) and using the Frame Sync pulse output feature (FRMEN bit (SPIxCON2[15]) = 1) in Client mode (SPIFSD bit (SPIxCON2[14]) = 1), the Frame Sync Pulse Edge Select bit (FRMDLY bit (SPIxCON2[1]) = 0) must be set to '0'.

Work around

There is no work around. The Frame Sync Pulse Edge Select bit, FRMDLY, cannot be set to produce a Frame Sync pulse that coincides with the first bit clock.

Affected Silicon Revisions

D1	D2						
X	X						

8. Module: UART

When using UTXISEL[1:0] = 01 (interrupt when last character is shifted out of the Transmit Shift Register (TSR)) and the final character is being shifted out through the TSR, the Transmit (TX) interrupt may occur before the final bit is shifted out.

Work around

If it is critical that the interrupt processing occurs only when all transmit operations are complete, hold off the interrupt routine processing by adding a loop at the beginning of the routine that polls the Transmit Shift Register Empty bit (TRMT) before processing the rest of the interrupt.

Affected Silicon Revisions

D1	D2						
X	X						

9. Module: PTG

When using the strobe output Step commands ('PTGCTRL 0b1110', 'PTGCTRL 0b1100' and 'PTGCTRL 0b1101') to write to the AD1CHS0 register, the PTGPWD[3:0] bits (PTGCON[7:4]) determine the number of times the PTG module will write to the AD1CHS0 register.

Work around

Set the PTGPWD[3:0] bits to '0000' so that the PTG module does not write to the AD1CHS0 register multiple times.

Affected Silicon Revisions

D1	D2						
X	X						

10. Module: PWM

When dead-time compensation is enabled (DTC[1:0] (PWMCONx[7:6]) = 11) in Center-Aligned mode (CAM (PWMCONx[2]) = 1), the dead time, as specified in the ALTDTRx register, is not being applied to the PWMxH output. The leading and trailing edges of the PWMxL output are extended by one-half the value of the ALTDTRx register, but the PWMxH leading and trailing edges are unaffected.

Work around

Using the values from **"High-Speed PWM"** (DS70000645), adjust the PWM parameters as follows:

- Subtract one-half of the ALTDTRx dead time from PDCx
- Use twice the value for ALTDTRx. For example:
  - Frequency of 60 kHz, duty cycle of 50%
  - Desired dead time of 833 ns and dead-time compensation of 833 ns

Using the specified values from **"High-Speed PWM"** (DS70000645):

- PHASEx = 1000
- PDCx = 500
- ALTDTRx = 833 ns/8.33 ns = 100
- DTRx = (833 ns/8.33 ns)/2 = 50

Applying the work around:

- ALTDTRx = 2 * 100 = 200
- PDCx = PDCx – 25 = 475

Affected Silicon Revisions

D1	D2						
X	X						

11. Module: PWM

The PWMx module can operate with variable period, duty cycle, dead time and phase values. The master period and other timing parameters can be updated in the same PWM cycle. With immediate updates disabled, the new values should take effect at the start of the next PWM cycle.

As a result of this issue, the updated master period takes effect on the next PWM cycle, while the update of the additional timing parameter is delayed by one PWM cycle. The parameters affected by this erratum are as follows:

Master Period Registers – Update effective on the next PWM cycle (PTPER).

Additional PWM Timing Parameters – Update effective one PWM cycle after master period update:

- Duty Cycle – PDCx and MDC registers
- Phase – PHASEx register
- Dead Time – DTRx and ALTDTRx registers and dead-time compensation signals
- Clearing of current-limit and Fault conditions, and application of External Period Reset signal

Work around

If the application requires the master period and other parameters to be updated at the same time, enable both immediate updates:

- EIPU (PTCON[10]) = 1 – To enable immediate period updates
- IUE (PWMCONx[0]) = 1 – To enable immediate updates of additional parameters listed above

Enabling immediate updates will allow updates to the master period and the other parameter to take effect immediately after writing to the respective registers.

Affected Silicon Revisions

D1	D2						
X	X						

12. Module: PWM

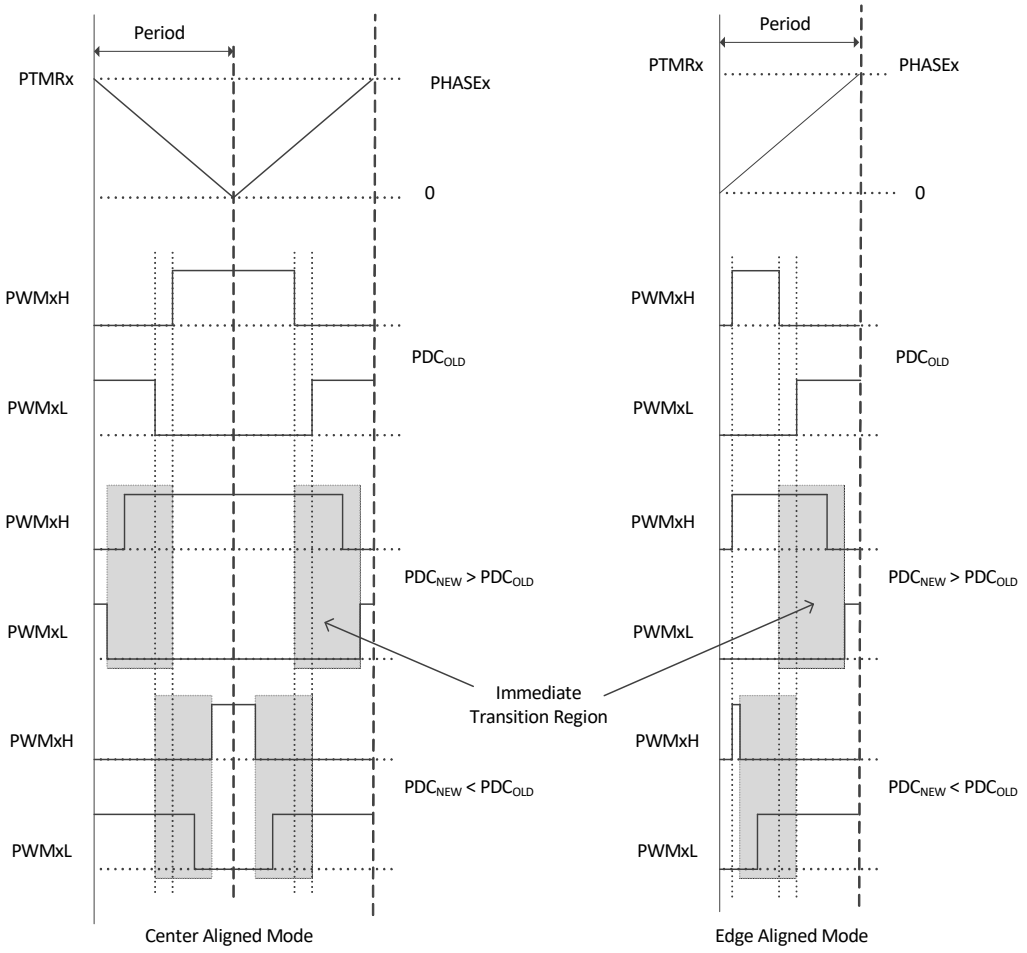
The PWM generator may not assert dead time on the edges of transitions. This has been observed when all of the following conditions are present:

- The PWM generator is configured to operate in Complementary mode with Independent Time Base (ITB) or master time base;
- Immediate update is enabled; and
- The value in the PDCx register is updated in such a manner that the PWMxH and PWMxL outputs make an immediate transition.

The current duty cycle, PDCOLD, newly calculated duty cycle, PDCNEW and the point at which a write to the Duty Cycle register occurs within the PWM time base will determine if the PWMxH and PWMxL outputs make an immediate transition. PWMxH and PWMxL outputs make an immediate transition if the Duty Cycle register is written with a new value, PDCNEW, at a point of time when the PWM time base is counting a value that is in between PDCNEW and PDCOLD. Additionally, writing to the Duty Cycle register, close to the instant of time where dead time is being applied, may result in a reduced dead time effective on the PWMxH and PWMxL transition edges.

In Figure 1, if the duty cycle write occurred in the shaded box, then PWMxH and PWMxL will make an immediate transition without dead time.

FIGURE 1: TIMING DIAGRAMS FOR CENTER-ALIGNED AND EDGE-ALIGNED MODES



Work around

None.

However, in most applications the duty cycle update timing can be controlled using the TRIGx trigger, or Special Event Trigger, such that the above mentioned conditions are avoided altogether.

Affected Silicon Revisions

D1	D2						
X	X						

13. Module: PWM

This issue is applicable when a PWM generator is configured to operate in Independent Time Base mode with either Center-Aligned Complementary mode or Edge-Aligned Complementary mode. When dead time is non-zero, PWMxL is not asserted for 100% of the time when PDCx is zero. Similarly, when dead time is non-zero, PWMxH is not asserted for 100% of the time when PDCx is equal to PHASEx. This issue applies to Master Time Base mode as well.

Work around

In Center-Aligned mode:

- To obtain 0% duty cycle, first zero out the ALTDTRx register, then write zero to the PDCx register.
- To obtain 100% duty cycle, first zero out the ALTDTRx register, then write (PHASEx + 2) to the PDCx register.

In Edge-Aligned mode:

- To obtain 0% duty cycle, first zero out the registers, DTRx and ALTDTRx, then write zero to the PDCx register.
- To obtain 100% duty cycle, first zero out the registers, DTRx and ALTDTRx, then write (PHASEx + 1) to the PDCx register.

Alternatively, in both Center-Aligned and Edge-Aligned PWM modes, 0% and 100% duty cycle can be obtained by enabling the PWM override (IOCONx[9:8] = `0b11`) with the Output Override Synchronization bit (IOCONx[0]) set as '`1`':

- For 0% duty cycle, set the Override Data bits (IOCONx[7:6]) for PWMxH and PWMxL as '`0b01`'.
- For 100% duty cycle, set the Override Data bits (IOCONx[7:6]) for PWMxH and PWMxL as '`0b10`'.

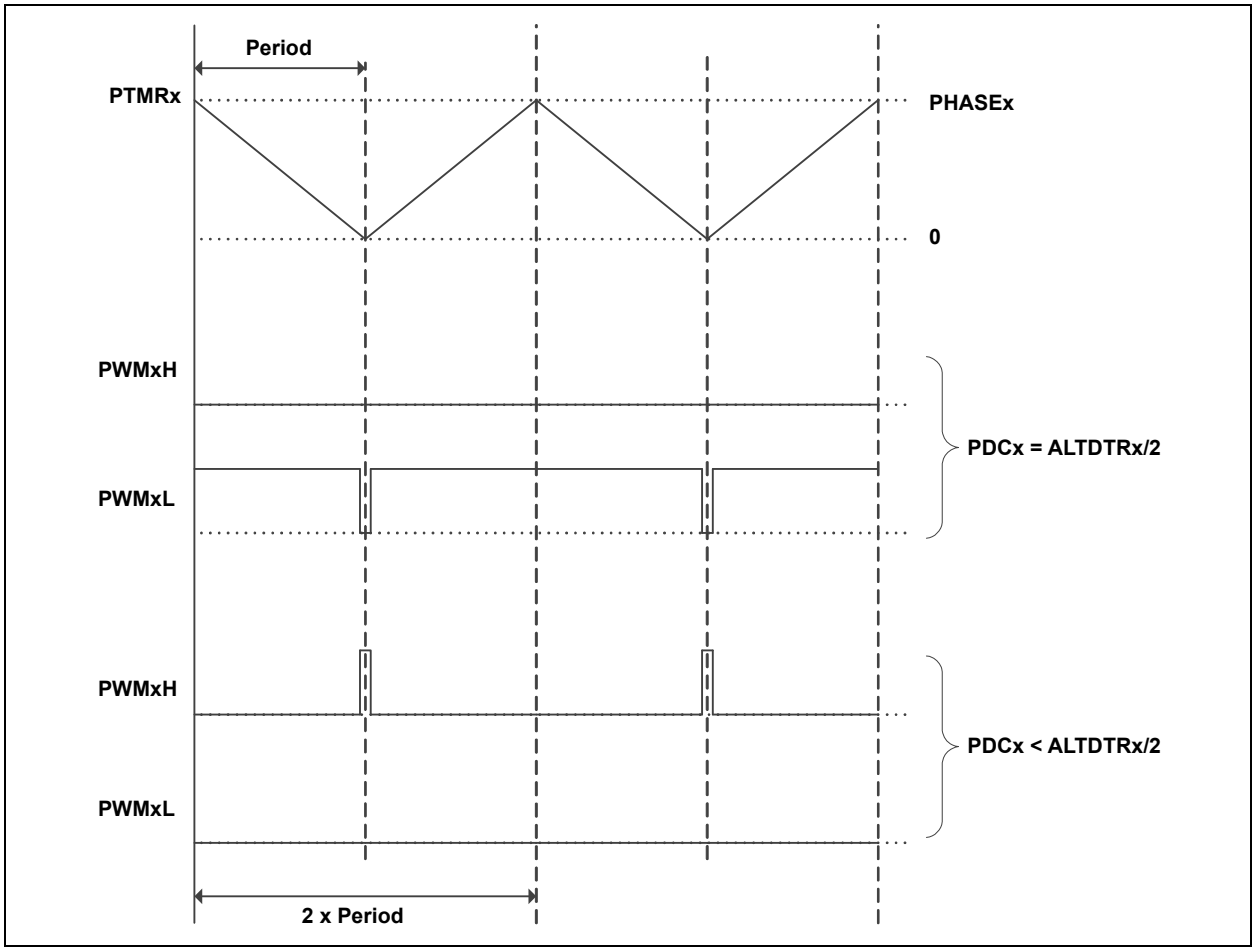
Affected Silicon Revisions

D1	D2						
X	X						

14. Module: PWM

In Center-Aligned Complementary mode with Independent Time Base, if the value in the PDCx register is less than one-half the value in the ALTDTRx register, the PWM generator will force the PWMxL to low, and on the PWMxH, generate pulses of width less than twice the dead time, as shown in Figure 2.

FIGURE 2: PWM GENERATOR TIMING DIAGRAM



Work around

Include a software routine to ensure that the duty cycle value written to the PDCx register is always at least one-half of the value in ALTDTRx. Example 2 shows one method, with `PDCtemp` representing the variable which has the value to be written to the PDCx register. Alternatively, for duty cycle values less than half the desired dead-time value, zero out the ALTDTRx register or dynamically reduce the value in the ALTDTRx register, such that ALTDTRx is always equal to 2 * PDCx, as shown in Example 3.

EXAMPLE 2: WORK AROUND CODE

```
Altdtr_by2 = ALTDTRx / 2;
if (PDCtemp < Altdtr_by2)
{
PDCx = Altdtr_by2;
}
else
{
PDCx = PDCtemp;
}
```

EXAMPLE 3: WORK AROUND CODE

```
#define DESIRED_DEADTIME 100
if (PDCtemp < (DESIRED_DEADTIME/2))
{
ALTDTRx = PDCtemp * 2;
PDCx = PDCtemp;
}
else
{
ALTDTRx = DESIRED_DEADTIME;
PDCx = PDCtemp;
}
```

Affected Silicon Revisions

D1	D2						
X	X						

15. Module: PWM

In Complementary mode after the PWMx module is enabled (PTEN = 1), if the PWM override is turned off, a 1 TOSC glitch will be present on the rising edge of either PWMxH or PWMxL, whichever occurs first, as shown in Figure 3. The glitch will be present on PWMxH/PWMxL every time the override state is changed from enabled to disabled. The width of this glitch is equal to 1 TOSC when PCLKDIV[2:0] = 000; increasing the PWM input clock prescaler setting will increase the width of the glitch accordingly.

Since the width of the glitch is just 1 TOSC at higher values of FOSC, the glitch may not be visible on the PWMxH/PWMxL pins due to pin and PCB trace capacitances.

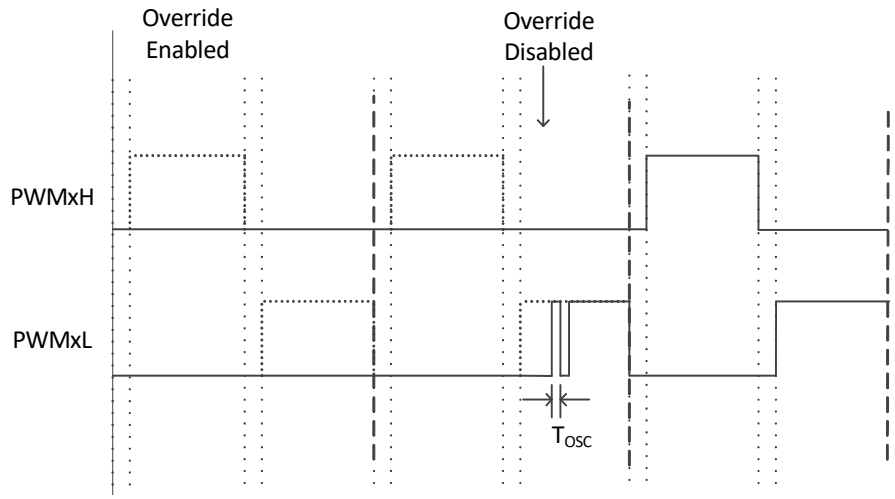
Work around

None.

Affected Silicon Revisions

D1	D2						
X	X						

FIGURE 3: ILLUSTRATION OF 1 TOSC GLITCH WHEN PWM OVERRIDE IS TURNED OFF



16. Module: PWM

In Edge-Aligned Complementary mode, changes to the PHASEx register under certain circumstances will result in missing dead time at the PWMxH-to-PWMxL transition. This has been observed only when all of the following are true:

- Master Time Base mode is enabled (PWMCONx[9] = 0);
- PHASEx is changed after the PWMx module is enabled; and
- The PHASEx register value is changed, so that either PHASEx < DTRx or PHASEx > PDCx.

Work around

None.

Affected Silicon Revisions

D1	D2						
X	X						

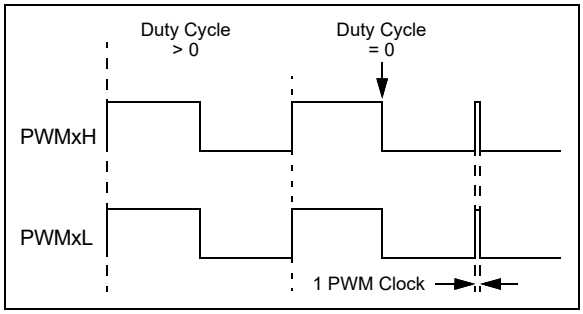
17. Module: PWM

In certain output modes, the PWMx module produces a pulse glitch of one PWM clock in width (Figure 4). This has been observed only when all of the following are true:

- Either Redundant or Push-Pull Output mode is selected (IOCONx[11:10] = 10 or 01);
- Immediate Update is disabled (PWMCONx[0] = 0); and
- The value of the current Duty Cycle register (either the PDCx or MDC register, as determined by PWMCONx[8]) is updated to zero from any non-zero value.

The pulse glitch has been observed to occur at the beginning of the following PWM boundary period.

FIGURE 4:



Work around

If the application requires a duty cycle of zero, two possible work arounds are available.

1. Use the PWM overrides to force the output to a low state instead of writing a '0' to the Duty Cycle register. When using this method, the PWM override must be disabled when the duty cycle is a non-zero value. If output override synchronization is configured to occur on CPU clock boundaries (IOCONx[0] = 0), enabling and disabling the override must be timed to occur as closely as possible to the PWM period boundary.
2. Configure the module for Immediate Update (PWMCONx[0] = 1) *before* enabling the module. In this mode, writes to the Duty Cycle register have an immediate effect on the output. As with the previous work around, writes to the Duty Cycle register must be timed to occur as close to the PWM period boundary as possible in order to avoid distortion of the output.

Affected Silicon Revisions

D1	D2						
X	X						

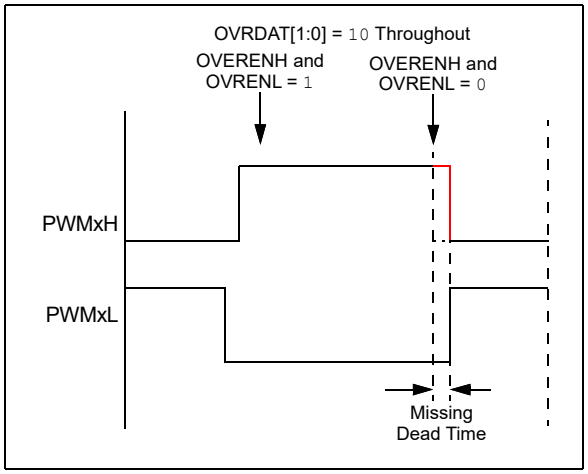
18. Module: PWM

In Complementary Output mode, the expected dead time between transitions of the PWMxH and PWMxL outputs may not be asserted when the following occurs:

- Output override synchronization is configured to occur on the CPU clock boundary (IOCONx[0] = 0);
- Both PWMxH and PWMxL overrides are enabled prior to the event (OVRENH and OVRENL are both '1'); and
- Both overrides are disabled (OVRENH and OVRENL are both '0') at the instant the dead time should be asserted (Figure 5).

This has been observed in both Center-Aligned and Edge-Aligned modes.

FIGURE 5:



Work around

None.

Affected Silicon Revisions

D1	D2						
X	X						

19. Module: PWM

In Center-Aligned Complementary mode with Independent Time Base, the expected dead time between transitions of the PWMxH and PWMxL outputs may not be asserted when SWAP is disabled under the following conditions:

- PWMx module is enabled (PTEN = 1).
- SWAP is enabled prior to this event.

Work around

None.

Affected Silicon Revisions

D1	D2						
X	X						

20. Module: PWM

In Center-Aligned Complementary mode with Independent Time Base, updates to the PHASEx register take effect in the middle of a center-aligned PWM cycle, as shown in Figure 6. This occurs only when the Immediate Update feature is disabled (IUE = 0). If Immediate Update is enabled (IUE = 1), the PHASEx register updates will take effect immediately.

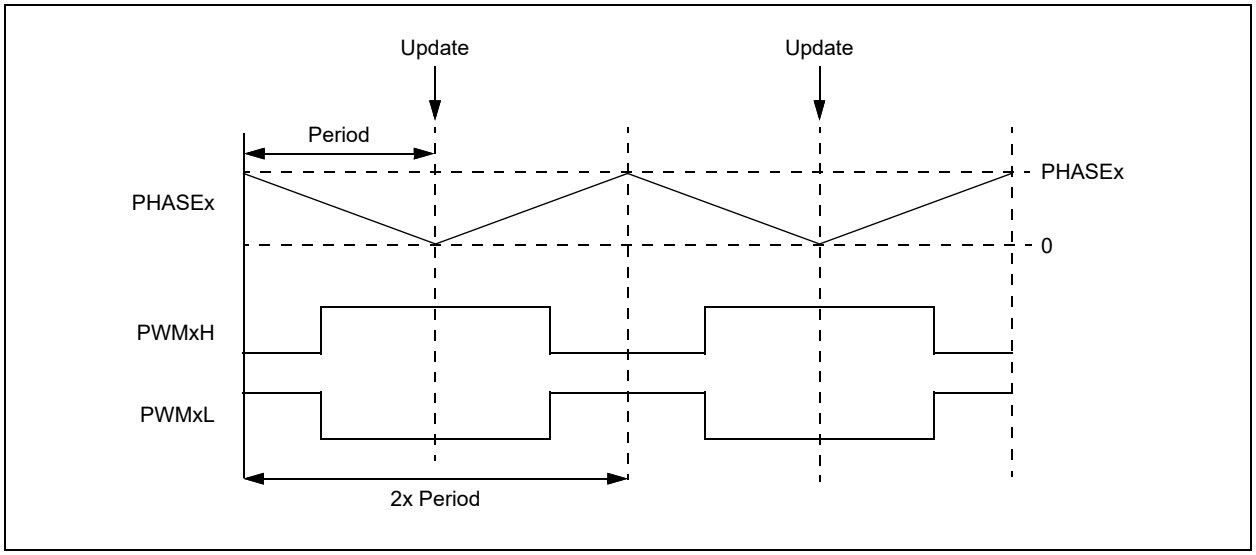
Work around

None.

Affected Silicon Revisions

D1	D2						
X	X						

FIGURE 6:



21. Module: QEI

In Quadrature Encoder mode (CCM[1:0] (QEIxCON[1:0]) = 00), the Index Counter registers (INDXxCNTH and INDXxCNTL) cannot be relied upon to increment when the last known direction was positive and an index pulse occurs. The Index Counter register can decrement even if the last known direction was positive. This does not apply to the External Clock or Internal Timer QEI modes.

Work around

The index event can be used to implement a software counter. The direction could be determined by comparing the current POSxCNT value to that of the previous index event.

Affected Silicon Revisions

D1	D2						
X	X						

22. Module: QEI

When Modulo Count mode (Mode 6) is selected for the position counter (PIMOD[2:0] (QEIxCON[12:10]) = 110), and the counter direction is set to negative (CNTPOL (QEIxCON[3]) = 1), the functions of the QEIxLEC and QEIxGEC registers are reversed.

Work around

When using Modulo Count mode in conjunction with a negative count direction (polarity), use the QEIxLEC register as the upper count limit and the QEIxGEC register as the lower count limit.

Affected Silicon Revisions

D1	D2						
X	X						

23. Module: QEI

The Velocity Counter x (VELxCNT) register is a 16-bit wide register that increments or decrements based on the signal from the quadrature decoder logic. Reading this register results in a Counter Reset. Typically, the user application should read the Velocity Counter at a rate of 1-4 kHz.

As a result of this issue, the Velocity Counter may miss a count if the user application reads the Velocity Counter x register at the same time as a (+1 or -1) count increment occurs.

Work around

None.

Affected Silicon Revisions

D1	D2						
X	X						

24. Module: ADC

Selection of channels for channel scan operation is limited to those available in the AD1CSSL register (AN0 through AN15). Selections in the AD1CSSH register, (OA1 through OA3, CTMU TEMP and CTMU Open) are not available.

Work around

There is no work around of the CTMU TEMP and CTMU Open selections. OA1 through OA3 can be scanned using AN3, AN0 and AN6 for Op Amp 1, Op Amp 2 and Op Amp 3, respectively.

Affected Silicon Revisions

D1	D2						
X	X						

25. Module: CTMU

The CTMU cannot be used with the A/D Converter when the converter is operating in 12-bit mode.

Work around

None.

Affected Silicon Revisions

D1	D2						
X	X						

26. Module: Input Capture

When an input capture module is selected as the Sync source for either an output compare module or another input capture module, synchronization may fail.

Work around

None.

Affected Silicon Revisions

D1	D2						
X	X						

27. Module: Output Compare

Under certain circumstances, an output compare match may cause the Output Compare Interrupt Flag (OCxIF) to become set prior to the Change-of-State (COS) of the OCx pin. This has been observed when all of the following are true:

- The module is in One-Shot mode (OCM[2:0] = `001`, `010` or `100`);
- One of the timer modules is being used as the time base; and
- A timer prescaler other than 1:1 is selected.

If the module is re-initialized by clearing the OCM[2:0] bits after the one-shot compare, the OCx pin may not be driven as expected.

Work around

After OCxIF is set, allow an interval (in CPU cycles) of at least twice the prescaler factor to elapse before clearing OCM[2:0]. For example, for a prescaler value of 1:8, allow 16 CPU cycles to elapse after the interrupt.

Affected Silicon Revisions

D1	D2						
X	X						

28. Module: Op Amp/Comparator

Op amp/comparator voltage reference can choose its source either from VREF+ or AVDD, depending on the CVRSS bit (CVRCON[4]) setting.

If the CVRSS bit is set to '1', the comparator voltage reference source will be CVRSRC = (VREF+) – (AVSS). Due to this issue, if the CVRSS bit is set to '1' and the voltage on VREF+ is less than 1.33V, the op amp/comparator voltage reference will malfunction.

Work around

None.

Affected Silicon Revisions

D1	D2						
X	X						

29. Module: MOSFET Gate Driver

When the MOSFET gate driver HVDD is momentarily sustained at near the POR threshold of 2.7V to 3.2V, followed by device normal operation, and if the MOSFET gate driver entered into Sleep mode, the MOSFET gate driver appears not to wake up from Sleep. The momentarily-sustained HVDD condition could occur with rising or falling HVDD. Only the Sleep mode is affected.

Work around

Use Standby mode of operation for MOSFET gate driver, if application desires lower power than the Active mode. Do not use Sleep mode on MOSFET gate driver.

Affected Silicon Revisions

D1	D2						
X							

30. Module: MOSFET Gate Driver

After any device Reset, when the high-side driver is enabled for the first time, an erroneous XUVLO (External MOSFET Undervoltage Lock Out) FAULT may be triggered. This will disable the HSx outputs. This issue affects only the XUVLO fault on high-side gate drivers.

Work around

Clear the XUVLO upon initiating high-side gate drive sequence using one of the following workaround options. After the workaround sequence, read the STAT0 and STAT1 registers to ensure the FAULT has been cleared successfully. Once the initial FAULT is cleared, the device will resume normal operation.

Workaround #1

1. Monitor $\overline{\text{FAULT}}$ signal until active.
2. Disable Output Enable (OE) pin.
3. Delay 400 µS.
4. Enable OE pin.

```
#define OE   LATAbits.LATA7
#define FAULT PORTAbits.RA10
while(!FAULT){
    OE = 0;
    Delay1uS(400); // delay of 400uS to
                   // avoid device entering
                   // standby mode after OE is
                   // set low
    OE = 1;
}
```

Workaround #2

1. Monitor $\overline{\text{FAULT}}$ signal until active.
2. Disable Output Enable (OE) pin.
3. Send new configuration data to CFG0 via DE2 communication pin.
4. Enable OE pin.

```
//initialize UART module for DE2 communication.
Refer to MOSFET Gate Driver device chapter
describing DE2 communication port.

#define OE   LATAbits.LATA7
#define FAULT PORTAbits.RA10
while(!FAULT){
    OE = 0;
    U1TXREG = 0x81; //send first byte, write
                    //to CFG0 register of
                    //MOSFET gate driver

    while(U1STAbits.URXDA == 0);

//wait for transmission to complete

    U1TXREG = 0x07; //configure MOSFET Gate
                    //Driver with XUVLO enabled

    while(U1STAbits.URXDA == 0);

//wait for transmission to complete

    OE = 1;        //enable OE
  }
```

Affected Silicon Revisions

D1	D2						
X	X						

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS70005292**F**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

None.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (9/2020)

Initial version of this document; issued for unreleased silicon revision.

Rev B Document (3/2022)

Updated for initial released silicon revision D1.

Rev C Document (5/2023)

Added silicon issue 29 (MOSFET Gate Driver).

The I^2C/SPI standards use the terminology “Master” and “Slave”. The equivalent Microchip terminology used in this document is “Host” and “Client”, respectively.

Rev D Document (1/2024)

Added Silicon Revision D2.

Rev E Document (5/2024)

Added silicon issue 30 (MOSFET Gate Driver).

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