BROADCOM®

Data Sheet

ACPL-M71U and ACPL-M72U

Wide Operating Temperature, High-Speed, Low-Power Digital Optocouplers with R2Coupler™ Isolation

Description

The Broadcom® ACPL-M71U and ACPL-M72U are high-temperature, digital CMOS optocouplers in SOIC-5 packages. These optocouplers use the latest CMOS IC technology to achieve outstanding performance and very low power consumption. All devices operate over the –40°C to 125°C temperature range.

The ACPL-M71U uses a high-speed LED, and the ACPL-M72U uses a low-current LED for lower power dissipation. The high-speed ACPL-M71U features a 35-ns maximum propagation delay (I_F = 10 mA). The ACPL-M72U optocoupler features very low power. With a low 4-mA LED drive current, the ACPL-M72U typical propagation delay is 60 ns.

Each digital optocoupler has a CMOS detector IC, an integrated photodiode, a high-speed transimpedance amplifier, and a voltage comparator with an output driver.

Broadcom R2Coupler™ isolation products provide the reinforced insulation and reliability needed for high-temperature industrial applications.

Features

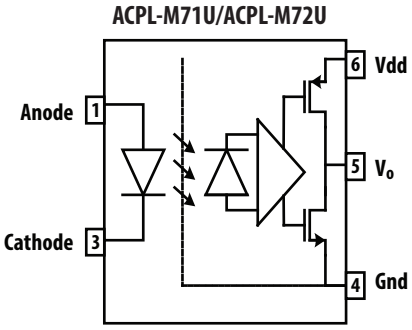
- 5V CMOS compatible
- Common-mode rejection 40 kV/µs at V_{CM} = 1000V
- Wide industrial temperature range: –40°C to 125°C
- Low propagation delay:
  - High-speed ACPL-M71U: 26 ns at I_F = 10 mA (typical)
  - Low-power ACPL-M72U: 60 ns at I_F = 4 mA (typical)
- Worldwide safety approval:
  - UL 1577 recognized, 3750 V_{rms} / 1 min
  - CSA approved
  - IEC/EN/DIN EN 60747-5-5 (for Option x60E)

Applications

- Industrial CANBus communications interface
- Industrial isolated high-speed gate drivers for IGBTs and power MOSFETs
- High-temperature digital signal isolation
- Microcontroller interface
- Digital isolation for A/D and D/A conversion

CAUTION! Take normal static precautions in handling and assembly of this component to prevent damage, degradation, or both that may be induced by ESD. The components featured in this data sheet are not to be used in military or aerospace applications or environments. The components are not AECQ100 qualified and are not recommended for automotive applications.

Functional Block Diagram



NOTE: A 0.1-µF bypass capacitor must be connected between pins 4 and 6.

Truth Table

LED	Output (V_0)
OFF	H
ON	L

Ordering Information

Part Number	Option RoHS-Compliant	Package	Surface Mount	Tape and Reel	IEC/EN/DIN EN 60747-5-5	Quantity
ACPL-M71U	-000E	SO-5	X			100 per tube
	-500E		X	X		1500 per reel
ACPL-M72U	-000E	SO-5	X			100 per tube
	-060E		X		X	100 per tube
	-500E		X	X		1500 per reel
	-560E		X	X	X	1500 per reel

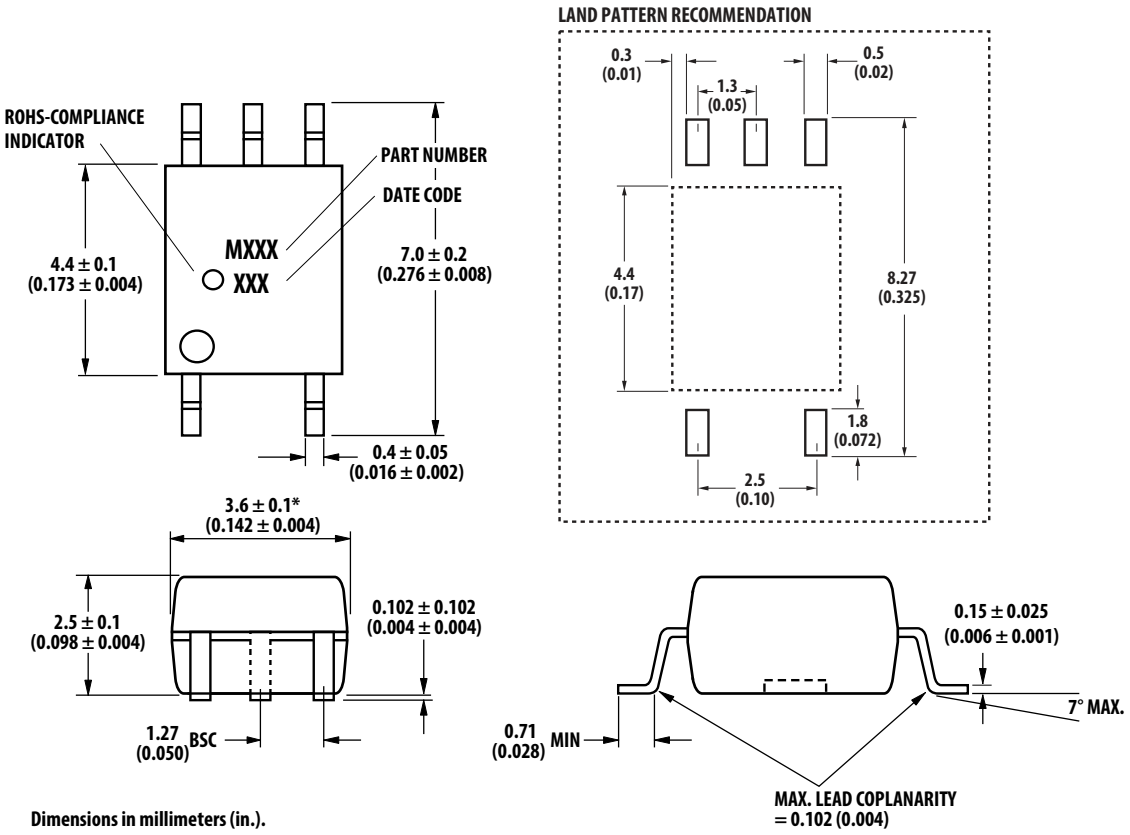
To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

For example, the part number ACPL-M71U-500E describes a device with a surface mount SOIC-5 package; delivered in tape and reel with 1500 parts per reel; and full RoHS compliance.

Option data sheets are available. Contact your Broadcom sales representative or authorized distributor for information.

Package Dimensions

ACPL-M71U/ACPL-M72U (JEDEC MO-155 Package)



Dimensions in millimeters (in.).
Note: Floating Lead Protrusion is 0.15 mm (6 mils) max.

*** Maximum Mold flash on each side is 0.15 mm (0.006 in.).**

Recommended Pb-Free IR Profile

The recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision). Use non-halide flux.

Regulatory Information

The ACPL-M71U and ACPL-M72U are approved by the following organizations.

UL	Approved under UL 1577, component recognition program up to V_{ISO} = 3750 V_{RMS} expected prior to product release.
CSA	Approved under CSA Component Acceptance Notice #5.
IEC/EN/DIN EN 60747-5-5	

Insulation and Safety Related Specifications

Parameter	Symbol	Value	Units	Conditions
Minimum External Air Gap (Clearance)	L(I01)	>5	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (Creepage)	L(I02)	>5	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08	mm	Insulation thickness between emitter and detector; also known as distance through insulation.
Tracking Resistance (Comparative Tracking Index)	CTI	>175	Volts	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa		Material Group (DIN VDE 0109)

IEC/EN/DIN EN 60747-5-5 Insulation Related Characteristics (Option x60E)

Description	Symbol	ACPL-M71U/ ACPL-M72U	Units
Maximum Working Insulation Voltage	V_{IORM}	567	V_{PEAK}
Input to Output Test Voltage, Method b $V_{IORM} \times 1.875 = V_{PR}$, 100% Production Test with t_m = 1 second, Partial Discharge < 5 pC	V_{PR}	1063	V_{PEAK}
Input to Output Test Voltage, Method a $V_{IORM} \times 1.6 = V_{PR}$, Type and Sample Test, t_m = 10 seconds, Partial Discharge < 5 pC	V_{PR}	907	V_{PEAK}
Highest Allowable Overvoltage (Transient Overvoltage, t_{ini} = 60 seconds)	V_{IOTM}	6000	V_{PEAK}
Safety Limiting Values (Maximum values allowed in the event of a failure)			
Case Temperature	T_S	175	°C
Input Current	$I_{s, INPUT}$	150	mA
Output Power	$P_{s,OUTPUT}$	600	mW
Insulation Resistance at T_S, V_{IO} = 500V	R_{IO}	$\geq 10^9$	Ω

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Condition
Storage Temperature	T_S	–55	+150	°C	
Ambient Operating Temperature	T_A	–40	+125	°C	
Supply Voltages	V_{DD}	0	6.5	V	
Output Voltage	V_O	–0.5	V_{DD} + 0.5	V	
Average Forward Input Current	I_F	—	20.0	mA	
Peak Transient Input Current (I_F at 1-µs pulse width, <10% duty cycle)	$I_{F(TRAN)}$	—	1	A	< 1-µs pulse width, 300 pps
		—	80	mA	< 1-µs pulse width,< 10% duty cycle
Reverse Input Voltage	V_r	—	5	V	
Input Power Dissipation	P_I	—	40	mW	
Output Power Dissipation	P_o	—	30	mW	
Lead Solder Temperature	260°C for 10 seconds, 1.6 mm below seating plane				

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Ambient Operating Temperature	T_A	–40	+125	°C
Supply Voltages	V_{DD}	3.0	5.5	V
Forward Input Current	$I_{F(ON)}$	4.0	15	mA
Forward Off State Voltage	$V_{F(OFF)}$	—	0.8	V
Input Threshold Current	I_{TH}	—	3.5	mA

Electrical Specifications

Over recommended temperature (T_A = –40°C to +125°C), 3.0V ≤ V_{DD} ≤ 5.5V. All typical specifications are at T_A = +25°C, V_{DD} = +5V.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Figure
Input Capacitance	C_{IN}	—	90	—	pF		
Input Reverse Breakdown Voltage	BV_R	5.0	—	—	V	I_R = 10 µA	
Logic High Output Voltage	V_{OH}	V_{DD} –0.6	—	—	V	I_{OH} = –4 mA	4
Logic Low Output Voltage	V_{OL}	—	—	0.6	V	I_{OL} = 4 mA	3
Logic Low Output Supply Current	I_{DDL}	—	0.9	1.5	mA		
Logic High Output Supply Current	I_{DDH}	—	0.9	1.5	mA		
LED Forward Voltage	V_f	1.45	1.5	1.75	V	I_F = 10 mA, Ta = 25°C	
		1.25	1.5	1.85	V	I_F = 10 mA, Ta = –40°C ~ 125°C	
V_f Temperature Coefficient		—	–1.5	—	mV/°C		

ACPL-M71U High-Speed Mode Switching Specifications

Over recommended temperature (T_A = –40°C to +125°C), 4.5 V ≤ V_{DD} ≤ 5.5 V. All typical specifications are at T_A = +25°C, V_{DD} = 5V.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Figure	Note
Propagation Delay Time to Logic Low Output[a]	t_{PHL}	—	26	35	ns	V_{in} = 4.5V to 5.5V, R_{in} = 390Ω ±5%, C_{in} = 100 pF, C_L = 15 pF	5, 6, 11	a, b, c
Propagation Delay Time to Logic High Output[a]	t_{PLH}	—	26	35	ns			
Pulse Width Distortion[b]	PWD	—	0	12	ns			
Propagation Delay Skew[c]	t_{PSK}	—	—	15	ns			
Output Rise Time (10% - 90%)	t_R	—	10	—	ns			
Output Fall Time (90% - 10%)	t_F	—	10	—	ns			
Common Mode Transient Immunity at Logic High Output[d]	$\lvert CM_H \rvert$	15	25	—	kV/µs	V_{in} = 0V R_{in} = 390Ω ±5%, C_{in} = 100 pF, V_{cm} = 1000V, T_A = 25°C	12	d
Common Mode Transient Immunity at Logic High Output[e]	$\lvert CM_L \rvert$	15	25	—	kV/µs	V_{in} = 4.5V to 5.5V, R_{in} =390Ω ±5%, C_{in} = 100 pF, V_{cm} = 1000V, T_A = 25°C	13	e

a. t_{PHL} propagation delay is measured from the 50% (Vin or If) on the rising edge of the input pulse to 0.8V on the falling edge of the V_O signal. t_{PLH} propagation delay is measured from the 50% (Vin or If) on the falling edge of the input pulse to the 80% level of the rising edge of the V_O signal.

b. PWD is defined as $|t_{PHL} - t_{PLH}|$.

c. t_{PSK} is equal to the magnitude of the worst case difference in t_{PHL} and/or t_{PLH} that will be seen between units at any given temperature within the recommended operating conditions.

d. CM_H is the maximum tolerable rate of rise of the common mode voltage to assure that the output will remain in a high logic state.

e. CM_L is the maximum tolerable rate of fall of the common mode voltage to assure that the output will remain in a low logic state.

ACPL-M72U Low Power Mode Switching Specifications

Over recommended temperature (–40°C to +125°C), 3.0V ≤ V_{DD} ≤ 5.5V. All typical specifications at +25°C and V_{DD} = 5V.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Figure	Note
Propagation Delay Time to Logic Low Output[a]	t_{PHL}	—	60	100	ns	I_F = 4 mA, C_L = 15 pF	7, 8, 9, 10, 14	a, b, c
Propagation Delay Time to Logic High Out[a]	t_{PLH}	—	35	100	ns			
Pulse Width Distortion[b]	PWD	—	25	50	ns			
Propagation Delay Skew[c]	t_{PSK}	—	—	60	ns			
Output Rise Time (10% to 90%)	t_R	—	10	—	ns			
Output Fall Time (90% to 10%)	t_F	—	10	—	ns			
Common Mode Transient Immunity at Logic High Output[d]	$\lvert CM_H \rvert$	25	40	—	kV/µs	Using Broadcom LED driving circuit, V_{IN} = 0V, R_1 = 350Ω ±5%, R_2 = 350Ω ±5%, V_{CM} = 1000V, T_A = 25°C	15	d
Common Mode Transient Immunity at Logic High Output[e]	$\lvert CM_L \rvert$	25	40	—	kV/µs	Using Broadcom LED driving circuit, V_{IN} = 4.5V to 5.5V, R_1 = 350Ω ±5%, R_2 = 350Ω, V_{CM} = 1000V, T_A = 25°C	16	e

a. t_{PHL} propagation delay is measured from the 50% (Vin or If) on the rising edge of the input pulse to 0.8V on the falling edge of the V_O signal. t_{PLH} propagation delay is measured from the 50% (Vin or If) on the falling edge of the input pulse to the 80% level of the rising edge of the V_O signal.

b. PWD is defined as $|t_{PHL} - t_{PLH}|$.

c. t_{PSK} is equal to the magnitude of the worst case difference in t_{PHL} and/or t_{PLH} that will be seen between units at any given temperature within the recommended operating conditions.

d. CM_H is the maximum tolerable rate of rise of the common mode voltage to assure that the output will remain in a high logic state.

e. CM_L is the maximum tolerable rate of fall of the common mode voltage to assure that the output will remain in a low logic state.

Package Characteristics

All typical at T_A = 25°C.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Input-Output Momentary Withstand Voltage	V_{ISO}	3750	—	—	V_{rms}	RH ≤ 50%, t = 1 min., T_A = 25°C
Input-Output Resistance	R_{I-O}	—	10^{14}	—	Ω	V_{I-O} = 500V dc
Input-Output Capacitance	C_{I-O}	—	0.6	—	pF	f = 1 MHz, T_A = 25°C

Performance Plots

Figure 1: Typical Diode Input Forward Current Characteristic

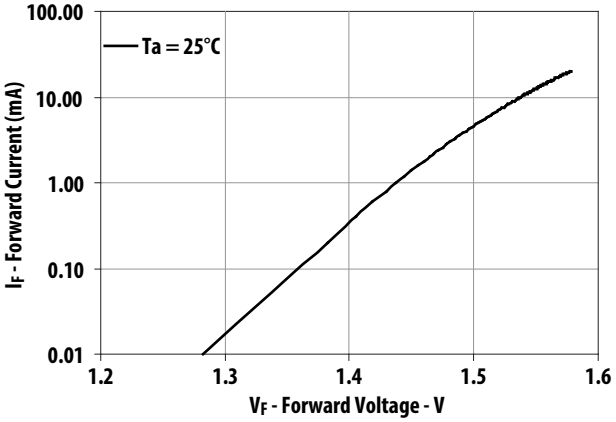


Figure 2: Typical Output Voltage vs. Input Forward Current

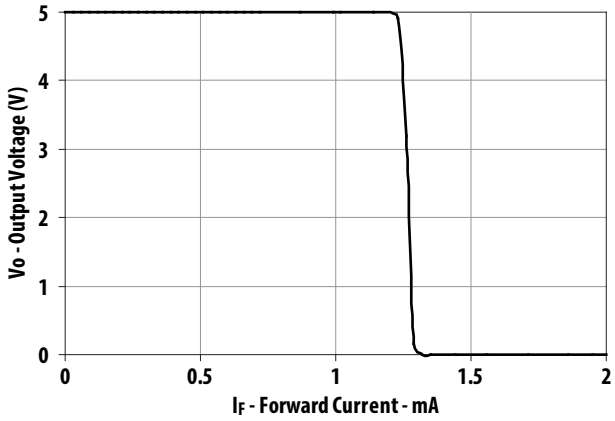


Figure 3: Typical Logic Low Output Voltage vs. Logic Low Output Current

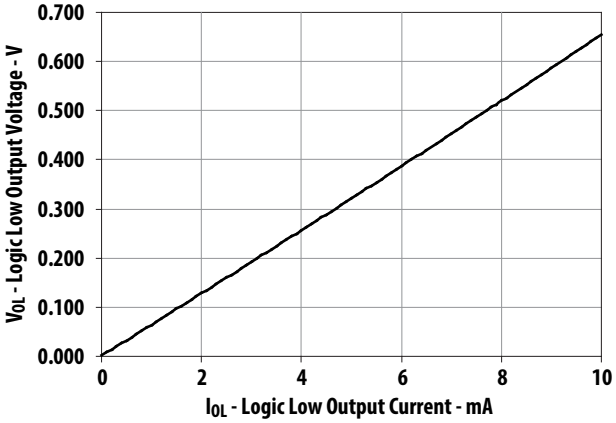


Figure 4: Typical Logic High Output Voltage vs. Logic High Output Current

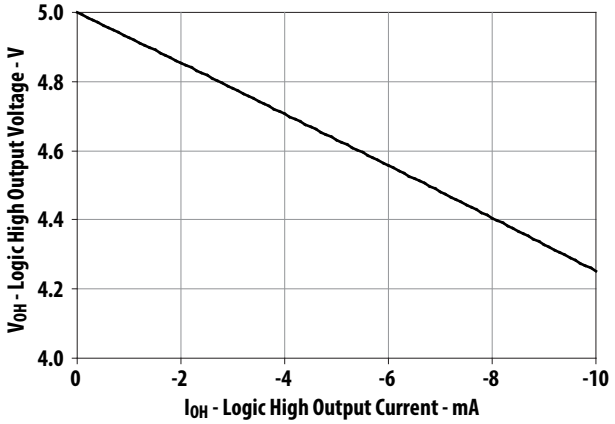


Figure 5: IACPL-M71U (High Speed) Typical Propagation Delay vs. Temperature

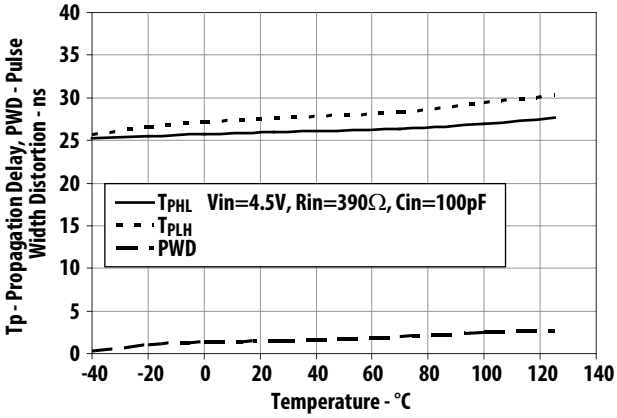


Figure 6: ACPL-M71U (High Speed) Typical Propagation Delay vs. Forward Current – I_F

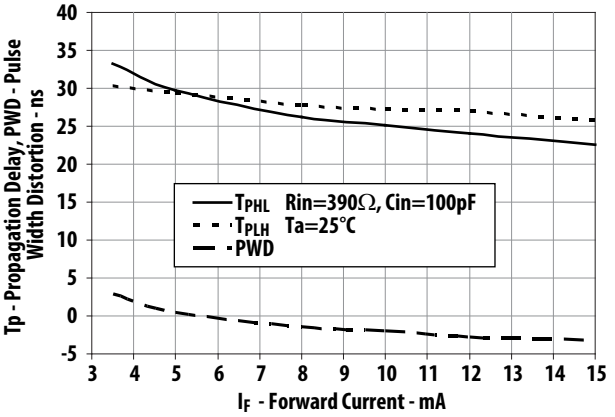


Figure 7: ACPL-M72U (5V) Typical Propagation Delay vs. Temperature

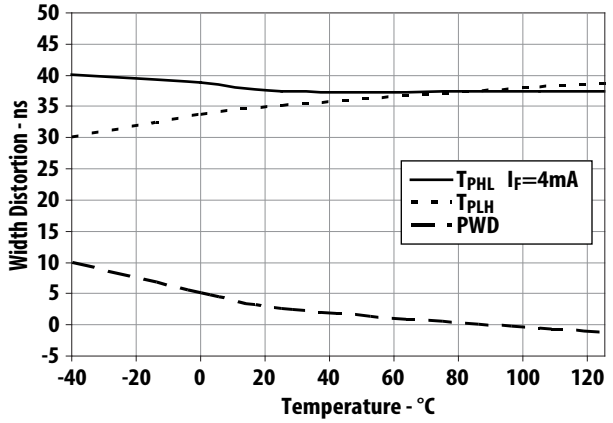


Figure 8: ACPL-M72U (5V) Typical Propagation Delay vs. Forward Current – I_F

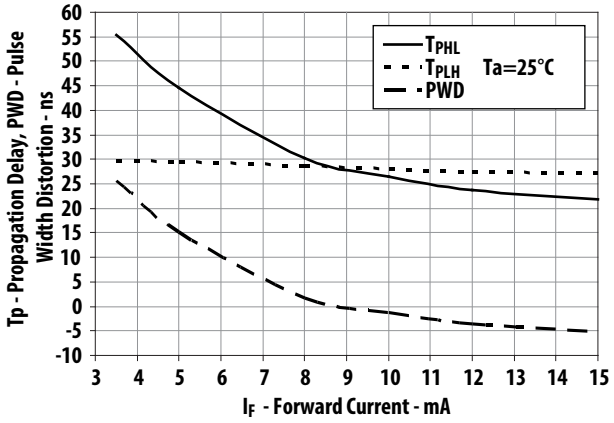


Figure 9: ACPL-M72U (3V) Typical Propagation Delay vs. Temperature

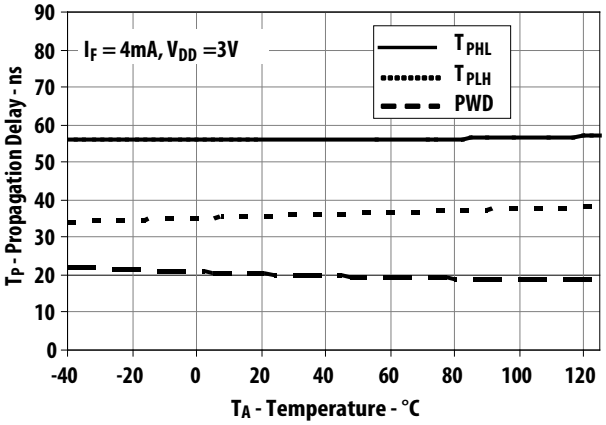
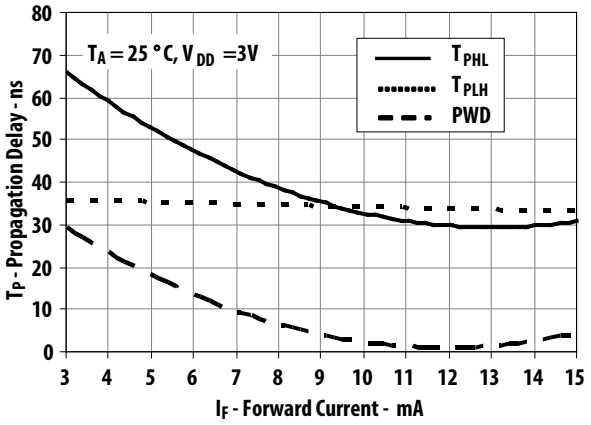


Figure 10: ACPL-M72U (3V) Typical Propagation Delay vs. Input Forward Current



Test Circuit Diagrams

ACPL-M71U High-Speed Mode

Figure 11: High-Speed Mode Test Circuit and Typical Waveform

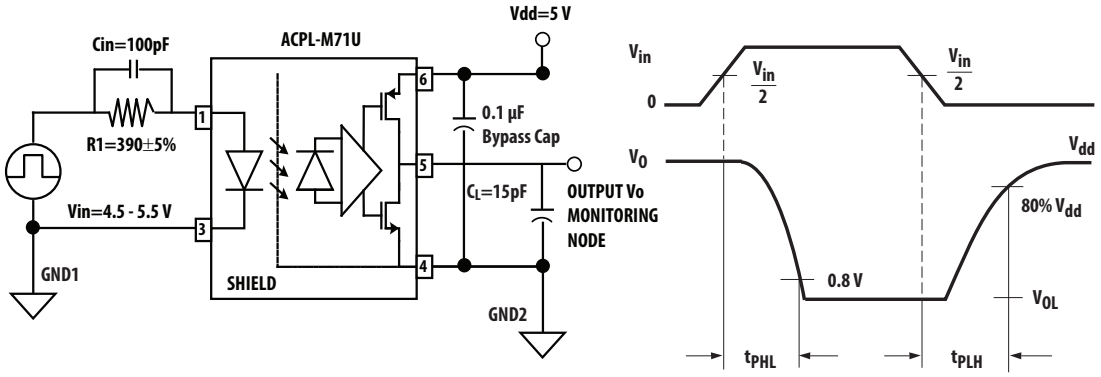


Figure 12: High-Speed Mode CMH Test Circuit and Typical Waveform

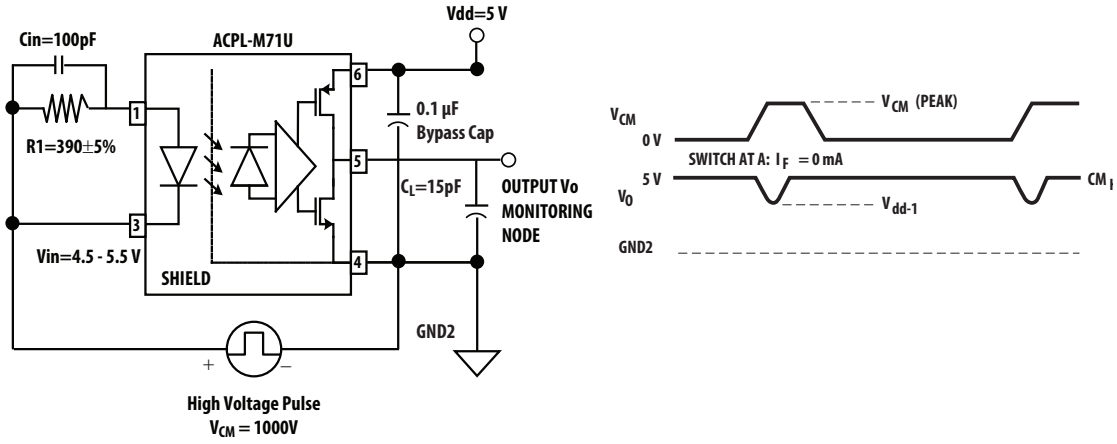
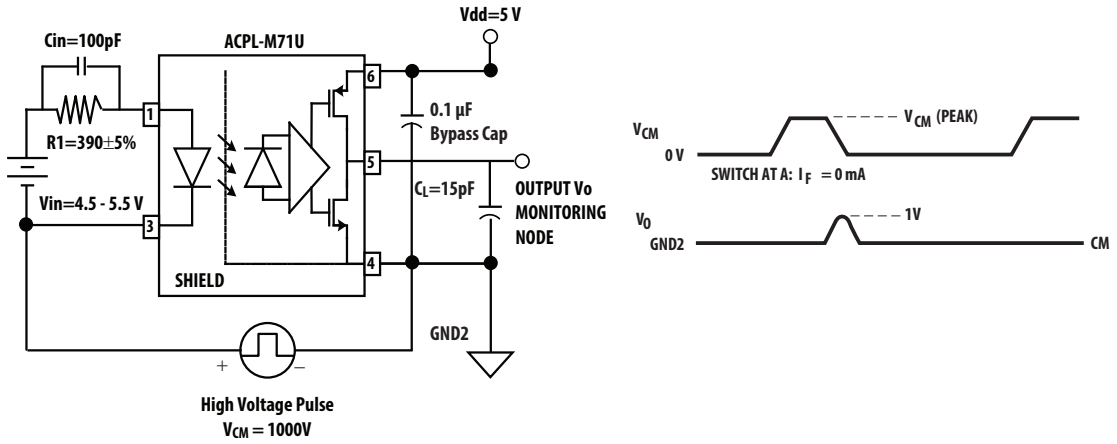


Figure 13: High-Speed Mode CML Test Circuit and Typical Waveform



ACPL-M71U Low-Speed Mode

Figure 14: Low-Power Mode Switching Test Circuit and Typical Waveform

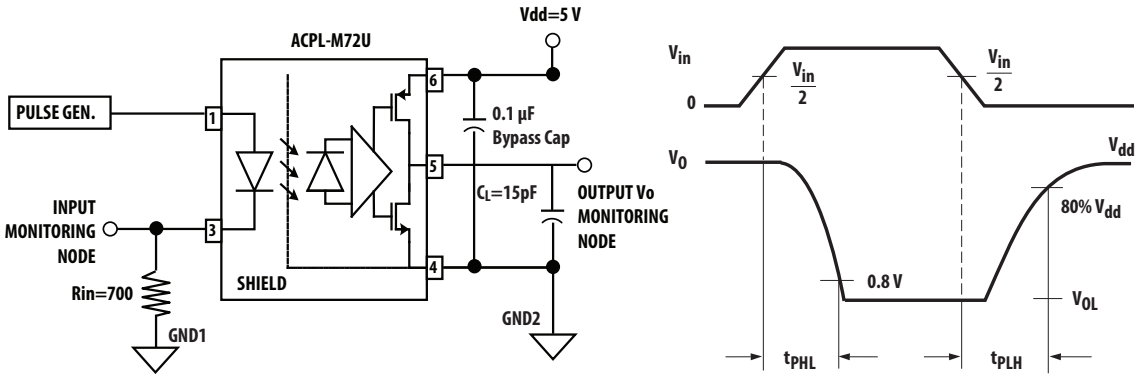


Figure 15: Low-Power Mode High CMR, CMH Test Circuit

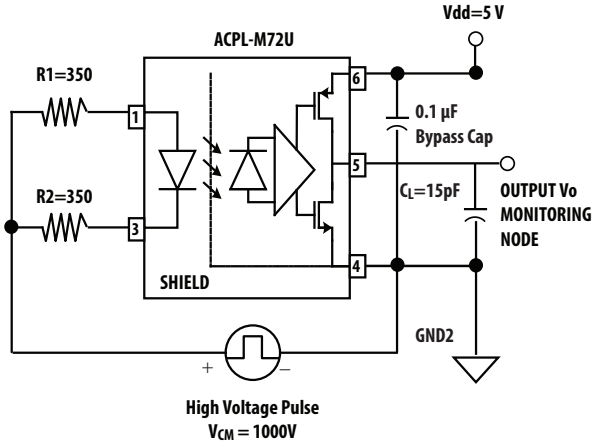
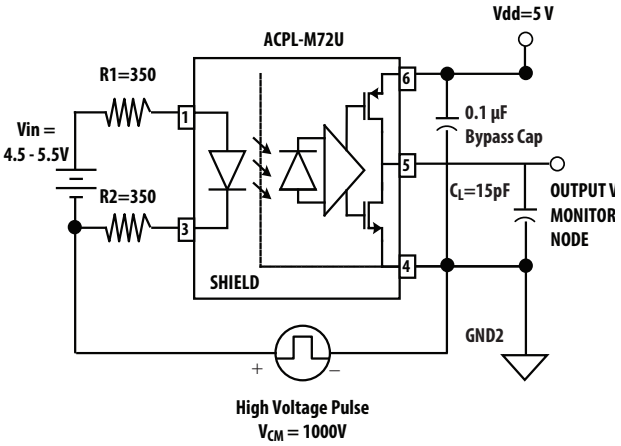
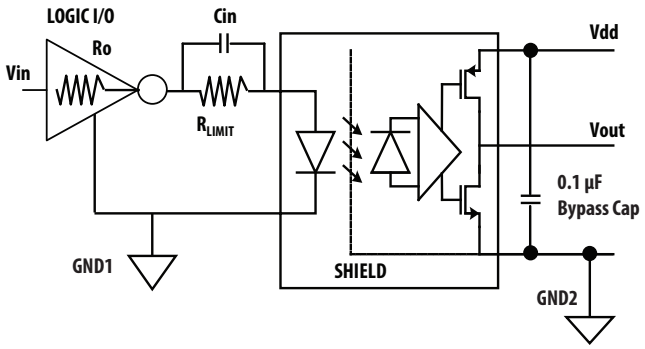


Figure 16: Low-Power Mode High CMR, CML Test Circuit



Application Circuits

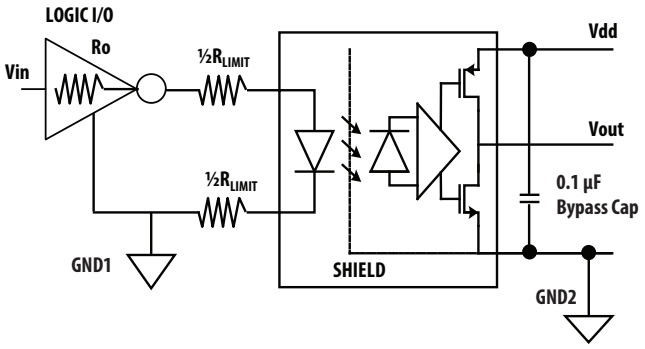
Figure 17: Recommended Application Circuit for ACPL-M71U High Speed Performance



Truth Table

V_{in}	LED	V_{out}
L	ON	L
H	OFF	H

Figure 18: Recommended Application Circuit for ACPL-M72U Low Power Performance



Truth Table

V_{in}	LED	V_{out}
L	ON	L
H	OFF	H

BROADCOM®

Lead (Pb) Free
RoHS 6 fully compliant
RoHS 6 fully compliant options available;
-xxxE denotes a lead-free product