

Document #:PB26383X Issue Date:15 Sep 2024

Title of Change:	NCP81075 datasheet specification update				
Effective date:	15 Sep 2024				
Contact information:	Contact your local onsemi Sales Office or KH.Lee@onsemi.com				
Type of notification:	This Product Bulletin is for notification purposes only. onsemi will proceed with implementation of this change upon publication of this Product Bulletin.				
Change Category:	Datasheet Specification Update				
Change Sub-Category(s):	Datasheet Specification Update				
Sites Affected:					
onsemi Sites		External Foundry/Subcon Sites			
None		None			

Description and Purpose:

The purpose of this notification is to inform customers about NCP81075 product datasheet update on the following sections;

- Change in min, typ and max spec for propagation delay parameters. Figure 12 and 13 were updated in relation to this change.
- The -40 to 125°C EC table lines in propagation delay parameters were already covered by the wider -40 to 140°C spec, so the redundant lines were eliminated."
- Change in min, typ and max spec for output delay matching parameters
- Provide clarity on UVLO (tDUVLO) delay time in relation to VDD slew rate. Fig 2 is updated to show this relationship.
- Updated tMON and tMOFF timing diagram (Fig 3) to show overlap in both edges. Figure 4 is updated in relation to tMON and tMOFF changes as well as Fig 6 to show response over temperature

There is no change in product die design or bill of material. The change will not impact the device's form, fit or function.

Electrical Specification table

CURRENT VERSION

NEW VERSION

Test	Test Condition	min	typ	max	Test	Test Condition	min	typ	max
tDLFF	Cload=0 (-40 to 125°C)		20	45	tDLFF	Cload=0 (-40 to 140°C)	14	20.6	30
	Cload=0 (-40 to 140°C)		20	50	IDLFF				
tDHFF	Cload=0 (-40 to 125°C)		20	45	tDHFF	Cload=0 (-40 to 140°C)	14	20.6	30
	Cload=0 (-40 to 140°C)		20	50	LUHFF				
tDLRR	Cload=0 (-40 to 125°C)		20	45	tDLRR	Cload=0 (-40 to 140°C)	12	18.8	28
	Cload=0 (-40 to 140°C)		20	50	LULKK				
tDHRR	Cload=0 (-40 to 125°C)		20	45	tDHRR	Cload=0 (-40 to 140°C)	12	18.8	28
	Cload=0 (-40 to 140°C)		20	50	LDHKK				
tMON			3.5	14	tMON		-10	-1.4	6
tMOFF			3.5	14	tMOFF		-10	-2.4	6

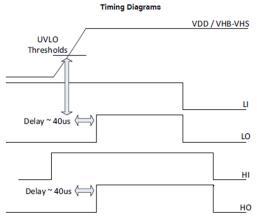
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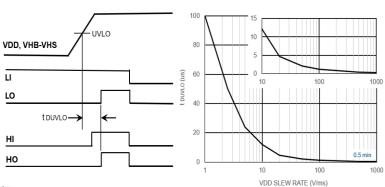
FIGURE 2: UVLO timing diagram

CURRENT VERSION



Note: If HI is set and the High-Side driver (VHB-VHS) crosses its UVLO threshold 100ns after the VDD UVLO then a rising edge on HI is required to pull HO High. Figure 2. UVLO

NEW VERSION



Notes:
If HI is set and the High-Side driver (VHB-VHS) crosses its UVLO threshold after the VDD UVLO, then another rising HI edge is required to force the HO output high as

For the case where both UVLOs are coincident or VDD UVLO occurs last, the HI, HO response will mimic the LI, LO response shown above.

FIGURE 4: Propagation Delay Timing Diagram

CURRENT VERSION

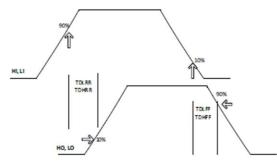


Figure 4. Propagation Delays

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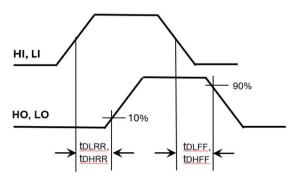
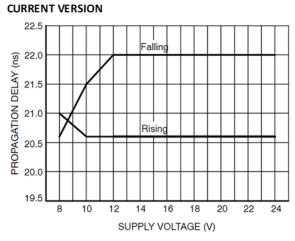
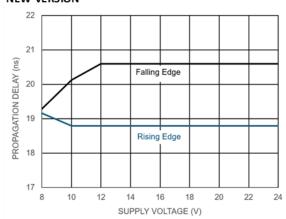


FIGURE 12: Propagation Delay vs Supply Voltage



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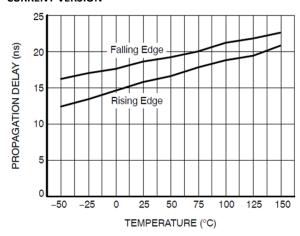


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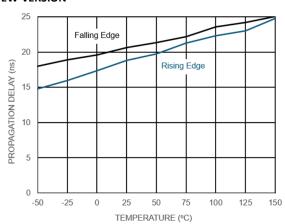
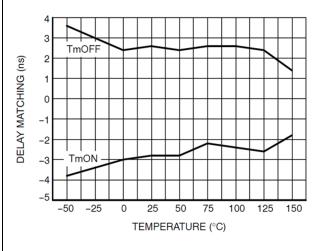


FIGURE 6: Delay Matching vs Temperature CURRENT VERSION



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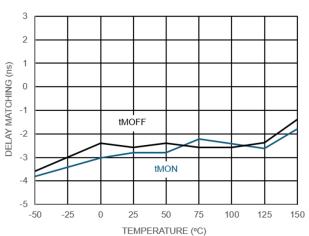
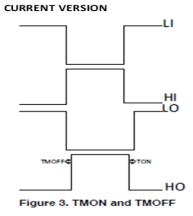
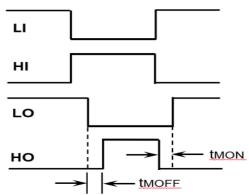


FIGURE 3: TMON and TMOFF



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List of Affected Standard Parts:

Note: Only the standard (off the shelf) part numbers are listed in the parts list. Any custom parts affected by this PCN are shown in the customer specific PCN addendum in the PCN email notification, or on the **PCN Customized Portal**.

NCP81075MNTXG	NCP81075MTTXG	NCP81075DR2G

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