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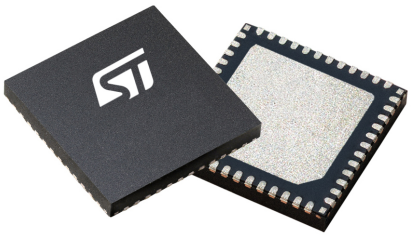
STPM098C

Datasheet

Automotive dual digital 8-phase controller with PMBus™



VFQFN 48+4L
(7x7x0.9 mm)

Product status link
STPM098C

Product summary		
Order code	Package	Packing
STPM098C	VFQPN48+4L	Tray
STPM098C-TR		Tape and reel

Features

- AEC-Q100 qualified
- Phase assignment between two loops: 8+0 to 4+4
- Output voltage range: 0.5 V to 2 V
- Switching frequency range: 200 kHz to 1.5 MHz
- Programmable dynamic phase shedding operation for light loads and active diode emulation for very light loads
- High-performance digital control Loop
- Embedded CPU ARM Cortex™ M0+ at 40 MHz
- Embedded NVM (nonvolatile memory)
- PMBus™ rev 1.2 (max freq. 400 kHz)
- Full ISO26262 compliant, ASIL-D systems ready
- Protection and diagnostic
  - PMBus™ readable input telemetry (voltage, current, power)
  - PMBus™ configurable overcurrent, undervoltage and over-power diagnostics and protection on input metrics
  - PMBus™ readable output telemetry (voltage, current, temperature) for each loop
  - PMBus™ configurable under/overcurrent, under/overvoltage diagnostics and protection on output metrics for each loop
  - PMBus™ configurable thermal warning and thermal shutdown diagnostics and protection on the output stage for each loop
  - PMBus™ readable single-phase current telemetry
  - PMBus™ configurable single-phase overcurrent diagnostics and protection
  - PMBus™ configurable general-purpose UV/OV diagnostic thorough pin AUX_SENSE
  - Feedback loop disconnection diagnostics
  - Internal overtemperature diagnostics and protection
  - PMBus™ readable T_j measurement
  - Ground loss diagnostics
  - System clock monitoring
  - Power supply pins VCC, VREF1, VREF2 overvoltage and undervoltage diagnostics
  - Fault status flag output through SM_ALERT, FAULT, VRRDY1, VRRDY2 pins

Application

- ADAS systems
- High-power microprocessors
- DDR memories

Description

STPM098C is a dual-loop digital multi-phase buck controller with built-in NVM and PMBus™ interface for automotive applications.

The product finds application in the power management of loads that require high power, such as cores of processors and memories. It controls up to 8 external drivers+MOS and, with its two loops, allows to supply up to two different voltages.

An advanced control loop architecture based on COT (constant on-time) scheme provides fast transient responses and high efficiency. The device also provides phase interleaving and dynamic phase add/drop for efficiency enhancement for light load range.

STPM098C supports a ver.1.2 compliant PMBus™ communication with 8 possible interface address values for reporting the telemetry of voltage, current, power, temperature and fault signaling.

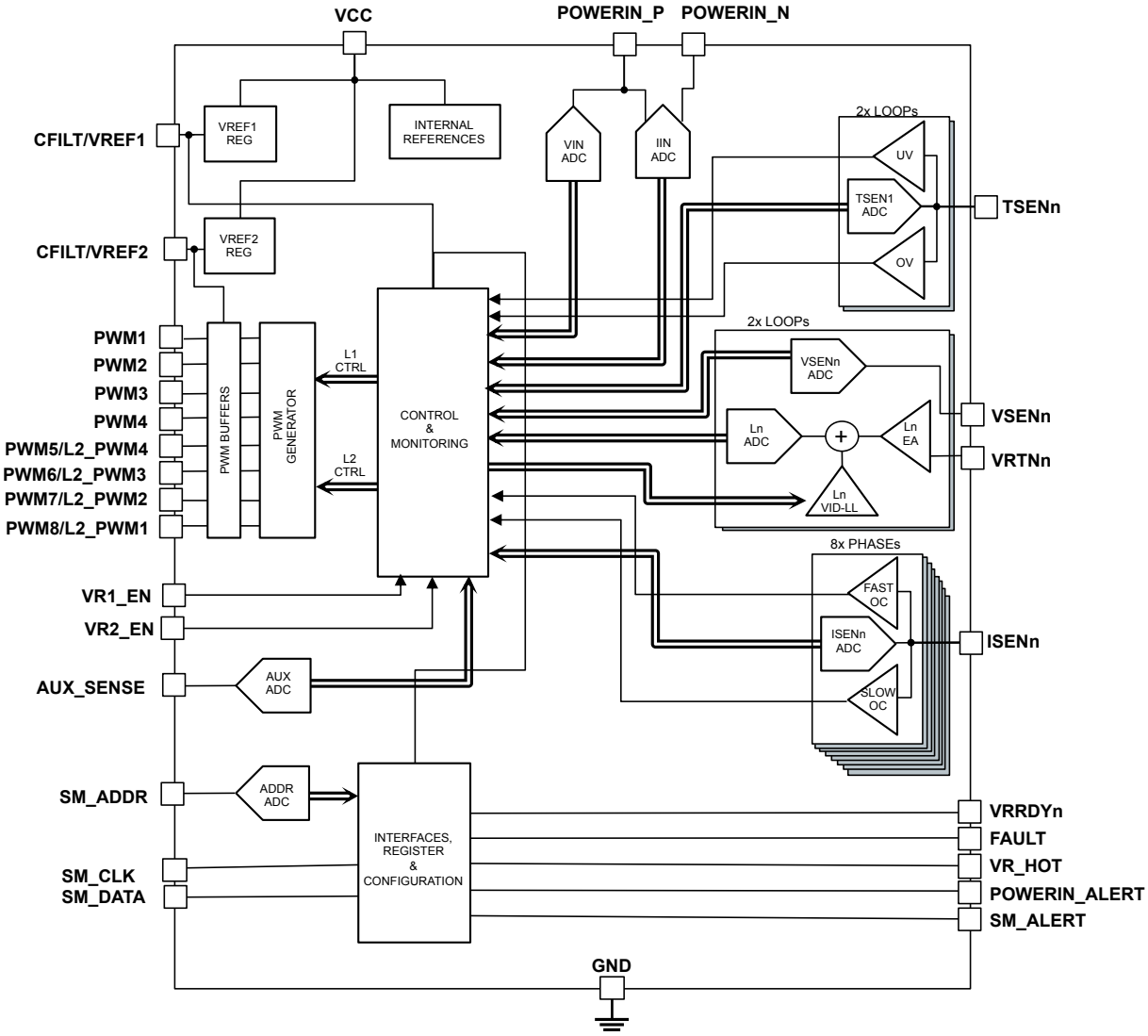
The device programmable parameters can be configured through the PMBus™ interface and stored in an on-chip NVM minimizing external components.

STPM098C additionally provides an extensive monitoring unit system and fault protection including independent UV/OV on output voltage, loop feedback disconnection, phase current unbalancing and dual-threshold overcurrent for both positive and negative phase currents.

1 Block diagram and pins description

1.1 Block diagram

Figure 1. **Simplified block diagram**



1.2 Pins description

Figure 2. **Pins connection diagram**

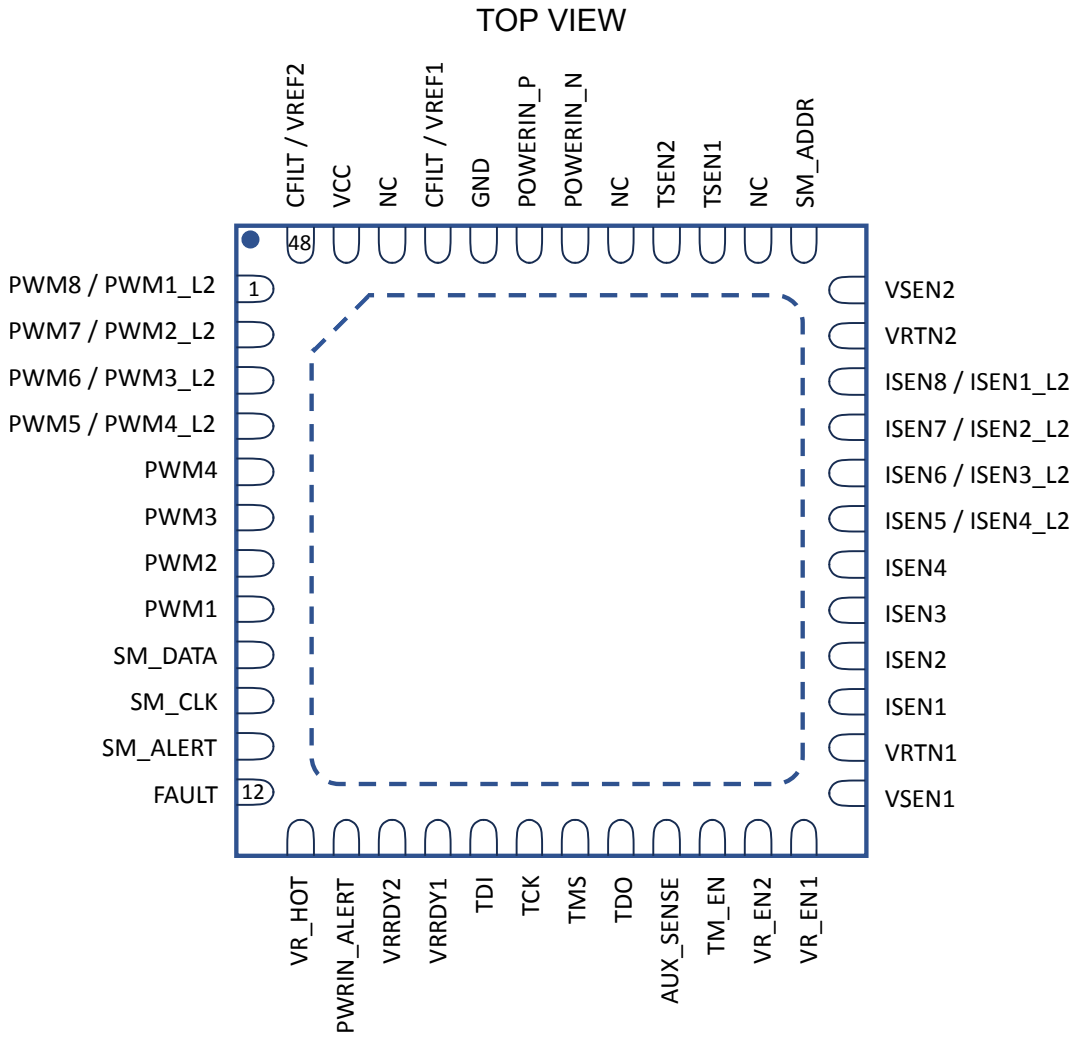


Table 1. Pins list description

#	Name	Description	Type	Class
1	PWM8/PWM1_L2	Loop 1 phase 8 pulse width modulation output. Keep floating if not used Loop 2 phase 1 pulse width modulation output. Keep floating if not used	O	Local
2	PWM7/PWM2_L2	Loop 1 phase 7 pulse width modulation output. Keep floating if not used Loop 2 phase 2 pulse width modulation output. Keep floating if not used	O	Local
3	PWM6/PWM3_L2	Loop 1 phase 6 pulse width modulation output. Keep floating if not used Loop 2 phase 3 pulse width modulation output. Keep floating if not used	O	Local
4	PWM5/PWM4_L2	Loop 1 phase 5 pulse width modulation output. Keep floating if not used Loop 2 phase 4 pulse width modulation output. Keep floating if not used	O	Local
5	PWM4	Loop 1 phase 4 pulse width modulation output. Keep floating if not used	O	Local
6	PWM3	Loop 1 phase 3 pulse width modulation output. Keep floating if not used	O	Local
7	PWM2	Loop 1 phase 2 pulse width modulation output. Keep floating if not used	O	Local
8	PWM1	Loop 1 phase 1 pulse width modulation output. Keep floating if not used	O	Local
9	SM_DATA	PMBus™ bidirectional serial data line. Connect to GND if not used	I/O	Local
10	SM_CLK	PMBus™ serial clock line. Connect to GND if not used	I/O	Local
11	SM_ALERT	PMBus™ alert line (active low). Keep floating if not used	O	Local
12	FAULT	System fault status output (active low). Keep floating if not used	O	Local
13	VRHOT	External temperature alert indicator output (active low). Keep floating if not used	O	Local
14	POWERIN_ALERT	Input power alert indicator output (active low). Keep floating if not used	O	Local
15	VRRDY2	Voltage regulator ready output for loop 2 (active high). Keep floating if not used	O	Local
16	VRRDY1	Voltage regulator ready output for loop 1 (active high). Keep floating if not used	O	Local
17	TDI (debug only)	JTAG interface test data in (connect to GND in final application)	I	NA
18	TCK (debug only)	JTAG interface test clock (connect to GND in final application)	I	NA
19	TMS (debug only)	JTAG interface test mode select (connect to VCC in final application)	I	NA
20	TDO (debug only)	JTAG interface test data out (leave unconnected in final application)	O	NA
21	AUX_SENSE	Auxiliary voltage sense input. Connect to GND if not used	I	Local
22	TM_EN (debug only)	Device test mode entry (connect to GND in final application)	I	NA
23	VR_EN2	Enable input for loop 2 (active high). Connect to GND if not used	I	Local
24	VR_EN1	Enable input for loop 1 (active high). Connect to GND if not used	I	Local
25	VSEN1	Voltage sense input for loop 1. Connect to GND if not used	I	Local
26	VRTN1	Voltage sense return input for loop 1. Connect to GND if not used	I	Local
27	ISEN1	Phase 1 current sense input. Keep floating if not used	I	Local
28	ISEN2	Phase 2 current sense input. Keep floating if not used	I	Local
29	ISEN3	Phase 3 current sense input. Keep floating if not used	I	Local
30	ISEN4	Phase 4 current sense input. Keep floating if not used	I	Local
31	ISEN5/ISEN4_L2	Phase 5 current sense input. Keep floating if not used Loop 2 phase 4 current sense input. Keep floating if not used	I	Local
32	ISEN6/ISEN3_L2	Phase 6 current sense input. Keep floating if not used Loop 2 phase 3 current sense input. Keep floating if not used	I	Local
33	ISEN7/ISEN2_L2	Phase 7 current sense input. Keep floating if not used Loop 2 phase 2 current sense input. Keep floating if not used	I	Local

#	Name	Description	Type	Class
34	ISEN8/ISEN1_L2	Phase 8 current sense input. Keep floating if not used	I	Local
		Loop 2 phase 1 current sense input. Keep floating if not used		
35	VRTN2	Voltage sense return input for loop 2. Connect to GND if not used	I	Local
36	VSEN2	Voltage sense input for loop 2. Connect to GND if not used	I	Local
37	SM_ADDR	PMBus™ device target address	I	Local
38	NC	Not connected	NA	NA
39	TSEN1	Temperature sense input for loop 1. Connect to GND if not used	I	Local
40	TSEN2	Temperature sense input for loop 2. Connect to GND if not used	I	Local
41	NC	Not connected	NA	NA
42	POWERIN_N	Input power sense negative input. Tied to POWERIN_P if not used(1)	I	Local
43	POWERIN_P	Input power sense positive input. GND if not used(1)	I	Local
44	GND	Signal ground (digital, analog, reference)	G	Local
45	CFILT/VREF1	1.8 V reference output voltage. Phase current sense bias	I/O	Local
46	NC	Not connected	NA	NA
47	VCC	Power supply input for internal circuitry	P	Local
48	CFILT/VREF2	3.3 V reference output voltage. PWM buffers bias	I/O	Local
-	Exp. PAD	Cooling slug to be connected to GND plane	-	-

1. *Pin configuration where POWERIN_P pin is used along with POWERIN_N unused at the same time is allowed. Pin configuration where POWERIN_P is unused along with POWERIN_N used is forbidden.*

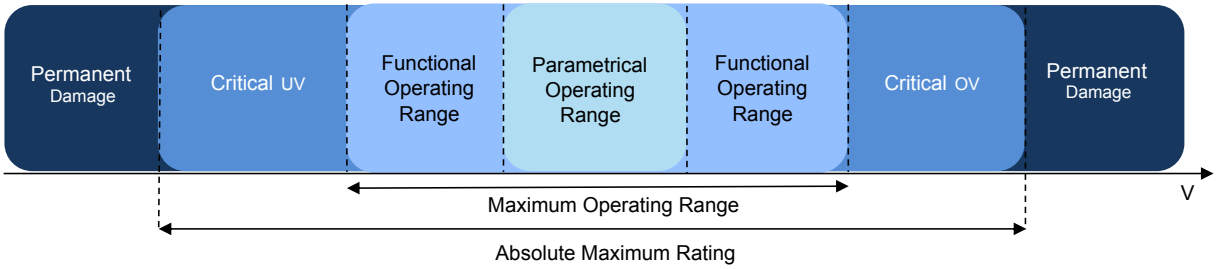
Note: I = Input, O = Output, P = Power supply, G = Ground, I/O = Input/Output.

2 Maximum ratings

In this section the voltage ranges of each pin are specified and divided into three categories:

- Functional operating range
- Parametrical operating range
- Absolute maximum rating

Figure 3. Pins voltage ranges



2.1 Maximum operating range (MOR)

2.1.1 Functional operating range

Within these operating ranges the part operates as specified in the circuit description, electrical characteristics are guaranteed only in the parametrical operating range, between these two ranges parametrical deviation may occur. The device may not operate properly if functional operating range conditions are exceeded. Once taken beyond the functional operative ratings and returned within, the part recovers with no damage or degradation (if AMR range is not exceeded). All analog and digital voltages are related to the potential at signal ground GND. All currents are assumed to be positive when current flows into the pin.

Table 2. Functional operating conditions

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
Power supply							
VCC_MOR	VCC: voltage range		VCC UV	-	VCC OV	V	See Table 7
VCC_MOR_PU	VCC: voltage range for power up		VCC_uv_th (max) + VCC_uv_hist (max)	-	-	V	See Table 7
VCC_MOR_SR	VCC: voltage slew-rate for power up/down		5	-	25	V/ms	Application information

2.1.2 Parametrical operating range (recommended operating range)

Within these operating range the part operates as specified and without parameter deviations. The device may show parameters deviation if parametrical operating conditions are exceeded.

Once taken beyond the operative ratings and returned within, the part will recover with no damage or degradation (if AMR range is not exceeded). All analog and digital voltages are related to the potential at signal ground GND. All currents are assumed to be positive when current flows into the pin.

Table 3. Parametrical operating conditions

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
Power supply							
VCC_MOR_PAR	VCC: voltage range		4.75	5	5.25	V	-

Note: All parameters are guaranteed and tested in the voltage ranges specified in Table 3 unless otherwise specified. Where not specified, parametrical operating range equals functional operating range.

2.1.3 Absolute maximum rating (AMR)

Maximum ratings are absolute ratings; exceeding any one of these values may cause permanent damage to the integrated circuit. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. All analog and digital voltages are related to the potential at signal ground GND. All currents are assumed to be positive when current flows into the pin.

Table 4. Absolute maximum ratings

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit	Notes
PWM outputs							
PWMN_AMR	PWMn: voltage range		-0.3	-	7	V	[n = 1, 2, 3, 4, 5, 6, 7, 8]
CFILT_VREF2_AMR	CFILT/VREF2: voltage range		-0.3	-	7	V	-
D_VCC_CFILT_VREF2_AMR	VCC - CFILT/VREF2: differential voltage between VCC and CFILT/VREF2		-0.3	-	7	V	-
PMBus interface							
SM_DATA_AMR	SM_DATA: voltage range		-0.3	-	7	V	-
SM_CLK_AMR	SM_CLK: voltage range		-0.3	-	7	V	-
SM_ALERT_AMR	SM_ALERT: voltage range		-0.3	-	7	V	-
SM_ADDR_AMR	SM_ADDR: voltage range		-0.3	-	7	V	-
Control loop enable							
VRN_EN_AMR	VRn_EN: voltage range		-0.3	-	2.5	V	[n = 1,2]
Output telemetry and loop control							
VSENN_AMR	VSENn: voltage range		-0.3	-	7	V	[n = 1, 2]
VRTNN_AMR	VRTNn: voltage range		-0.3	-	7	V	[n = 1, 2]
d_ VSENN_ VRTNN_AMR	VSENn – VRTNn: differential voltage between VSENn and VRTNn		-0.3	-	7	V	[n = 1, 2]
ISENN_AMR	ISENn: voltage range		-0.3	-	7	V	[n = 1, 2, 3, 4, 5, 6, 7, 8]
CFILT_ VREF1_AMR	CFILT/VREF1: voltage range		-0.3	-	2.5	V	-
D_VCC_CFILT_VREF1_AMR	VCC - CFILT/VREF1: differential voltage between VCC and CFILT/VREF1		-0.3	-	7	V	-
Input telemetry							
POWERINP_AMR	POWERINP: voltage range		-0.3	-	20	V	-
POWERINN_AMR	POWERINN: voltage range		-0.3	-	20	V	-
d_ POWERINP _ POWERINN _AMR	POWERINP - POWERINN: differential voltage between POWERIN_P and POWERIN_N		-0.3	-	5	V	-
Diagnosis and alerts							
VRRDYN_AMR	VRRDYn: voltage range		-0.3	-	7	V	[n = 1, 2]
VRHOT_AMR	VRHOT: voltage range		-0.3	-	7	V	-
POWERIN_ALERT_AMR	POWERIN_ALERT: voltage range		-0.3	-	7	V	-

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit	Notes
FAULT_AMR	FAULT: voltage range		-0.3	-	7	V	-
AUX_SENSE_AMR	AUX_SENSE: voltage range		-0.3	-	7	V	-
TSENN_AMR	TSENn: voltage range		-0.3	-	7	V	[n = 1, 2]
Power supply							
VCC_AMR	VCC: voltage range		-0.3	-	7	V	-
Grounds							
GND_AMR	AGND, DGND		-0.6	-	0.6	V	-

Note: Integrated protection and diagnostics are designed to prevent device damage under the fault conditions defined in the functional description. Fault conditions are out of normal operating range. Protection functions are not designed for a continuous repetitive operation.

2.2 ESD resistivity

Table 5. ESD resistivity (pin level)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
HBM_ ESD	HBM (1)	All pins	-2	-	2	kV	Class 2
CDM _ESD	CDM (1)	All pins	-500	-	500	V	Class C3
CDM_COR_ESD	CDM (1)	Corner pins	-750	-	750	V	Class C4
LUT	Latch up (2)	All pins	-100	-	100	mA	-

1. *According to AEC-Q100-011.*
2. *According to AEC-Q100-004.*

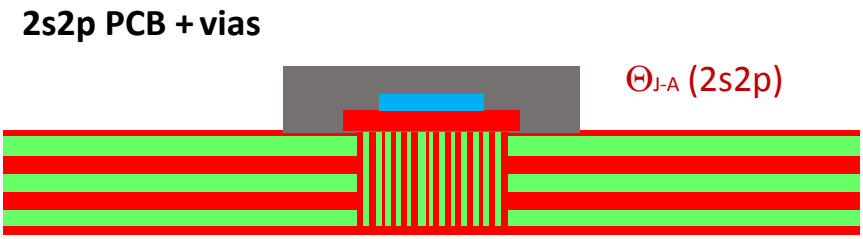
2.3 Temperature ranges and thermal data

Table 6. Temperature ranges and thermal data

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
T_{amb}	Operating temperature (ECU environment)		-40	-	125	°C	-
T_j (1)	Operating junction temperature		-40	-	150	°C	-
T_{sto}	Storage temperature		-55	-	150	°C	-
R_{thJ-A} (2)	Thermal resistance junction-to-ambient		-	26	-	°C/W	Homogeneous internal power distribution (3)
R_{Thj-t} (2)	Thermal resistance junction-to-case-top		-	0.1	-	°C/W	Homogeneous internal power distribution

1. *All parameters are guaranteed, and tested, in the temperature range -40 ≤ T_j ≤ 150°C unless otherwise specified. The device is still operative and functional at higher temperatures (up to T_j 175°C). Device functionality at high temperature is guaranteed by bench validation, electrical parameters are guaranteed by correlation with ATE tests at reduced temperature and adjusted limits (if needed).*
2. *Not subject to production test, guaranteed by design.*
3. *R_{thJA} value is retrieved according to Jedec JESD51-2, -5, -7 guideline with a 2s2p board.*

Figure 4. **2s2p PCB with vias**



Note: In "2s2p", the "s" suffix stands for "signal" and the number before indicates how many PCB layers are dedicated to signal wires. The "p" suffix stands for "power" and the number before indicates how many PCB layers are dedicated to power planes.

3 Functional description

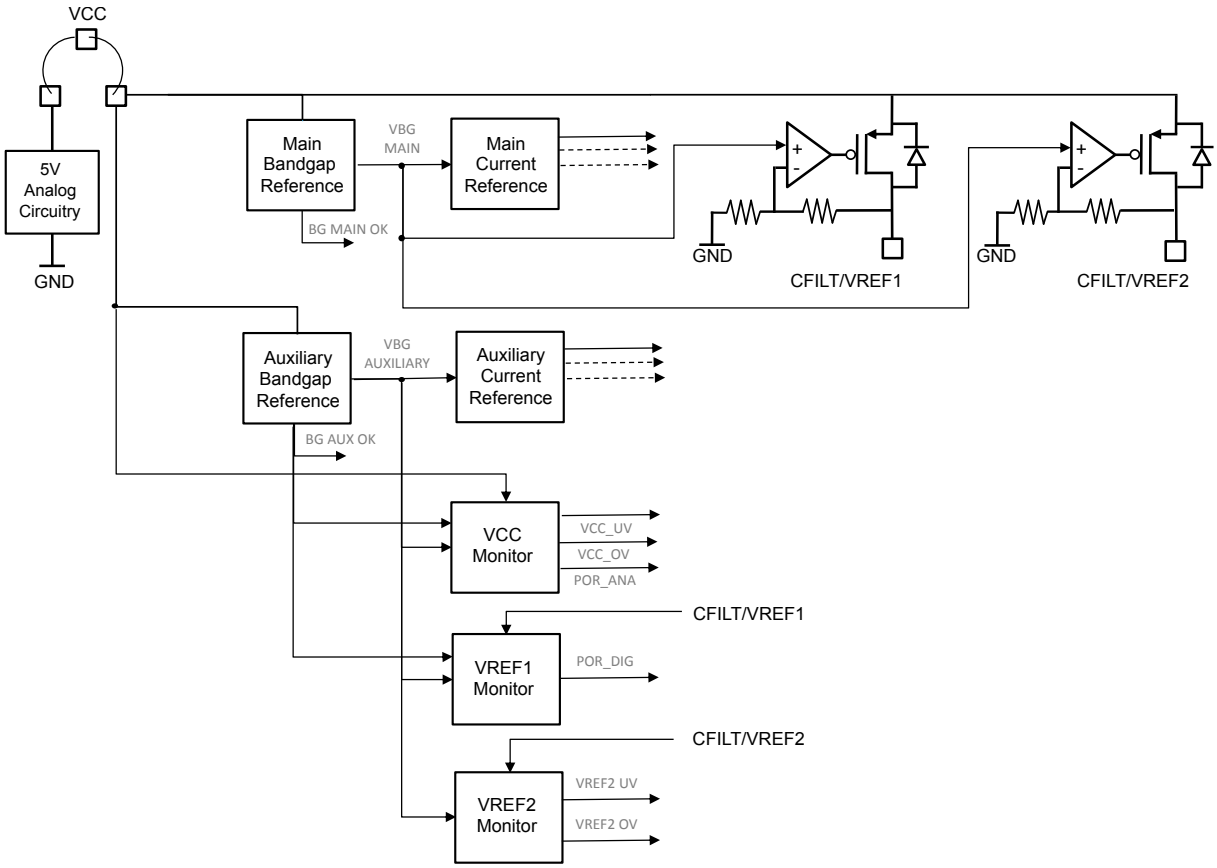
3.1 Internal supply

3.1.1 VCC power supply

The VCC power supply is the main power input of STPM098C. The VCC rail starts the power-up and the power-down sequences by feeding the subsequent internal purpose circuitries (that is, bandgaps, monitoring units and internal regulators control loops).

Starting form VCC pin the reference structures are replicated into two independent instances to avoid common-cause failures (a main one and an auxiliary one).

Figure 5. Internal power supply simplified block diagram



3.1.1.1 *VCC monitor*

VCC voltage level is monitored by means of dedicated UV and an OV diagnosis. Abnormal behavior on the internal supply level causes the generation of a POR_ANA (analog power-on reset) event that consequently sends STPM098C into SAFE_HIZ state. Hysteresis on thresholds and filtering time are implemented.

If VCC ≤ VCC_uv_th occurs for an interval longer than T_vcc_uv_flt, VCC_UV flag is set, POR_ANA is asserted low and SAFE_HIZ is established. The error flag remains set until the failure condition is removed and a rising edge on VR1_EN or VR2_EN is detected. The failure condition can be removed also by PMBUS command CLEAR_FAULTS or by dedicated commands (depending on PMBUS configurations).

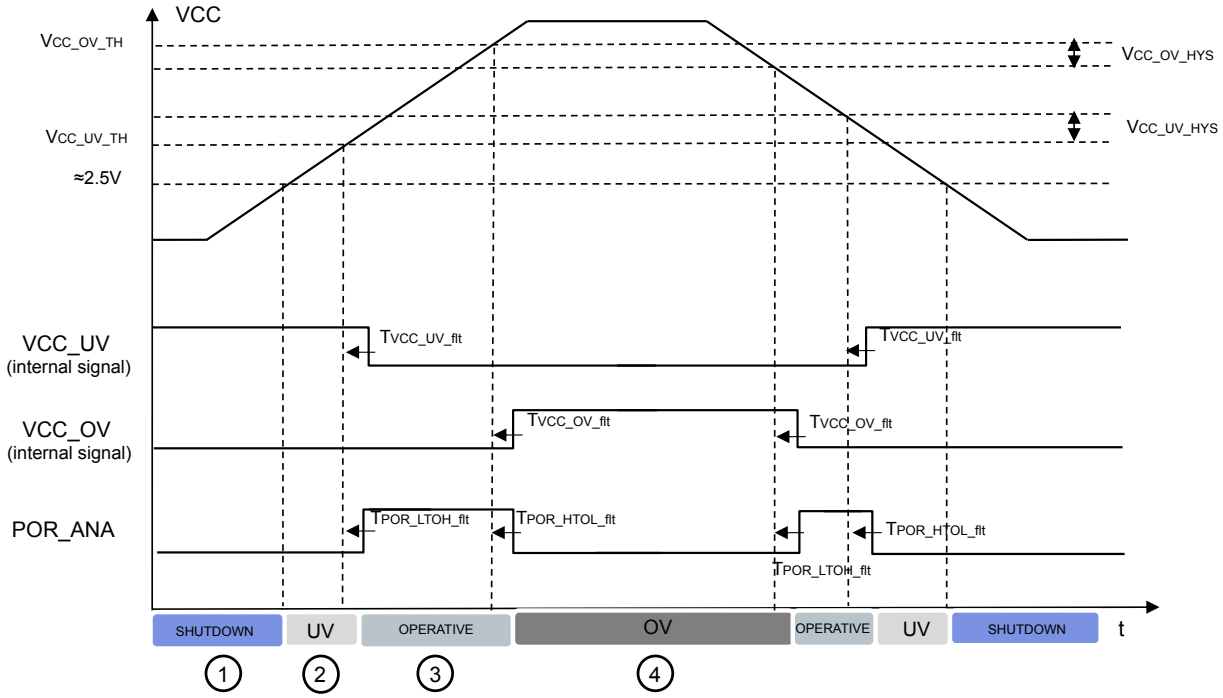
If VCC ≥ VCC_ov_th occurs for an interval longer than T_vcc_ov_flt, VCC_OV flag is set, POR_ANA is asserted low and SAFE_HIZ is established. The error flag remains set until the failure condition is removed and a rising edge on VR1_EN or VR2_EN is detected. The failure condition can be removed also by PMBUS command CLEAR_FAULTS or by dedicated commands (depending on PMBUS configurations).

VCC monitor is safety relevant and then a self-check procedure is implemented.

Table 7. VCC monitor electrical characteristic

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
VCC_uv_th	VCC undervoltage threshold		4	4.19	4.4	V	Comparator output low to high
VCC_uv_hys	VCC undervoltage hysteresis		60	120	180	mV	
VCC_ov_th	VCC overvoltage threshold		5.3	5.5	5.7	V	Comparator output Low to high
VCC_ov_hys	VCC overvoltage hysteresis		25	70	125	mV	
T_vcc_uv_flt	VCC undervoltage		9	10	11	us	Digital filter
T_vcc_ov_flt	VCC overvoltage		9	10	11	us	Digital filter
T_apor_ltoh_flt	POR ANA Low to high state filter time		3.5	5.5	7.5	µs	Analog filter
T_apor_htol_flt	POR ANA high to Low state filter time		7	11	15	µs	Analog filter

Figure 6. VCC power supply operative range



Note:

1. *0 V ≤ VCC ≤ 2.5 V(1)*
   STPM098C is shut down. Internal reference voltage/currents levels are shut down. Internal registers are under reset.
2. *2.5 V ≤ VCC ≤ VCC_uv_th(Max) + VCC_uv_hyst (max)*
   VCC is in undervoltage and SAFE_HIZ is established. Internal reference voltage/currents levels are degraded. Internal registers are out of reset.
3. *VCC_uv_th ≤ VCC ≤ VCC_ov_th*
   Internal supply and reference voltage/currents are available. Internal registers are out of reset (if no LTC faults are detected the device status depends on VR1_EN/VR2_EN status).
4. *VCC_ov_th ≤ VCC*
   VCC is in overvoltage and SAFE_HIZ is established. The internal supply and reference voltage/currents are available and possibly degraded. Internal registers are out of reset.

1. *Indicative value. Not covered by production test or guaranteed by design. In operative conditions VCC is supposed to be within the operating range or at 0 V; values in between are supposed to be applied only during power-up/down transients for an interval based on VCC slew rate requirements.*

3.1.2 VREF1 regulator

The internal supply rail for the digital core on STPM098C is generated by a current limited LDO regulator with a PMOS output stage and an external tank capacitance supplied by VCC pin. Additionally, the VREF1 regulator is intended as the reference voltage for up to eight external DrMOS current measurement analog output.

Figure 7. Regulator simplified block diagram

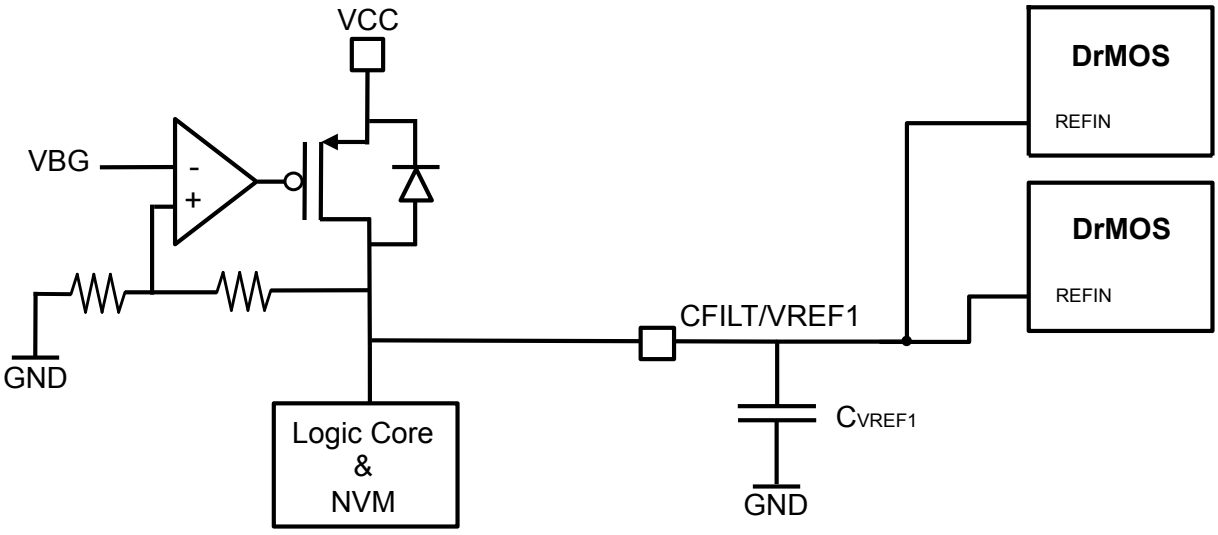


Table 8. VREF1 regulator electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
VREF1_iout	VREF1 output current for no VREF1_UV		0	-	200	mA	Total load = ext.+ int.
VREF1_vout	VREF1 output voltage	Iload = 0-150 mA C_{VREF1} = 4.7 µF	1.71	1.8	1.89	V	Total load = ext.+ int.
VREF1_ilim	VREF1 current limitation	VREF1 = 0 V	200	325	450	mA	Total load = ext.+ int.
VREF1_load_srv	VREF1 static load regulation voltage	VCC = 5 V Iload = 0-150 mA C_{VREF1} = 4.7 µF	-15	-	15	mV	Total load = ext.+ int.
VREF1_load_trv	VREF1 transient load regulation voltage	VCC = 5 V Iload = 0-150 mA dIload/dt = 60 mA/µs C_{VREF1} = 4.7 µF	-50	-	50	mV	Total load = ext.+ int. Guaranteed by design
T_vref1_boot_time	VREF1 boot time	VREF1 10% to 90% Iload = 100 mA C_{VREF1}= 4.7 µF	0.07	0.1	0.2	ms	-
VREF1_ext_cap	External capacitor	ESR = 2 mΩ	3.76	4.7	5.64	uF	Application information

3.1.2.1 *VREF1 voltage monitor*

VREF1 voltage level is monitored by means of dedicated UV and an OV diagnosis. Abnormal behavior on the internal supply level causes the generation of a POR_DIG (digital power-on reset) event that consequently sends STPM098C into RESET state. Hysteresis on thresholds and filtering time are implemented.

If VREF1 ≤ VREF1_uv_th occurs for an interval longer than T_por_htol_flt, POR_DIG is asserted low and internal reset is triggered. After POR_DIG is deasserted, the INT_RST flag is by default set to 1 and then flag can be cleared by VR1_EN or VR2_EN rising edge detection. The failure condition can be removed also by PMBus™ command CLEAR_FAULTS or by dedicated commands.

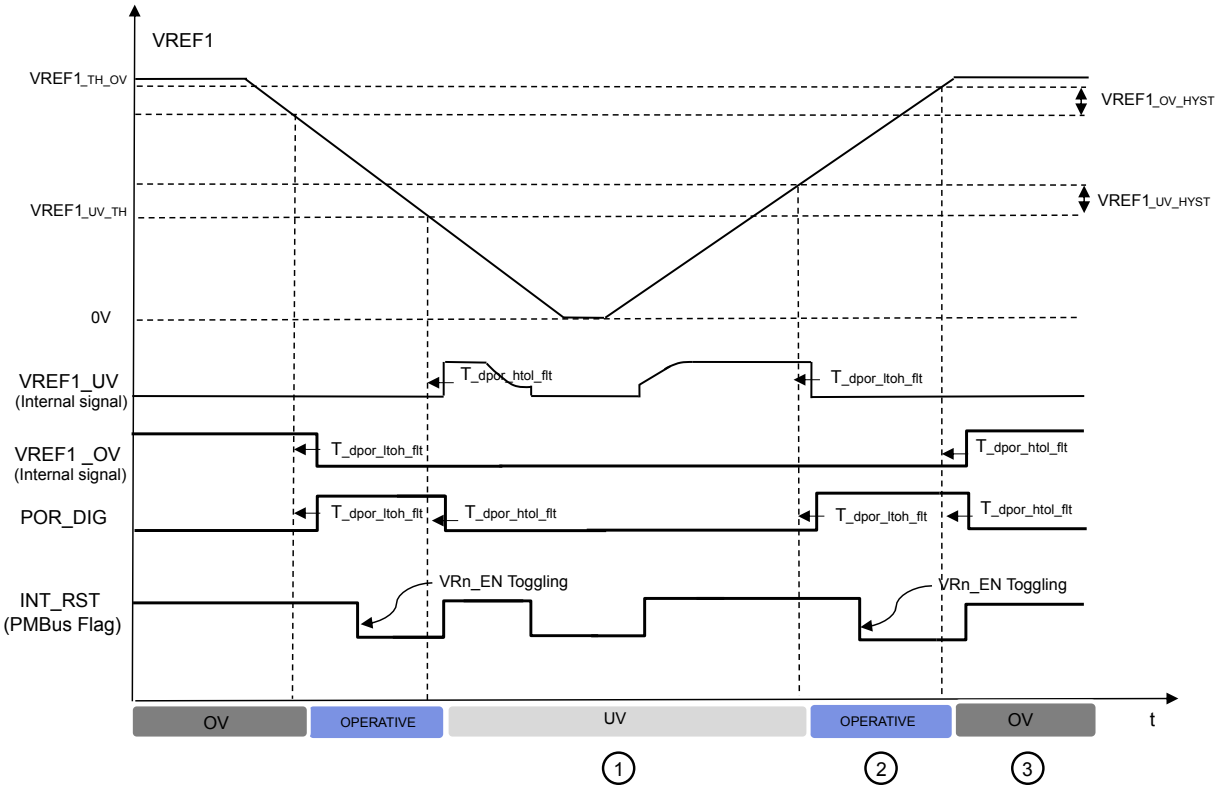
If VREF1 ≥ VREF1_ov_th occurs for an interval longer than T_por_htol_flt, POR_DIG is asserted low and internal reset is triggered. After POR_DIG is deasserted, the INT_RST flag is by default set to 1 and then flag can be cleared by VR1_EN or VR2_EN rising edge detection. The failure condition can be removed by also PMBus™ command CLEAR_FAULTS or by dedicated commands.

VREF1 monitor is safety relevant and then a self-check procedure is implemented.

Table 9. VREF1 monitor electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
VREF1_uv_th	VREF1 undervoltage threshold		1.4	1.5	1.6	V	Comparator output low to high
VREF1_uv_hys	VREF1 undervoltage hysteresis		50	105	150	mV	-
VREF1_ov_th	VREF1 overvoltage threshold		1.9	2	2.1	V	Comparator output low to high
VREF1_ov_hys	VREF1 overvoltage hysteresis		20	55	100	mV	-
T_dpor_ltoh_flt	POR DIG Low to high state filter time		3.5	5.5	7.5	µs	Analog filter
T_dpor_htol_flt	POR DIG high to Low state filter time		7	11	15	µs	Analog filter

Figure 8. VREF1 power supply operative range



Note:

1. *VREF1 ≤ VREF1_uv_th (max) + VREF1_uv_hyst (max)*
   VREF1 is in undervoltage and STPM098C is sent into RESET state. Internal registers are under reset.
2. *VREF1_uv_th ≤ VREF1 ≤ VREF1_ov_th*
   Internal registers are out of reset (if no LTC faults are detected the device status depends on VR1_EN/ VR2_EN status).
3. *VREF1_ov_th ≤ VREF1*
   VREF1 is in overvoltage and STPM098C sent into RESET state. Internal registers are out of reset.

3.1.2.2 *VREF1 thermal-overload monitor*

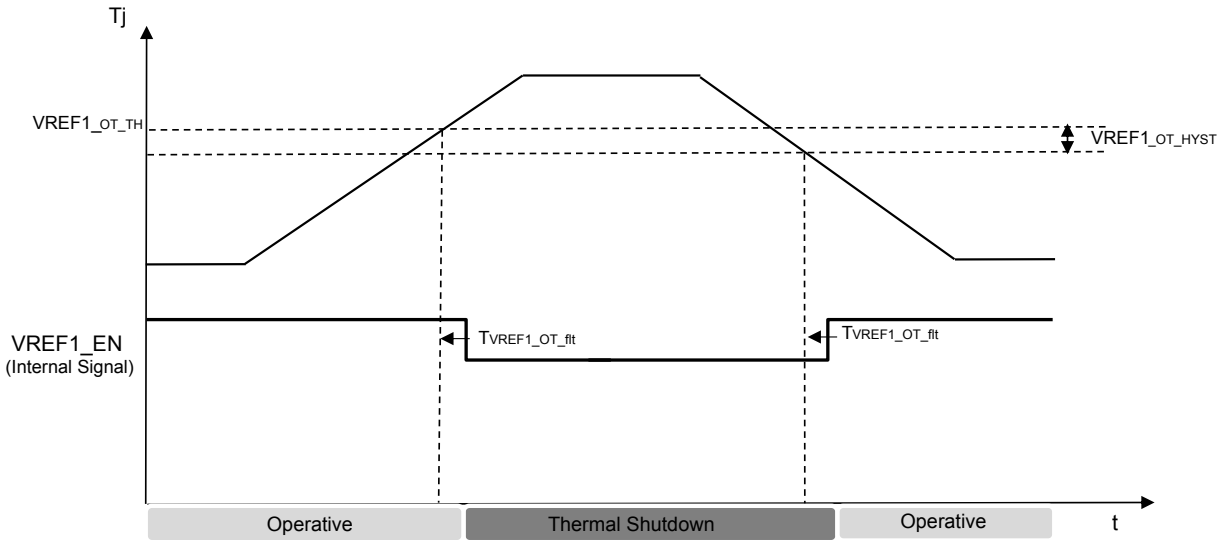
VREF1 load level is monitored by means of dedicated OT (overtemperature) diagnosis. Hysteresis on thresholds and filtering time are implemented.

If T_j (output stage) ≥ VREF1_ot_th occurs for an interval longer than T_ vref1_ot_flt, VREF1_EN is asserted low and the VREF1 regulator is disabled. The VREF1 regulator remains disabled until the failure condition is removed.

Table 10. VREF1 thermal-overload monitor electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
VREF1_ot_th	VREF1 overtemperature threshold		175	190	215	°C	Comparator output low to high
VREF1_ot_hys	VREF1 overtemperature hysteresis		3	5	7	°C	-
T_vref1_ot_flt	VREF1 overtemperature detection filter time		1	3	5	µs	Analog filter

Figure 9. VREF1 thermal-overload behavior



3.1.3 VREF2 regulator

The internal supply rail for the PWM output buffer is generated by a current limited LDO regulator with a PMOS output stage and an external tank capacitance supplied by VCC pin. Additionally, the VREF2 regulator is intended as a supply voltage for external pull-up resistances (4.7 kΩ) of PMBus™ pins SM_DATA, SM_CLK and SM_ALERT.

Figure 10. VREF2 regulator simplified block diagram

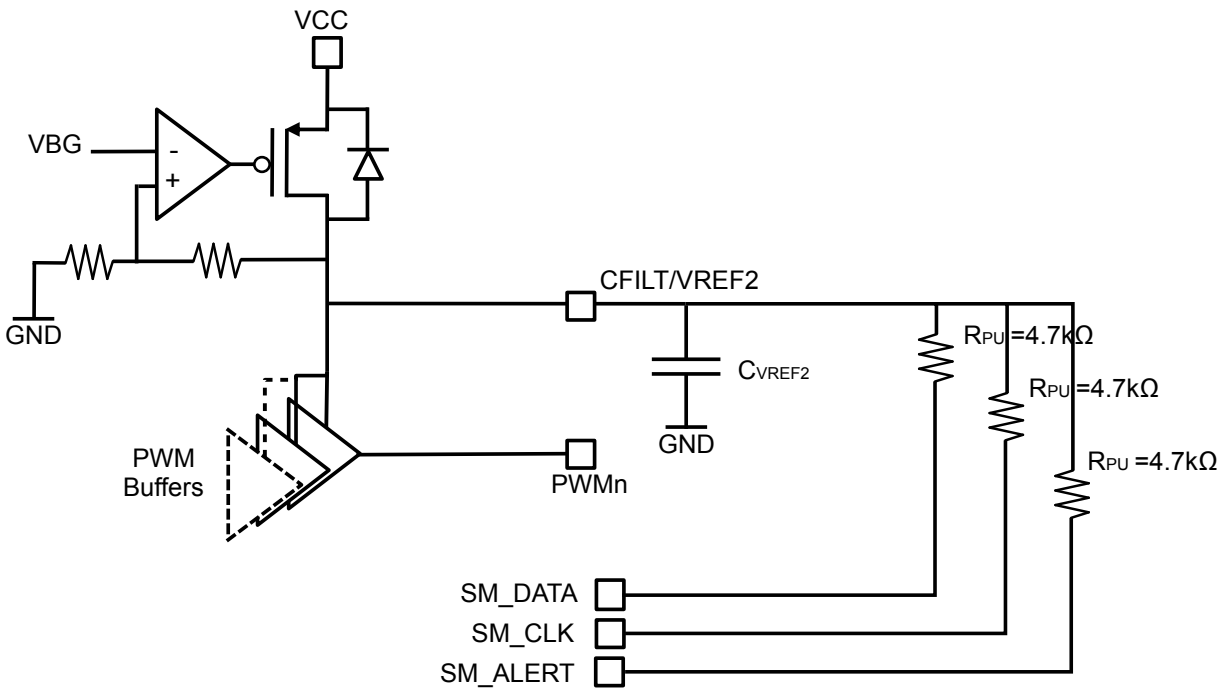


Table 11. VREF2 regulator electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
VREF2_iout	VREF2 rated output current		0	-	100	mA	Total load = ext.+ int.
VREF2_vout	VREF2 output voltage	Iload = 0-100 mA C_{VREF2} = 4.7 µF	3	3.3	3.6	V	Total load = ext.+ int.
VREF2_ilim	VREF2 current limitation	VREF2 = 0 V	110	200	330	mA	Total load = ext.+ int.
VREF2_load_srv	VREF2 static load regulation voltage	VCC = 5 V Iload = 0-100 mA C_{VREF2} = 4.7 µF	-15	-	15	mV	Total load = ext.+ int.
VREF2_load_trv	VREF2 transient load regulation voltage	VCC = 5 V Iload = 0-100 mA dIload/dt = 100 mA/µs C_{VREF2} = 4.7 µF	-50	-	50	mV	Total load = ext.+ int. Guaranteed by design
T_vref2_boot_time	VREF2 boot time	VREF2 10% to 90% Iload = 100 mA C_{VREF2}= 4.7 µF	0.07	0.1	0.2	ms	-
VREF1_ext_cap	External capacitor	ESR = 2 mΩ	3.76	4.7	5.64	µF	Application information

3.1.3.1 *VREF2 voltage monitor*

VREF2 voltage level is monitored by means of dedicated UV and OV diagnosis. Hysteresis on thresholds and filtering time are implemented.

If VREF2 ≤ VREF2_uv_th occurs for an interval longer than T_vref2_uv_flt, VREF2_UV flag is set and SAFE_HIZ is established. The error flag remains set until the failure condition is removed and a rising edge on VR1_EN or VR2_EN is detected. If analog input buffers are available, the failure condition can be removed by PMBus™ command CLEAR_FAULTS or by dedicated commands.

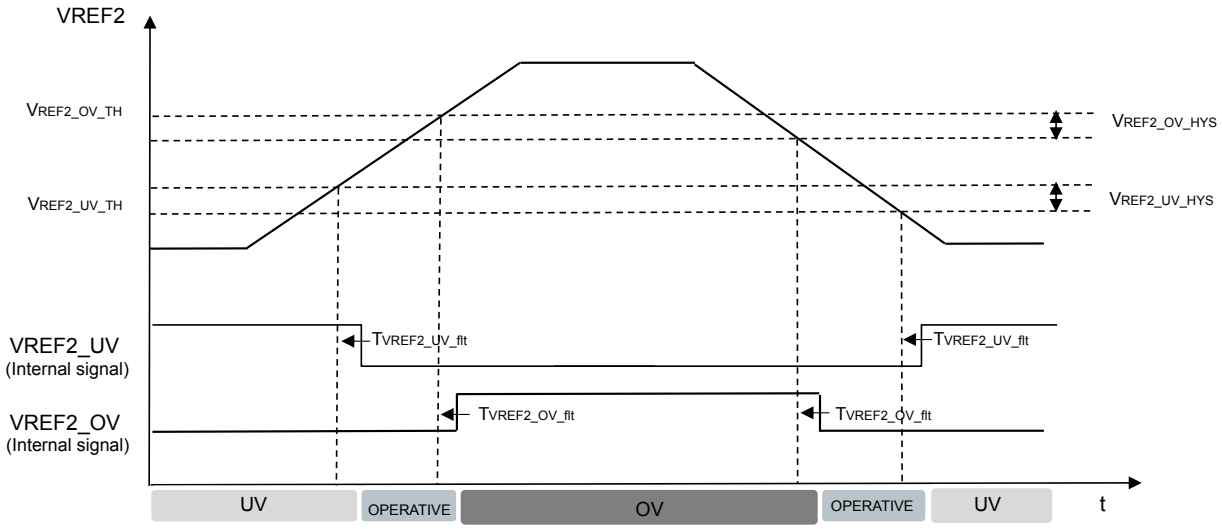
If VREF1 ≥ VREF2_ov_th occurs for an interval longer than T_vref2_ov_flt VREF2_OV flag is set and SAFE_HIZ is established. The error flag remains set until the failure condition is removed and a rising edge on VR1_EN or VR2_EN is detected. If analog input buffers are available, the failure condition can be removed by PMBUS command CLEAR_FAULTS or by dedicated commands.

VREF2 monitor is safety relevant, then a self-check procedure is implemented.

Table 12. VREF2 monitor electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
VREF2_uv_th	VREF2 undervoltage threshold		2.5	2.7	2.8	V	Comparator output low to high
VREF2_uv_hys	VREF2 undervoltage hysteresis		30	75	120	mV	-
VREF2_ov_th	VREF2 overvoltage threshold		3.6	3.8	4	V	Comparator output low to high
VREF2_ov_hys	VREF2 overvoltage hysteresis		90	160	230	mV	-
T_vref2_uv_flt	VREF2 undervoltage detection filter time	CLK_SSM_EN = 0	9	10	11	µs	Digital filter
T_vref2_ov_flt	VREF2 overvoltage detection filter time	CLK_SSM_EN = 0	9	10	11	µs	Digital filter

Figure 11. Power supply operative range



Note:

1. *VREF2 ≤ VREF2_uv_th (max) + VREF2_uv_hyst (max)*
   VREF2 is in undervoltage and SAFE_HIZ is established.
2. *VREF2_uv_th ≤ VREF2 ≤ VREF2_ov_th*
   If no other LTC faults are detected the device mode depends on VR1_EN/VR2_EN status.
3. *VREF2_ov_th ≤ VREF2*
   VREF2 is in overvoltage and SAFE_HIZ is established.

3.1.3.2 *VREF2 thermal-overload monitor*

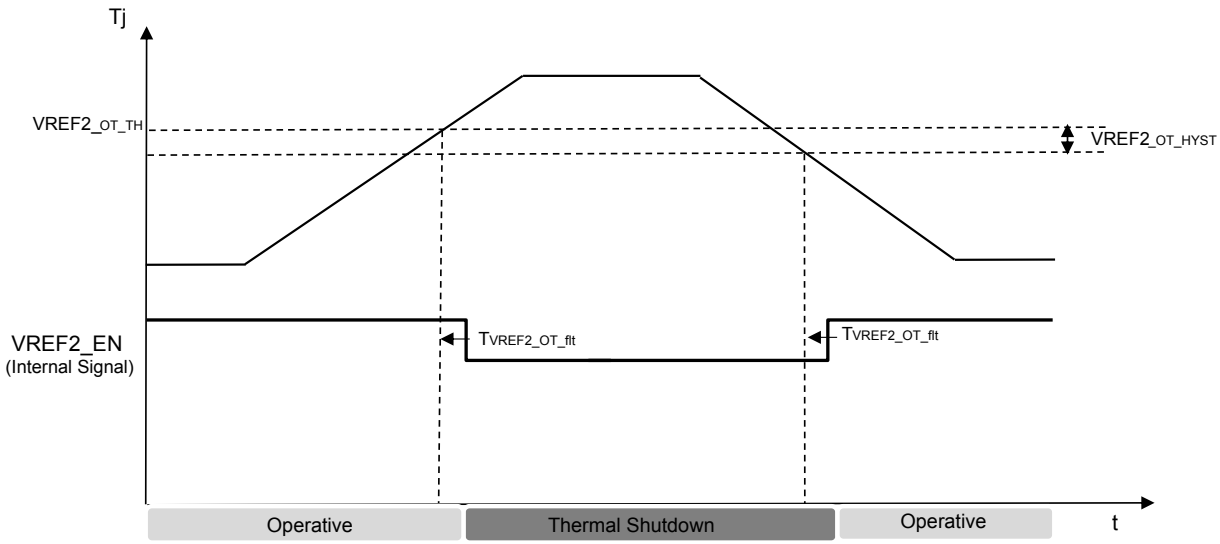
VREF2 load level is monitored by means of dedicated OT (overtemperature) diagnosis. Hysteresis on thresholds and filtering time are implemented.

If T_j (output stage) ≥ VREF2_ot_th occurs for an interval longer than T_ vref2_ot_flt, VREF2_EN is asserted low and the VREF2 regulator is disabled. The VREF2 regulator remains disabled until the failure condition is removed.

Table 13. VREF2 thermal-overload monitor electrical characteristics

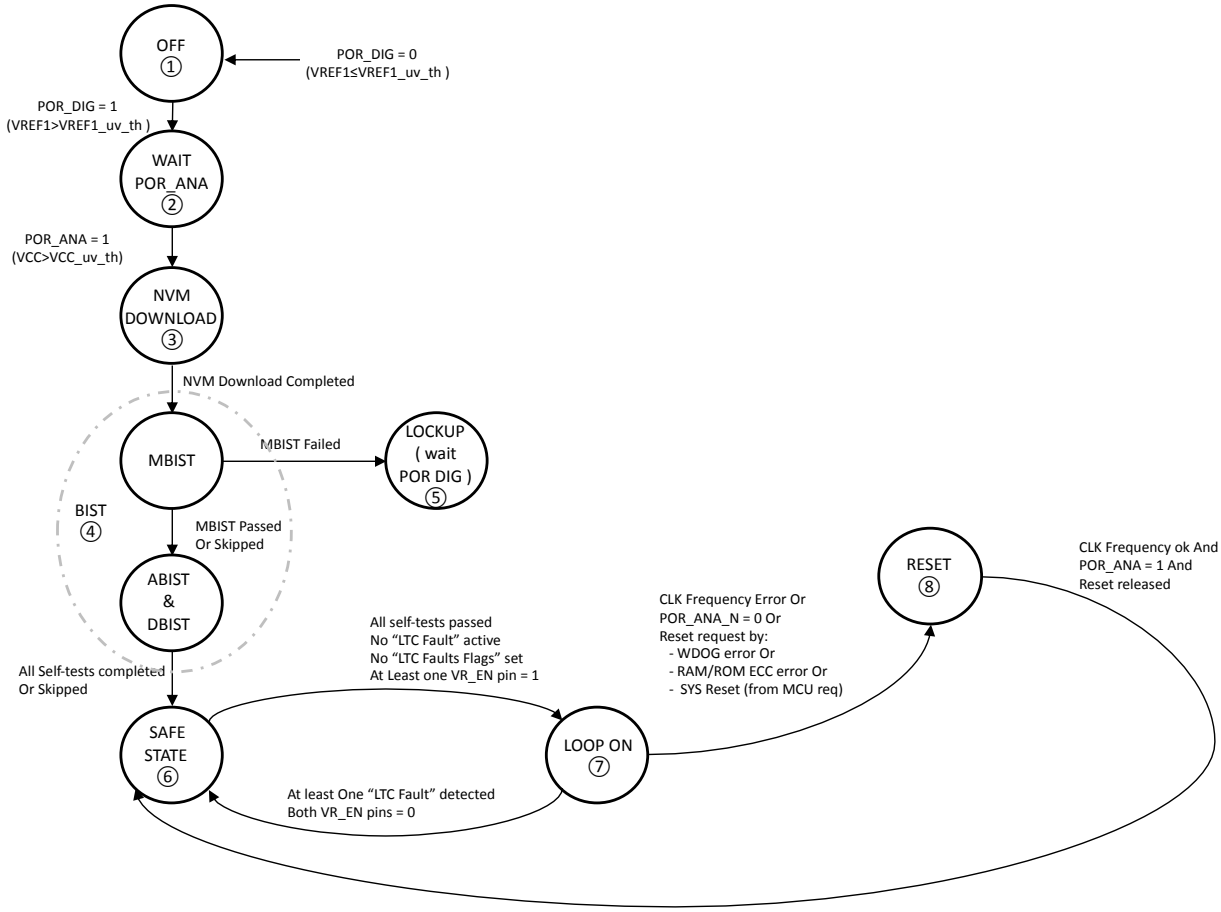
Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
VREF2_ot_th	VREF2 overtemperature threshold		175	190	215	C°	Comparator output low to high
VREF2_ot_hys	VREF2 overtemperature hysteresis		3	5	7	C°	-
T_vref2_ot_flt	VREF2 overtemperature detection filter time		1	3	5	µs	Analog filter

Figure 12. VREF2 thermal-overload behavior



3.2 Device operation state machine

Figure 13. **Device operational state machine**



Note:

1. *OFF STATE*
   Internal supply and reference voltage/currents levels are degraded or shutdown.
   The main logic is under reset.
   All functions are disabled:
   - *Input/output telemetry and monitoring units are disabled;*
   - *Control loop is disabled and PWMn outputs are in HIZ;*
   - *PMBus™ read/write operations are not available.*

   The device persists in this state if POR_DIG='0' (internal signal).
2. *WAIT POR_ANA RELEASE STATE*
   Internal supply and reference voltage/currents levels are degraded or shutdown.
   All functions are disabled:
   - *Input/output telemetry and monitoring units are disabled;*
   - *Control loop is disabled and PWMn outputs are in HIZ;*
   - *PMBus™ read/write operations are not available.*

   The device persists in this state if POR_ANA = '0' (internal signal).
3. *NVM DOWNLOAD STATE*
   Internal supply and reference voltage/currents are available possibly exceeding spec parametrical ranges.
   Main functions are disabled:
   - *Input/output telemetry and monitoring units are disabled;*
   - *Control loop is disabled and PWMn outputs are in HIZ;*
   - *PMBus™ read/write operations are not available.*

   In this mode a CRC check on NVM data is first performed:
   - *If no CRC error is detected the NVM content is deployed into the main logic register and the next state is BIST STATE;*
   - *If a CRC error is detected the related main logic registers are reset to default values (all '0') and the NVM_CRC_FAIL flag is set to '1' and the next state is LOCKUP STATE;*
   - *The device persists in this state until the download procedure and CRC check process ends.*
4. *BIST STATE*
   Internal supply and reference voltage/currents are available and within spec ranges.
   All functions are disabled:
   - *Input/output telemetry and monitoring units are disabled;*
   - *Control loop is disabled and PWMn outputs are in HIZ;*
   - *PMBus™ read/write operations are not available.*

   In this mode the following mechanisms are enabled:
   - *ABIST and LBIST:*
     - *If it fails the next state is SAFE STATE;*
     - *If it does not fail the next state is SAFE STATE;*
   - *MBIST:*
     - *If it fails the next state is LOCKUP STATE;*
     - *If it does not fail the next state is SAFE STATE;*

   The device persists in this state until all checks end.
5. *LOCKUP STATE*
   All functions are disabled:
   - *Input/output telemetry and monitoring units are disabled;*
   - *Control loop is disabled and PWMn outputs are in HIZ;*
   - *PMBus™ read/write operations are not available.*

   System reboot is needed.
6. *SAFE STATE MODE*
   Internal supply and reference voltage/currents are available and within spec ranges.
   Main functions:
   - *Input/output telemetry and monitoring units is partially enabled;*
   - *Control loop is disabled and PWMn outputs are in HIZ;*

– *PMBus™ read/write operations are available.*

If no fault is present and the fault flag is cleared and at least one VRn_EN pin is high the next state is LOOP ON STATE.

7. *LOOP ON STATE*
Internal supply and reference voltage/currents are available and within spec ranges.
Main functions:
   – *Input/output telemetry and monitoring units enabled;*
   – *Control loop is enabled and PWMn status depends on control logic assessment;*
   – *PMBus™ read/write operations are available.*
8. *RESET STATE*
Internal supply and reference voltage/currents levels are degraded or shutdown.
The main logic is under reset.
All functions are disabled:
   – *Input/output telemetry and monitoring units are disabled;*
   – *Control loop is disabled and PWMn outputs are in HIZ;*
   – *PMBus™ read/write operations are not available.*

   The device persists in this state if POR_DIG = '0' (internal signal).

Table 14. Device operation modes summary

Operation mode	Logic core	PWMn outputs	Telemetry and diagnostic	PMBus™ access
OFF	Reset	HIZ	Disabled	Disabled
RESET	Reset	HIZ	Disabled	Disabled
WAIT POR_ANA REL	Functional	HIZ	Disabled	Disabled
NVM DWNL	Functional	HIZ	Disabled	Disabled
BIST	Functional	HIZ	Disabled	Disabled
LOOP ON	Functional	Functional/HIZ	Enabled	Read/Write
SAFE STATE	Functional	HIZ	Partially enabled	Read/Write
LOCKUP STATE	Functional	HIZ	Disabled	Disabled

3.3 BIST mode

A built-in self-test (BIST) procedure is implemented to check safety relevant circuitries both in digital core and in the analog monitor circuits on STPM098C at each device power-up. The BIST procedure is then divided into memory BIST (MBIST) and analog BIST (ABIST).

The purpose of MBIST is to check the integrity of embedded ROM/RAM structures.

The purpose of ABIST procedure is to check the correct functionality of analog structures involved in safety relevant monitors and of the safety isolated off path, by detecting stuck or line interruptions on critical signal paths.

BIST mode access

The BIST mode access state machine flow is based on NVM based register defining the enabling of MBIST and ABIST as follows:

Table 15. MBIST activation register

MBIST_EN	Description
0	MBIST procedure disabled
1	MBIST procedure enabled (default)

Table 16. **ABIST activation register**

ABIST_EN	Description
0	ABIST procedure disabled (default)
1	ABIST procedure enabled

When both are enabled, the MBIST procedure is carried out first.

When MBIST is performed:

- If no MBIST error is detected, the procedure is ended and the state machine evolves to the next stage;
- If an MBIST error is detected, the device reacts by establishing SAFE_HIZ and preventing any further device operation. The device persists in this state until another power-up sequence is forced.

When ABIST is performed:

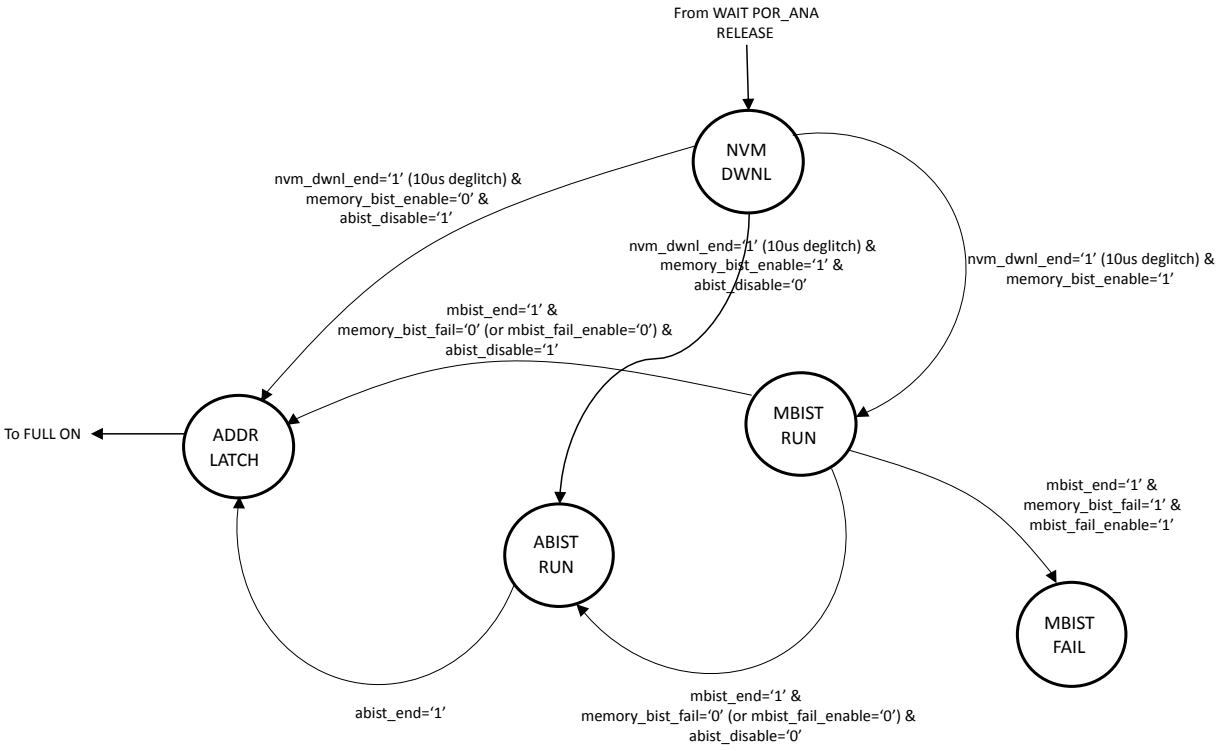
- If no ABIST error is detected, the procedure is ended and the state machine evolves to the next stage;
- If an ABIST error is detected, the ABIST_FAIL bit is set and the state machine evolves to the next stage.

Table 17. **ABIST status register**

ABIST_FAIL	Description
0	NO ABIST failure
1	ABIST procedure failure

MBIST FAIL state corresponds to LOCKUP STATE.

Figure 14. **BIST procedure state machine**



BIST mode retriggering

In case of a fault detection during the analog BIST check at power-up (ABIST_FAIL = 1), a fault confirmation can be performed by triggering an additional procedure run through the two dedicated PMBus™ commands MFR_ABIST_RESTART and MFR_ADC_SELFTEST_RESTART.

Note: During ABIST, the functionality of the involved monitoring unit is suspended for the entire duration of the procedure. It is of the utmost importance that BIST mode retriggering is performed with loop controller disabled (VR_ENn = 0).

3.4 Fault handling management (FHM)

The fault set is divided into two main categories based on the required corrective action:

- LTC (latched fault): this subset includes highly dangerous faults for the IC or the application, requiring quick corrective actions to avoid harming;
- IGN (ignore): this subset includes all those faults against which the application and the device are tolerant and the corrective actions can be waived.

STPM098C allows a certain degree of fault management customization; a subset of available faults can be configured by setting the proper FHC registers.

Table 18. Fault reaction summary

Fault flag	Source diagnosis	Self-check	Failure reaction	Fault description
INT_RST = 1	VREF1 monitor	YES	RESET (LTC)	Undervoltage on VREF1
INT_RST = 1	VREF1 monitor	YES	RESET (LTC)	Overvoltage on VREF1
INT_RST = 1	VREF1 monitor	YES	RESET (LTC)	Overtemperature on VREF1
VREF2_UV = 1	VREF2 monitor	YES	SAFE_HIZ (LTC)	Undervoltage on VREF2
VREF2_OV = 1	VREF2 monitor	YES	SAFE_HIZ (LTC)	Overvoltage on VREF2
VREF2_OT = 1	VREF2 monitor	YES	RESET (LTC)	Overtemperature on VREF2
VCC_UV = 1	VCC monitor	YES	SAFE_HIZ (LTC)	Undervoltage on VCC
VCC_OV = 1	VCC monitor	YES	SAFE_HIZ (LTC)	Overvoltage on VCC
INT_RST = 1	ICM	YES	RESET and SAFE_HIZ (LTC)	Main clock stuck violation
CLK_MISMATCH = 1 CLK1_TIME_OUT = 1 CLK2_TIME_OUT = 1	ICM	YES	RESET and SAFE_HIZ (LTC)	Oscillators mismatch or clock stuck violation
AGND_LOSS = 1 DGND_LOSS = 1	GLM	YES	Flag only (IGN)	Loss of power or signal grounds
OTM_SD = 1	OTM	NO	Configurable	Thermal shutdown
OTM_WR = 1	OTM	NO	Flag only (ignore)	Thermal warning
VIN_UV = 1	VIN monitor	NO	Configurable	Input overvoltage
IIN_OC = 1	IIN monitor	NO	Configurable	Input overcurrent
PIN_OP = 1	PIN monitor	NO	Configurable	Input overpower
VOUTn_UV = 1	VOUT monitor	NO	Configurable	Undervoltage on VSENn [n = 1, 2]
VOUTn_OV = 1	VOUT monitor	NO	Configurable	Overvoltage on VSENn [n = 1, 2]
IOUTn_OC_FAST = 1(1)	IOUT monitor	YES	Configurable	Phase FAST overcurrent [n = 1, 2, 3, 4, 5, 6, 7, 8]
IOUTn_OC_SLOW = 1(1)	IOUT monitor	YES	Configurable	Phase SLOW overcurrent [n = 1, 2, 3, 4, 5, 6, 7, 8]
IOUTn_OC_SUM = 1	IOUT monitor	NO	Configurable	Current sum overcurrent [n = 1, 2]
TSENn_OT_SD = 1	TSEN monitor	NO	Configurable	Overtemperature shutdown on TSENn [n = 1, 2]
TSENn_OT_WR = 1	TSEN monitor	NO	Configurable(2)	Overtemperature warning on TSENn [n = 1, 2]

Fault flag	Source diagnosis	Self-check	Failure reaction	Fault description
TSENn_OV = 1	TSEN monitor	YES	Configurable	Overvoltage on TSENn [n = 1, 2]
TSENn_UV = 1	TSEN monitor	YES	Configurable	Undervoltage on TSENn [n = 1, 2]
VSENn_DISC = 1	FB disconnection monitor	YES	Configurable	Feedback disconnection on VSENn [n = 1, 2]
VRTNn_DISC = 1	FB disconnection monitor	YES	Configurable	Feedback disconnection on VSENn [n = 1, 2]
IOUTn_SHARING_WR = 1	IOUT monitor	NO	Flag only (IGN)	Phase current overbalancing
IOUTn_UC_ = 1	IOUT monitor	NO	Configurable	Phase undercurrent (phase fault)
PMBUS_ERR = 1	PMBus™ monitor	NA	Ignore command	PMBus™ comm fault
NVM_CRC_FAIL = 1	NVM data CRC check	NA	SAFE_HIZ (LTC)	NVM data CRC check
SRR_CRC_FAIL = 1	SRR data CRC check	NA	SAFE_HIZ (LTC)	SRR data CRC check
NA	MBIST	NA	LOCKUP	MBIST failure
ABIST_FAIL = 1	ABIST	NA	Flag only (IGN)	ABIST failure

1. *Phase positive and negative overcurrents share the same flag.*
2. *TSENn_OT_WR fault reaction is always ignored and cannot be configured differently. The related FHC register allows to enable/disable the related pin signaling.*

3.4.1 Fault handling configuration (FHC) registers

The STPM098C default FHM configuration can be modified by properly writing the FHC registers through CONFIG mode. FHC are considered as SRR (safety relevant registers).

3.4.1.1 Fault reaction configuration (FRC)

For each of the configurable faults listed in the Table 18 (except overvoltage on VSENn) a configuration bit allows to define whether the corrective action shall be automatically implemented by the device itself or if it can be waived.

Table 19. Fault reaction configuration bits

<FLT_REF>_FAULT_RESPONSE	Description
0	Ignore - ignore fault detection, device remains in NORMAL mode(1)
1	Latched - disable all PWM outputs, device moves to SAFE_HIZ mode (default)(2)

1. *Fault danger for the application is considered low. The fault can be ignored with no corrective action applied neither internal or external.*
2. *Fault danger for the application is considered high. The corrective action shall be taken as soon as it is detected by the device by establishing SAFE_HIZ.*

Overvoltage on VSENn fault handling configuration allows three different mechanisms programmable through two configuration bits.

Table 20. VSENn_OV reaction configuration bits

<FLT_REF>_FAULT_RESPONSE1	<FLT_REF>_FAULT_RESPONSE	Description
0	0	Ignore - ignores fault detection, device remains in NORMAL mode(1)
0	1	Latched - disables all PWM outputs, device moves to SAFE_HIZ mode(2)
1	0	Unused

<FLT_REF>_FAULT_RESPONSE1	<FLT_REF>_FAULT_RESPONSE	Description
1	1	Latched with active pull-down - enables active pull-down first and disable all PWM outputs subsequently; the device moves to SAFE_HIZ mode (default)(3)

1. *Fault danger for the application is considered low. The fault can be ignored with no corrective action applied neither internal or external.*
2. *Fault danger for the application is considered high. The corrective action shall be taken as soon as it is detected by the device by establishing SAFE_HIZ.*
3. *Fault danger for the application is considered high. The corrective action shall be taken as soon as it is detected by the device by activating an active pull-down and successively establishing SAFE_HIZ.*

3.4.1.2 *Fault output redirection (FOR)*

STPM098C implements a multiple source of fault signaling by means of pins FAULT, SM_ALERT, VRRDY1/2, VR_HOT, POWERIN_ALERT and through a dedicated PMBus™ flag.

Fault output redirection pins are asserted LOW while the PMBus™ flag is set to '1' each time an LTC fault is detected according to the following table.

Note: While the PMBus™ flag is always asserted in case of fault event, the pin signaling is strictly related to fault reaction. Pin signaling of a fault is only active if the fault has a configurable or nonconfigurable LTC reaction.

Table 21. FOR summary

PMBus™ flag signaling	Source diagnosis	Fault output pin signaling	Fault description
INT_RST = 1	VREF1 monitor	FAULT = SM_ALERT = VRRDY1 = VRRDY2 = 0	Undervoltage on VREF1
INT_RST = 1	VREF1 monitor	FAULT = SM_ALERT = VRRDY1 = VRRDY2 = 0	Overvoltage on VREF1
INT_RST = 1	VREF1 monitor	FAULT = SM_ALERT = VRRDY1 = VRRDY2 = 0	Overtemperature on VREF1
VREF2_UV = 1	VREF2 monitor	FAULT = SM_ALERT = VRRDY1 = VRRDY2 = 0	Undervoltage on VREF2
VREF2_OV = 1	VREF2 monitor	FAULT = SM_ALERT = VRRDY1 = VRRDY2 = 0	Overvoltage on VREF2
VREF2_UV = 1	VREF2 monitor	FAULT = SM_ALERT = VRRDY1 = VRRDY2 = 0	Overtemperature on VREF2
VCC_UV = 1	VCC monitor	FAULT = SM_ALERT = VRRDY1 = VRRDY2 = 0	Undervoltage on VCC
VCC_OV = 1	VCC monitor	FAULT = SM_ALERT = VRRDY1 = VRRDY2 = 0	Overvoltage on VCC
INT_RST = 1	ICM	FAULT = SM_ALERT = VRRDY1 = VRRDY2 = 0	Main clock stuck violation
CLK_MISMATCH = 1 CLK1_TIME_OUT = 1 CLK2_TIME_OUT = 1	ICM	FAULT = SM_ALERT = VRRDY1 = VRRDY2 = 0	Oscillators mismatch or auxiliary clock stuck violation
AGND_LOSS = 1 DGND_LOSS = 1	GLM	No pin signaling	Loss of power or signal grounds
OT_SD = 1	OTM	FAULT = SM_ALERT = VRRDY1 = VRRDY2 = 0	Thermal shutdown
OTM_WR = 1	OTM	No pin signaling	Thermal warning
VIN_UV = 1	VIN monitor	FAULT = SM_ALERT = VRRDY1 = VRRDY2 = 0	Input Overvoltage
IIN_OC = 1	IIN monitor	FAULT = SM_ALERT = VRRDY1 = VRRDY2 = 0	Input over-current

PMBus™ flag signaling	Source diagnosis	Fault output pin signaling	Fault description
PIN_OP = 1	PIN monitor	FAULT = SM_ALERT = VRRDY1 = VRRDY2 = POWERIN_ALERT = 0	Input Overpower
VOUTn_UV = 1	VOUT monitor	FAULT = SM_ALERT = VRRDY1n = 0	Undervoltage on VSENn [n = 1, 2]
VOUTn_OV = 1	VOUT monitor	FAULT = SM_ALERT = VRRDY1n = 0	Overvoltage on VSENn [n = 1, 2]
IOUTn_OC_FAST = 1	IOUT monitor	FAULT = SM_ALERT = VRRDYm = 0	FAST over-current on ISENn [n = 1, 2, 3, 4, 5, 6, 7, 8] [m = 1, 2]
IOUTn_OC_SLOW = 1	IOUT monitor	FAULT = SM_ALERT = VRRDYm = 0	SLOW Overcurrent on ISENn [n = 1, 2, 3, 4, 5, 6, 7, 8] [m = 1, 2]
IOUTn_OC_SUM = 1	IOUT monitor	FAULT = SM_ALERT = VRRDY1n = 0	SLOW Overcurrent on VSENn [n = 1, 2]
TSENn_OT_SD = 1	TSEN monitor	FAULT = SM_ALERT = VRRDYn = VR_HOT = 0	Overtemperature shutdown on TSENn [n = 1, 2]
TSENn_OT_WR = 1	TSEN monitor	VR_HOT = 0	Overtemperature warning on TSENn [n = 1, 2]
TSENn_OV = 1	TSEN monitor	FAULT = SM_ALERT = VRRDYn = 0	Overvoltage on TSENn [n = 1, 2]
TSENn_UV = 1	TSEN monitor	FAULT = SM_ALERT = VRRDYn = 0	Undervoltage on TSENn [n = 1, 2]
FBn_NO_CONN = 1	FB disconnection monitor	FAULT = SM_ALERT = VRRDYn = 0	Feedback disconnection on VSENn [n = 1, 2]
IOUTn_SHARING_WRM = 1	IOUT monitor	No pin signaling	Phase current overbalancing [n = 1, 2, 3, 4, 5, 6, 7, 8]
IOUTn_UC_ = 1	IOUT monitor	FAULT = SM_ALERT = VRRDYn = 0	Phase undercurrent (phase fault) [n = 1, 2, 3, 4, 5, 6, 7, 8]
PMBUS_ERR = 1	PMBus™ monitor	SM_ALERT = 0(1)	PMBus™ comm fault
NVM_CRC_FAIL = 1	NVM data CRC check	FAULT = SM_ALERT = VRRDY1 = VRRDY2 = 0	NVM data CRC check
SRR_CRC_FAIL = 1	SRR data CRC check	FAULT = SM_ALERT = VRRDY1 = VRRDY2 = 0	SRR data CRC check
NA	MBIST	FAULT = SM_ALERT = VRRDY1 = VRRDY2 = 0	MBIST failure
ABIST_FAIL = 1	ABIST	FAULT = SM_ALERT = 0(2)	BIST failure

1. *Configurable through PMBus™ command STATUS_CML.*
2. *Configurable through PMBus™ command MFR_FAULT_CONFIG_1 bit 8.*

3.4.2 Fault reaction scenarios

Here below, the scenarios of each different fault case are described separately. In case multiple faults take place at the same time the following priority in reaction is used:

- Latched fault
- Ignored fault

3.4.2.1 *Latched faults*

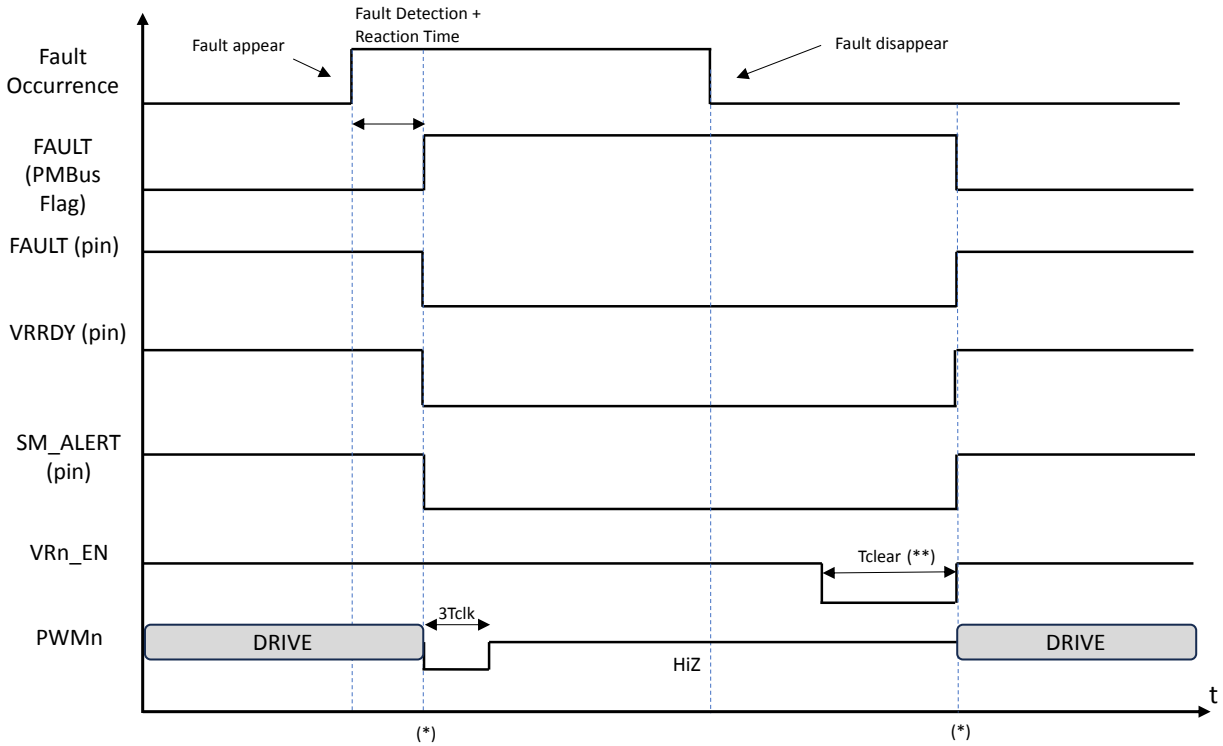
When a latched fault is detected, the related PMBus™ flag is set to '1' and related fault redirection pins are asserted low. Internal logic reacts by establishing a SAFE_HIZ state: PWM outputs go in HIZ mode so that PWMn = HIZ [n = 1, 2, 3, 4, 5, 6, 7, 8].

The SAFE_HIZ mode can be left when all the following conditions are met in this sequence:

1. Latched fault is removed.
2. Clear mechanism - One of the following actions, required by application software:
   - VR_EN1/VR_EN2 is asserted low for at least T_clear and then asserted back high.
   - CLEAR_FAULTS command by PMBus™ (clears all faults).
   - Dedicated clear commands by PMBus™ (clears single fault).

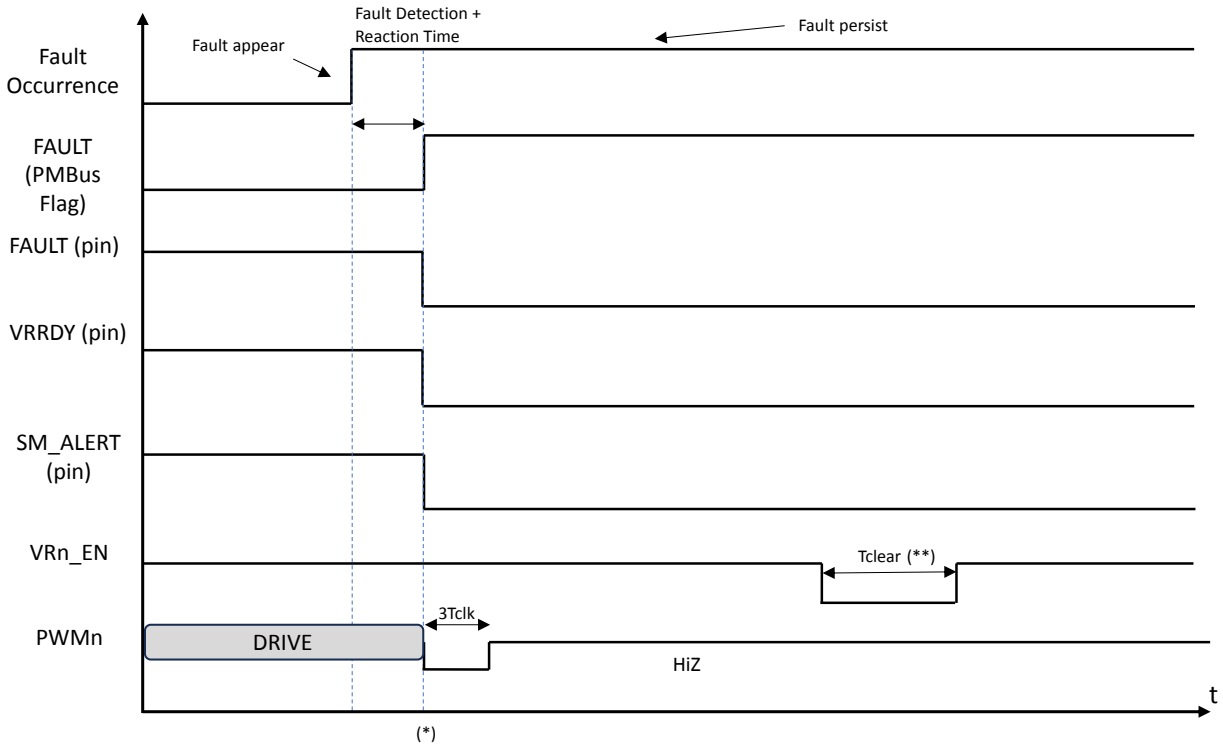
Note:
- *VR1_EN toggling is used to clear specific fault affecting loop 1. VR2_EN toggling is used to clear specific fault affecting loop 2. Generic faults affecting both loops can be cleared by toggling either VR1_EN or VR2_EN.*
- *Faults clearing through the PMBus™ command make use of paging for faults affecting the specific loop. Generic faults affecting both loops can be cleared independently of the command page.*

Figure 15. Latched fault - Transient fault timing diagram



(*) Signaling Filter Time = Fault Detection + Reaction Time
(**) Tclear is the minimum time VRn_EN shall be asserted LOW for fault clear to be effective

Figure 16. **Latched fault - Permanent fault timing diagram**



(*) Signaling Filter Time = Fault Detection + Reaction Time
(**) Tclear is the minimum time VRn_EN shall be asserted LOW for fault clear to be effective

Table 22. **VRn_EN clear time electrical characteristics**

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
VRn_EN_tclear	Minimum time interval to assert a low value on VRn_EN		10	-	-	µs	[n = 1, 2]

3.4.2.2 *Latched fault with active pull-down*

This fault reaction scenario is intended to reduce the undershoot on the output voltage when recovery from an overvoltage condition. When an overvoltage fault is detected and the related FHC register is programmed at “11”, the related PMBus™ flag is set to ‘1’ and related fault redirection pins are asserted low.

Internal logic reacts in first place by setting all PWM output assigned to the loop to ‘0’, then the internal logic reacts by establishing SAFE_HIZ state if either of the following conditions is verified:

- VSENn ≤ 0.25 V_th for an interval longer than T_tout_mon_detect_dly
- ISENn - CFILT/VREF1 ≤ -IOUTm_noc_slow_th

The SAFE_HIZ mode can be left when all the following conditions are met in this sequence:

1. Latched fault is removed.
2. Clear mechanism - One of the following actions, required by application software:
   – VR_EN1/VR_EN2 is asserted low for at least T_clear and then asserted back high.
   – CLEAR_FAULTS command by PMBus™ (clears all faults).
   – Dedicated clear commands by PMBus™ (clears single fault).

Figure 17. **Latched fault with active PD, VSEN < 0.25 V detection - Transient fault timing diagram**

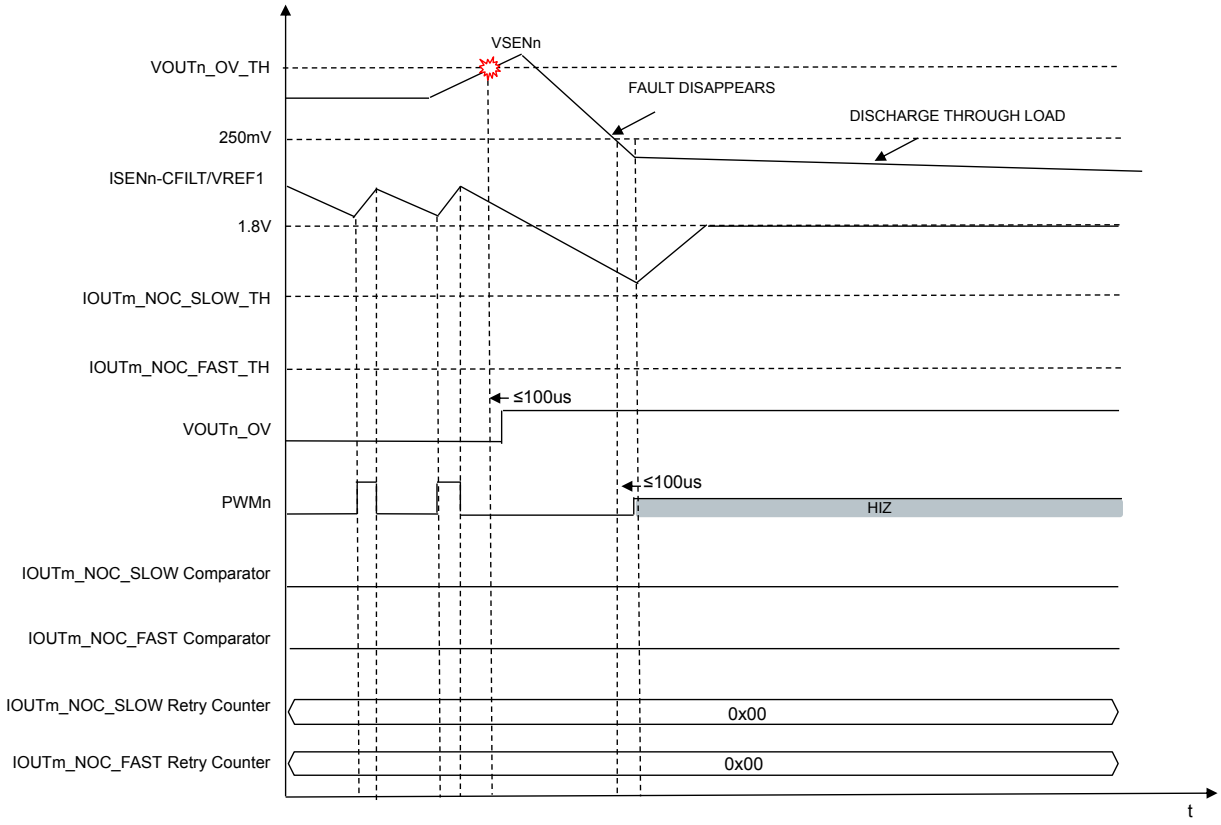


Figure 18. **Latched fault with active PD, VSEN < 0.25 V detection - Permanent fault timing diagram**

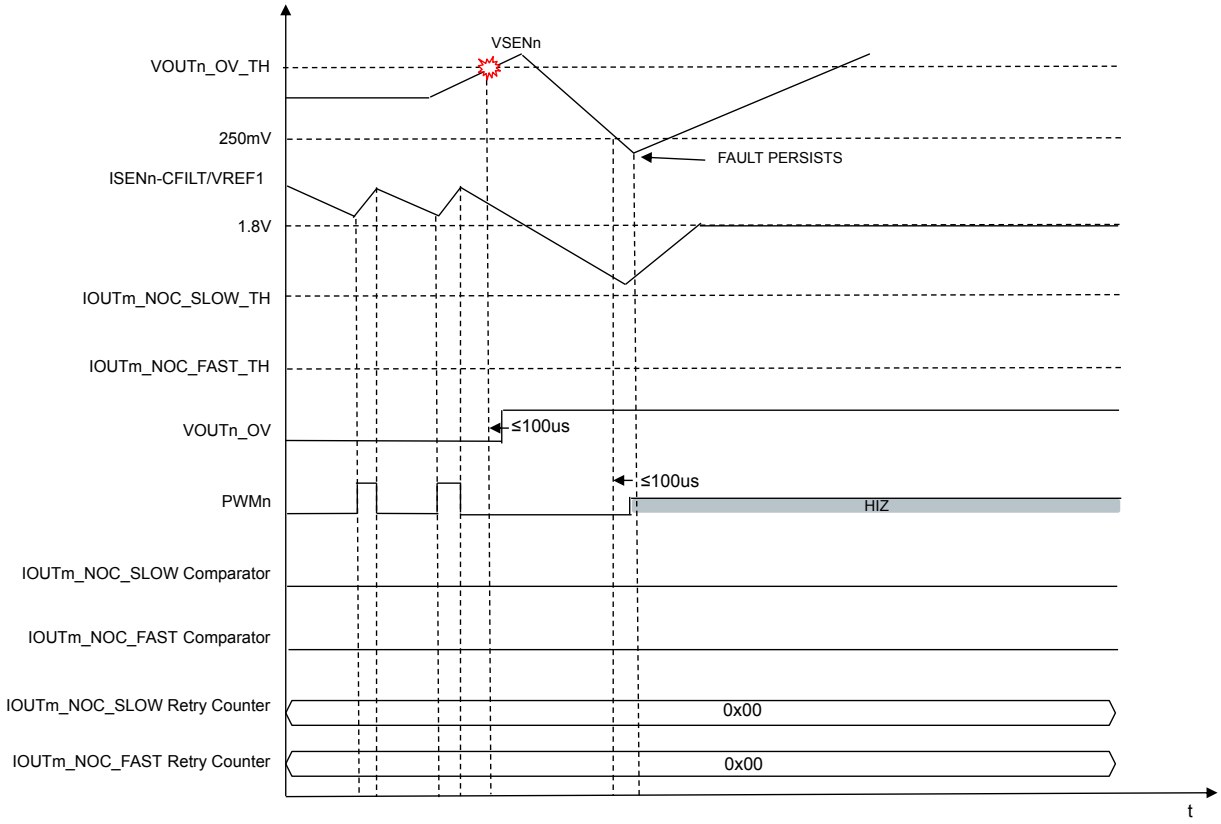


Figure 19. **Latched fault with active PD, NOC detection - Transient fault timing diagram**

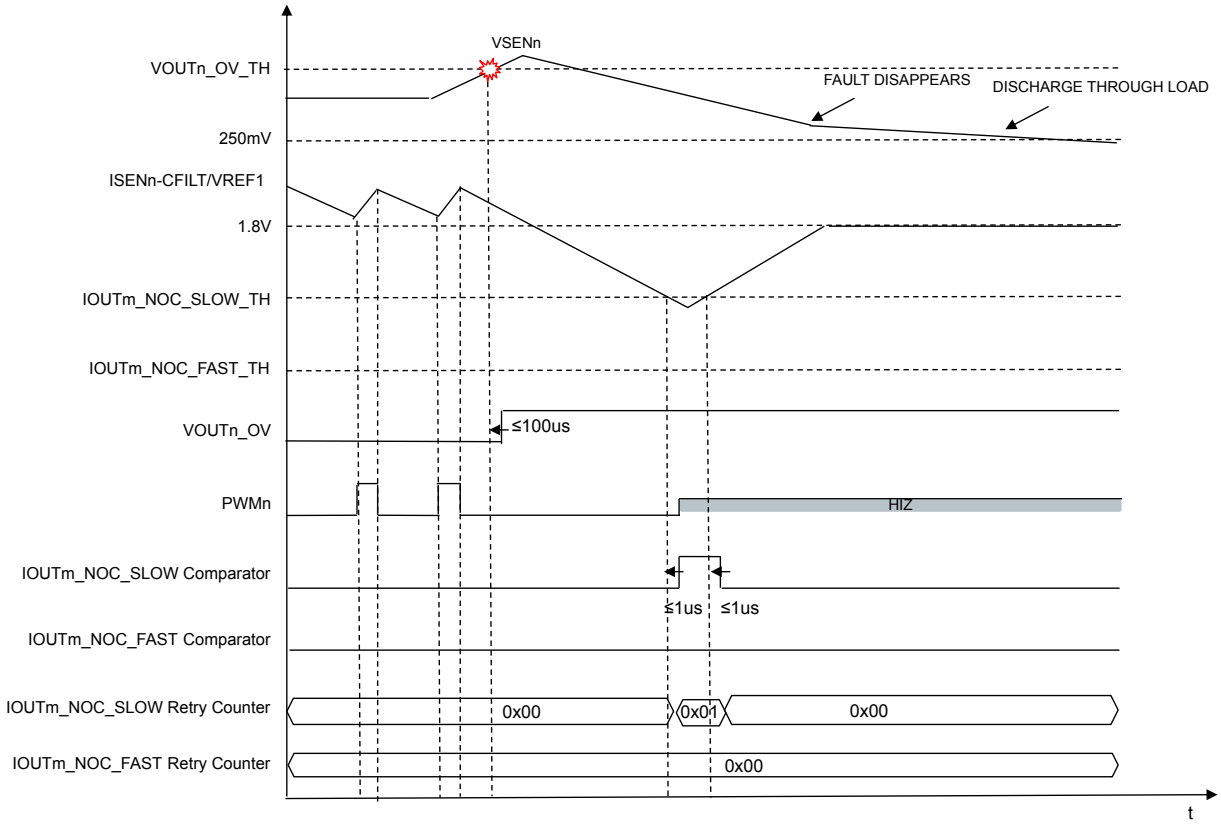
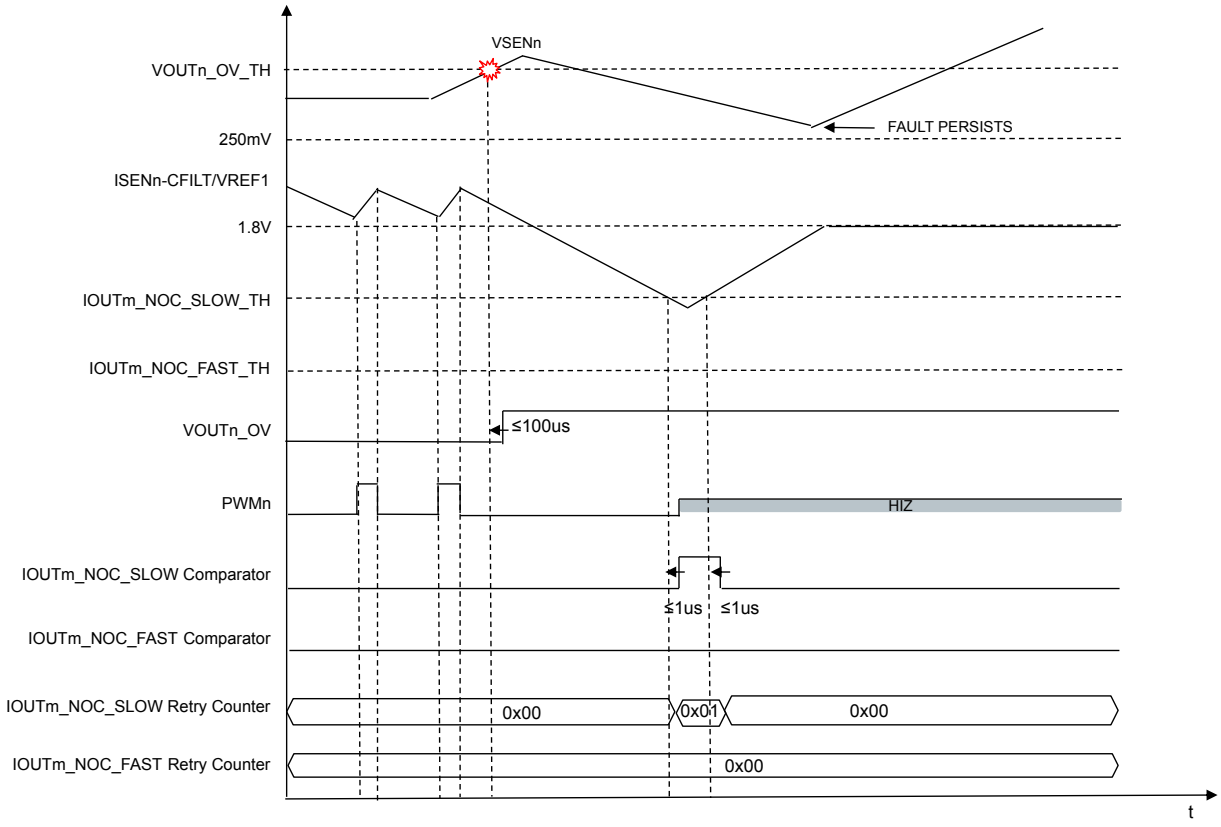


Figure 20. **Latched fault with active PD, NOC detection - Permanent fault timing diagram**

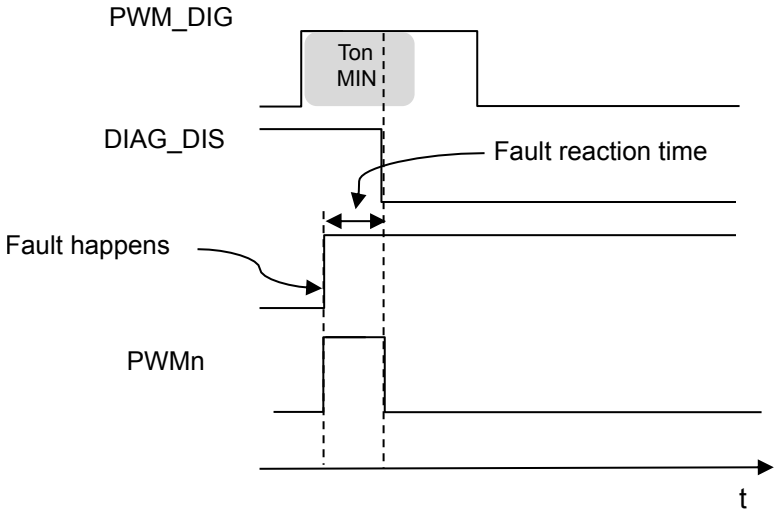


During normal operation the PWM pins driving is managed by the digital section of the loop controller which is in charge of the TON and TOFF generation along with their minimum value limitations (MFR_T_MIN). In case of fault event, the PWM pin driving is overridden by the diagnostic control which applies to the configured reaction (as instance: 3Tclk turn-off then HIZ, cycle-by-cycle turn-off, etc.).

Since fault events are not synchronous with normal PWM generation and since reaction countermeasure shall be applied within a specific fault tolerant time, it turns out that PWM driving by loop and by diagnostic controllers cannot be synchronous as well and diagnostic shall have the highest priority.

In case of fault events requiring PWM turn-off or switch to HiZ, the MINIMUM ON/OFF time configured in MFR_T_MIN cannot be guaranteed.

Figure 21. Minimum TON clipping during LTC fault reaction



3.4.2.3 *Ignore faults*

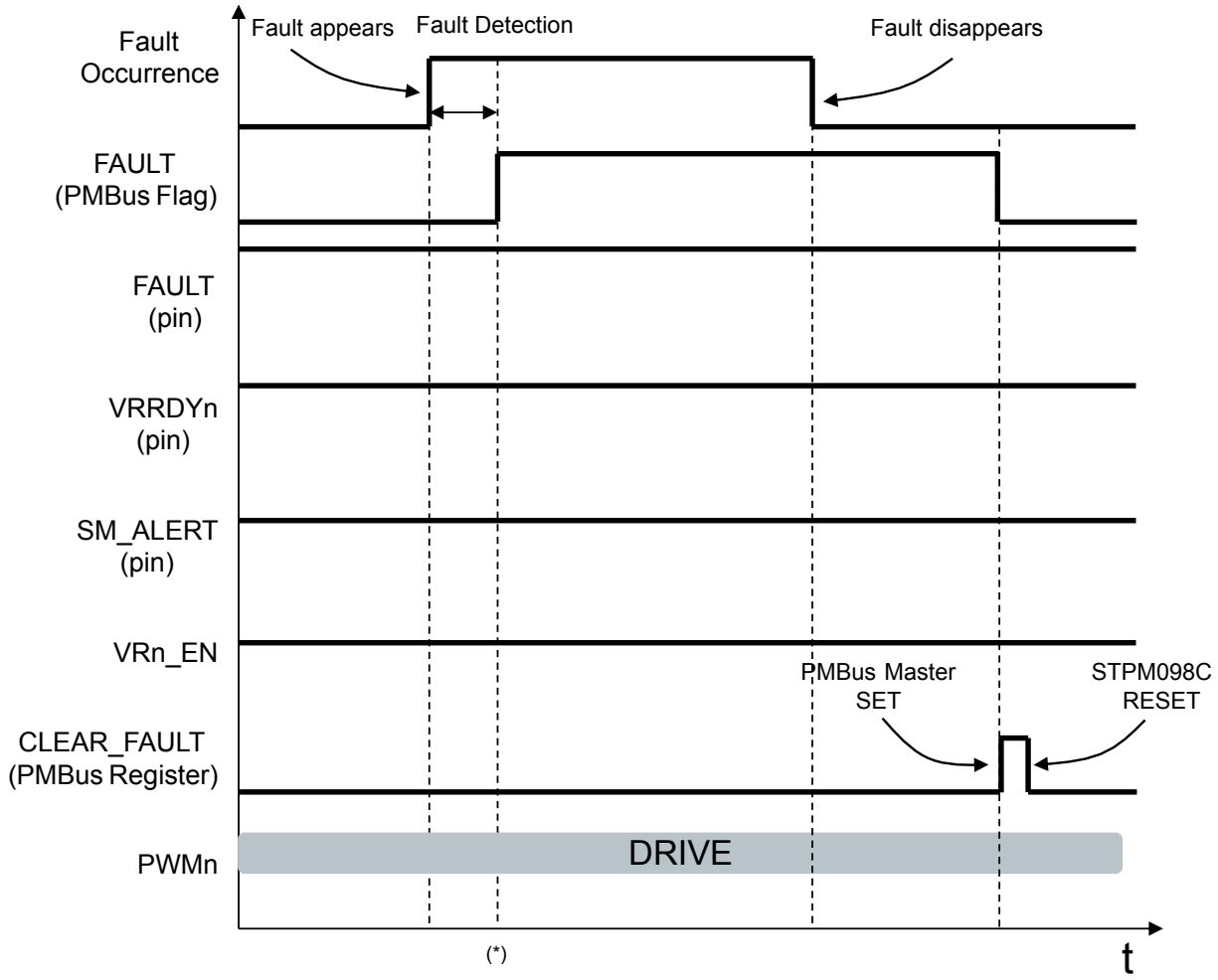
When a fault whose reaction is set as “ignore” is detected, the related PMBus™ flag is set to ‘1’. Logic performs no corrective action. The PMBus™ flag can be cleared when all the following conditions are met in this sequence:

1. Fault is removed.
2. Clear mechanism - One of the following actions, required by application software:
   - VR_EN1/VR_EN2 is asserted low for at least T_clear and then asserted back high.
   - CLEAR_FAULTS command by PMBus™ (clears all faults).
   - Dedicated clear commands by PMBus™ (clears single fault).

Note:

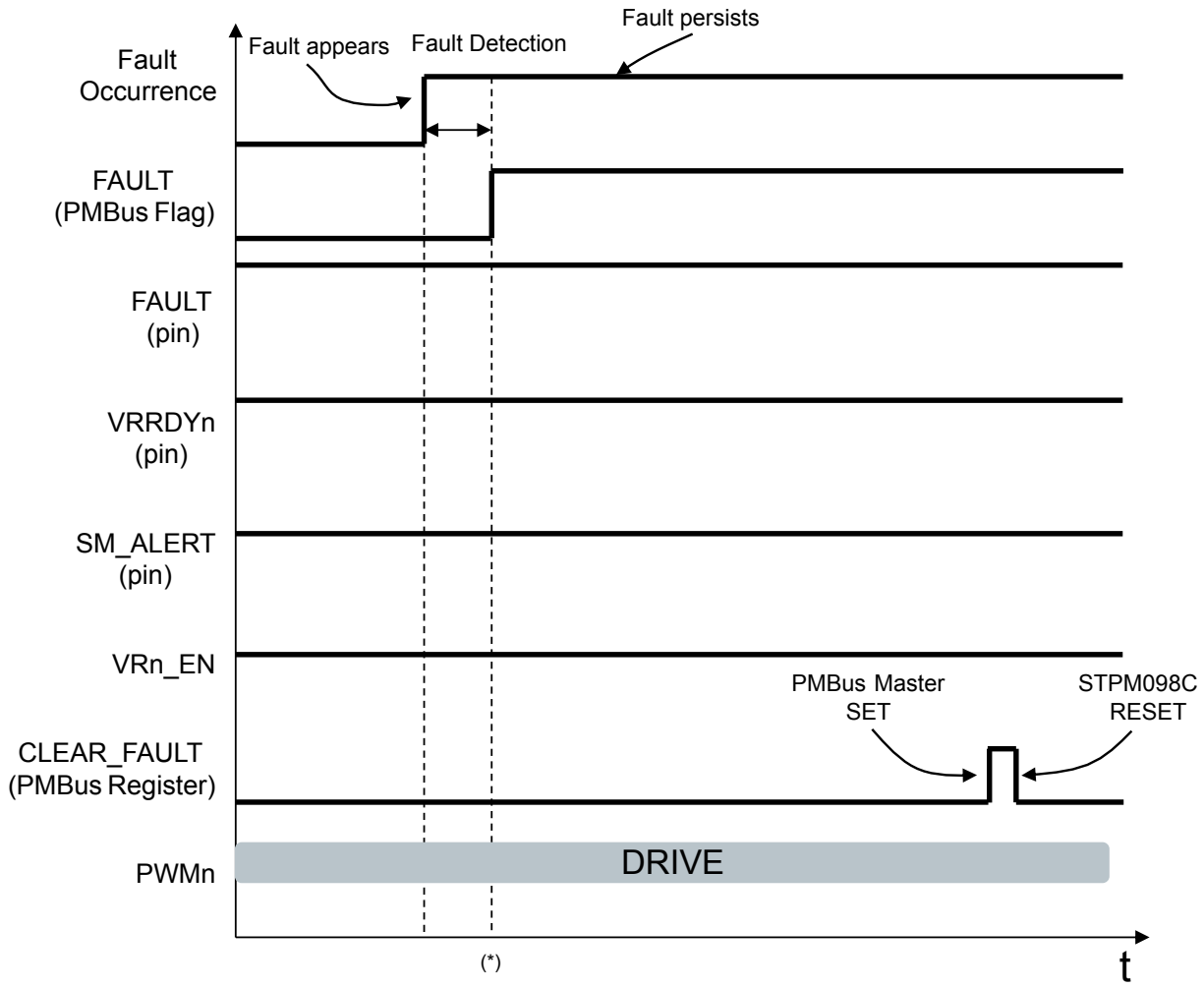
- *VR1_EN toggling is used to clear specific fault affecting loop 1. VR2_EN toggling is used to clear specific fault affecting loop 2. Generic faults affecting both loops can be cleared by toggling either VR1_EN or VR2_EN.*
- *Faults clearing through the PMBus™ command make use of paging for faults affecting the specific loop. Generic faults affecting both loops can be cleared independently of the command page.*

Figure 22. **Ignore faults - Transient fault timing diagram**



(*) Signaling Filter Time = Fault Detection + Reaction Time

Figure 23. **Ignore - Permanent fault timing diagram**



(*) Signaling Filter Time = Fault Detection + Reaction Time

3.5 Recommended power-up/power-down sequences

Figure 24. **Power-up sequence - Fast VCC rise-up**

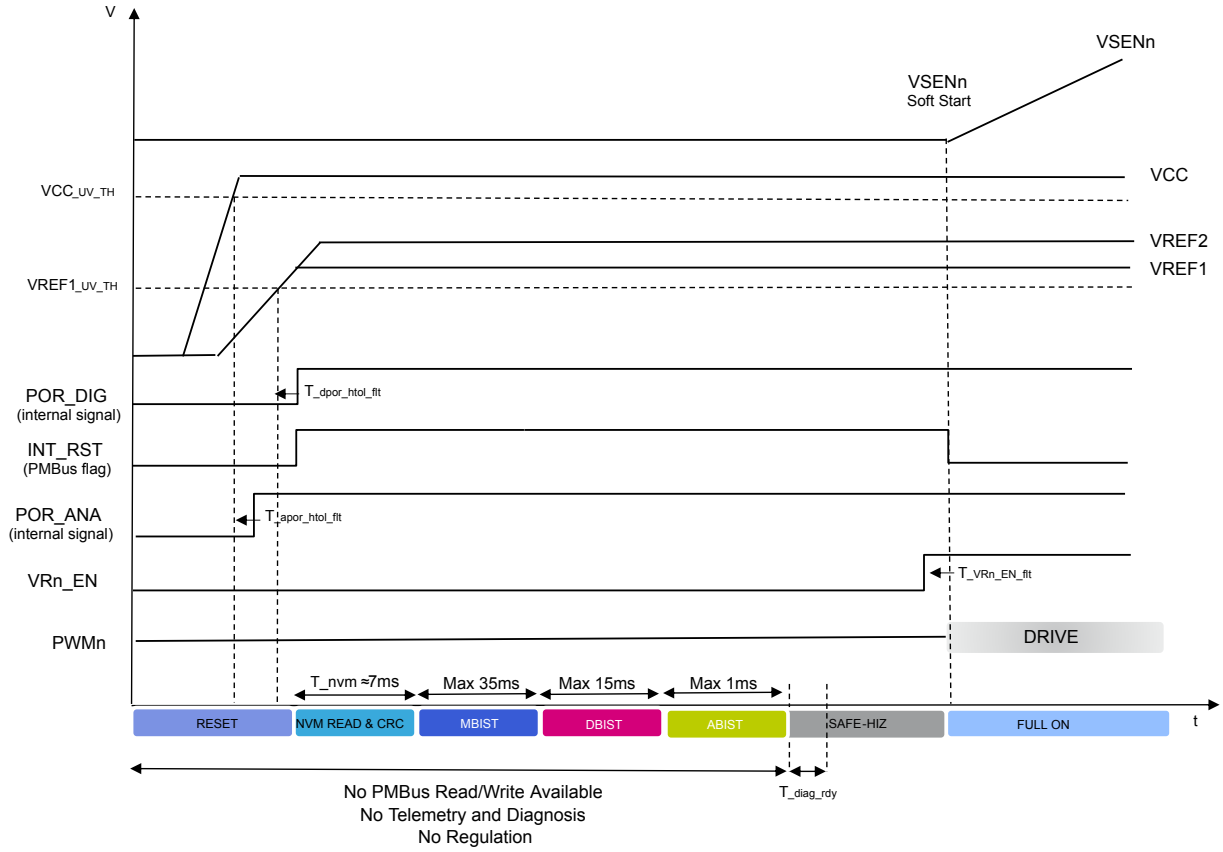
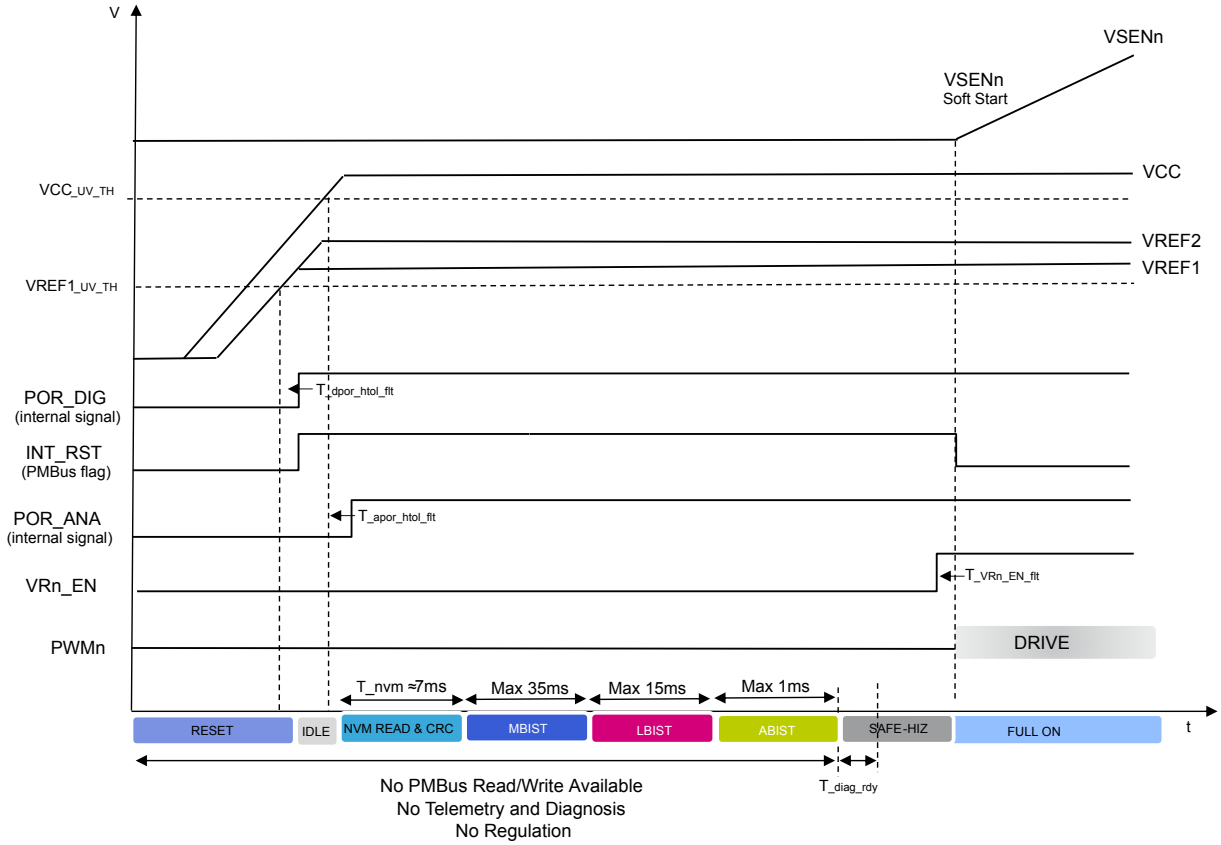


Figure 25. **Power-up sequence - Slow VCC rise-up**



When control loop enable is asserted through VR_ENn pin, for a correct regulation startup a low to high transition on its input voltage (battery line) shall take place after power-up sequence is completed (that is, after ABIST completion).

Direct connection of VR_ENn to VCC or VREFn shall be avoided.

Loop enabling/disabling logic is based on VR_ENn voltage level and edge as follows:

- VID reference is triggered according to the VR_ENn voltage edge: low to high on VR_ENn enables VID output as configured in VOUT_COMMAND, high to low transition disables VID output;
- The loop controller is triggered according to VR_ENn voltage level: high level on VR_ENn enables loop controller (except VID), low level disables loop controller.

As a consequence, applying a high logic level to VR_ENn without a clean low to high transition after power-up (ex. connecting VR_ENn to VREF1) will enable loop controller but not VID reference and will result in output loop trying to regulate the VID DAC offset.

Table 23. **Power-up timings**

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
T_nvm	NVM data deploy & CRC duration		-	-	7	ms	Application information
T_mbist	MBIST procedure duration		-	-	35	ms	Application information
T_dbist	DBIST procedure duration		-	-	15	ms	Application information
T_abist	ABIST procedure duration		-	-	1	ms	Application information
T_diag_rdy	Wait time for VRn_EN rising after PWUP sequence completion		2	-	-	ms	Application information

Figure 26. **Power-down sequence - Recommended (VRn_EN LOW before VCC drop)**

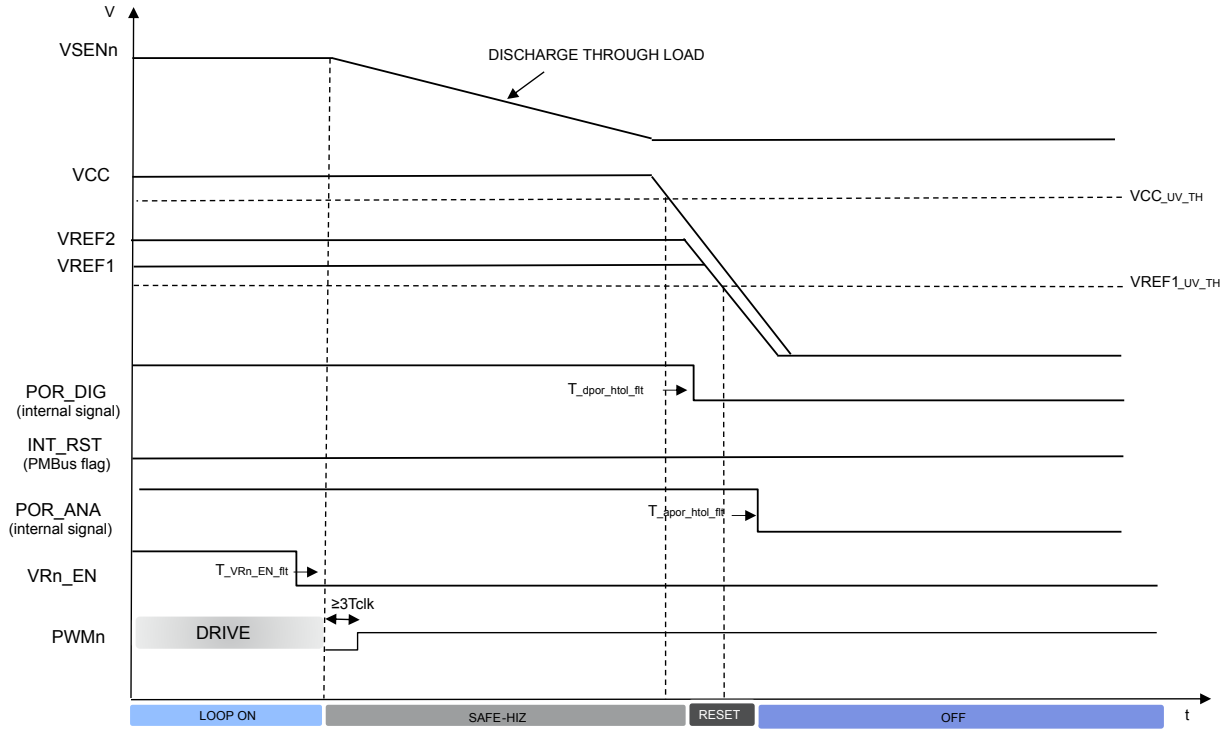
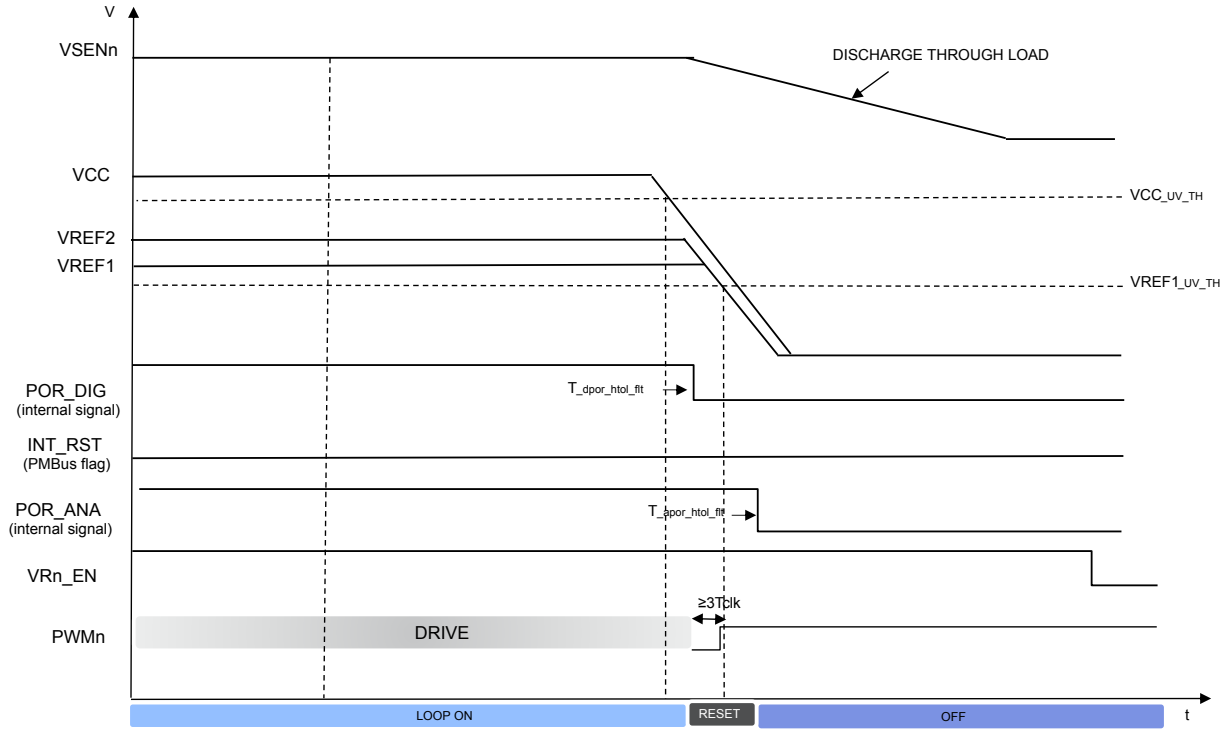


Figure 27. **Power-down sequence (VCC drop before VRn_EN LOW)**



3.5.1 Loop start/stop sequence

STPM098C loop controllers allow different methods to Start/Stop regulation by properly configuring PMBus™ standard commands:

- OPERATION
- ON_OFF_CONFIG

The OPERATION command is used to enable/disable the n-th control loop in conjunction with the VR_ENn pin and the MFR_VR_EN command.

This command defines also whether the n-th control loop has to work in margin mode (LOW/HIGH) or in NO margin mode.

- OPERATION[7:6] = 00, the control loop is directly disabled.
- OPERATION[5:4] = 00, the control loop is enabled in NO margin mode.
- OPERATION[5:4] = 01, the control loop is enabled in LOW margin mode.
- OPERATION[5:4] = 10, the control loop is enabled in HIGH margin mode.

Independently from bit [5:4] configuration, if an output overvoltage or undervoltage fault is detected STPM098C treats this fault as programmed in the related fault response command.

The ON_OFF_CONFIG command is used to configure the combination of VR_ENn pin input and serial bus OPERATION and MFR_VR_EN commands needed to enable/disable the n-th control loop.

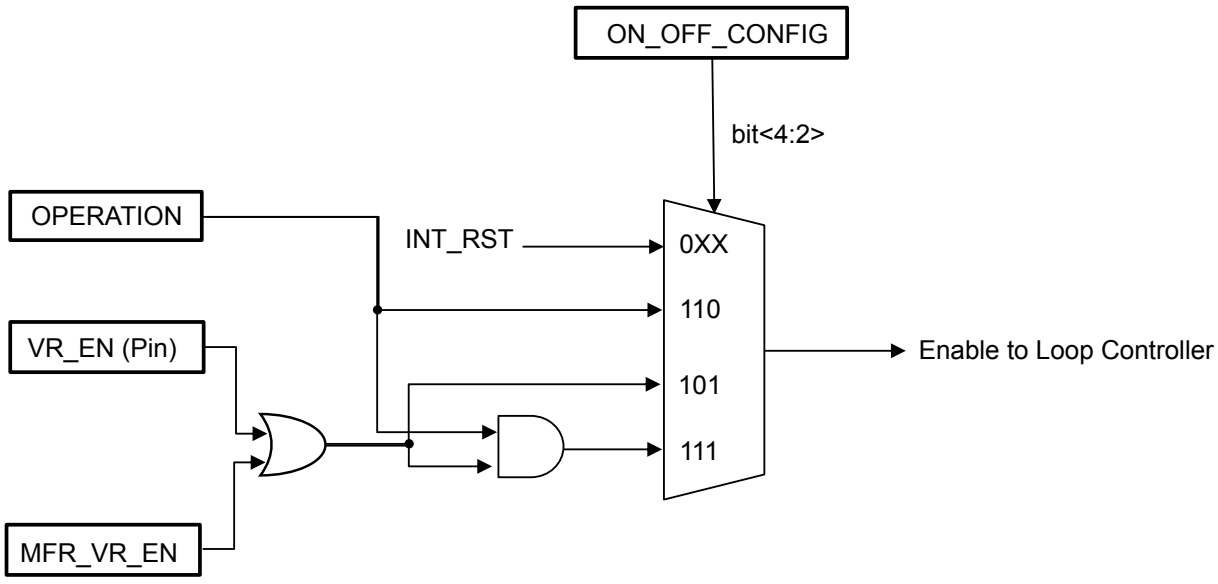
- ON_OFF_CONFIG[4:2] = 0xx, the loop is enabled and operates any time bias power is available regardless of the setting of bits [3:2].
- ON_OFF_CONFIG[4:2] = 110, the control loop is enabled/disabled only by OPERATION command.
- ON_OFF_CONFIG[4:2] = 101, the control loop is enabled/disabled only by logic OR between VR_ENn pin and MFR_VR_EN command.
- ON_OFF_CONFIG[4:2] = 111, the control loop is enabled when both the OPERATION command AND the VR_ENn pin ORMFR_VR_EN are commanding the loop to be on. If either an OPERATION command OR the VR_ENn pin AND MFR_VR_EN commands the control loop to be off.

Note: For both OPERATION and ON_OFF_CONFIG settings:

- *Any value not listed is an invalid command.*
- *Any bit not listed in the table is a don`t care.*

The ON_OFF_COMMAND operations can be depicted in the following simplified block diagram:

Figure 28. ON_OFF_CONFIG operation simplified block diagram



STPM098C loop can be configured to separately start each control loop by adjusting the relative delay through a dedicated PMBus™ command as follows:

$$TON_{DELAY} = \Delta_{LSB} \times TON_{DELAY[8:0]} \quad (1)$$

Where:

Δ_{LSB} is the minimum voltage step [1 ms].

TON_DELAY are the dedicated PMBus™ configuration bits.

Default value is TON_{DELAY} = 0x000. In case TON_{DELAY} = 0x000 the enabled delay is disabled.

TON_{DELAY} is carried out by means of a digital counter clocked at Tclk/125 (31.25 µs). As a consequence, since the VR_ENn value sampling is affected by a ±1Tclk uncertainty, TON_{DELAY} is affected by a ±31.25 µs uncertainty.

This effect is mostly visible at the default value when a delay between 0 µs and 31.25 µs shall be expected.

Figure 29. TON_DELAY simplified block diagram

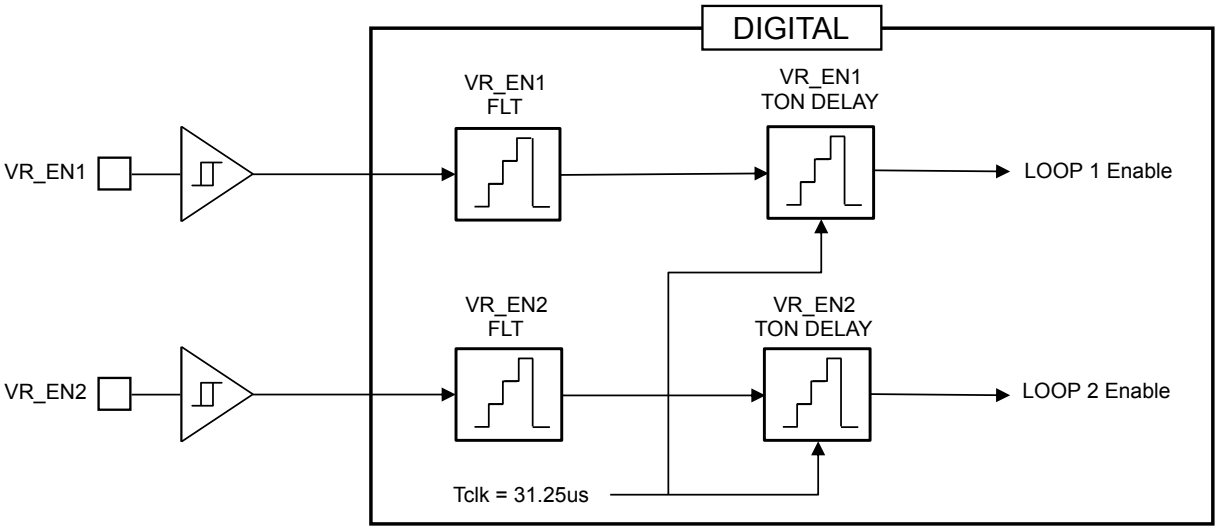
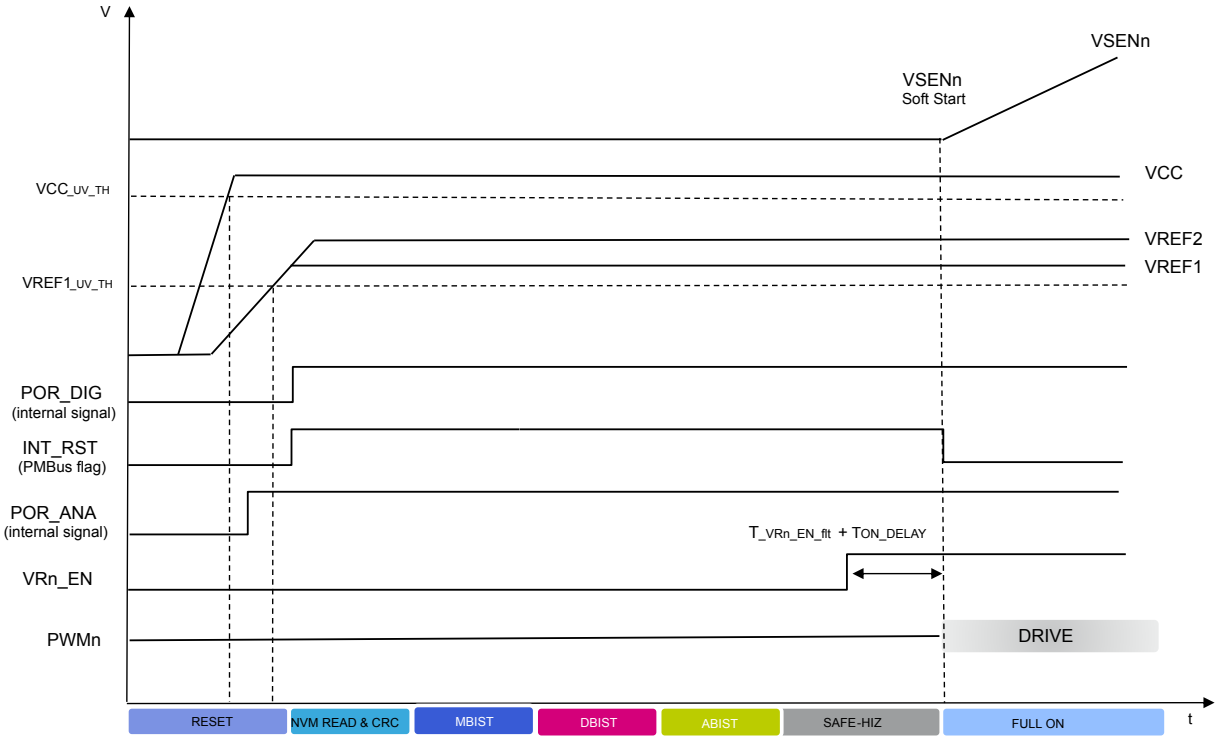


Figure 30. TON_DELAY function timing diagram



3.6 Digital I/O

3.6.1 Digital input (DI)

Digital input pins on STPM098C are used to transfer digital communications coming from an external source and supply domain to the internal logic and its related 1.8 V domain.

Table 24. Digital input pins functional partitioning

Pin	Default state	Description
SM_DATA, SM_CLK	Type A - No internal pull-up/down	PMBus™ pins
VRn_EN [n = 1, 2]	Type B - Internal current pull-down	Safety related pins (VRn_EN)

Digital input pin interface is protected by a CMOS Schmitt trigger supplied by the internal VCC power supply.

Figure 31. Digital input simplified structures - Type A and B

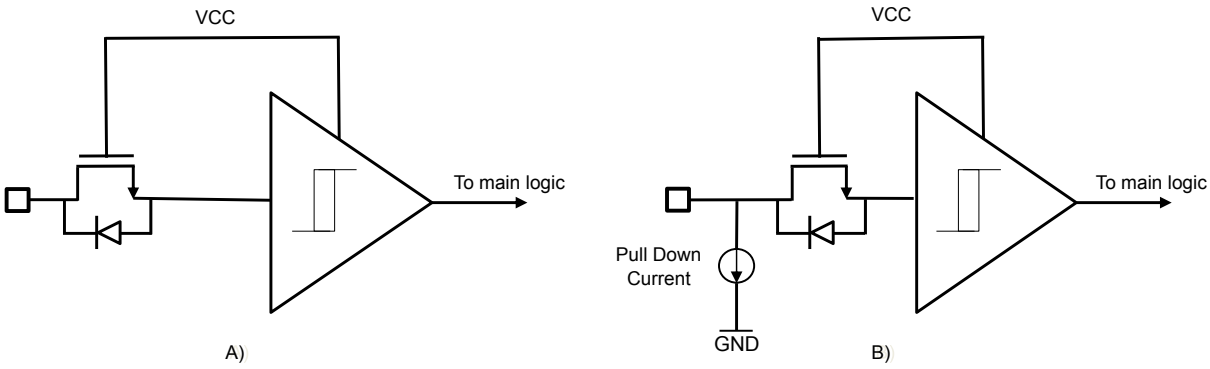


Table 25. Input electrical characteristics - Type A

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
DIA_in_hl	High input voltage range		1.35	-	-	V	-
DIA_in_ll	Low input voltage range		-	-	0.8	V	-
DIA_in_hyt	Threshold hysteresis		120	220	270	mV	-
DIA_in_leak	Input leakage current	Pin = GND/VCC	-5	-	5	µA	-

Table 26. Input electrical characteristics - Type B

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
DIB_in_hl_th	High input voltage range		0.78	-	-	V	-
DIB_in_ll_th	Low input voltage range		-	-	0.42	V	-
DIB_in_ltoh_th	High level threshold		0.42	0.68	0.78	V	Schmitt trigger output low to high
DIB_in_htol_th	High level threshold		0.42	0.46	0.78	V	Schmitt trigger output high to low
DIB_in_hyt	Threshold hysteresis		100	190	240	mV	-
DIB_in_pd	Input pull-down current	Pin = 1.8 V	30	40	60	µA	-
T_dib_in_flt	Deglitch filter time	CLK_SSM_EN = 0	9	10	11	µs	Digital filter

3.6.2 Digital output (DO)

Digital output pins on STPM098C are used to transfer an internal digital information to an external voltage domain.

Table 27. Digital input pins functional partitioning

Pin	Default state	Description
PWMn [n = 1, 2, 3, 4, 5, 6, 7, 8]	Type A - Push-pull	PWM pins
SM_DATA, SM_CLK, SM_ALERT, FAULT, VR_HOT, POWERIN_ALERT, VRRDY1, VRRD2	Type B - Open drain	PMBus™ pins and FOR pins

Type A digital output allows HIZ state. HIZ state is achieved by switching of pull-up and pull-down sources. No active sources are available on output pin in this state. When unsupplied, type A digital output goes directly in HIZ state.

Figure 32. Digital output simplified structures - Type A and B

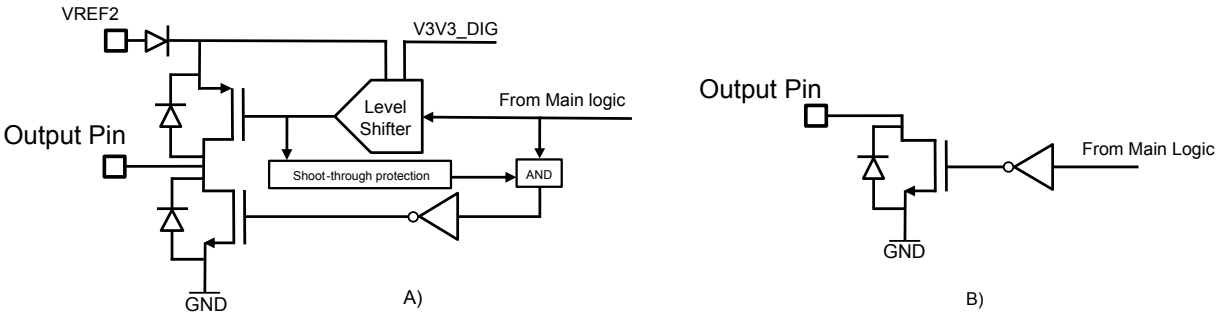


Table 28. Output electrical characteristics - Type A

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
DOA_out_hl	High output voltage	Iload = -1 mA	VREF2-0.2	-	-	V	-
DOA_out_ll	Low output voltage	Iload = 1 mA	0	-	0.2	V	-
DOA_out_hiz_leak	Output leakage in HIZ	Pin = 1.7 V	-5	-	5	uA	-
T_doa_rt	Output rise time	Cload = 120 pF from 10% to 70%	5	10	15	ns	-
T_doa_ft	Output fall time	Cload = 120 pF from 70% to 10%	5	10	15	ns	-

Table 29. Output electrical characteristics - Type B

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
DOB_in_ll	Low output voltage	Iload = 350 µA	-	-	0.4	V	-
T_dob_ft	Output fall time	Cload = 120 pF from 70% to 10%	8	12.5	16	ns	-

3.7 Internal clock

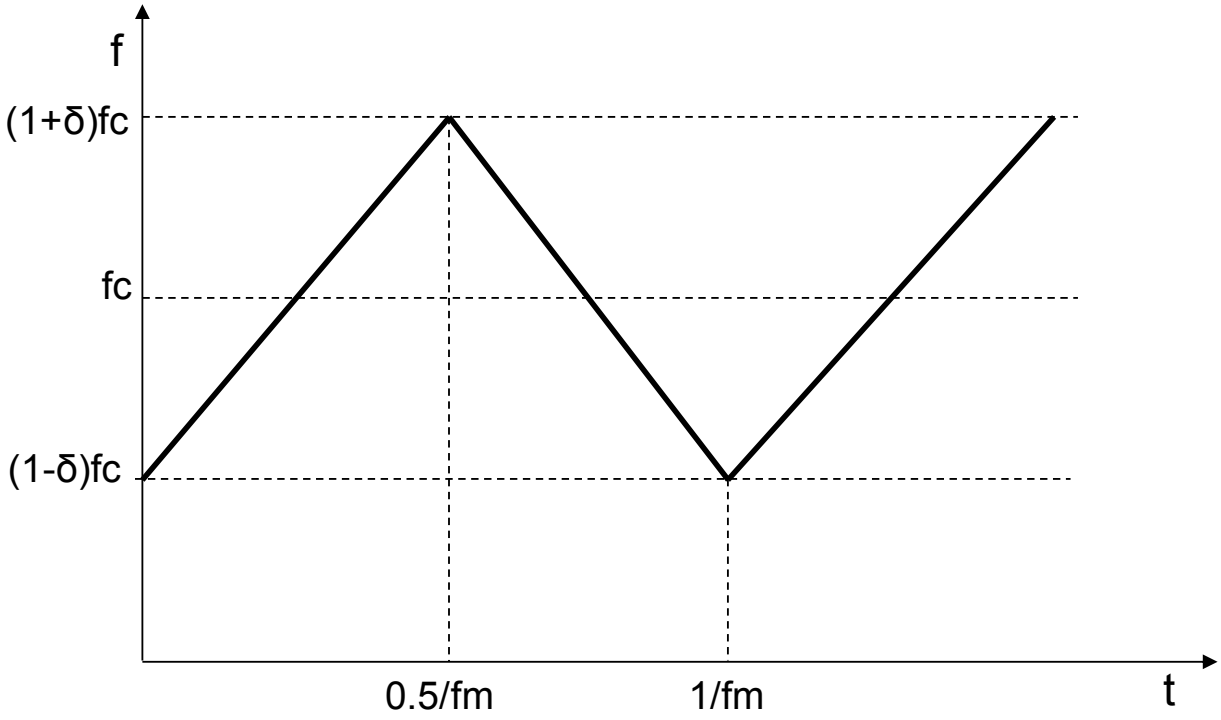
Table 30. Internal clock electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
CLK_freq	System clock frequency	CLK_SSM_EN = 0	-	40	-	MHz	-
CLK_freq_acc	System clock frequency accuracy	CLK_SSM_EN = 0	-5	-	+5	%	-
CLK_freq_match	Main vs. auxiliary frequency matching	CLK_SSM_EN = 0	-10	-	+10	%	-

3.7.1 Spread spectrum modulation (SSM)

STPM098C clock generator implements a frequency modulation (spread spectrum modulation) feature to reduce the main logic emissions around the main frequency by spreading the power spectrum over a larger frequency range.

Figure 33. Clock spread spectrum modulation details



The carrier frequency fc (typ = 40 MHz) is modulated by means of a triangular modulating signal with frequency fm and a spreading range δ.

Table 31. Clock spread spectrum electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
SSM_spreading	Spread spectrum modulation spreading range		1.5	-	3	%	Application information
SSM_freq	Spread spectrum modulating frequency		9.7	-	39	kHz	Application information

The clock spread spectrum modulation function can be enabled by a dedicated PMBus™ bit as follows:

Table 32. Clock spread spectrum enable bit

CLK_SSM_EN	Description
0	Clock SSM disabled (default)
1	Clock SSM enabled

Note:

- *When the clock spread spectrum is enabled, the internal digital timings are affected by a timing jitter equal to the selected spread spectrum spreading range.*
- *ICM timeout accuracy is valid only in case of sudden stuck fault. In case of progressive clock frequency degradation, such an accuracy range is no more valid.*
- *If no oscillator clock is available, the PMBus™ data processing cannot work properly: STPM098C delivers always the latest answer.*

3.7.2 Internal clock monitor (ICM)

The correct operation and the precision of the internal synchronization signal is safety relevant and therefore STPM098C implements a monitoring unit to detect abnormal deviation of the clock signal frequency.

The monitoring unit is based on the use of two oscillators and two monitor chains (a main one and an auxiliary one) to avoid common-cause failures. The main oscillator feeds, by default, the internal logic as system clock, while the auxiliary oscillator is used for diagnosis purpose only.

Each monitor chain compares the other clock period, the first one samples CLK1 by means of CLK2 and the second one samples CLK2 by means of CLK1.

If $\Delta f1=|(f_{CLK1} - f_{CLK2})/f_{CLK2}| \geq$ ICM_err_th: the flag CLK_MISMATCH is set. Internal reset is triggered.

If $\Delta f2=|(f_{CLK2} - f_{CLK1})/f_{CLK1}| \geq$ ICM_err_th: the flag CLK_MISMATCH is set.

If $T_{CLK1} \geq$ ICM_timeout_th: the flags INT_RST and CLK1_TIME_OUT are set. Internal reset is triggered.

If $T_{CLK2} \geq$ ICM_timeout_th: the flag CLK2_TIME_OUT is set.

If one of the previous conditions is verified the device state moves to SAFE STATE. The error flags remain set until the failure condition is removed and the flags are cleared by PMBus™ command or VR1_EN or VR2_EN.

The correct level of the clock monitor is safety relevant, thus a self-check procedure is implemented on its monitor.

Table 33. Internal clock monitor electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
ICM_err_th	ICM frequency mismatch threshold accuracy		-	25	-	%	Application information
ICM_timeout_th	ICM timeout accuracy		-	14	-	µs	Application information

3.8 Ground loss monitor (GLM)

STPM098C implements one ground reference pin GND dedicated to the low power internal analog/digital circuitry.

For EMI robustness GND pin is internally split in two GND reference PADs: AGND (ground reference for analog circuitry supplied from VCC and VREF2) and DGND (ground reference for digital circuitry supplied by VREF1). AGND is connected to the GND ESD ring by means of a direct metal connection and biases the substrate through SUB plugs placed all around the IC border.

STPM098C implements a monitoring unit to detect disconnection affecting ground references.

If VGND_DIG-VGND_ANA ≥ VTH_GND occurs for an interval longer than T_glm_loss_flt, the DGND_LOSS flag is set.

If VGND_ANA-VGND_DIG ≥ VTH_GND occurs for an interval longer than T_glm_loss_flt, the AGND_LOSS flag is set.

The correct operation ground loss monitor stage is safety relevant and then a self-check procedure is implemented.

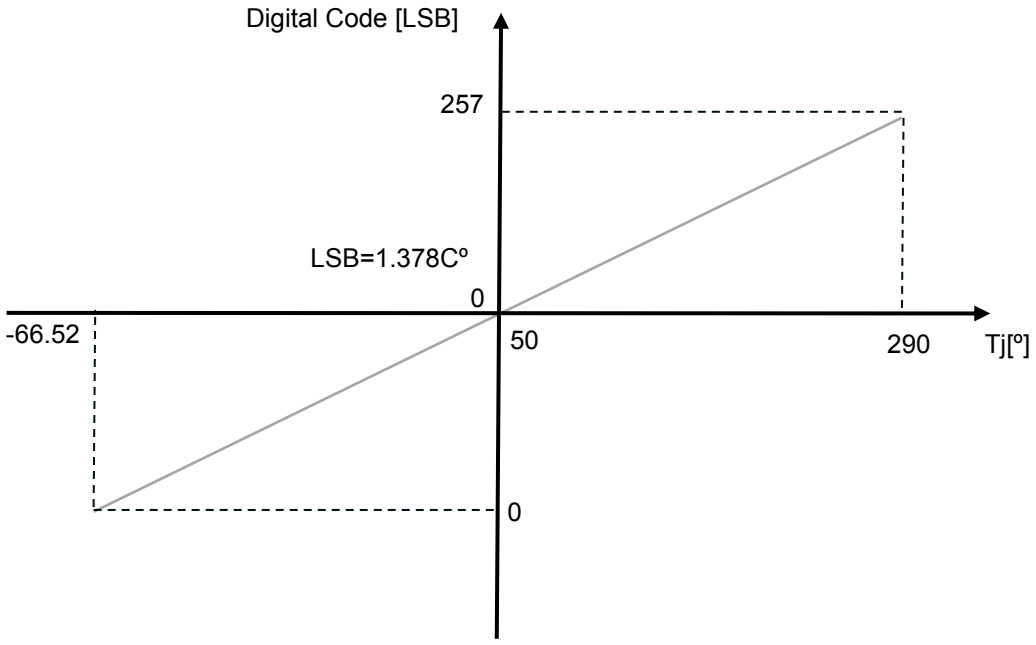
Table 34. GLM electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
GLM_th	GLM detection threshold VTH_GND		0.24	0.4	0.55	V	-
T_glm_loss_flt	GLM filter time	CLK_SSM_EN = 0	1	1.25	1.5	ms	Digital filter

3.9 Overtemperature monitor (OTM)

STPM098C implements a monitoring unit of the average junction temperature able to detect excessive overheating conditions affecting the device.

Figure 34. Temperature monitor ADC characteristics



Temperature measurement data is stored in a dedicated register and can be retrieved by PMBus™ readout of register READ_TEMPERATURE_2. Die temperature can be calculated with the following formula:

$$T_j[°C] = \left(1.378\,°C \times D_{TEMP_{READ}}\right) - 66.52\,°C \quad (2)$$

Where:

$D_{TEMP_{READ}}$ is the digital word stored in READ_TEMPERATURE_2.

The digitized temperature information is compared by two hysteresis comparators with selectable threshold based on the following scheme:

- If DTEMP ≥ DTEMP_WR_TH occurs for an interval longer than T_otm_wr_flt, the OTM_WR flag is set. The error flag remains set until the failure condition is removed.
- If DTEMP ≥ DTEMP_SD_TH (= 175 deg.) occurs for an interval longer than T_otm_sd_flt, the OTM_SD flag is set and SAFE_HIZ is established. The error flag remains set until the failure condition is removed and a rinsing edge on VR1_EN or VR2_EN is detected.

Thermal warning thresholds can be independently configured by the following PMBus™ bit sets:

Table 35. Thermal warning configuration bits

OT_WARN_LIMIT1	OT_WARN_LIMIT0	Description
0	0	130 deg.
0	1	140 deg. (default)
1	0	150 deg.
1	1	160 deg.

Figure 35. **Junction temperature range 1**

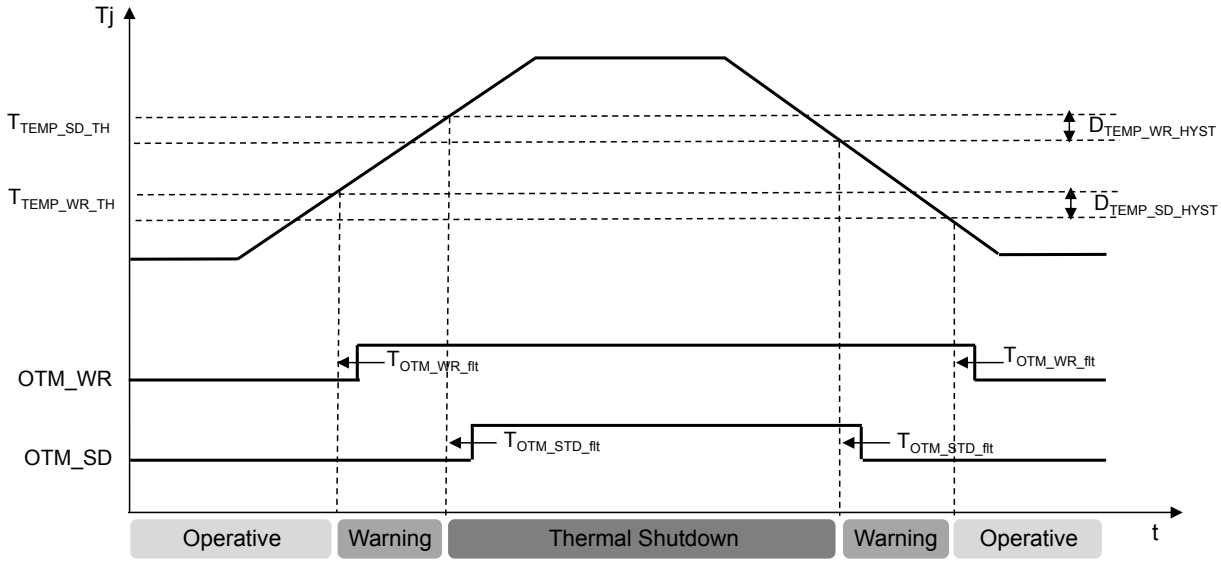
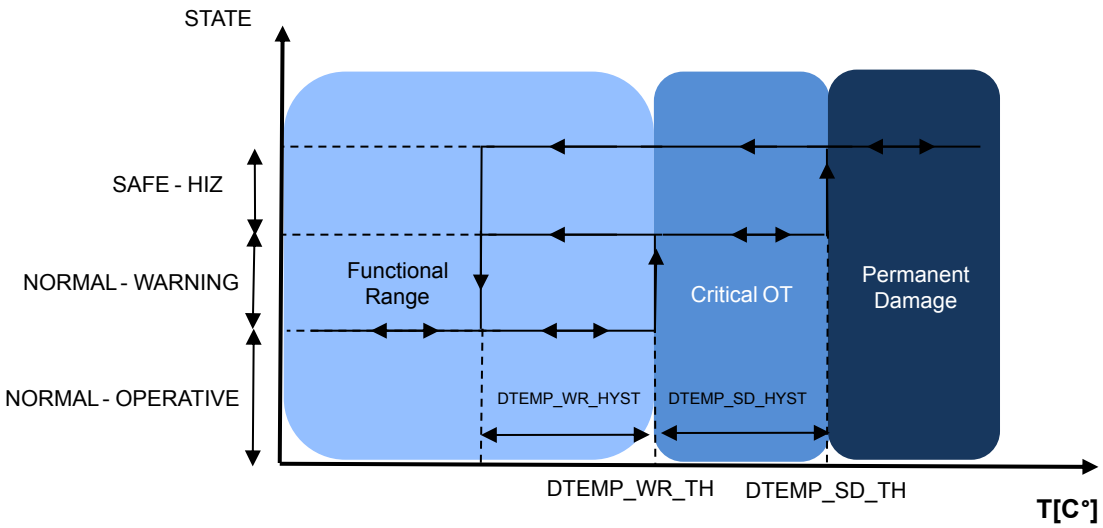


Figure 36. **Junction temperature range 2**



Temperature Range: Parametrical/Functional Range

STPM098C is in LOOP ON mode. No damage affects STPM098C and no wrong operation takes place. All static and dynamic parameters stay within specification limits.

Temperature Range: Critical OT Range

STPM098C is set into SAFE STATE mode. No damage affects STPM098C and no wrong operation takes place. Static and dynamic parameters may deviate from specification limits.

Exposure to critical OT conditions for extended periods may affect device reliability.

Table 36. **OTM electrical characteristics**

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
ADC input							
OTM_hys	OTM detection threshold hysteresis		5	10	15	°C	Application information

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
ADC input Resolution							
OTM_readout_red	OTM resolution		-	8	-	bits	Design information
OTM_readout_lsb	OTM LSB		-	1.378	-	°C	Design information
ADC input accuracy							
OTM_acc	OTM ADC conversion accuracy		-10	-	10	°C	Temperature Read out accuracy
ADC input dynamic characteristics							
OTM_sr	OTM ADC sample rate	CLK_SSM_EN = 0	-	10	-	kHz	Application information
OTM_latency	OTM ADC conversion latency	CLK_SSM_EN = 0	-	0.205	1	ms	Application information

3.10 Auxiliary voltage monitor (AVM)

STPM098C implements a general-purpose voltage monitor through pin AUX_SENSEs to allow a dedicated UV and OV diagnosis for external voltage references. Hysteresis on thresholds and filtering time are implemented. The digitized voltage information is compared with a selectable threshold based on the following scheme:

If AUX_SENSE ≤ AUX_SENSE_uv_th occurs for an interval longer than T_avm_detect_dly, fault is asserted and the AUX_SENSE_UV flag is set. Fault pins are asserted LOW according to FHC configuration and FOR table.

If AUX_SENSE ≥ AUX_SENSE_ov_th occurs for an interval longer than T_avm_detect_dly, fault is asserted and the AUX_SENSE_OV flag is set. Fault pins are asserted LOW according to FHC configuration and FOR table.

The reference thresholds for the AVM monitor unit AUX_SENSE_uv_th and AUX_SENSE_ov_th can be separately configured through a dedicated PMBus™ register as follows:

$$AUX_{SENSE_{UV_{TH}}} + AVM_{th_{hyst}} = AVM_{th_{lsb}} \times AUX_{SENSE_{UV_{TH[2:0]}}} + OFS \quad (3)$$

$$AUX_{SENSE_{OV_{TH}}} + AVM_{th_{hyst}} = AVM_{th_{lsb}} \times AUX_{SENSE_{OV_{TH[2:0]}}} + OFS$$

Where:

AVM_adc_lsb is the minimum voltage step [131 mV = 7 * AVM_adc_lsb].

AUX_SENSE_uv_th [2:0] are the dedicated PMBus™ configuration bits [0.486 V ~ 1.402 V].

AUX_SENSE_ov_th [2:0] are the dedicated PMBus™ configuration bits [0.617 V ~ 1.533 V].

OFS is the starting value [486 mV = 26 * AVM_adc_lsb].

The default value is AUX_SENSE_uv_th =0x0 and AUX_SENSE_ov_th = 0x0.

In case AUX_SENSE_uv_th = 0x0 the AVM UV function is disabled and no UV detection is performed.

In case AUX_SENSE_ov_th = 0x0 the AVM OV function is disabled and no OV detection is performed.

The absolute value of the maximum input voltage slew rate detectable by IIN monitor is given by AVM_adc_lsb/ AVM_adc_latency.

Figure 37. **AVM timing diagram**

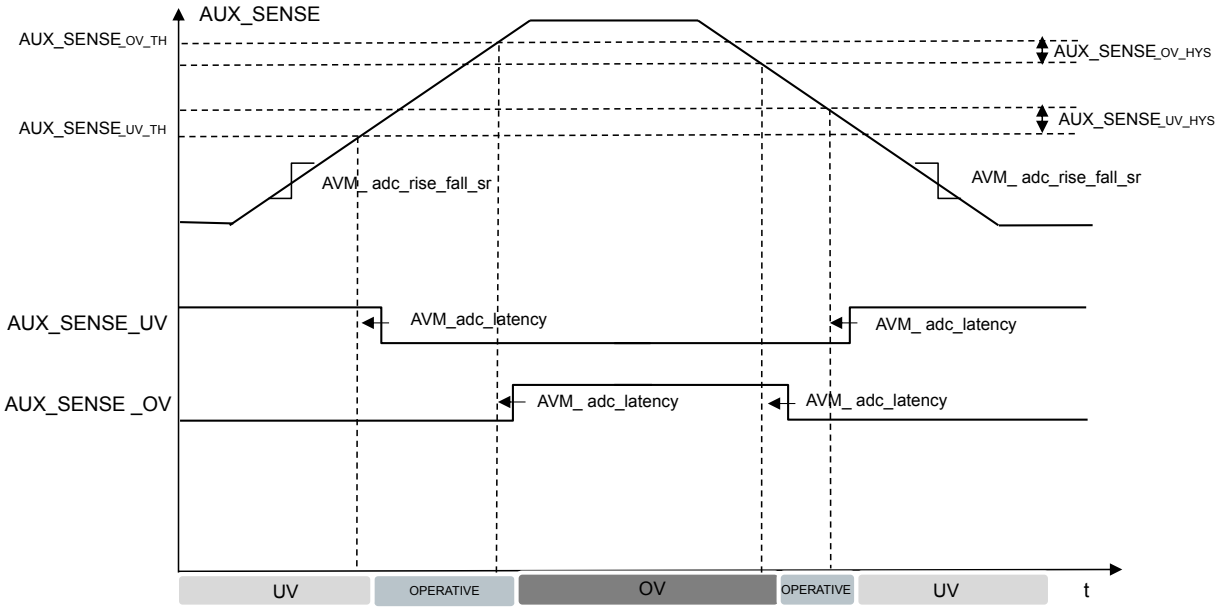


Table 37. **AVM ADC electrical characteristics**

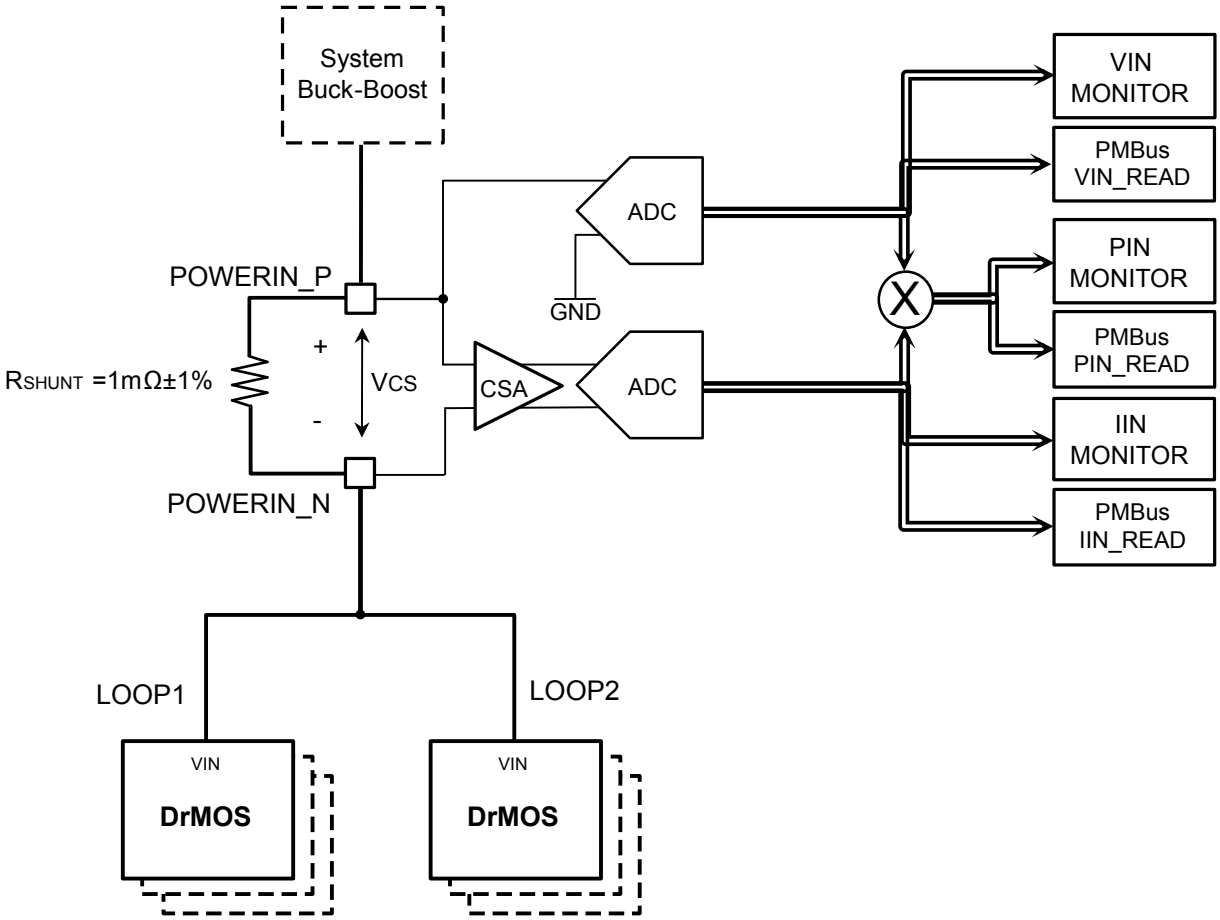
Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
ADC input							
AVM_adc_range	AVM ADC voltage input range		0	-	2	V	-
AVM_adc_ic	AVM ADC input current	AUX_SENSE = 5 V VCC = 5 V	20	30	40	µA	-
ADC input Resolution							
AVM _adc_resolution	AVM ADC resolution		-	7	-	bits	Application information
AVM_adc_lsb	AVM ADC LSB		-	18.7	-	mV	Application information
ADC input accuracy							
AVM_adc_tot_err1	AVM ADC total error1	0 V ≤ AUX_SENSE < 0.5 V	-100	-	100	mV	-
AVM_adc_tot_err2	AVM ADC total error2	0.5 V ≤ AUX_SENSE < 2 V	-20	-	20	%	-
ADC input dynamic characteristics							
AVM_adc_in_sr	AVM ADC sample rate		-	10	-	MHz	Application information
AVM_adc_latency	AVM ADC conversion latency		-	65	100	µs	Application information
AVM characteristics							
AVM_th_lsb	AVM monitoring threshold step		-	131	-	mV	Application information
AVM_th_hyst	AVM monitoring hysteresis		-	131	-	mV	Application information
AVM_th_range	AVM monitoring threshold range		0.486	-	1.533	V	Application information

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
T_avm_detect_dly	AVM detection delay	CLK_SSM_EN = 0	-	65	100	µs	Application information

3.11 Input metrics telemetry (IMT)

STPM098C implements a full set of telemetry measurements on the converter`s input voltage, current and power metrics through pins POWERIN_P and POWERIN_N.

Figure 38. Input telemetry simplified block diagram



3.11.1 Input voltage measurement

Input voltage is directly measured at POWERIN_P pin by means of a dedicated 10-bit ADC converter. The digitized voltage information is made available on PMBus™ register READ_VIN<15:0>.

Table 38. Input voltage ADC electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
ADC input							
VIN_adc_range	VIN ADC voltage input range		0	-	20	V	-
VIN_adc_ic	VIN ADC input current	POWERIN_P = 20 V VCC = 5 V	300	-	500	µA	-
VIN_adc_ilkg	VIN ADC input leakage	POWERIN_P = 20 V VCC = 0 V	-	-	200	nA	-

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
ADC input resolution							
VIN_adc_resolution	VIN ADC resolution		-	10	-	bits	Application information
VIN_adc_lsb	VIN ADC LSB		-	22.3	-	mV	Application information
ADC input accuracy							
VIN_adc_tot_err1	VIN ADC total error1	0 V ≤ POWERIN_P < 4.5 V	-135	-	135	mV	-
VIN_adc_tot_err2	VIN ADC total error2	4.5 V ≤ POWERIN_P < 20 V	-3	-	3	%	-
ADC input dynamic characteristics							
VIN_adc_in_sr	VIN ADC sample rate		-	10	-	MHz	Application information
VIN_adc_latency	VIN ADC conversion latency	CLK_SSM_EN = 0	-	65	100	µs	Application information

3.11.1.1 *Input voltage monitor (VIN monitor)*

Input voltage level is monitored by means of dedicated UV diagnosis based on VIN conversion. A hysteresis on thresholds and filtering time is implemented.

If POWERIN_P ≤ VIN_off_th occurs for an interval longer than T_vin_mon_detect_dly, the fault is asserted and the VIN_UV flag is set. Fault pins are asserted LOW according to FHC configuration and FOR table.

If POWERIN_P ≥ VIN_on_th occurs for an interval longer than T_vin_mon_detect_dly, the VIN_UV fault is released. VIN_UV clearing depends on FHC configuration.

The reference thresholds for the VIN monitor unit VIN_off_th and VIN_on_th can be separately configured through a dedicated PMBus™ register as follows:

$$VIN_{OFF_{TH}} = VIN_{MON_{th_{lsb}}} \times VIN_{OFF_{TH[7:0]}} \quad (4)$$

$$VIN_{ON_{TH}} = VIN_{MON_{th_{lsb}}} \times VIN_{ON_{TH[7:0]}} \quad (5)$$

Where:

VIN_MON_th_lsb is the minimum voltage step [89.2 mV].

VIN_OFF_TH/VIN_ON_TH [7:0] are the dedicated PMBus™ configuration bits [0 V ~ 22.8 V].

The default value is VIN_ON_TH =0x07B (11 V) and VIN_OFF_TH = 0x078 (10.7 V).

In case VIN_OFF_TH = 0x000 the input voltage monitor function is disabled, and no UV detection is performed.

The absolute value of the maximum input voltage slew rate detectable by VIN monitor is given by VIN_adc_lsb/ VIN_adc_latency.

Figure 39. **Input voltage monitor timing diagram**

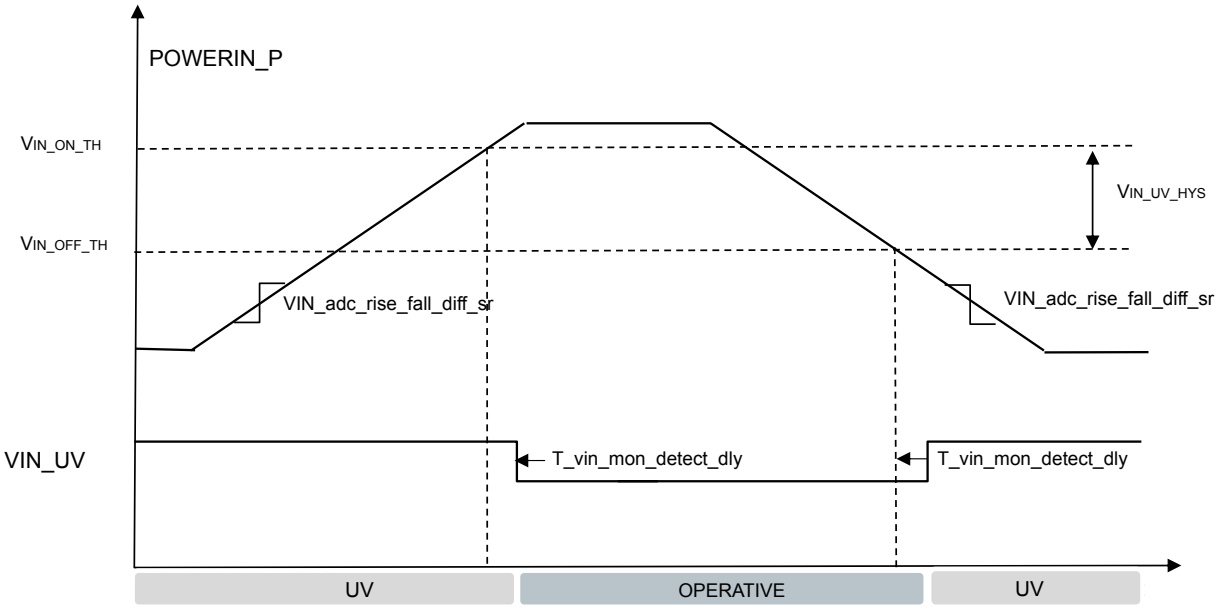


Table 39. **VIN monitor electrical characteristics**

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
VIN_MON_th_lsb	VIN monitoring threshold step		-	89.2	-	mV	Application information
VIN_MON_th_range	VIN monitoring threshold range		0.125	-	22.8	V	Application information
T_vin_mon_detect_dly	VIN monitoring detection delay	CLK_SSM_EN = 0	-	65	100	µs	Application information

3.11.2 Input current measurement

Input current is converted by an external shunt resistance (1 mΩ ±1%) into a differential voltage measured across the input pins POWERIN_P and POWERIN_N.

A current sense amplifier (CSA) is used to amplify the differential voltage then converted via an internal 10-bit ADC. The digitized current information is made available on PMBus™ register READ_IIN<15:0>.

Table 40. **Input current ADC electrical characteristics**

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
ADC input							
IIN_adc_diff_range	IIN ADC voltage differential input range		0	-	50	mV	-
IIN_adc_cm_range	IIN ADC voltage common mode input range		4.5	-	20	V	-
IIN_adc_ic	IIN ADC input current	POWERIN_N = 20 V VCC = 5 V	5	-	45	uA	-
IIN_adc_ilkg	IIN ADC input leakage	POWERIN_N = 20 V VCC = 0 V	-	-	200	nA	-
ADC input resolution							
IIN_adc_resolution	IIN ADC resolution		-	10	-	bits	Application information

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
IIN_adc_lsb	IIN ADC LSB	CLK_SSM_EN = 0	-	53.2	-	µV	Application information
ADC input accuracy							
IIN_adc_gain_err	IIN ADC gain error		-3	-	3	%	-
IIN_adc_offset_err	IIN ADC input referred offset error		-1	-	1	mV	-
IIN_adc_tot_err	IIN ADC total error		-	-	-	mV	See note
ADC input dynamic characteristics							
IIN_adc_in_sr	IIN ADC sample rate		-	10	-	MHz	Application information
IIN_adc_latency	IIN ADC conversion latency	CLK_SSM_EN = 0	-	65	100	µs	Application information

Note: IIN_ADC conversion total error can be calculated as follows:

*IIN_adc_tot_err = IIN_adc_gain_err * (POWERIN_P - POWERIN_N) + IIN_adc_offset_err*

Example:

- *| POWERIN_P-POWERIN_N | = 10 mV*
- *Total ADC conversion error = ±1 mV ±(3% * 10 mV) = ±1 mV ±0.3 mV*
- *The value read by PMBus™ has a range between 10 mV - (1 mV + 0.3 mV) and 10 mV + (1 mV + 0.3 mV)*

3.11.2.1 *Input current monitor (IIN monitor)*

Input current level is monitored by means of dedicated OC diagnosis based on IIN conversion. A hysteresis on thresholds and filtering time is implemented.

If POWERIN_P- POWERIN_N ≥ IIN_off_th occurs for an interval longer than T_iin_mon_detect_dly, the fault is asserted and the IIN_OC flag is set. Fault pins are asserted LOW according to FHC configuration and FOR table.

If POWERIN_P- POWERIN_N ≤ IIN_on_th occurs for an interval longer than T_iin_mon_detect_dly, the IIN_ OC fault is released. IIN_OC clearing depends on FHC configuration.

The reference thresholds for the IIN monitor unit IIN_off_th and IIN_on_th can be separately configured through a dedicated PMBus™ register as follows:

$$IIN_{OFF_{TH}} = IIN_{MON_{th_{lsb}}} \times IIN_{OFF_{TH}[9:0]} \quad (6)$$

$$IIN_{ON_{TH}} = IIN_{MON_{th_{lsb}}} \times IIN_{ON_{TH}[9:0]} \quad (7)$$

Where:

IIN_MON_th_lsb is the minimum voltage step [53.2 µV].

IIN_OFF_TH/IIN_ON_TH [9:0] are the dedicated PMBus configuration bits [53.2 µV ~ 54.4 mV].

The default value is IIN_OFF_TH =0x11A (15 mV) and IIN_ON_TH = 0x0E1 (12 mV).

In case IIN_OFF_TH = 0x000 the input current monitor function is disabled, and no OC detection is performed.

The absolute value of the maximum input voltage slew rate detectable by IIN monitor is given by IIN_adc_lsb/ IIN_adc_latency.

Figure 40. **Input current monitor timing diagram**

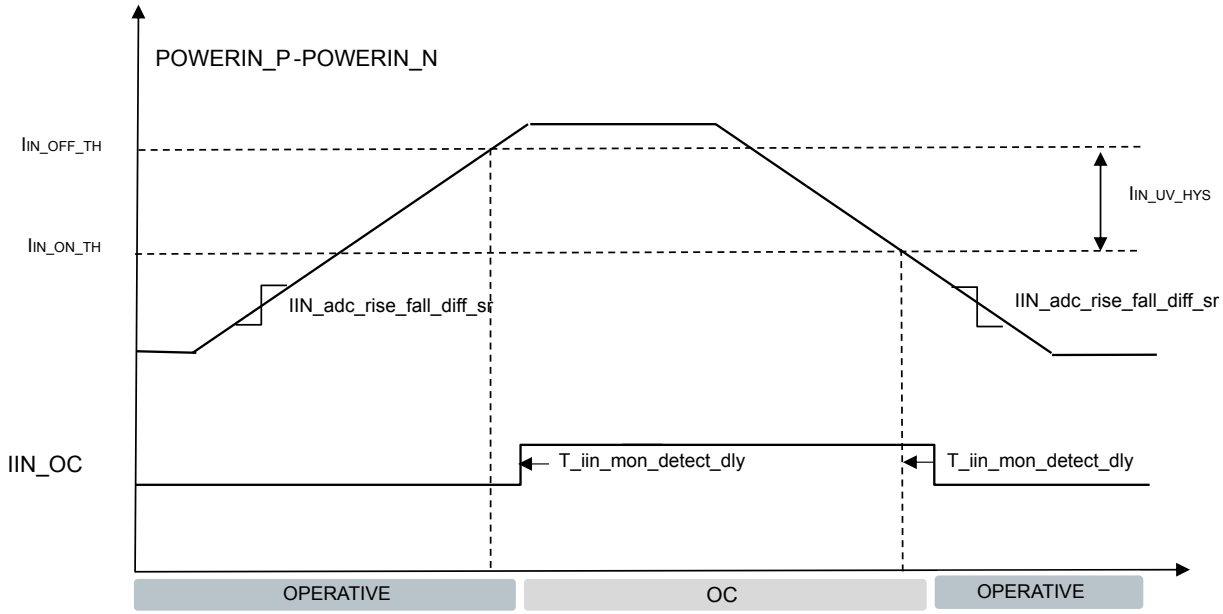


Table 41. **IIN monitor electrical characteristics**

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
IIN_MON_th_lsb	IIN monitoring threshold step		-	53.2	-	µV	Application information
IIN_MON_th_range	IIN monitoring threshold range		0.0532	-	54.4	mV	Application information
T_iin_mon_detect_dly	IIN monitoring detection delay	CLK_SSM_EN = 0	-	65	100	µs	Application information

3.11.3 Input power calculation

Based on input voltage and input current measurements the input power is computed by multiplying the converted values. The power information is made available on PMBus™ register READ_PIN<15:0>.

Table 42. **Input power calculation characteristics**

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
Power multiplier output							
PIN _range	PIN computation range		0	-	500	W	Application information
Power multiplier Resolution							
PIN _resolution	PIN computation resolution		-	16	-	bits	Application information
PIN_lsb	PIN LSB		-	18.98	-	mW	Application information
Power multiplier dynamic characteristics							
PIN_latency	PIN computation latency	CLK_SSM_EN = 0	-	65	100	µs	Application information

3.11.3.1 *Input power monitor (PIN monitor)*

Input power level is monitored by means of dedicated OP diagnosis based on PIN calculation. A hysteresis on thresholds and filtering time is implemented.

If PIN ≥ PIN_off_th occurs for an interval longer than PIN_latency, the fault is asserted and the PIN_OP flag is set. Fault pins are asserted LOW according to the FHC configuration and FOR table.

If PIN ≤ PIN_on_th occurs for an interval longer than PIN_latency, the PIN_OP fault is released. PIN_OP clearing depends on FHC configuration.

The reference thresholds for the IIN monitor unit PIN_off_th and PIN_on_th can be separately configured through a dedicated PMBus™ register as follows:

$$PIN_{OFF_{TH}} = PIN_{MON_{th_{lsb}}} \times > PIN_{OFF_{TH}[10:0]} \quad (8)$$

$$PIN_{ON_{TH}} = PIN_{MON_{th_{lsb}}} \times > PIN_{ON_{TH}[10:0]} \quad (9)$$

Where:

PIN_MON_th_lsb is the minimum voltage step [0.3 W].

PIN_OFF_TH/PIN_ON_TH [10:0] are the dedicated PMBus™ configuration bits [0.3 W ~ 500 W].

The default value is PIN_ON_TH = 0x1F4(150 W) and PIN_OFF_TH = 258 (180 W).

In case PIN_OFF_TH = 0x000 the input current monitor function is disabled, and no OP detection is performed.

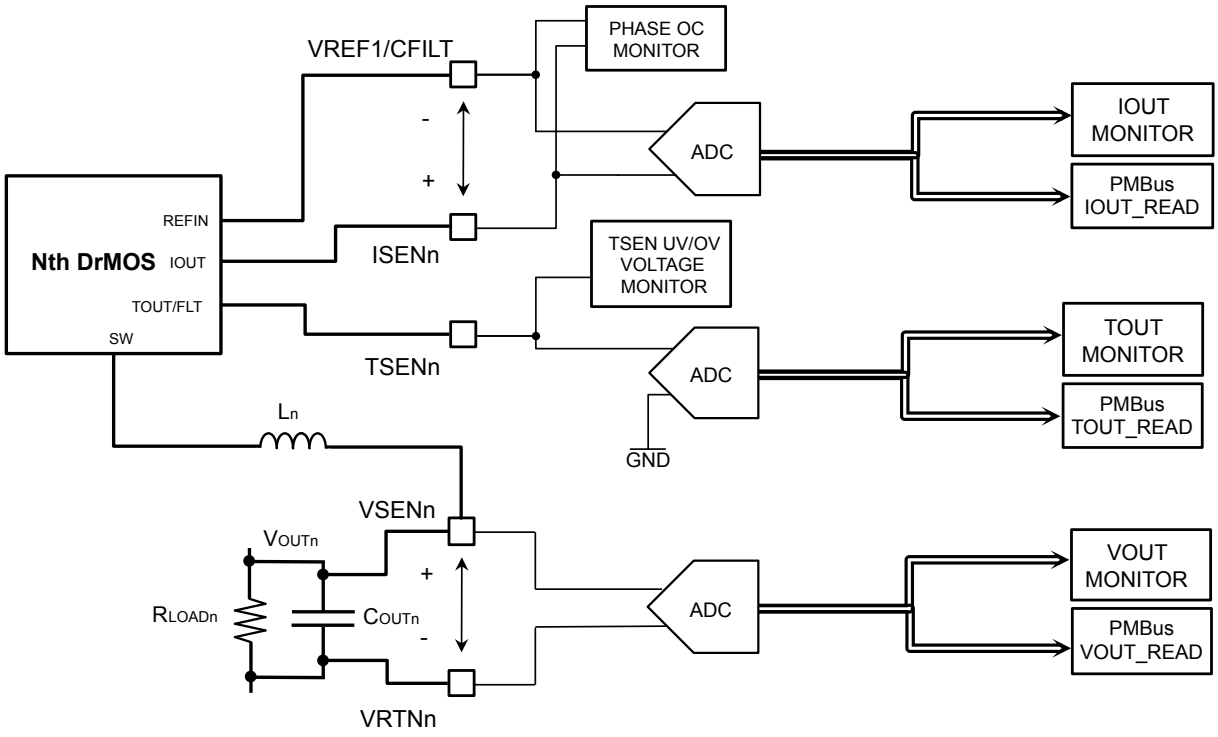
Table 43. PIN monitor electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
PIN_MON_th_lsb	PIN monitoring threshold step		-	0.3	-	W	Application information
PIN_MON_th_range	PIN monitoring threshold range		0.25	-	500	W	Application information

3.12 Output metrics telemetry (OMT)

STPM098C implements a full set of telemetry measurements on the converter's output voltage and currents, and output stages temperature metrics for each control loops.

Figure 41. Output telemetry simplified block diagram



3.12.1 Output stages temperature telemetry

The output stages maximum temperature for each loop can be directly measured at the input pin TSENn by means of a dedicated 9-bit ADC converter. The digitized voltage information is made available on PMBus™ paged register READ_TEMPERATUREn_1<15:0> [n = 1, 2].

- TSENn pin is intended to be connected to the DrMOS terminal TOUT. All TOUT pins of DrMOS referring to the same control loop are supposed to be shorted together;
- Output stage telemetry ADC and the related monitoring unit design is based on the following DrMOS temperature sensor output characteristics:

Figure 42. DrMOS temperature sense output reference characteristics

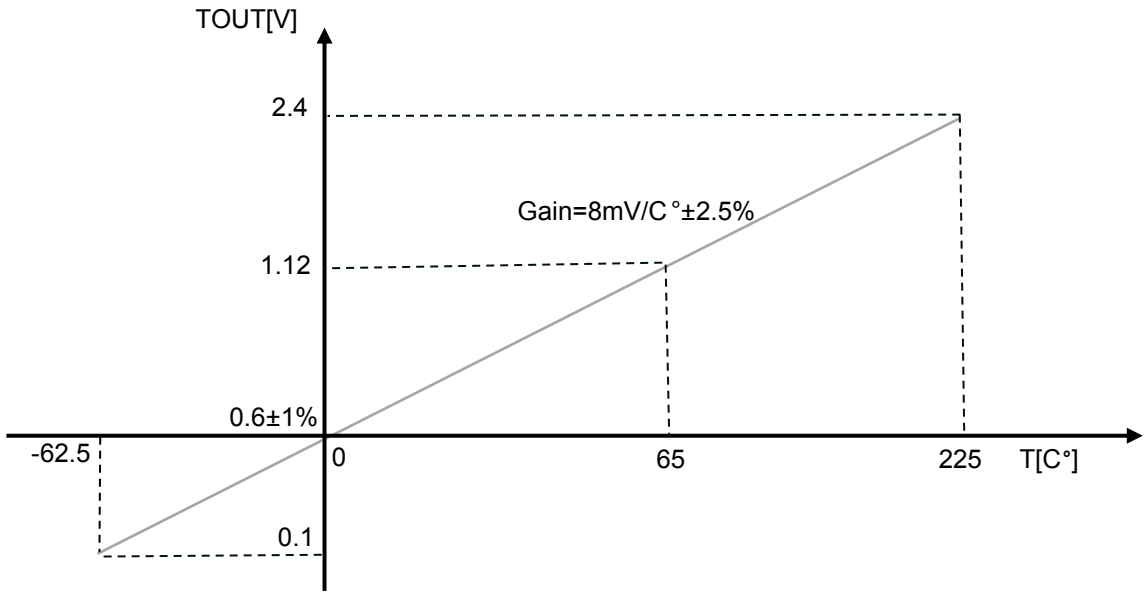


Table 44. Output Stage temperature ADC electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
ADC input							
TOUT_adc_range	TOUT ADC voltage input range		0.1	-	2.4	V	-
TOUT_adc_ic	TOUT ADC input current	TSENn = 5 V VCC = 5 V	60	100	150	µA	[n = 1, 2]
ADC input resolution							
TOUT_adc_resolution	TOUT ADC resolution		-	9	-	bits	Application information
TOUT_adc_lsb	TOUT ADC LSB		-	5.33	-	mV	Application information
ADC input accuracy							
TOUT_adc_total_err	TOUT ADC total error	0.28 V ≤ TSENn < 2 V	-40	-	40	mV	[n = 1, 2]
ADC input dynamic characteristics							
TOUT_adc_in_sr	TOUT ADC sample rate		-	10	-	MHz	Application information
TOUT_adc_latency	TOUT ADC conversion latency	CLK_SSM_EN = 0	-	65	100	µs	Application information

3.12.1.1 *Output stages temperature monitor (TOUT monitor)*

The digitized output stage temperature information is compared with selectable thresholds based on the following scheme:

- If TSENn ≥ TOUTn_wr_th occurs for an interval longer than T_tout_mon_detect_dly, the TOUTn_OT_WR flag is set. The error flag remains set until the failure condition is removed [n = 1, 2].
- If TSENn ≥ TOUTn_sd_th occurs for an interval longer than T_tout_mon_detect_dly, the TOUTn_OT_SD flag is set. Fault pins and safe state activation depends on FHC configuration. TOUTn_OT_SD clearing depend on FHC configuration [n = 1, 2].

The reference thresholds for the TOUTn monitor unit TOUTn_wr_th and TOUTn_sd_th can be separately configured through a dedicated PMBus™ register as follows:

$$TOUT_{n_{OT_{WR_{TH}}}} = TOUT_{MON_{th_{lsb}}} \times TOUT_{n_{OT_{WR_{TH}[8:0]}}} \quad (10)$$

$$TOUT_{n_{OT_{SD_{TH}}}} = TOUT_{MON_{th_{lsb}}} \times TOUT_{n_{OT_{SD_{TH}[8:0]}}} \quad (11)$$

Where:

TOUT_MON_th_lsb is the minimum voltage step.

TOUTn_OT_WR_TH/TOUTn_OT_SD_TH [8:0] are the dedicated PMBus™ configuration bits.

The default values are TOUTn_OT_WR_TH = 0x12C (125 deg.) and TOUTn_OT_SD_TH = 0x152 (150 deg.).

In case TOUTn_OT_WR_TH = 0x00 or TOUTn_OT_SD_TH = 0x000 the related temperature monitor functions are disabled and no detection is performed.

The absolute value of the maximum input voltage slew rate detectable by TOUT monitor is given by TOUT_adc_lsb/TOUT_adc_latency.

Figure 43. Output stage temperature monitor timing diagram

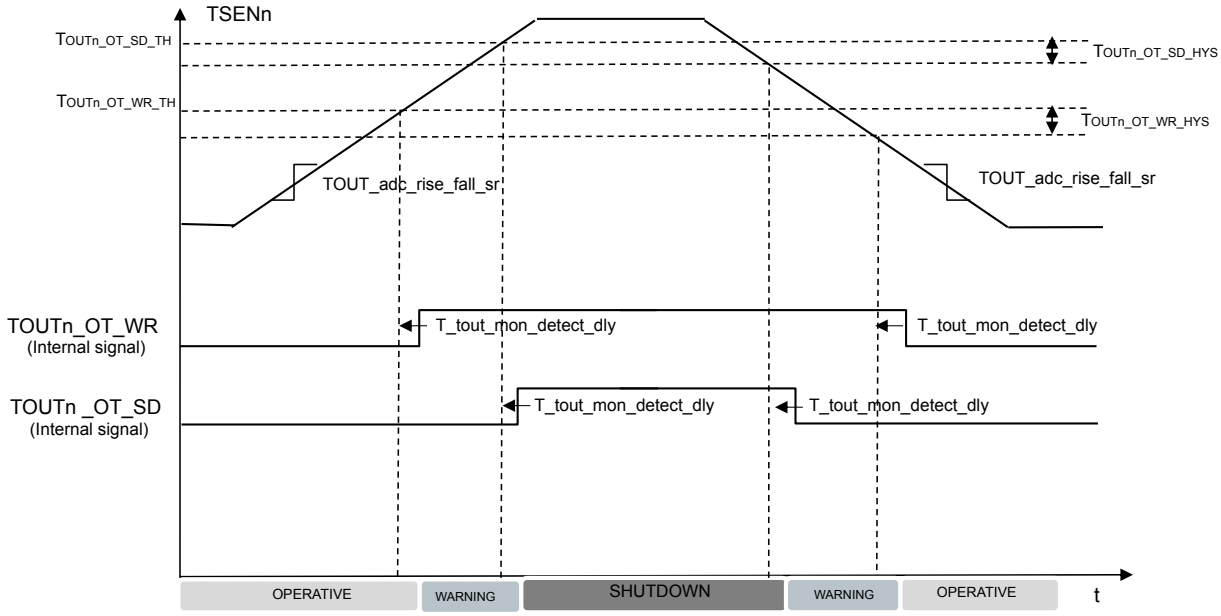


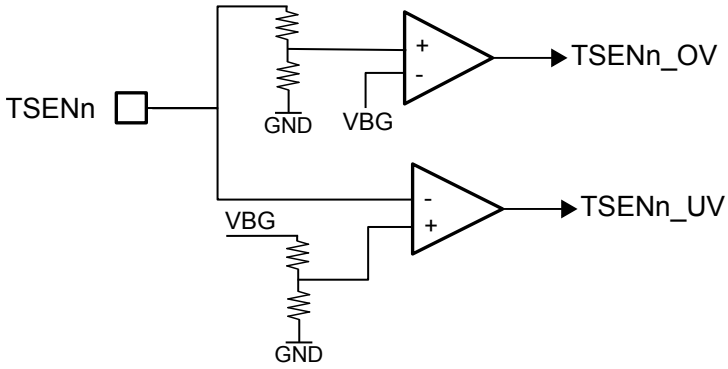
Table 45. TOUT monitor electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
TOUT_MON_th_lsb	TOUT monitoring threshold step		-	5.33	-	mV	Application information
TOUT_MON_th_hyst	TOUT monitoring hysteresis		-	42.64	-	mV	Application information
TOUT_MON_th_range	TOUT monitoring threshold range		0.1	-	2.7	V	Application information
T_tout_mon_detect_dly	TOUT monitoring detection delay	CLK_SSM_EN = 0	-	65	100	µs	Application information

3.12.1.2 *TSEN voltage monitor*

TSENn voltage level is monitored by means of dedicated UV and OV diagnosis.

Figure 44. TSEN voltage monitor simplified block diagram



If TSENn ≤ TSEN_uv_th occurs for an interval longer than T_tsen_uv_flt, the flag TSENn_UV flag is set. Fault pins and safe state activation depends on FHC configuration. TSENn_UV clearing depend on FHC configuration [n = 1, 2].

If TSENn ≥ TSENn_ov_th occurs for an interval longer than T_tsen_ov_flt, the flag TSENn_OV flag is set. Fault pins and safe state activation depends on FHC configuration. TSENn_OV clearing depend on FHC configuration [n = 1, 2].

TSEN monitor is safety relevant and then a self-check procedure is implemented.

Figure 45. TSEN voltage monitor timing diagram

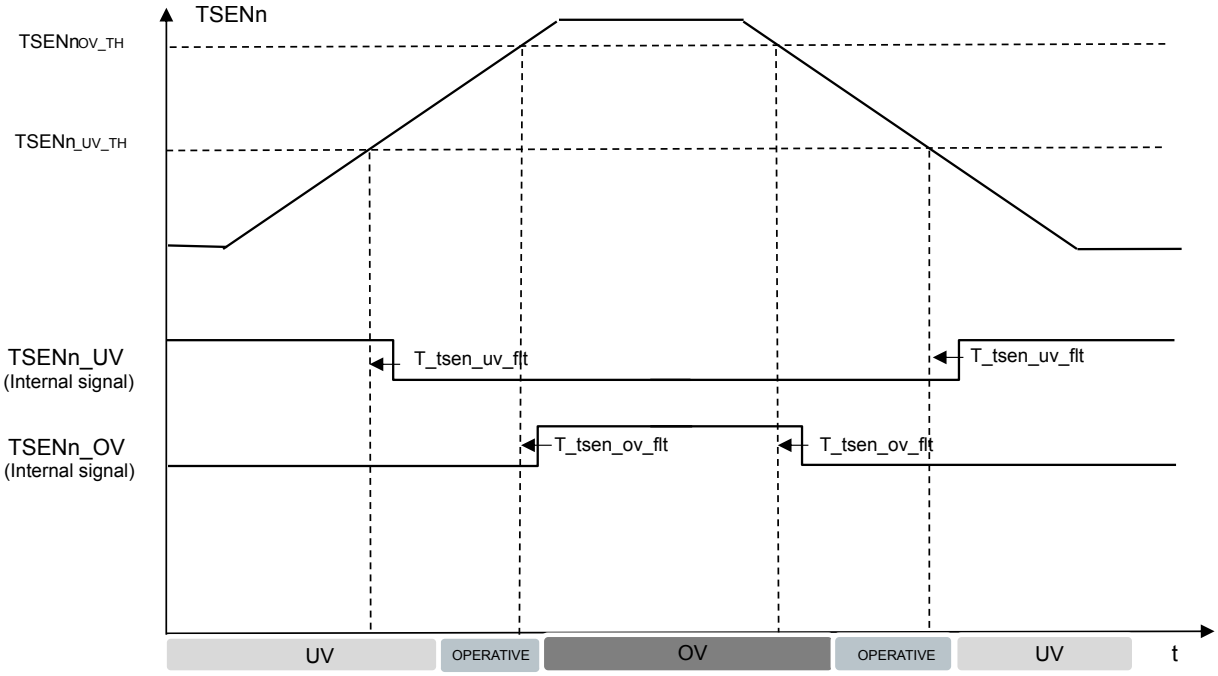


Table 46. TSEN voltage monitor electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
TSEN_uv_th	TSEN undervoltage threshold		0.18	0.2	0.21	V	Comparator output Low to high
TSEN _uv_hys	TSEN undervoltage hysteresis		-	0	-	mV	-

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
TSEN_ov_th	TSEN overvoltage threshold		2.85	3	3.15	V	Comparator output Low to high
TSEN _ov_hys	TSEN overvoltage hysteresis		-	0	-	mV	-
T_tsen_uv_flt	TSEN undervoltage detection filter time	CLK_SSM_EN = 0	75	-	100	µs	Digital filter
T_ tsen _ov_flt	TSEN overvoltage detection filter time	CLK_SSM_EN = 0	75	-	100	µs	Digital filter

3.12.2 Output voltage telemetry

The regulated output voltage of each loop is directly measured across input pins VSENn and VRTNn by means of a dedicated 12-bit ADC converter. The digitized voltage information is made available on PMBus™ paged register READ_VOUTn<15:0> [n=1, 2].

Table 47. Output voltage ADC electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
ADC input							
VOUT_adc_range	VOUT ADC voltage input range		0	-	3.5	V	-
ADC input Resolution							
VOUT_adc_resolution	VOUT ADC resolution		-	12	-	bits	Application information
VOUT_adc_lsb	VOUT ADC LSB		-	0.952	-	mV	Application information
ADC input accuracy							
VOUT_adc_total_err1	VOUT ADC total error1	0.5 V ≤ VID < 1.5 V	-10	-	10	mV	-
VOUT_adc_total_err2	VOUT ADC total error2	1.5 V ≤ VID < 3.5 V	-1	-	1	%	-
ADC input dynamic characteristics							
VOUT_adc_in_sr	VOUT ADC sample rate	CLK_SSM_EN = 0	-	10	-	MHz	Application information
VOUT_adc_latency	VOUT ADC conversion latency	CLK_SSM_EN = 0	-	65	100	µs	Application information

3.12.2.1 Output voltage monitor (VOUT monitor)

The regulated output voltage level of each loop is monitored by means of dedicated UV and an OV diagnosis based on VOUTn conversion [n = 1, 2].

If VSENn-VRTNn ≤ VOUTn_uv_th occurs for an interval longer than T_vout_mon_detect_dly, fault is asserted and the VOUTn_UV flag is set. Fault pins are asserted LOW according to FHC configuration and FOR table [n = 1, 2].

If VSENn-VRTNn ≥ VOUTn_ov_th occurs for an interval longer than T_vout_mon_detect_dly fault is asserted and the VOUTn_OV flag is set. Fault pins are asserted LOW according to the FHC configuration and FOR table. VOUT_OV clearing depends on FHC configuration [n = 1, 2].

The reference thresholds for the VOUTn monitor unit VOUTn_uv_th and VOUT_ov_th can be separately configured through a dedicated PMBus™ register as follows:

$$VOUTn_{UV_{TH}} = VOUT_{MON_{th_{lsb}}} \times VOUTn_{UV_{FAULT_{LIMIT}[8:0]}} \quad (12)$$

$$VOUTn_{OV_{TH}} = VOUT_{MON_{th_{lsb}}} \times VOUTn_{OV_{FAULT_{LIMIT}[8:0]}} \quad (13)$$

Where:

VOUT_MON_th_lsb is the minimum voltage step [7.616 mV].

VOUTn_UV_FAULT_LIMIT/VOUTn_FAULT_LIMIT[8:0] are the dedicated PMBus™ configuration bits [0 V ~ 3.5 V].

The default value is VOUTn_UV_FAULT_LIMIT = 0x058 (670 mV).

The default value is VOUTn_OV_FAULT_LIMIT = 0x06D (830 mV).

In case VOUTn_UV_FAULT_LIMIT = 0x000 the related voltage monitor function is disabled and no detection is performed.

In case VOUTn_OV_FAULT_LIMIT = 0x000 the related voltage monitor function is disabled and no detection is performed.

The absolute value of the maximum input voltage slew rate detectable by VOUT monitor is given by VOUT_adc_lsb/VOUT_adc_latency.

Figure 46. Output voltage monitor timing diagram

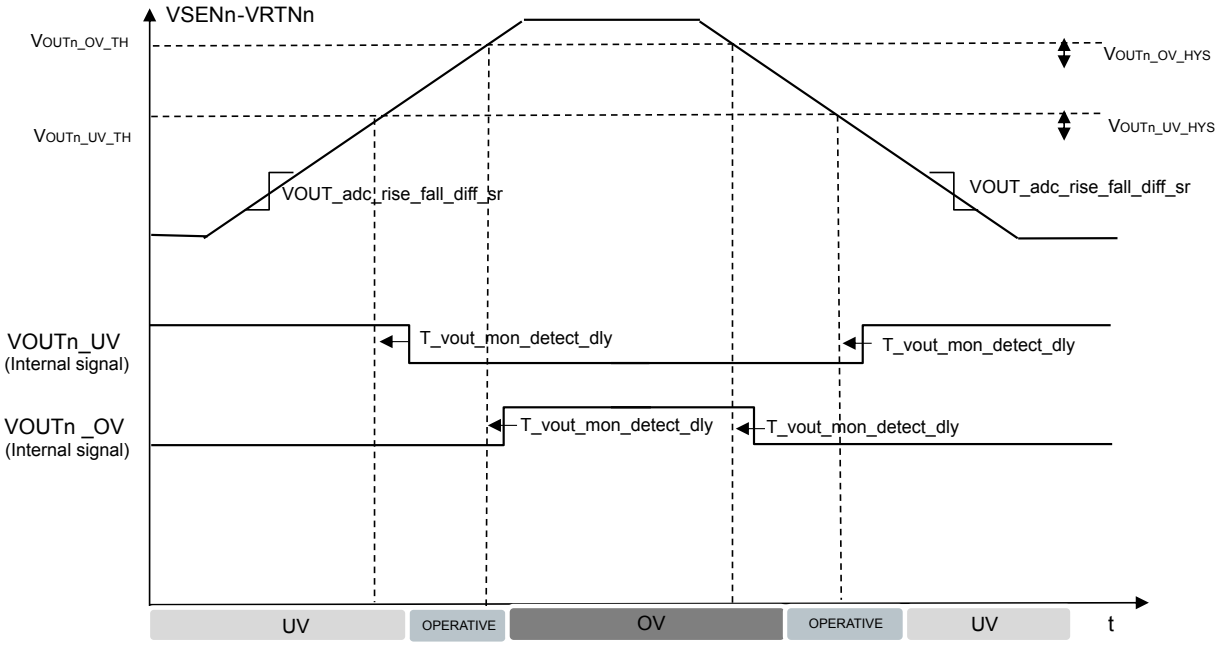


Table 48. VOUT monitor electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
VOUT_MON_th_lsb	VOUT monitoring threshold step		-	7.616	-	mV	Application information
VOUT_MON_th_range	VOUT monitoring threshold range		0	-	3.5	V	Application information
T_vout_mon_detect_dly	VOUT monitoring detection delay	CLK_SSM_EN = 0	-	65	100	µs	Application information

3.12.3 Output current telemetry

Current of each phase is directly measured across input pins ISENn and CFILT/VREF1 by means of a dedicated 11-bit ADC converter. The digitized voltage information is made available on PMBus™ register MFR_READ_IOUTn [n = 1, 2, 3, 4, 5, 6, 7, 8] for the single phase current and on the paged register READ_IOUTm<15:0> [m = 1, 2] for the sum current on each loop.

Output stage telemetry ADC and the related monitoring unit design are based on the following DrMOS current sense output characteristics:

Figure 47. **DrMOS current sense output reference characteristic**

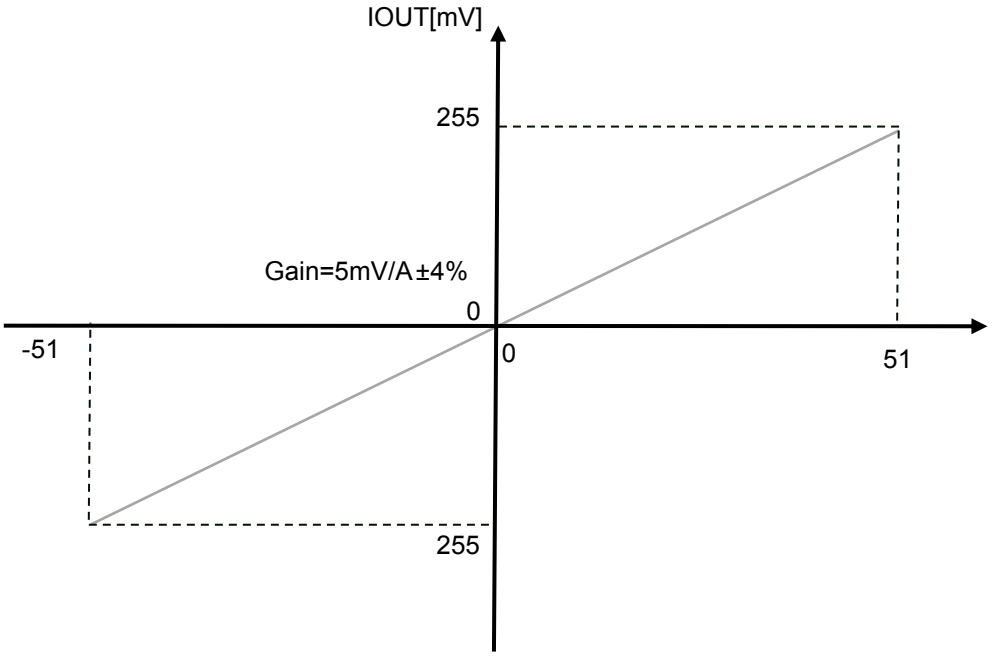


Table 49. **Phase current ADC electrical characteristics**

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
ADC input							
IOUT_adc_range	IOUT ADC voltage input range		-255	-	255	mV	-
ADC input resolution							
IOUT_adc_resolution	IOUT ADC resolution		-	11	-	bits	Application information
IOUT_adc_lsb	IOUT ADC LSB		-	0.293	-	mV	Application information
ADC input accuracy							
IOUT _adc_gain_err	IOUT ADC gain error		-3	-	3	%	-
IOUT _adc_offset_err	IOUT ADC input referred offset error		-10	-	10	mV	-
IOUT_adc_tot_err	IOUT ADC total error		-	-	-	mV	See note
ADC input dynamic characteristics							
IOUT_adc_in_sr	IOUT ADC sample rate	CLK_SSM_EN = 0	-	10	-	MHz	Application information
IOUT_adc_latency	IOUT ADC conversion latency	CLK_SSM_EN = 0	-	65	100	µs	Application information

Note: IOUT_ADC conversion total error can be calculated as follows:
*IOUT_adc_tot_err = IOUT_adc_gain_err * (ISENn - VREF1/CFILT) + IOUT_adc_offset_err*
Example:

- *| ISENn-VREF1/CFILT | = 100 mV*
- *Total ADC conversion error = ±10 mV ±(3% * 100 mV) = ±10 mV ±3 mV*
- *The value read by PMBus™ has a range between 100 mV - (10 mV + 3 mV) and 100 mV + (10 mV + 3 mV)*

Based on single phase current measurements the sum current for each regulation loop is computed by adding the single converted values. The current sum information is made available on PMBus™ paged register READ_IOUTm [m = 1, 2].

Table 50. Output current sum calculation characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
Current adder output							
IOUT_SUM _range1	IOUT_SUM input range on loop 1		-480	-	480	A	-
IOUT_SUM _range2	IOUT_SUM input range on loop 2		-240	-	240	A	-
Current adder resolution							
IOUT_SUM_resolution	IOUT_SUM computation resolution		-	14	-	bits	Application information
IOUT_SUM_lsb	IOUT_SUM LSB		-	58.6	-	mA	Application information(1)
Current adder accuracy							
IOUT_SUM_adc_tot_err	IOUT_SUM error		-	-	-	mV	(2)
Current adder dynamic characteristics							
IOUT_SUM_latency	IOUT_SUM computation latency	CLK_SSM_EN = 0	-	65	100	µs	Application information

1. *LSB is 0.0586 A, considering DrMOS current gain is 5 mV/A (0.293 mV/5 mV/A = 0.0586 A).*
2. *The total error affecting the READ_IOUTm [m = 1, 2] measurement can be retrieved as the sum of the error affecting the single MFR_READ_IOUTn [n = 1-8] conversion since the digital adder is simply introducing a sum operation on ISENn converted codes.*

$$READ_{IOUTm} = \sum_{i=1}^{N} MFR_{READ_{IOUTi}} = \sum_{i=1}^{N} \frac{1}{\Delta_{IOUT_{adc_{lsb}}}} \left[\left(\left(ISEN_i - \frac{VREF1}{CFILT} \right) (1 \pm G_{err}) \right) \pm V_{OFS} \right] = \sum_{i=1}^{N} \frac{1}{\Delta_{IOUT_{adc_{lsb}}}} \left[\left(ISEN_i - \frac{VREF1}{CFILT} \right) \right] \pm \left(\sum_{i=1}^{N} \frac{1}{\Delta_{IOUT_{adc_{lsb}}}} \left[\left(ISEN_i - \frac{VREF1}{CFILT} \right) G_{err} \right] + \frac{NV_{OFS}}{\Delta_{IOUT_{adc_{lsb}}}} \right) \quad (14)$$

$$READ_{IOUTm}ERROR = \pm \left(\sum_{i=1}^{N} \frac{1}{\Delta_{IOUT_{adc_{lsb}}}} \left[\left(ISEN_i - \frac{VREF1}{CFILT} \right) G_{err} \right] + \frac{NV_{OFS}}{\Delta_{IOUT_{adc_{lsb}}}} \right)$$

Where N is the number of active phases, Δlout_adc_lsb is the phase current ADC lsb, Gerr is the gain error of the single ISEN ADC conversion (3%), Vofs is the offset of the single ISEN ADC conversion (10 mV).

Note: The previous relationship is always true as it refers to the single ISEN ADC voltage conversion (MFR_READ_IOUTn [n = 1~8]) and to their sum (READ_IOUTm [m = 1, 2]). It includes only errors introduced by STPM098C conversion on ISENn. When the LOAD current (in Amps) is to be estimated starting from the READ_IOUTm readout additional error contributions (external to STPM098C) come into play and shall be considered.

DrMOS current sense errors

Between the converter current information and the STPM098C converter, there is the DrMOS current sensing. To retrieve Iload (in Amps) the multiplication by A_{DrMOS} shall be performed.

$$I_{LOAD} = A_{DrMOS} \sum_{i=1}^{N} \frac{1}{\Delta_{IOUT_{adc_{lsb}}}} \left[\left(\left(ISEN_i - \frac{VREF1}{CFILT} \right) (1 \pm G_{err}) \right) \pm V_{OFS} \right] = A_{DrMOS} \sum_{i=1}^{N} \frac{1}{\Delta_{IOUT_{adc_{lsb}}}} \left[\left(ISEN_i - \frac{VREF1}{CFILT} \right) \right] \pm \left(A_{DrMOS} \sum_{i=1}^{N} \frac{1}{\Delta_{IOUT_{adc_{lsb}}}} \left[\left(ISEN_i - \frac{VREF1}{CFILT} \right) G_{err} \right] + \frac{NV_{OFS}}{\Delta_{IOUT_{adc_{lsb}}}} \right) \quad (15)$$

Following:

$$I_{LOAD} = \left(A_{DrMOS} \pm A_{CC_{ALL}}\right) \sum_{i=1}^{N} \frac{1}{\Delta_{IOUT_{adc_{lsb}}}} \left[\left(\left(ISEN_i - \frac{VREF1}{CFILT}\right)(1 \pm G_{err})\right) \pm V_{OFS}\right]$$

$$= A_{DrMOS} \sum_{i=1}^{N} \frac{1}{\Delta_{IOUT_{adc_{lsb}}}} \left[\left(ISEN_i - \frac{VREF1}{CFILT}\right)\right] \pm \left(A_{CC_{ALL}} \sum_{i=1}^{N} \frac{1}{\Delta_{IOUT_{adc_{lsb}}}} \left[\left(ISEN_i - \frac{VREF1}{CFILT}\right)\right] + \left(A_{DrMOS} + A_{CC_{ALL}}\right) \sum_{i=1}^{N} \frac{1}{\Delta_{IOUT_{adc_{lsb}}}} \left[\left(ISEN_i - \frac{VREF1}{CFILT}\right)G_{err}\right] + \frac{NV_{OFS}}{\Delta_{IOUT_{adc_{lsb}}}}\right)$$

$$I_{LOAD}ERROR = \pm\left(A_{CC_{ALL}} \sum_{i=1}^{N} \frac{1}{\Delta_{IOUT_{adc_{lsb}}}} \left[\left(ISEN_i - \frac{VREF1}{CFILT}\right)\right] + \left(A_{DrMOS} + A_{CC_{ALL}}\right) \sum_{i=1}^{N} \frac{1}{\Delta_{IOUT_{adc_{lsb}}}} \left[\left(ISEN_i - \frac{VREF1}{CFILT}\right)G_{err}\right] + \frac{NV_{OFS}}{\Delta_{IOUT_{adc_{lsb}}}}\right) \quad (16)$$

3.12.3.1 *Output current monitor (IOUT monitor)*

Single phase and sum current levels are monitored by means of a multiple sets of dedicated diagnosis.

Single phase undercurrent diagnosis (phase fault)

A dedicated UC monitoring on single phase current conversion is performed to detect the condition.

If |ISENn-CFILT/VREF1| ≤ IOUTm_uc_th occurs for an interval longer than T_iout_uc_detect_dly, the IOUTn_UC flag is set and SAFE_HIZ is established. Fault pins are asserted LOW according to FHC configuration and FOR table [n = 1, 2, 3, 4, 5, 6, 7, 8] and [m = 1, 2].

The reference thresholds for the IOUTn undercurrent monitor unit IOUTn_uc_th can be separately configured for loop 1 and 2 through dedicated PMBus™ registers as follows:

$$IOUTm_{UC_{TH}} = IOUT_{MON_{UC_{th_{lsb}}}} \times IOUTm_{UC_{FAULT_{LIMIT}[7:0]}} \quad (17)$$

Where:

IOUT_MON_UC_th_lsb is the minimum voltage step [0.293 mV].

IOUTm_UC_FAULT_LIMIT [7:0] is the dedicated PMBus™ configuration bits [0 ~ 75 mV].

The default value is IOUTm_UC_ FAULT_LIMIT = 0x33 (15 mV).

In the case IOUTm_UC_ FAULT_LIMIT = 0x00 the related undercurrent monitor function is disabled, and no detection is performed.

The absolute value of the maximum input voltage slew rate detectable by the IOUT monitor is given by IOUT_adc_lsb/IOUT_adc_latency.

Figure 48. Output undercurrent monitor timing - Diagram 1

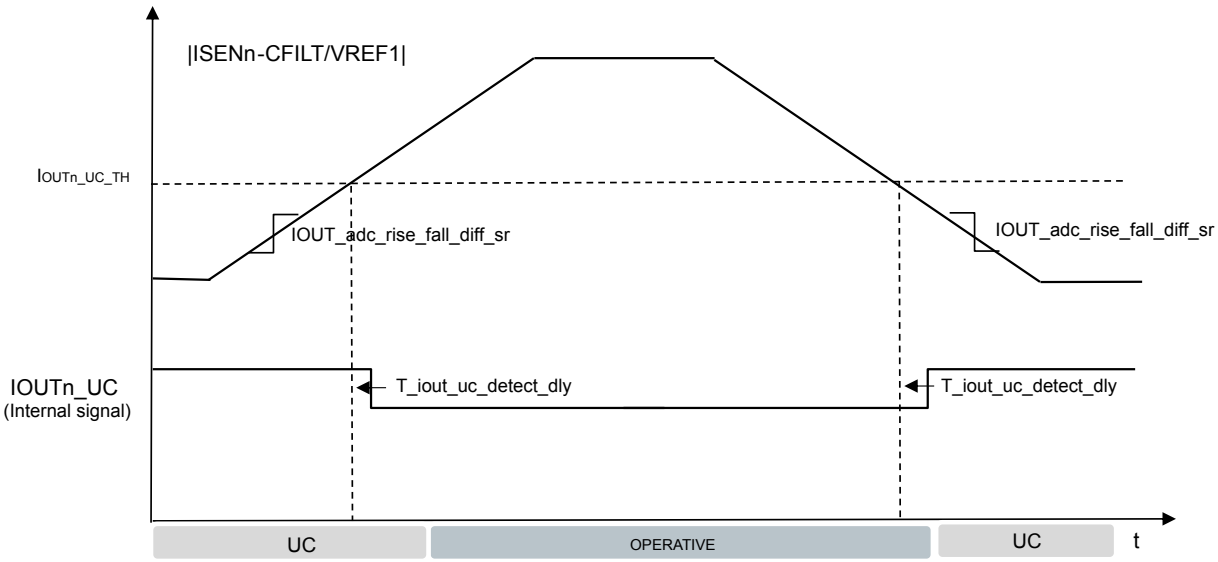


Figure 49. **Output undercurrent monitor timing - Diagram 2**

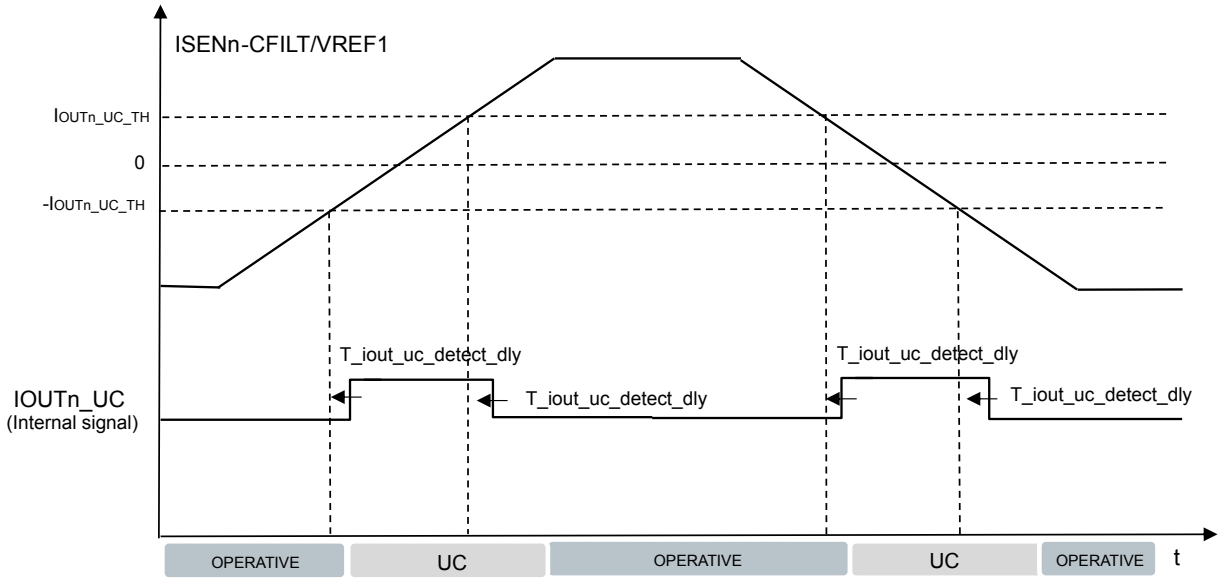
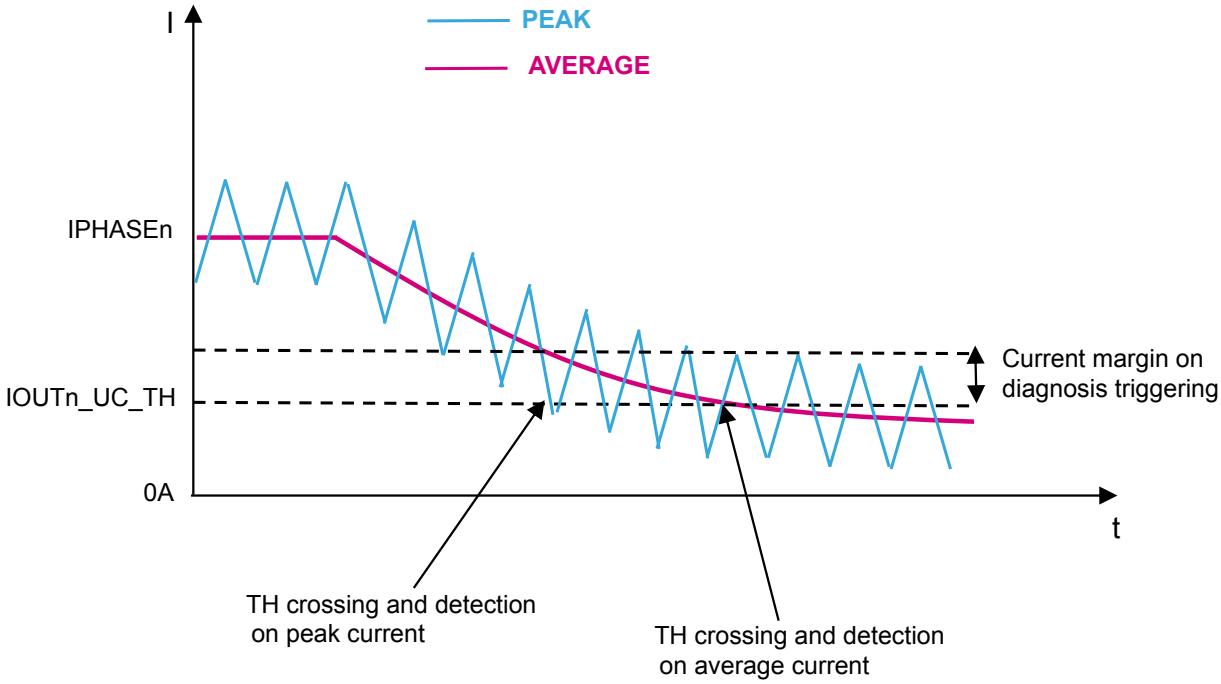


Table 51. **IOUT undercurrent monitor electrical characteristics**

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
IOUT_MON_UC_th_lsb	IOUT UC monitoring threshold step		-	0.293	-	mV	Application information
IOUT_MON_UC_th_range	IOUT UC monitoring threshold range		0.293	-	75	mV	Application information
T_iout_uc_detect_dly	IOUT UC monitoring detection delay	CLK_SSM_EN = 0	-	65	100	µs	Application information

A proper configuration of phase UC thresholds and FHC for the single phase shall be chosen to avoid protection triggering during light load operations.

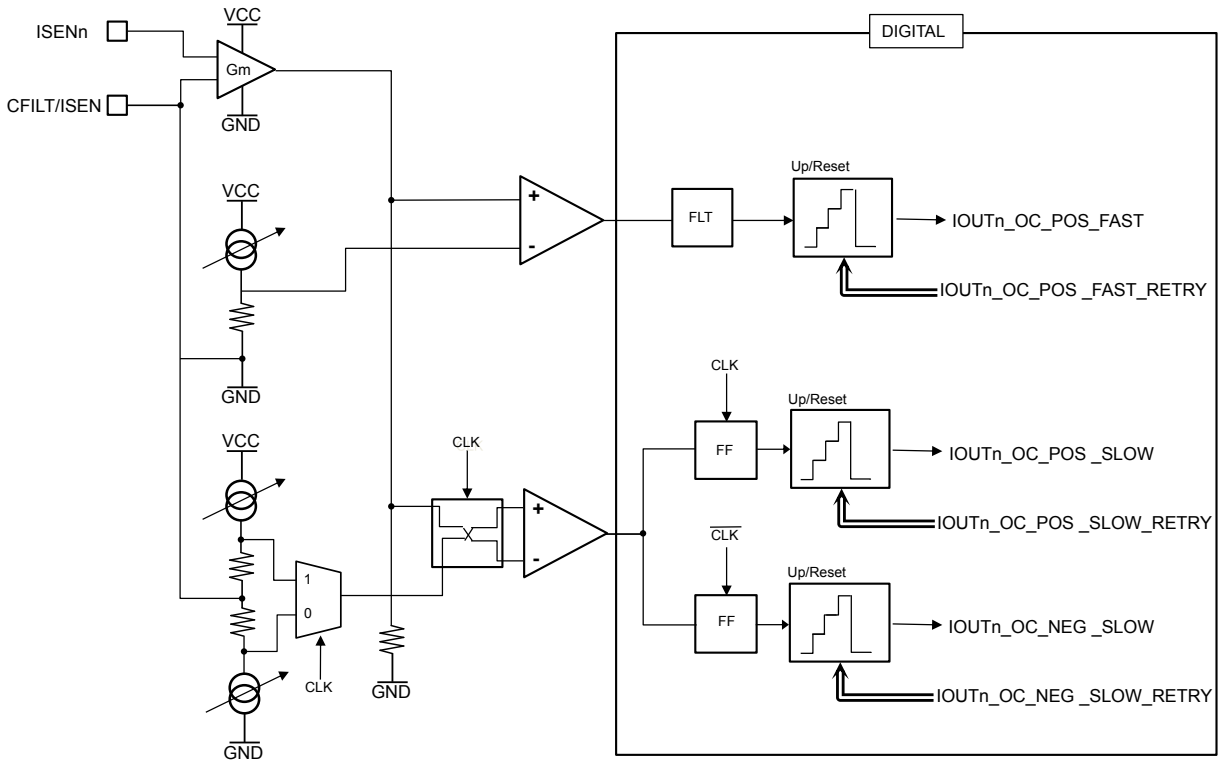
Figure 50. **Output undercurrent monitor timing - Diagram 3**



Single phase overcurrent diagnosis

A dedicated OC monitoring on single phase current is performed by means of a dedicated analog comparator set.

Figure 51. **Single phase overcurrent simplified block diagram**



If ISENn-CFILT/VREF1 ≥ IOUTm_oc_pos_slow_th occurs IOUTm_oc_pos_slow_retry times consecutively, the IOUTn_OC_POS_SLOW flag is set. Fault pins and safe state activation depend on FHC configuration. IOUTn_OC_POS_SLOW clearing depends on FHC configuration [n = 1, 2, 3, 4, 5, 6, 7, 8] and [m = 1, 2].

If ISENn-CFILT/VREF1 ≥ IOUTm_oc_pos_fast_th occurs IOUTm_oc_pos_fast_retry times consecutively, the IOUTn_OC_POS_FAST flag is set. Fault pins and safe state activation depend on FHC configuration. IOUTn_OC_POS_FAST clearing depends on FHC configuration [n = 1, 2, 3, 4, 5, 6, 7, 8] and [m = 1, 2].

If ISENn-CFILT/VREF1 ≤ -IOUTm_oc_neg_slow_th occurs IOUTm_oc_neg_slow_retry times consecutively, the IOUTn_OC_NEG_SLOW flag is set. Fault pins and safe state activation depend on FHC configuration. IOUTn_OC_NEG_SLOW clearing depends on FHC configuration [n = 1, 2, 3, 4, 5, 6, 7, 8] and [m = 1, 2].

Where *m* is the loop reference.

Single-phase overcurrent comparators are safety relevant and then a self-check procedure is implemented.

The reference thresholds for the IOUTn overcurrent monitor unit IOUTm_oc_pos_slow_th, IOUTm_oc_neg_slow_th and IOUTm_oc_pos_fast_th can be separately configured for loop 1 and 2 through dedicated PMBus™ register as follows:

$$IOUTm_{OC_{POS_{SLOW_{TH}}}} = IOUT_{MON_{OC_{th_{lsb}}}} \times IOUTm_{OC_{POS_{SLOW_{TH}[9:0]}}} \quad (18)$$

$$IOUTm_{OC_{POS_{FAST_{TH}}}} = IOUT_{MON_{OC_{th_{lsb}}}} \times IOUTm_{OC_{POS_{FAST_{TH}[9:0]}}} \quad (19)$$

$$IOUTm_{OC_{NEG_{SLOW_{TH}}}} = IOUT_{MON_{OC_{th_{lsb}}}} \times IOUTm_{OC_{NEG_{SLOW_{TH}[9:0]}}} \quad (20)$$

Where:

IOUT_MON_OC_th_lsb is the minimum voltage step.

IOUTm_OC_POS_SLOW_TH, IOUTm_OC_POS_FAST_TH and IOUTm_OC_NEG_SLOW_TH, are the dedicated PMBus™ configuration bits.

Note: For a correct functionality of the single phase FAST overcurrent diagnosis, the following relationship must be fulfilled under every system condition:

$$ISENn - \frac{VREF1}{CFILT} - IOUTm_{OC_{POS_{FAST_{TH}}}} < 125\,mV$$

[n = 1, 2, 3, 4, 5, 6, 7, 8]

A correct single-phase FAST overcurrent operation is not guaranteed when the previous relationship is not guaranteed.

Example:

ISENn maximum value (maximum DrMOS current monitor output) = 2.055 V; then IOUTm_OC_POS_FAST_TH = 130 mV (2.055 V ~ 1.8 V ~ 125 mV) is the minimum valid threshold to get correct diagnosis operation.

Default values are:

IOUTm_OC_POS_SLOW_TH = 0x348 (210 mV, 42 A)

IOUTm_OC_POS_FAST_TH = 0x384 (225 mV, 45 A)

IOUTm_OC_NEG_SLOW_TH = 0x348 (210 mV, 42 A)

In case any of the above listed thresholds is 0, the related overcurrent monitor function is disabled and no detection is performed.

The reference retry times for the IOUTn overcurrent monitor unit IOUTm_oc_pos_slow_retry, IOUTm_oc_neg_slow_ retry and IOUTm_oc_pos_fast_retry can be separately configured for loop 1 and 2 through dedicated PMBus™ registers as follows:

$$IOUTm_{OC_{POS_{SLOW_{RETRY}}}} = IOUT_{MON_{OC_{retry_{lsb}}}} \times IOUTm_{OC_{POS_{SLOW_{RETRY}[9:0]}}} \quad (21)$$

$$IOUTm_{OC_{POS_{SFAST_{RETRY}}}} = IOUT_{MON_{OC_{retry_{lsb}}}} \times IOUTm_{OC_{POS_{FAST_{RETRY}[9:0]}}} \quad (22)$$

$$IOUTm_{OC_{NEG_{SLOW_{RETRY}}}} = IOUT_{MON_{OC_{retry_{lsb}}}} \times IOUTm_{OC_{NEG_{SLOW_{RETRY}[9:0]}}} \quad (23)$$

Where:

IOUT_MON_OC_retry_lsb is the minimum step.

IOUTm_OC_POS_SLOW/FAST_RETRY and IOUTm_OC_NEG_SLOW_RETRY[7:0] are the dedicated PMBus™ configuration bits.

Default values are:

IOUTn_OC_POS_SLOW_RETRY = 0x80 (128)

IOUTm_OC_POS_FAST_RETRY = 0x01 (1)

IOUTn_OC_NEG_SLOW_RETRY = 0x80 (128)

The correct operation of single phase overcurrent monitor stage is safety relevant and then a self-check procedure is implemented.

Figure 52. Single phase positive over-current monitor timing diagram - SLOW_RETRY = 5, FAST_RETRY = 5

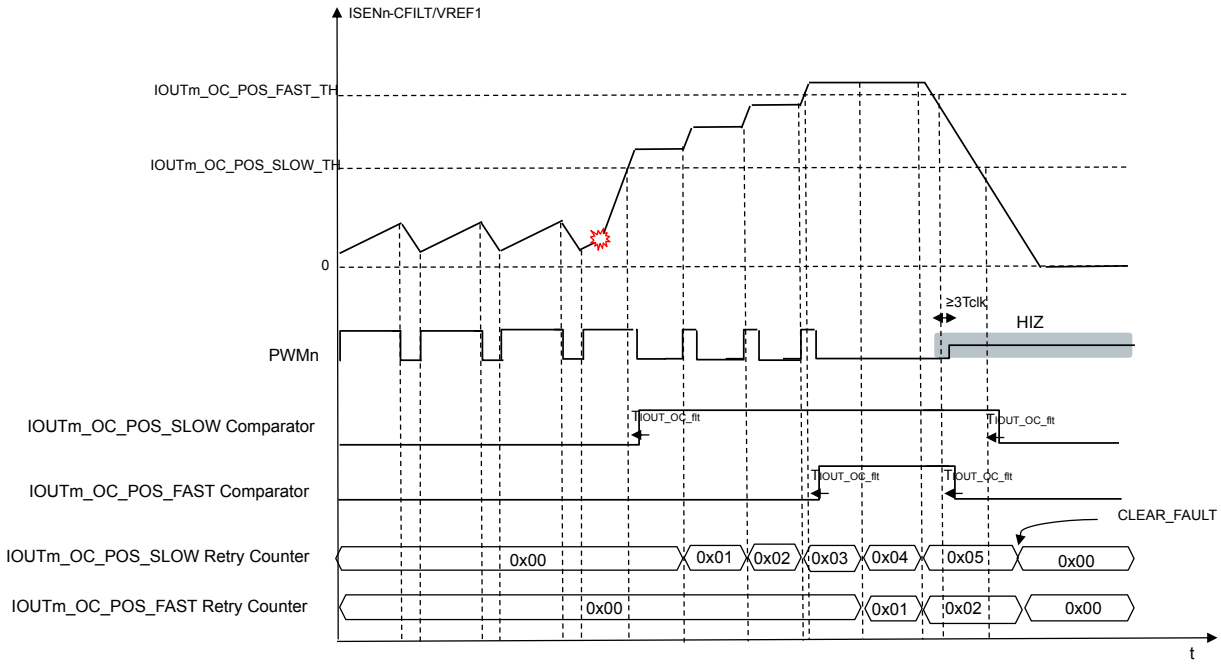


Figure 53. Single phase positive over-current monitor timing diagram - SLOW_RETRY = 5, FAST_RETRY = 1

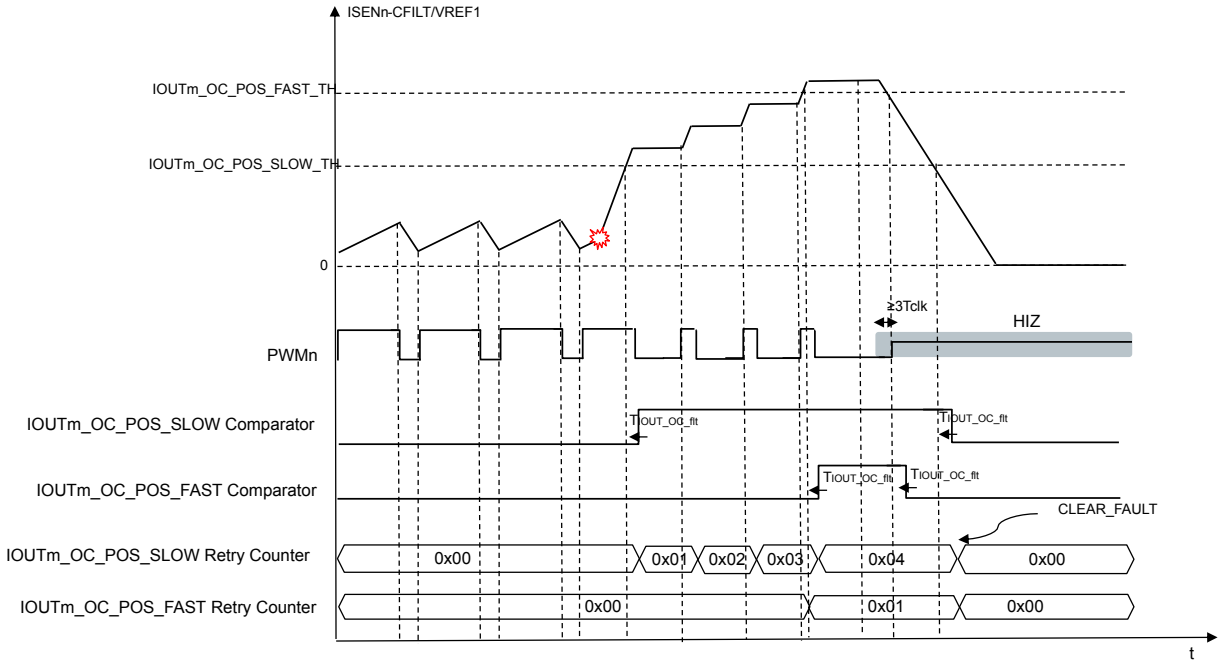


Figure 54. **Single phase negative over-current monitor timing diagram - SLOW_RETRY = 1**

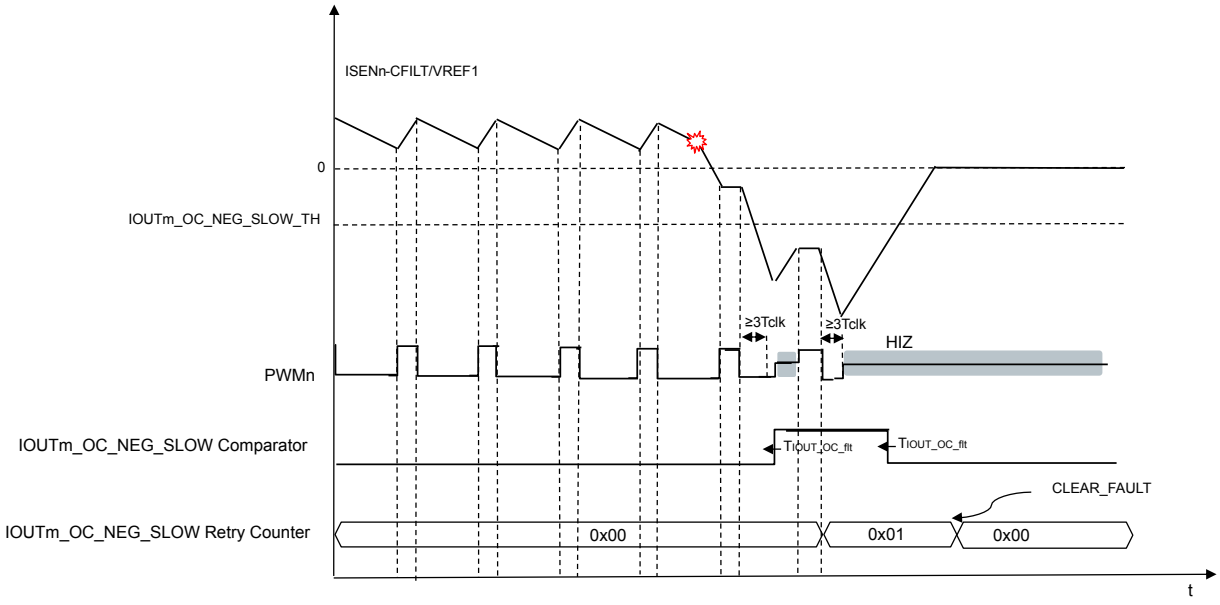


Table 52. **IOUT single phase overcurrent monitor electrical characteristics**

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
IOUT_MON_OC_th_lsb	IOUT OC monitoring threshold step		-	0.25	-	mV	Application information
IOUT_MON_OC_th_range	IOUT OC monitoring threshold range		-255	-	255	mV	Application information
T_iout_oc_flt	IOUT OC switch-off reaction time		-	-	1	µs	Analog delay
T_iout_fast_oc_dly1	IOUT FAST OC switch-off reaction time1	d(ISENn - VREF1/CFILT)/dt ≥ 0.5 V/µs IOUTm_oc_pos_fast_retr = 0x0 SLOW_FAST_OC_PATH = 0x2	-	-	260	ns	POC FAST Guaranteed by design
T_iout_fast_oc_dly2	IOUT FAST OC switch-off reaction time2	d(ISENn - VREF1/CFILT)/dt ≥ 0.5 V/µs IOUTm_oc_pos_fast_retr = 0x1 SLOW_FAST_OC_PATH = 0x2	-	-	245	ns	POC FAST Guaranteed by design
T_iout_fast_oc_dly3	IOUT FAST OC switch-off reaction time3	d(ISENn - VREF1/CFILT)/dt ≥ 0.5 V/µs IOUTm_oc_pos_fast_retr = 0x0 SLOW_FAST_OC_PATH = 0x5	-	-	185	ns	POC FAST Guaranteed by design
T_iout_fast_oc_dly4	IOUT FAST OC switch-off reaction time4	d(ISENn - VREF1/CFILT)/dt ≥ 0.5 V/µs IOUTm_oc_pos_fast_retr = 0x1 SLOW_FAST_OC_PATH = 0x5	-	-	170	ns	POC FAST Guaranteed by design

Single phase current overbalance

A dedicated monitor compares the single active phase current with the average current of the respective loop to detect excessive unbalancing of phase current. Hysteresis on thresholds and filtering time are implemented.

If the current read on a phase differs from the average of all phases current readings by more than a threshold value, then a dedicated error flag is raised.

(24)

If $\left|\left(ISEN_i - CFILT_{VREF1}\right) - \frac{1}{m}\sum_{j=1}^{m}\left(ISEN_j - CFILT_{VREF1}\right)\right|$ ≥ IOUTn_sharing_wr_th, the IOUTn_SHARING_WR flag is set.

Where m is the number of active phases for the specific loop.

The reference thresholds for the IOUTn overbalance monitor unit IOUTn_sharing_wr_th can be separately configured for loop 1 and 2 through a dedicated PMBus™ register as follows:

$$IOUTn_{SHARING_{WR_{TH}}} = IOUT_{MON_{UMB_{th_{lsb}}}} \times IOUTn_{SHARING_{WR_{TH}[5:0]}}$$

Where:

IOUT_MON_UMB_th_lsb is the minimum voltage step [0.94 A].

IOUTn_SHARING_WR_TH [5:0] are the dedicated PMBus™ configuration bits.

The default value is IOUTn_SHARING_WR_TH = 0x03.

In case IOUTm_SHARING_WR_TH = 0x00, the related overcurrent monitor function is disabled and no detection is performed.

The absolute value of the maximum input voltage slew rate detectable by IOUT monitor is given by IOUT_adc_lsb/IOUT_adc_latency.

Figure 55. Phase current overbalance timing diagram

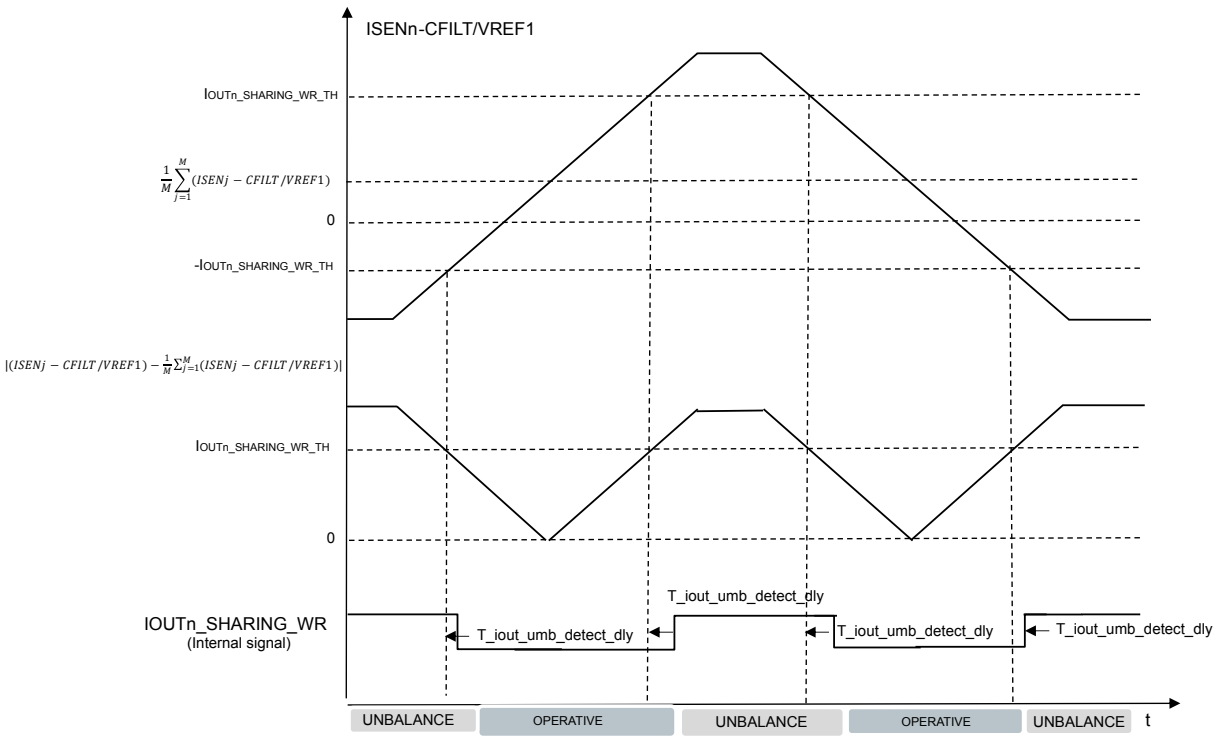


Table 53. **IOUT overbalancing monitor electrical characteristics**

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
IOUT_MON_UMB_th_lsb	IOUT UMB monitoring threshold step		-	0.94	-	A	Application information
IOUT_MON_UMB_th_range	IOUT UMB monitoring threshold range		0.94	-	29.14	A	Application information
T_iout_umb_detect_dly	IOUT UMB monitoring detection delay	CLK_SSM_EN = 0	-	65	100	µs	Application information

Current sum overcurrent diagnosis

A dedicated OC monitoring on the phase current sum of each loop is performed. This diagnosis is based upon the sum of converted current information of all phases referred to the specific loop.

If $\sum_{j=1}^{m}\left(ISEN_j - \frac{CFILT}{VREF1}\right) \geq$ IOUTn_oc_sum_th occurs IOUTm_sum_retry times, the IOUTn _OC_SUM flag is set. [n = 1, 2].

The reference thresholds for the IOUTn overcurrent monitor unit IOUTn_oc_sum_th can be separately configured for loop 1 and 2 through a dedicated PMBus™ register as follows:

$$IOUTn_{OC_{SUM_{TH}}} = IOUT_{MON_{OC_{SUM_{th_{lsb}}}}} \times IOUTn_{OC_{SUM_{TH}[7:0]}} \quad (25)$$

Where:

IOUT_MON_OC_SUM_th_lsb is the minimum voltage step [0.94 A].

IOUTn _OC_FAULT_LIMIT[7:0] are the dedicated PMBus™ configuration bits. [0 ~ 239.7A].

Default value is IOUTn_OC_SUM_TH = 0xBF (180 A) for loop 1 and 0x35 (50 A) for loop 2.

In case IOUTn_OC_SUM_TH = 0x00 the related overcurrent monitor function is disabled and no detection is performed.

The reference retry times for the IOUTn_SUM overcurrent monitor unit IOUTn_oc_sum_retry can be separately configured for loop 1 and 2 through a dedicated PMBus™ register as follows:

$$IOUTm_{OC_{SUM_{RETRY}}} = IOUT_{MON_{OC_{SUM_{retry_{lsb}}}}} \times IOUTm_{OC_{SUM_{RETRY}[7:0]}} \quad (26)$$

Where:

IOUT_MON_OC_SUM_retry_lsb is the minimum step.

IOUTm_OC_SUM_RETRY [7:0] are the dedicated PMBus™ configuration bits.

The default value is IOUTm_OC_SUM_RETRY = 0x05.

The absolute value of the maximum input voltage slew rate detectable by IOUT monitor is given by IOUT_adc_lsb/IOUT_adc_latency.

Figure 56. **Current sum overcurrent timing diagram**

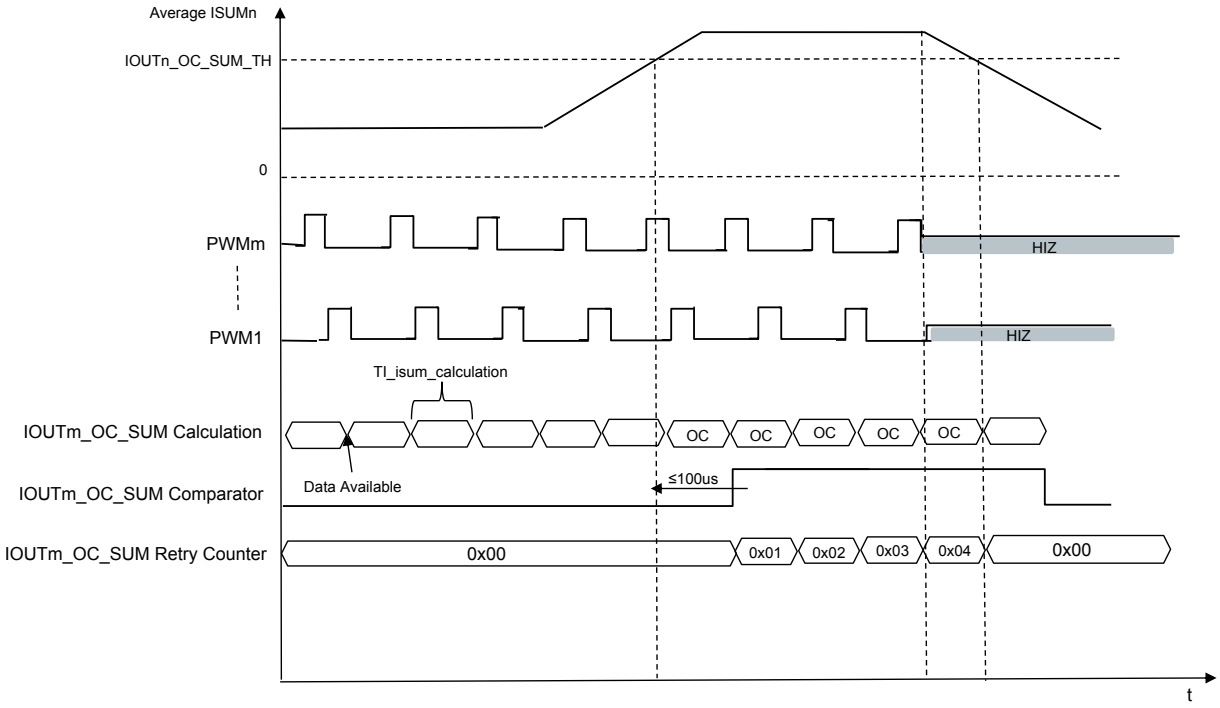


Table 54. **IOUT sum overcurrent monitor electrical characteristics**

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
IOUT_MON_OC_SUM_th_retry_lsb	IOUT OC SUM monitoring threshold step(1)		-	0.293	-	A	Application information
IOUT_MON_OC_SUM_th_range	IOUT OC SUM monitoring threshold range		0	-	239.7	A	Application information
T_iout_umb_detect_dly	IOUT OC SUM monitoring detection delay	CLK_SSM_EN = 0	-	65	100	µs	Application information

1. *IOUTn_oc_sum_th<7:0> LSB: is 0.9376 A considering DrMOS current gain 5 mV/A, it corresponds to 16 READ_IOUTm LSB (0.293 mV * 16 = 4.688 mV, using 5 mV/A DrMOS current gain becomes 0.9376 A).*

3.13 Feedback disconnection monitor (FDM)

STPM098C implements a dedicated diagnosis at both voltage sensing terminals (VSENn, VRTNn) of each control loop to detect feedback disconnection events before regulation startup. The FDM diagnosis unit is composed by a force stage and a monitor stage. The force stage has the purpose of weakly pulling up the voltage of VSENn and VRTNn terminals up to VCC.

If VSENn ≥ VFB_DISC_TH occurs for an interval longer than T_vfb_disc_flt after a T_vfb_dics_blank, FB_DISC flag is set and SAFE_HIZ is established. The error flag remains set until the failure condition is removed and a rising edge on VRn_EN [n = 1, 2] is detected.

If VRTNn ≥ VFB_DISC_TH occurs for an interval longer than T_vfb_disc_flt after a T_vfb_dics_blank, FB_DISC_RTN flag is set and SAFE_HIZ is established. The error flag remains set until the failure condition is removed and a rising edge on VRn_EN [n = 1, 2] is detected.

The FDM is safety relevant and then a self-check procedure is implemented.

Figure 57. **Feedback disconnection simplified block diagram**

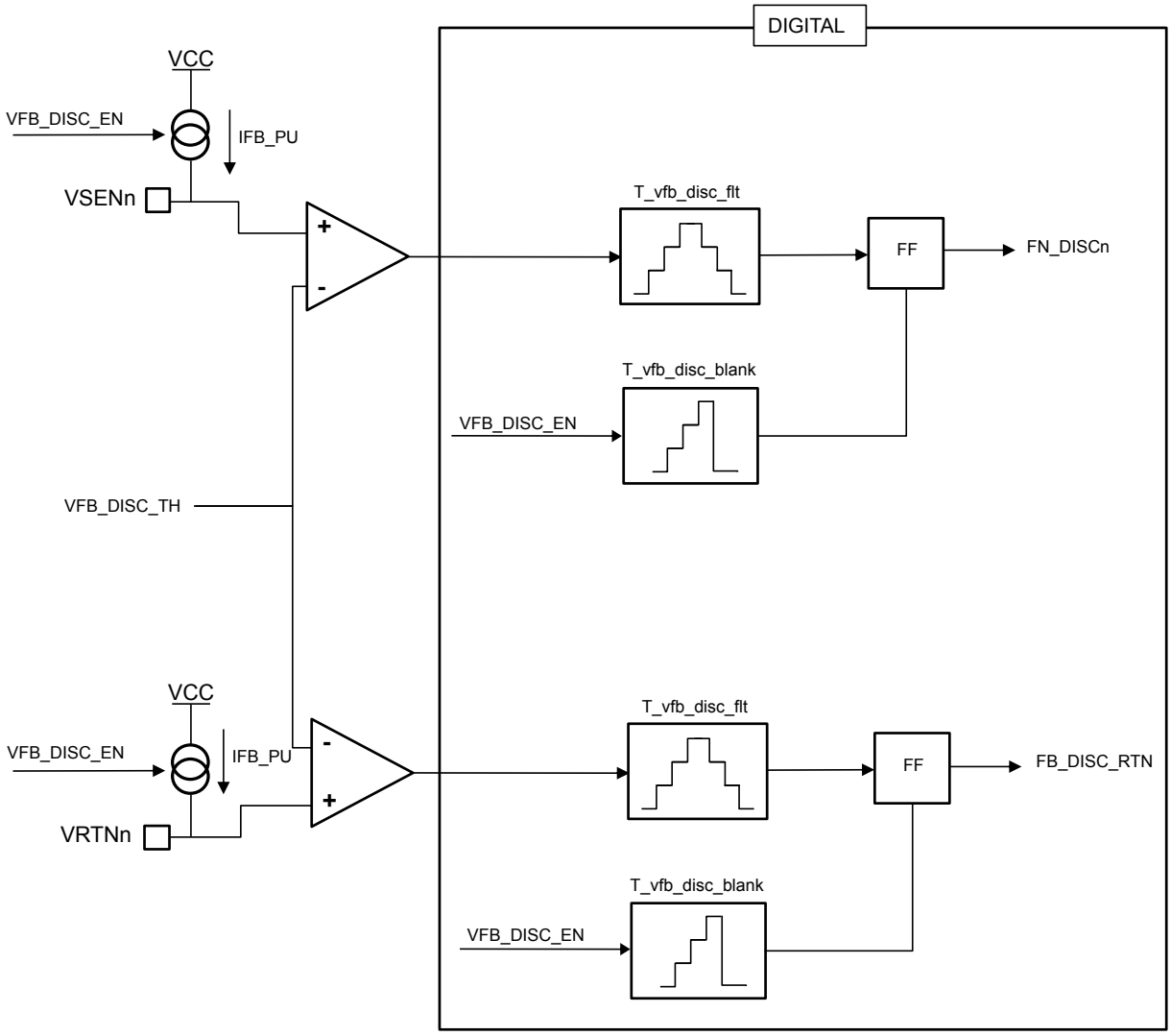
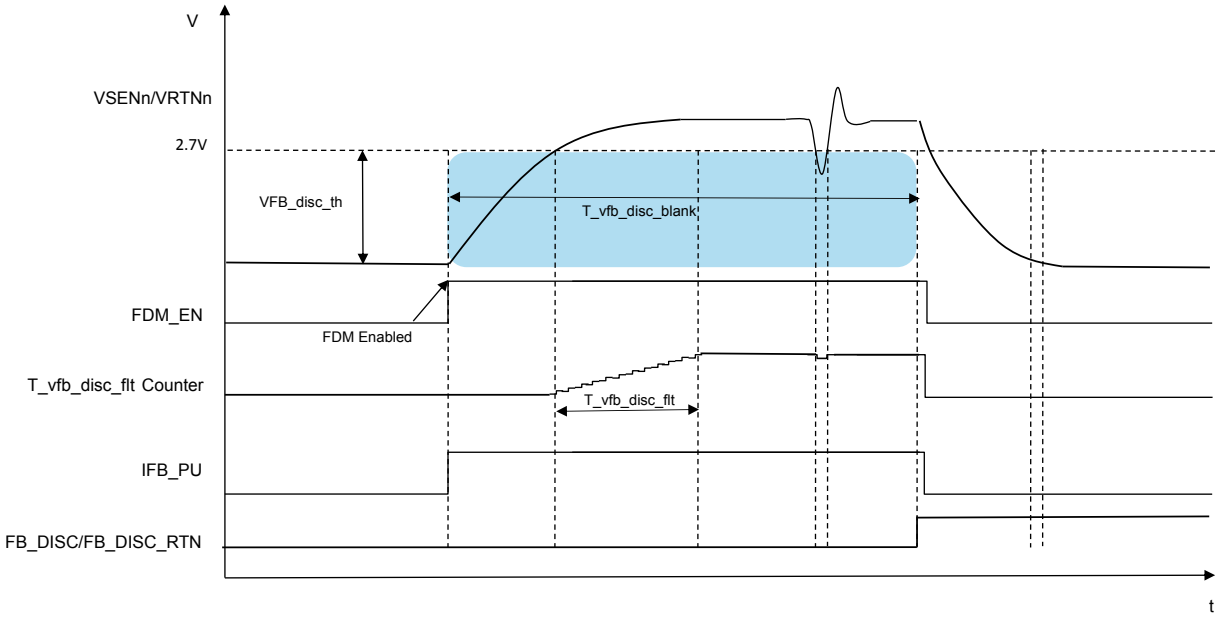


Table 55. **FDM electrical characteristics**

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
VFB_disc_th	Feedback disconnection voltage threshold		2.2	2.4	2.7	V	Comparator output low to high
VFB_disc_ipu	Feedback disconnection detection pull-up current		-110	-90	-60	µA	-
T_vfb_disc_flt	Feedback disconnection detection filter time	CLK_SSM_EN = 0	88	-	132	µs	Digital filter
T_vfb_disc_blank	Feedback disconnection blanking time	CLK_SSM_EN = 0	0.92	1	1.05	ms	Digital filter

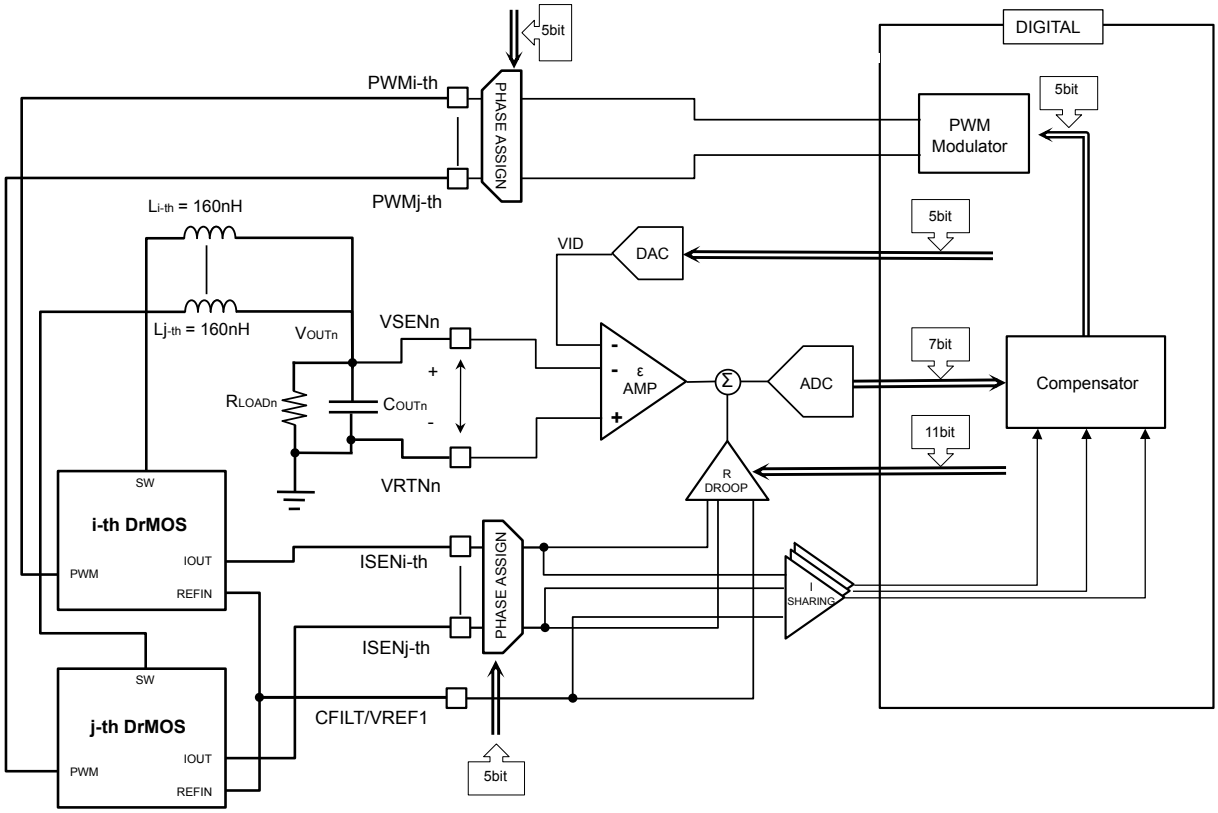
Figure 58. **FDM timing diagram**



3.14 Loop controller

STPM098C implements two separated and fully configurable loop controllers for a multiphase buck regulator.

Figure 59. **Loop controller simplified block diagram**



Regulated output voltage sensing is performed differentially through pins VSEN and VRTN in order to compensate board and other components parasitic effects. The error between output voltage and the programmable set point is computed and properly shifted to fit the cascaded ADC dynamic range. Voltage error combined with drooping voltage from the load-line circuitry is digitized by a high-speed ADC and fed to the digital controller. The compensator uses a PID with two additional poles to provide the digital equivalent of a type III analog compensator.

The PWM modulator combines the outputs of the PID and the phase current balancing control to define the ON time duration for the single phase. The PWM modulator has enough resolution to ensure that there are no limit cycles.

3.14.1 Open Loop control (OLC)

STPM098C optionally allows to bypass the closed control loop by properly setting a PMBus™ command as follows:

Table 56. Open loop control configuration bits

OPEN_LOOP_CONFIG<15:0>	Description
OPEN_LOOP_CONFIG<0>	Open loop control enable
OPEN_LOOP_CONFIG<4:1>	Number of active phases
OPEN_LOOP_CONFIG<10:5>	Fine ON time tuning. LSB = 25 ns /64
OPEN_LOOP_CONFIG<15:11>	Coarse ON time tuning. LSB = 25 ns

Once enabled, the open loop control drives the programmed PWM outputs with the fixed programmed frequency and ON time without any link with actual output voltage and load current.

3.14.2 Phase assignment programming (PSP)

STPM098C controller supports up to 8 phases driving that can be distributed between loop 1 and loop 2 so that:

$$\begin{cases} N + M \leq 8 \\ M \leq 4 \end{cases} \quad (27)$$

Where:

N is the number of phases assigned to the Loop 1.

M is the number of phases assigned to the Loop 2.

Unassigned phases have the related PWM set to HIZ state and ISEN monitor is disabled.

Phase assignment between Loop 1 and Loop 2 can be programmed by a dedicated PMBus™ command as follows:

Table 57. Phase assignment bits

PHASE_CFG (0x)	Loop 1 active phases	Loop 2 active phases	Loop 1 phase count	Loop 2 phase count
0	0 (loop disabled)	0 (loop disabled)	0 (loop disabled)	0 (loop disabled)
1	1	0	1	0
2	1-2	0	2	0
3	1-3	0	3	0
4	1-4	0	4	0
5	1-5	0	5	0
6	1-6	0	6	0
7	1-7	0	7	0
8	1-8	0	8	0
9	1	8	1	1
A	1-2	8	2	1

PHASE_CFG (0x)	Loop 1 active phases	Loop 2 active phases	Loop 1 phase count	Loop 2 phase count
B	1-3	8	3	1
C	1-4	8	4	1
D	1-5	8	5	1
E	1-6	8	6	1
F	1-7	8	7	1
10	1	7-8	1	2
11	1-2	7-8	2	2
12	1-3	7-8	3	2
13	1-4	7-8	4	2
14	1-5	7-8	5	2
15	1-6	7-8	6	2
16	1	6-8	1	3
17	1-2	6-8	2	3
18	1-3	6-8	3	3
19	1-4	6-8	4	3
1A	1-5	6-8	5	3
1B	1	5-8	1	4
1C	1-2	5-8	2	4
1D	1-3	5-8	3	4
1E	1-4	5-8	4	4
1F	5-8	5-8	5-8	5-8

Actual active phase number is automatically adjusted by DPS function to optimize phase interleaving for minimum output ripple. Phase interleaving results in a ripple frequency that is the product of the switching frequency and the number of phases. A high ripple frequency results in reduced ripple voltage, thereby minimizing the output filter capacitance requirements, resulting in significant total BOM cost reduction.

For a correct control loop functionality it is of the utmost importance that all assigned phases correspond to a physical connection at system level (i.e. no assigned phase is unconnected/unused at system level).

3.14.3 Voltage sensing and error calculation

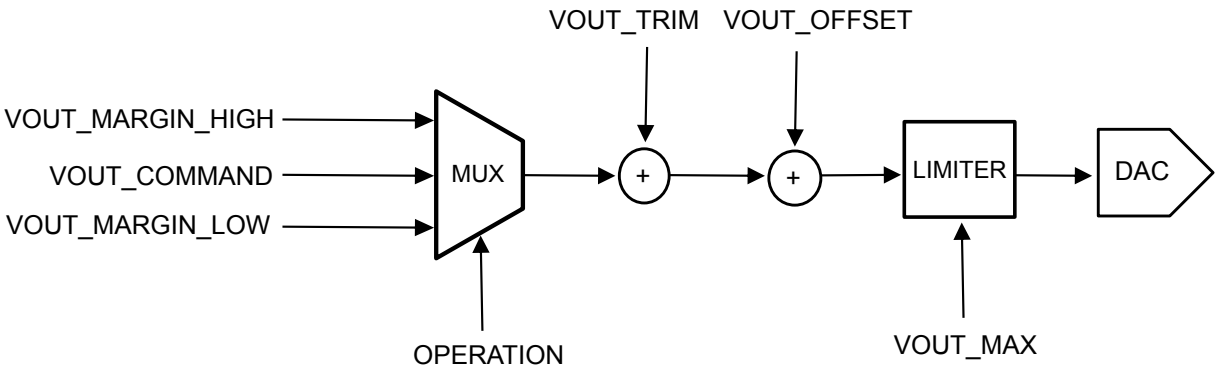
The output voltage sensed at VSENn - VTRNn is subtracted in the analog domain to the corresponding internal references VID-VID_GND to compute the residual error.

The set-point VID is affected by several PMBus™ command as defined in PMBus™ standard:

- VOUT_COMMAND
- VOUT_TRIM
- VOUT_OFFSET
- VOUT_MAX
- VOUT_MARGIN_HIGH
- VOUT_MARGIN_LOW

The impact of each command can be depicted in the following simplified block diagram:

Figure 60. **Voltage setpoint definition simplified block diagram**



The reference voltage (VID_Ln-VID_GND) for the n-th loop is generated by means of a dedicated resistive string DAC and can be programmed through a dedicated PMBus™ register as follows:

$$VID\_Ln = VID\_DAC\_out\_lsb \times (VOUT\_COMMAND\,[4:0] + 9) \quad (28)$$

Where:

VID_DAC_out _lsb is the minimum voltage step [50 mV].

VOUT_COMMAND [4:0] are the dedicated PMBus™ configuration bits [0.5 V ~ 2 V].

The default value is VOUT_COMMAND = 0x06.

In case VOUT_COMMAND = 0x00, VID_Ln is 0 V.

Table 58. **VOUT_COMMAND configuration bits**

VOUT_COMMAND	VID_Ln voltage value	VOUT_COMMAND	VID_Ln voltage value
1	0.5	11	1.3
2	0.55	12	1.35
3	0.6	13	1.4
4	0.65	14	1.45
5	0.7	15	1.5
6	0.75 (default)	16	1.55
7	0.8	17	1.6
8	0.85	18	1.65
9	0.9	19	1.7
A	0.95	1A	1.75
B	1	1B	1.8
C	1.05	1C	1.85
D	1.1	1D	1.9
E	1.15	1E	1.95
F	1.2	1F	2
10	1.25	-	-

Note:

- *VOUT_COMMAND is not supposed to be changed dynamically while regulation is working. Voltage changes are intended to be performed when the related control loop is disabled.*
- *VOUT_COMMAND LSB of 50 mV corresponds to 40-41*VID_DAC_out _lsb through an internal look-up table.*

The reference voltage (VID_Ln - VID_GND) for the n-th loop can be adjusted with respect to the programmed value through a dedicated PMBus™ register as follows:

$$VID\_OFFSET\_Ln = VID\_DAC\_out\_lsb \times (VOUT\_TRIM[5:0] + VOUT\_OFFSET[5:0])$$

Where:

VID_DAC_out _lsb is the minimum voltage step [1.22 mV].

VOUT_OFFSET [5:0], VOUT_TRIM [5:0] are the dedicated PMBus™ configuration bits (2's complement).

The default value is VOUT_OFFSET = VOUT_TRIM = 0x00.

This is intended especially for DDR memory applications where voltages required are higher than the standard VID. VOUT_OFFSET and VOUT_TRIM have the same offset effect on the setpoint; thus, the resulting offset is the sum of the two parameters.

The margin mode voltage (VOUT_MARGIN_HIGH/LOW - VOUT_COMMAND) for the n-th loop can be adjusted with respect to programmed value through a dedicated PMBus™ register as follows:

$$VID_{Ln} = VOUT_{COMMAND} + VOUT_{MARGIN_{HIGH}} = VOUT_{COMMAND} + VID_{DAC_{out_{lsb}}} \times VOUT_{MARGIN_{HIGH}[5:0]} \quad (29)$$

$$VID_{Ln} = VOUT_{COMMAND} + VOUT_{MARGIN_{LOW}} = VOUT_{COMMAND} + VID_{DAC_{out_{lsb}}} \times VOUT_{MARGIN_{LOW}[5:0]}$$

Where:

VID_DAC_out _lsb is the minimum voltage step [1.22 mV].

VOUT_MARGIN_HIGH [5:0], VOUT_MARGIN_LOW [5:0] are the dedicated PMBus™ configuration bits (module).

The default value is VOUT_MARGIN_HIGH = VOUT_MARGIN_LOW = 0x00.

The reference voltage VID for the n-th loop can be safe-guarded against accidental excessive voltage programming on previous commands through a dedicated PMBus™ register as follows:

$$VID\_MAX = VID\_MAX\_lsb \times VOUT\_MAX[5:0] \quad (30)$$

Where:

VID_MAX_lsb is the minimum voltage step [50 mV].

VOUT_MAX [5:0] are the dedicated PMBus™ configuration bits.

The default value is VOUT_MAX = 0x00.

If $VOUT_{COMMAND} + VOUT_{TRIM} + VOUT_{OFFSET} < VOUT_{MAX}$, then:

$$VID_{Ln} = (VOUT_{COMMAND} + 9) \times VOUT\_COMMAND\_lsb + (VOUT_{TRIM} + VOUT_{OFFSET}) \times VID\_DAC\_out\_lsb$$

If $VOUT_{COMMAND} + VOUT_{TRIM} + VOUT_{OFFSET} \geq VOUT_{MAX}$, then:

$$VID_{Ln} = \left[2^5 \times (VOUT_{MAX} + 1) - 1\right] \times VID_{DAC_{out_{lsb}}} \quad (31)$$

At loop controller startup the VID_Ln reference is linearly increased by control logic from 0V to the programmed setpoint in order to develop a soft-start boot ramp on output voltage. The SS slew rate can be programmed through a dedicated PMBus™ register as follows:

$$SS_{SR} = SS_{SR_{lsb}} \times SS_{SRn_{CFG}[3:0]}$$

Where:

SS_SR _lsb is the minimum slew rate step [1 V/ms].

SS_SRn_CFG [3:0] are the dedicated PMBus™ configuration bits [1 V/ms ~ 10 V/ms].

The default value is SS_SRn_CFG = 0x5 (5 V/ms).

To allow power state management at system level, STPM098C implements a procedure to runtime change the regulation setpoint (VID). As an accidental runtime NVM configuration change must be avoided, a dedicated PMBus™ unlock command key is made available.

MFR_UNLOCK [7:0] = 0x55

LOCK can be achieved by writing MFR_UNLOCK ≠ 0x55

Note: The MFR_UNLOCK command is intended only to support dynamic setpoint variation and related diagnostics that need tuning. MFR_UNLOCK usages different from what specified are not recommended or guaranteed.

The target setpoint for the VID transition is configured by programming the standard PMBus™ commands:

- VOUT_COMMAND
- VOUT_TRIM
- VOUT_OFFSET

To avoid diagnostic triggering during output voltage transition (ex. UV/OV) a monitoring threshold adjustment should be applied along with the target VID configuration. This operation is supposed to be carried out by application software: no automatic threshold changes or diagnosis masking is performed by STPM098C.

Dynamic VID change can be configured and applied by means of the dedicated PMBus™ command MFR_SVID_CTRL, which contains several parameters:

Table 59. Dynamic VID control configuration bits

MFR_SVID_CTRL [18:0]	Description
MFR_SVID_CTRL [18]	VID_TRIGGER activation command 0 = No action 1 = VID setpoint change start
MFR_SVID_CTRL [17:16]	VID_MODE: VID slew rate mode 00 = DVID_SR_FAST 01= DVID_SR_SLOW
MFR_SVID_CTRL [15:12]	SLEW_RATE_SELECTOR shift factor for DVID_SR_SLOW
MFR_SVID_CTRL [11:6]	DVID_SR_SLOW
MFR_SVID_CTRL [5:0]	DVID_SR_FAST

Note:
- *MFR_DVID_SR_SELECTOR only effective values are 0x1, 0x2, 0x4, 0x8.*
- *MFR_DVID_SR_SELECTOR values 0x2 and 0x0 have equal effect.*

VID transition (current to target) slew rate can be configured according to the following equation:

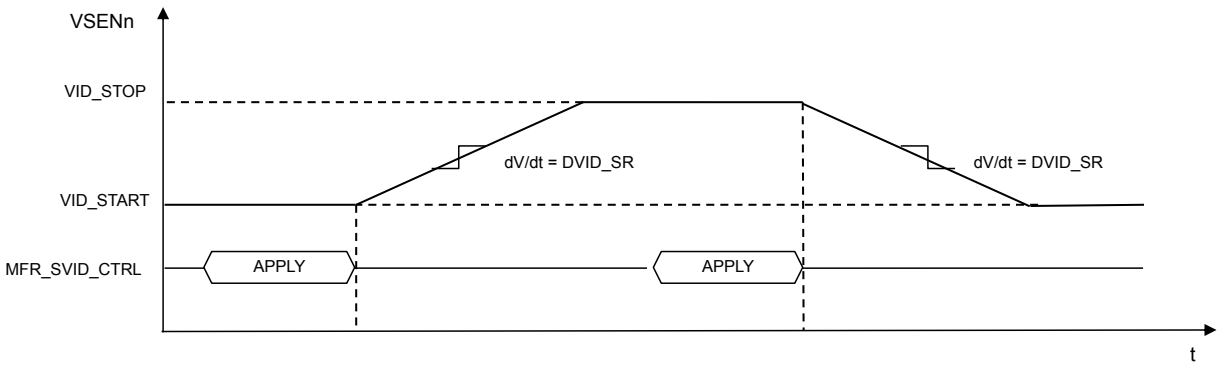
$$DVID_{SR} = \frac{VID\_DAC\_out\_lsb}{4 \times Tclk \times DVID\_SR\_slow \times MFR\_DVID\_SLOW\_SR\_SELECTOR} \quad (32)$$

Where:
VID_DAC_out _lsb is the minimum voltage step [1.22 mV].
Tclk is the system clock period [25 ns].
DVID_SR_SLOW [11:6] are the dedicated PMBus™ configuration bits.
MFR_DVID_SLOW_SR_SELECTOR is a scaling factor.
Default values are: DVID_SR_SLOW = 0x00, MFR_DVID_SR_SELECTOR = 0x0.
In case VID_MODE = 0x01 the equation above becomes:

$$DVID_{SR} = \frac{VID\_DAC\_out\_lsb}{2 \times Tclk \times DVID\_SR\_FAST} \quad (33)$$

Where:
VID_DAC_out _lsb is the minimum voltage step [1.22 mV].
Tclk is the system clock period [25 ns].
DVID_SR_FAST [5:0] are the dedicated PMBus™ configuration bits.
The default value is DVID_SR_FAST [5:0] = 0x00
The loop controller applies the setpoint step up/down as soon as MFR_SVID_CTRL command is issued by setting VID_TRIGGER field to ‘1’.

Figure 61. DVID transition timing diagram



Important: *DVID change is intended to be applied when regulation is in stationary conditions: no other system parameter is changing during VID transition (VIN, Iload, etc.).*

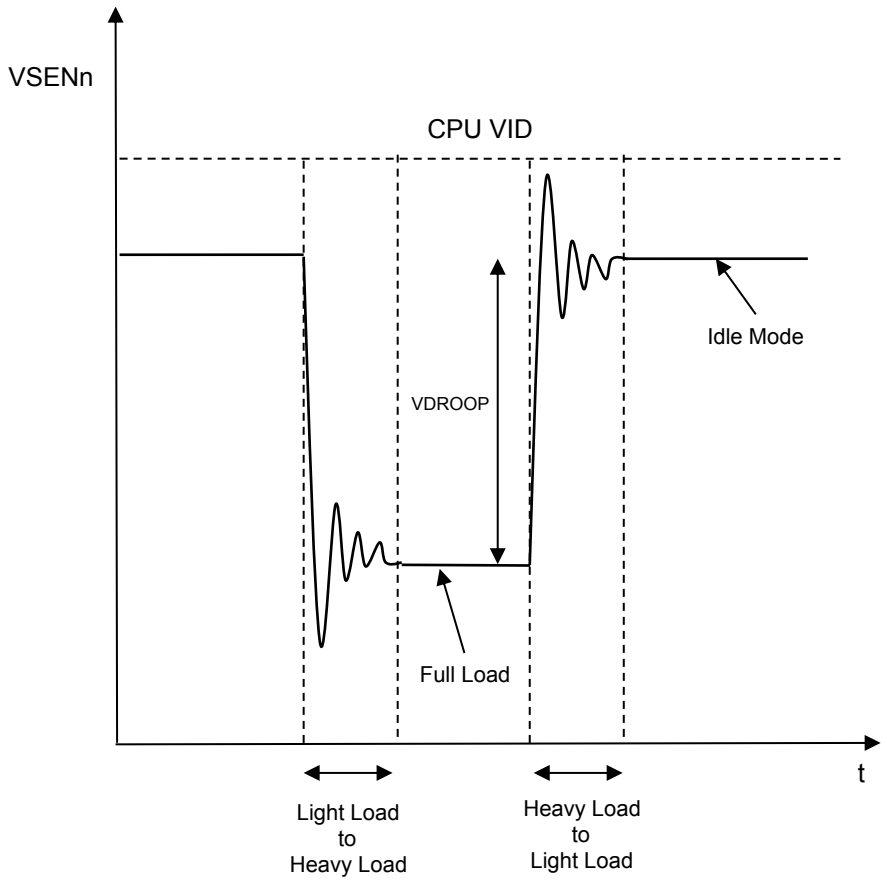
Table 60. VID DAC electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
VID DAC output							
VID_DAC_out_range_max	VID DAC output range max		0	-	2.5	V	-
VID DAC output resolution							
VID_DAC_out_dac_res	VID DAC resolution		-	11	-	bits	-
VID_DAC_out _lsb	VID DAC LSB		-	1.22	-	mV	-
VID DAC output accuracy							
VID_DAC_total_err1	VID DAC total error1	0.5 V ≤ VID < 1.5 V	-10	-	10	mV	-
VID_DAC_total_err2	VID DAC total error2	1.5 V ≤ VID < 2.5 V	-1	-	1	%	-

3.14.4 Load-line function (VDROOP)

For both control loops STPM098C implements a load-line function. This function introduces an intentional voltage loss (VDROOP) proportional to the load current in order to increase the headroom and recovering part of ESR during load transients.

Figure 62. Load-line functionality simplified behavior



The load-line function can be enabled through a dedicated PMBus™ command as follows:

Table 61. **Load-Line enable command bit**

EN_DRP	Description
0	Load-line function disabled (default)
1	Load-line function enabled

The droop resistance RDROOP can be programmed through a dedicated PMBus™ register as follows:

$$VOUT\_DROOP = VDROOP\_DAC\_out\_lsb \times (1 + VOUT\_DROOPn\_CFG) \quad (34)$$

Where:

VDROOP_DAC_out _lsb is the minimum drooping step [9.765 µΩ].

VOUT_DROOPn_CFG [9:0] are the dedicated PMBus™ configuration bits [9.76 5µΩ ~ 9.99 mΩ].

The default value is VOUT_DROOPn_CFG = 0x00.

In case VOUT_DROOPn_CFG = 0x00 the related load-line function is disabled and no voltage drooping is performed.

Note: The droop resistance shall be chosen so that, at the maximum output current, the output voltage is the minimum acceptable. On the other hand, when the output current is close to zero, the output voltage shall be near to the maximum.

Table 62. **VDROOP DAC electrical characteristics**

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
VDROOP DAC output							
VDROOP_DAC_out_range_max	VDROOP DAC output range max		9.765	-	9999	µΩ	-
VDROOP DAC output resolution							
VDROOP_DAC_out_dac_res	VDROOP DAC resolution		-	10	-	bits	-
VDROOP_DAC_out _lsb	VDROOP DAC LSB		-	9.765	-	µΩ	-
VDROOP DAC accuracy							
VDROOP_DAC_gain_err	VDROOP DAC gain error		-6	-	6	%	-
VDROOP_DAC_offset	VDROOP DAC offset		-10	-	10	mV	-
VDROOP_DAC_total_err	VDROOP DAC total error		-	-	-	mV	-

VRDOOP total error can be calculated as follows:

$$VDROOP_{DAC_{total_{err}}} = \pm \left(VDROOP_{DAC_{offset}} \times N \times \frac{R_{DROOP}}{A} + 0.4\,mV \right) \pm \left(VDROOP_{DAC_{gain_{err}}} \times R_{DROOP} \times Iload \right)$$

Where:

- Rdroop is the selected droop resistance (that is, 9.765 µΩ to 9999 µΩ).
- ILoad is the load current.
- A is the DrMOS current sense gain (that is, 5 mV/A).

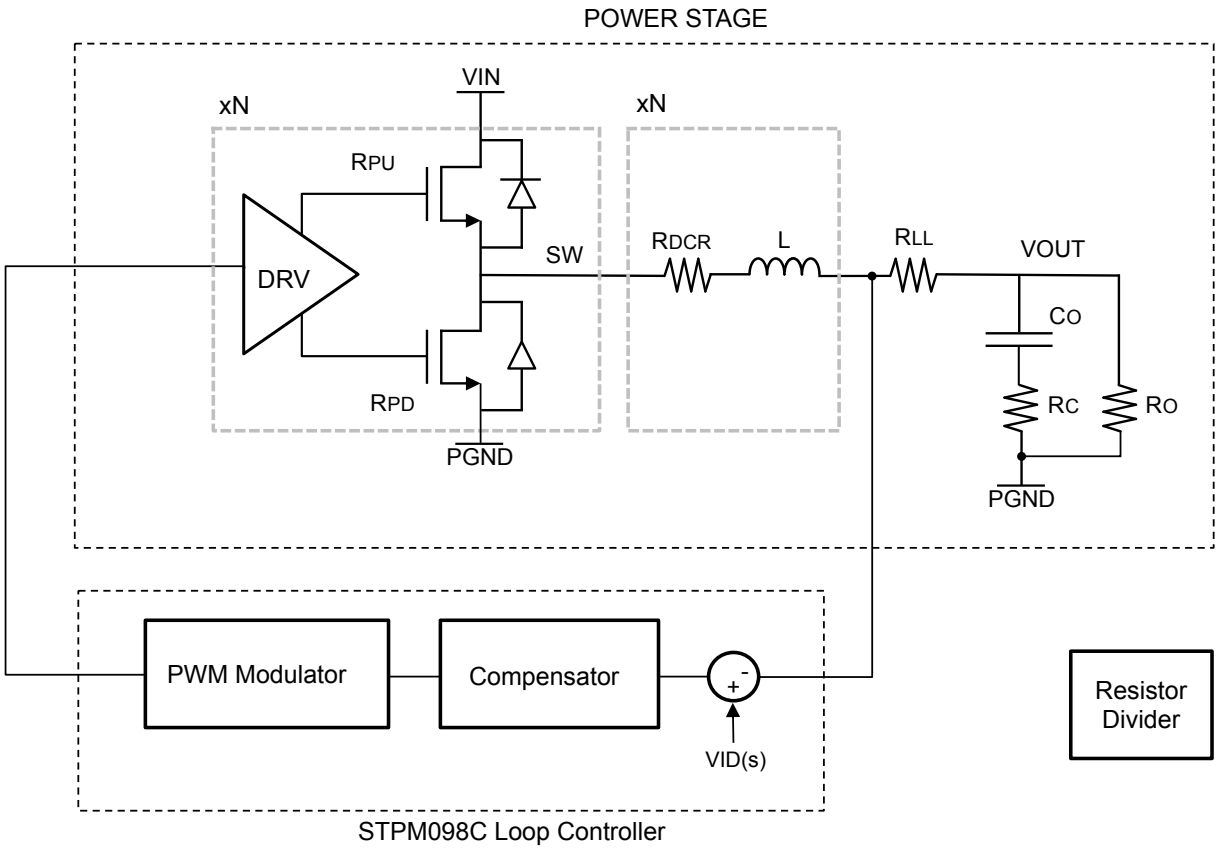
Example:

- A = 5 mΩ
- Iload = 170 A
- Rdroop = 0.3 mΩ
- N = 5
- Target Vdroop = 51 mV
- Total error = (10 mV * 5 * 0.3 mΩ/5mΩ + 0.4 mV) + (6% * 51 mV) = 3.4 mV + 3.06 mV = 6.46 mV

3.14.5 Loop compensator

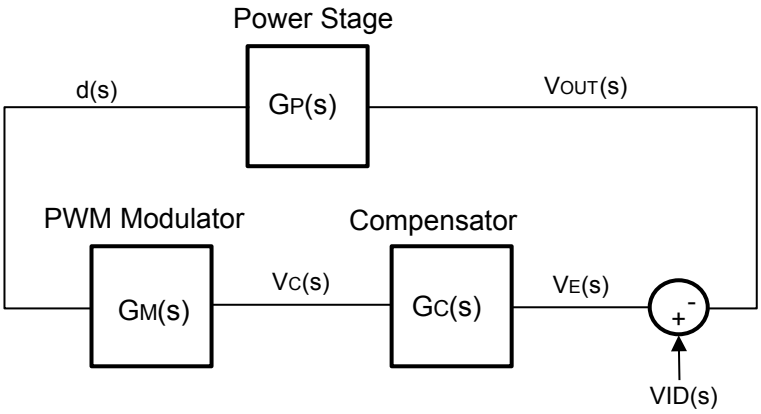
The converter block diagram can be simplified as illustrated in the Figure 63, where an equivalent single-phase converter is considered along with only first order parasitics (inductance DCR and output capacitance ESR).

Figure 63. Converted simplified block diagram



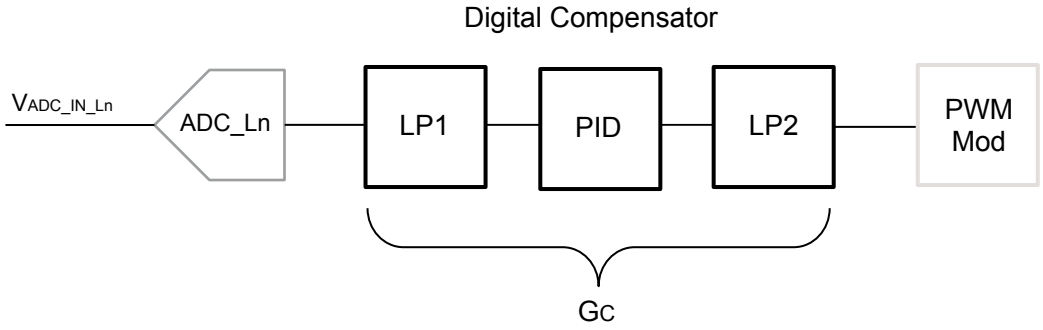
The small-signal average model of the control loop can be represented as follows:

Figure 64. Closed loop transfer function



In order to guarantee a good closed-loop stability along with a full set of power stages, the converted error signal is fed to a cascade of a first single-pole LP filter followed by the PID (proportional integral derivative) compensator and an additional single-pole LP filter.

Figure 65. **Digital compensator simplified block diagram**



The PID LP filter 1 and filter 2 can be programmed through a dedicated PMBus™ register as follows:

$$MFR_{FILTER_{PRE_{POST}}[14:7]} = \frac{T_{ck}}{(T_{ck}+\tau_{LP1})}2^8 \quad (35)$$

$$MFR_{FILTER_{PRE_{POST}}[6:0]} = \frac{T_{ck}}{(T_{ck}+\tau_{LP2})}2^7 \quad (36)$$

The PID Kn parameters for the n-th loop can be programmed through a dedicated PMBus™ register as follows:

$$MFR_{PID1[18:0]} = 8\left(K_p + \frac{K_d}{T_{ck}}\right) \quad (37)$$

$$MFR_{PID2[15:0]} = 2^{16}K_iT_{CK} \quad (38)$$

$$MFR_{PID3[15:0]} = \frac{K_d}{T_{ck}} \quad (39)$$

Where:

Tck is the system clock period.

MFR_FILT_PRE_POST [6:0] are the dedicated PMBus™ configuration bits.

In order to prevent compensator persistent integration after a heavy to light load transition, a digital error clamp limit can be set through a dedicated PMBus™ command as follows:

$$VERR_{CLAMP} = \Delta_{LSB} \times \left(63 - \mathrm{VERR_{CLAMP[5:0]}}\right) \quad (40)$$

Where:

ΔLSB is the minimum slew rate step [2 mV].

VERR_CLAMP [5:0] is the dedicated PMBus™ configuration bits [0 ~ 126 mV].

The default value is VERR_CLAMP = 0x00.

To enhance control loop dynamic performances during load transients, STPM098C implements a function that doubles the controller proportional gain factor when digital error exceeds a programmable threshold.

Transient gain boost function can be configured by means of TGB_CONFIG register as follows:

$$TGB_{TH} = \mathrm{TGB_{TH_{lsb}}} \times \mathrm{TGB_{CONFIG[7:2]}} \quad (41)$$

Where:

TGB_TH_lsb is the minimum drooping step [2 mV].

TGB_CONFIG [7:2] are the dedicated PMBus™ configuration bits [0 mV ~ 126 mV].

The default value is TGB_CONFIG [7:2] = 0x3F.

$$TGB_{EN} = \mathrm{TGB_{CONFIG[7:2]}} \quad (42)$$

Where:

TGB_CONFIG [1:0] are the dedicated PMBus™ configuration bits:

00, TGB disabled.

01, TGB is enabled only when N ≥ 2 (N is the number of active phases).

10, TGB always enabled.

10, TGB always enabled. TBG threshold = 2x TGB_TH

For further details concerning loop compensator and deeper details on mathematical aspects, refer to the Application note: “STPM098C_AN_PID_setting”.

3.14.6 PWM modulator

PWM modulator macrosection is a halfway analog/digital section responsible for generating the PWMn signal aligned to the compensated voltage according to the COT scheme.

3.14.6.1 Digitally-controlled oscillator (DCO) and interleaver

The PWM modulator core is based on a digitally controlled oscillator (DCO). The oscillator output is used as a time-base to trigger the PWM ON-pulses of each phase. This triggering pulse is then multiplexed to each phase by means of a shift register thus accomplishing the phase interleaving.

The carrier frequency can be programmed through a dedicated PMBus™ register as follows:

Table 63. PWM period selection bits

TSWITCH	PWM period [µs]	PWM frequency [MHz]	TSWITCH	PWM period [µs]	PWM frequency [MHz]
0	5	0.200	10	1.675	0.597
1	4.45	0.225	11	1.6	0.625
2	4	0.250	12	1.55	0.645
3	3.625	0.276	13	1.475	0.678
4	3.325	0.301	14	1.425	0.702
5	3.075	0.325	15	1.375	0.727
6	2.85	0.351	16	1.325	0.755
7	2.675	0.374	17	1.3	0.769
8	2.5	0.400	18	1.25	0.800
9	2.35	0.426	19	1.1	0.909
A	2.225	0.449	1A	1	1.000
B	2.1	0.476	1B	0.9	1.111
C	2 (default)	0.500 (default)	1C	0.825	1.212
D	1.9	0.526	1D	0.775	1.290
E	1.825	0.548	1E	0.725	1.379
F	1.75	0.571	1F	0.675	1.481

3.14.6.2 ON time generator

PWM signals to be delivered to each phase are composed starting from the DCO signal on which the computed ON time is applied.

To safeguard the external power stage from wrong operation due to PWM marginality, STPM098C allows to introduce a limitation over the minimum ON and OFF time applied on PWM pins.

The minimum ON/OFF time limitation can be programmed by means of the dedicated PMBus™ command MFR_T_MIN [7:0].

$$T_{OFF_{MIN}} = \mathrm{T_{MIN_{lsb}}} * MFR_{T_{MIN}[7:4]} \quad (43)$$

$$T_{ON_{MIN}} = \mathrm{T_{MIN_{lsb}}} * MFR_{T_{MIN}[3:0]} \quad (44)$$

Where:

T_MIN _lsb is the minimum timing step [25 ns].

Default values are:

T_OFF_MIN = 0x02 (50 ns)

T_ON_MIN = 0x03 (75 ns)

No internal limitation is applied to programmed MFR_T_MIN: this means that if the configured value is zero, then no MIN TON/TOFF is applied.

STPM098C allows two possible methods for the controller to compute the nominal PWM ON time:

- Feedforward;

- Fixed ON time

Feedforward

The feedforward method can be enabled through a dedicated PMBus™ register as follows:

Table 64. Closed-loop feedforward enable bit

FEED_FORWARD_EN	Description
0	Closed-loop feedforward disabled (default)
1	Closed-loop feedforward enabled

With this method, the control loop automatically computes the PWM nominal ON time based on direct measurement of input voltage through the VIN ADC conversion.

$$T_{ON} = \frac{V_{OUT}}{V_{IN}} T_{PWM} \quad (45)$$

Where:

Vout is the programmed output voltage.

VIN is the input voltage measured on POWERIN_P.

T_{PWM} is the programmed PWM period.

Fixed ON time

The fixed method is active if feedforward is disabled. With this method the nominal ON time is fixed and defined by means of a dedicated PMBus™ register as follows:

$$FEED_{FORWARD_{CONST}[9:0]} = \frac{1.22\ \text{mV} \times 2^{19}}{V_{IN(TYP)}} \quad (46)$$

Where:

FEED_FORWARD_CONST [9:0] are the dedicated PMBus™ configuration bits [0 ~ 1024].

The default value is FEED_FORWARD_CONST = 0x000 (corresponds to nominal on time of 3Tck).

As a COT-based architecture the PWM frequency variation is used to compensate for the load current variation so that it is not inherently a constant frequency scheme.

To overcome this drawback the nominal ON time defined by the main control loop is adjusted by a second loop in order to lock the steady state frequency of the PWM signal to the programmed value (frequency locked loop).

The FLL compares the difference between DCO period and the period programmed in TSWITCH divided by N (number of active phases), and proportionally changes the delay line control thus adjusting ON time to lock the PWM frequency in steady conditions.

The FLL control gain can be configured by means of a dedicate PMBus™ command as follows:

$$FLL_{COEFF} = \Delta_{LSB} \times \text{FLL}_{\text{COEF}[9:0]} \quad (47)$$

Where:

ΔLSB is the minimum slew rate step [1].

FLL_COEFF [9:0] is the dedicated PMBus™ configuration bits [0 ~ 1024].

In case FLL_COEFF = 0x000, the frequency locked loop function is disabled and, as a consequence, the PWM frequency may deviate from the programmed one.

The default value is FLL_COEFF = 0x002.

The FF maximum correction can be configured as well by means of a dedicated PMBus™ command as follows:

Table 65. FLL limit configuration bits

FLL_LIMIT_STRAT1	FLL_LIMIT_STRAT0	Description
0	0	Maximum ON time correction = ±100% TON (default)
0	1	Maximum ON time correction = ±0% TON
1	0	Maximum ON time correction = ±25% TON
1	1	NO maximum ON time correction

3.14.6.3 *PWM spread spectrum modulation*

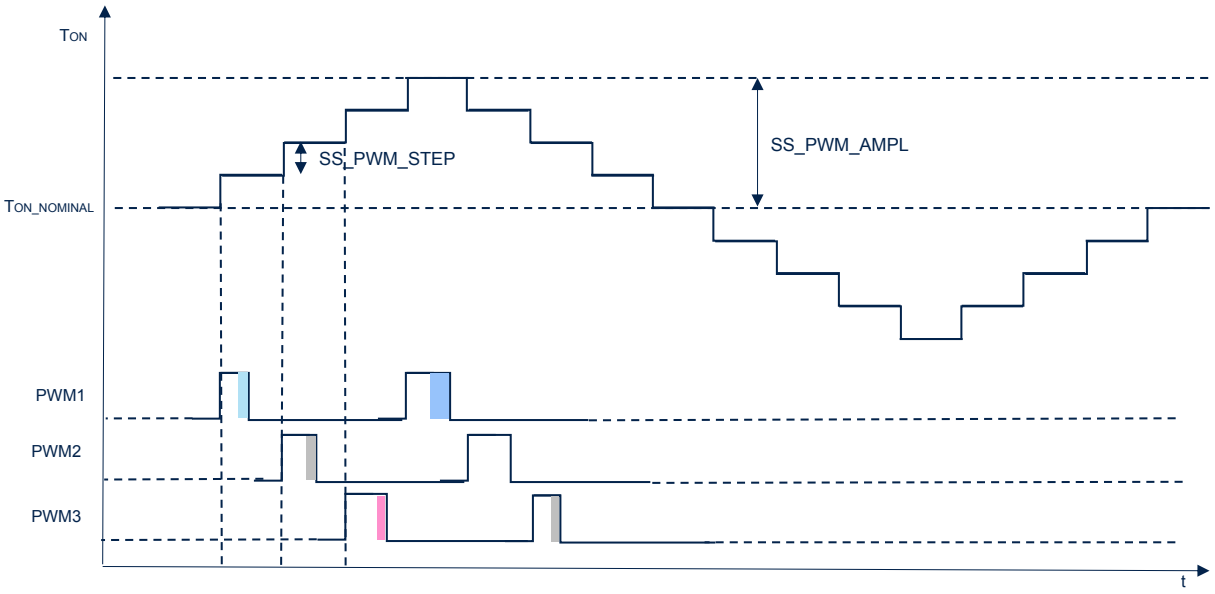
STPM098C PWM modulator implements a frequency modulation (spread spectrum modulation) feature to reduce the power stages emissions around the main frequency by spreading the power spectrum over a larger frequency range. PWM SSM can be enabled by a dedicated PMBus™ bit as follows:

Table 66. PWM SSM enable bit

BUCK_CLK_SSM_EN	Description
0	PWM SSM disabled (default)
1	PWM SSM enabled

The implemented mechanism makes use of FLL to introduce a linear variation on the ON time to be converted as a period modulation by the main control loop.

Figure 66. PWM SSM modulation operation



The PWM SSM parameter can be programmed by means of the dedicated PMBus™ commands:

$$SS_{PWM_{AMPL}} = SSM_{lsb} \times SS_{PWM_{AMPL[15:0]}} \quad (48)$$

$$SS_{PWM_{STEP}} = SSM_{lsb} \times SS_{PWM_{STEP[14:0]}} \quad (49)$$

Where:

SSM_lsb is the minimum timing step [25 ns/128].

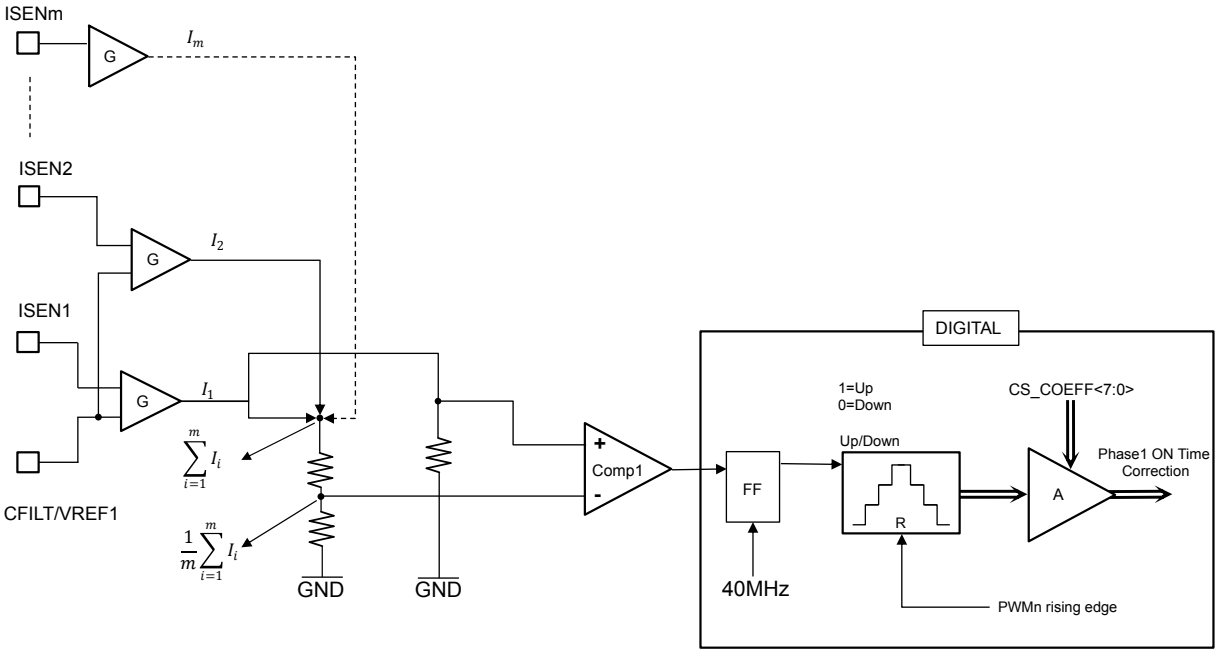
Default values are SS_PWM_AMPL = 0x0000 and SS_PWM_STEP = 0x0000

PWM SSM operation makes use of FLL structure; as a consequence, to enable buck SSM, FFL shall be enabled as well. PWM SSM is effective in steady state conditions. During transients events (load, VIN, VID etc.) frequency is determined by the main control loop. PWM SSM varies the steady state frequency periodically, as a consequence an enhanced voltage ripple on output node shall be expected.

3.14.6.4 *Phase current balancing (PCB)*

STPM098C integrates an in-loop current balancing architecture in order to control the phase current balancing. This feature is accomplished by converting cycle by cycle the difference between the single phase current and the loop average phase current. The converted value optionally multiplied by a factor A, is used to fine-tune the single phase ON time to equalize all phase currents.

Figure 67. Phase current balancing simplified block diagram



The current balancing gain can be programmed by means of a dedicated PMBus™ command as follows:

$$A = CS_{COEFF[7:0]} \times 2^{-6} \quad (50)$$

Where:

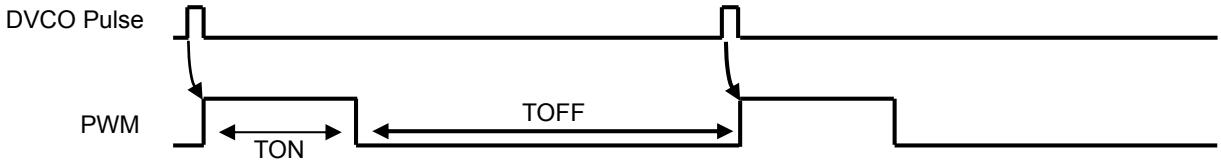
CS_COEFF [7:0] is the dedicated PMBus™ configuration register [1 ~ 256].

The default value is CS_COEFF = 0x80.

3.14.6.5 *Pulse merging (MULTIPULSE)*

In steady state condition the period imposed by the DCO for the single phase is always higher than the nominal ON time.

Figure 68. T_on time, steady state

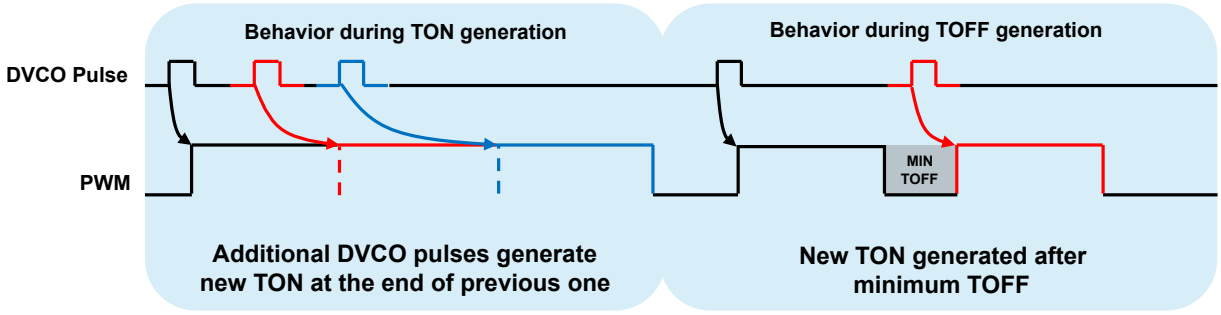


In case the DCO output period is forced to be reduced below the nominal ON time, STPM098C allows to select four different strategies for generating the ON/OFF timing through the MULTI_PULSE_STRAT register configuration.

MULTI_PULSE_STRAT = 0x00

Pulse merger multiplies the ON time duration by the number of the DCO pulses received during the nominal ON time. If a DCO pulse is received during the minimum TOFF window the next ON time is generated after a minimum TOFF interval.

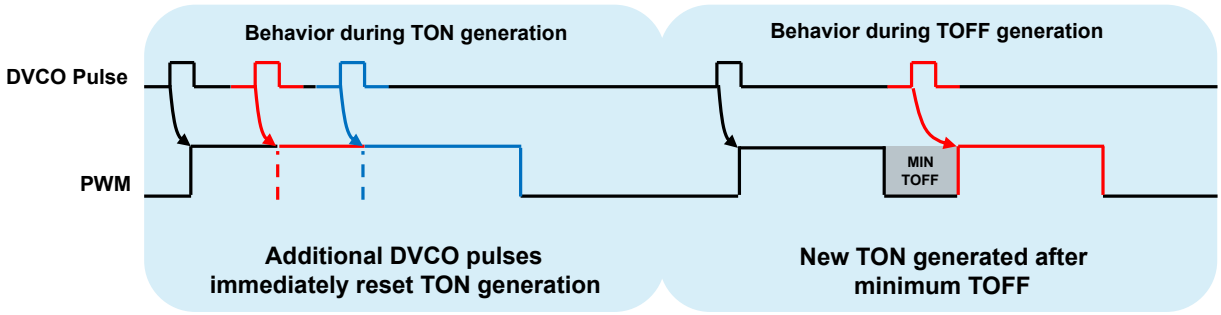
Figure 69. T_on time with MULTI_PULSE_STRAT = 0x00



MULTI_PULSE_STRAT = 0x01

Pulse merger restarts the nominal ON time generation each time a DCO pulse is received during the nominal ON time itself. If a DCO pulse is received during the minimum TOFF window the next ON time is generated after a minimum TOFF interval.

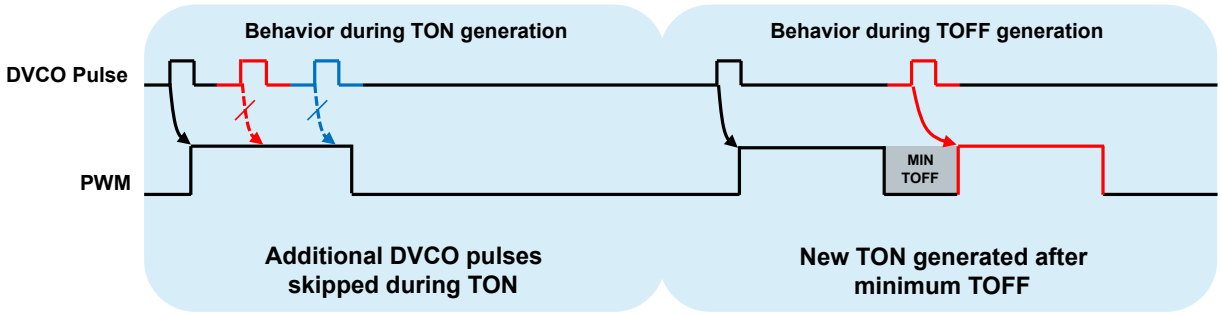
Figure 70. T_on time with MULTI_PULSE_STRAT = 0x01



MULTI_PULSE_STRAT= 0x02

Pulse merger skips DCO pulses received during the nominal ON time itself. If a DCO pulse is received during the minimum TOFF window the next ON time is generated after a minimum TOFF interval.

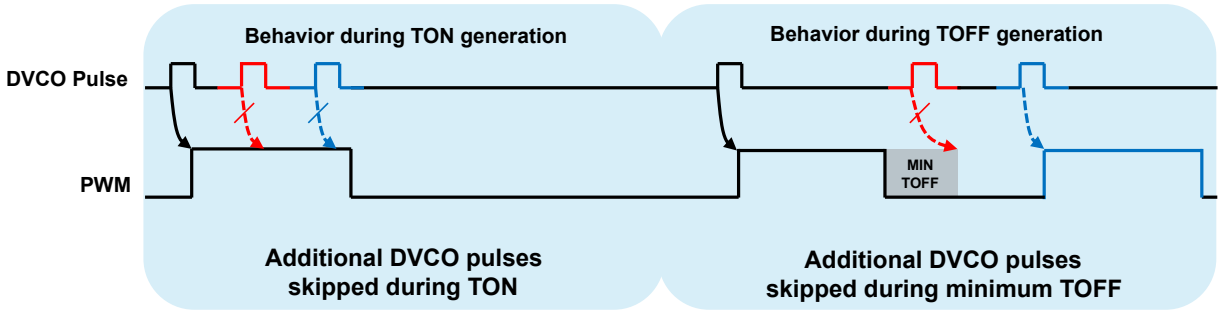
Figure 71. T_on time with MULTI_PULSE_STRAT = 0x02



MULTI_PULSE_STRAT= 0x03

Pulse merger skips DCO pulses received during the nominal ON time itself as well as DCO pulses received during the minimum TOFF window.

Figure 72. T_on time with MULTI_PULSE_STRAT = 0x03



3.14.7 Efficiency enhancement

3.14.7.1 *Dynamic phase shedding (DPS)*

In order to maximize conversion efficiency over the whole load range, the STPM098C loop controller allows the possibility to automatically adjust the number of active phases among the available subset defined by phase assignment programming.

Active phases are added/dropped basing on the comparison between the converted load current level measurement and a programmable threshold thus optimizing efficiency over the whole load range.

If $\sum_{j=1}^{m}\left(ISEN_j - \frac{CFILT}{VREF1}\right) \geq$ PHASEn_ADD_TH occurs for an interval longer than IOUT ADC conversion latency, the n-th phase contribution is added to the control loop (n-th PWM enabled, ISENn monitor enabled).

If $\sum_{j=1}^{m}\left(ISEN_j - \frac{CFILT}{VREF1}\right) \leq$ PHASEn_DROP_TH occurs for an interval longer than IOUT ADC conversion latency plus the configured DROP_DELAY, the n-th phase contribution is dropped from the control loop (n-th PWM disabled (HIZ), ISENn monitor disabled).

The DPS add/drop thresholds can be programmed through a dedicated PMBus™ register as follows:

$$PHASE2_{ADD_{TH}} = \Delta_{LSB} \times MFR_{PHASE2_{ADD_{CFG}}[7:0]} \quad (51)$$

$$PHASE2_{DROP_{TH}} = \Delta_{LSB} \times MFR_{PHASE2_{DROP_{CFG}}[7:0]} \quad (52)$$

$$PHASE3_{ADD_{TH}} = \Delta_{LSB} \times MFR_{PHASE3_{ADD_{CFG}}[7:0]} \quad (53)$$

$$PHASE3_{DROP_{TH}} = \Delta_{LSB} \times MFR_{PHASE3_{DROP_{CFG}}[7:0]} \quad (54)$$

$$PHASE4_{ADD_{TH}} = \Delta_{LSB} \times MFR_{PHASE4_{ADD_{CFG}}[7:0]} \quad (55)$$

$$PHASE4_{DROP_{TH}} = \Delta_{LSB} \times MFR_{PHASE4_{DROP_{CFG}}[7:0]} \quad (56)$$

$$PHASE5_{ADD_{TH}} = \Delta_{LSB} \times MFR_{PHASE5_{ADD_{CFG}[7:0]}} \quad (57)$$

$$PHASE5_{DROP_{TH}} = \Delta_{LSB} \times MFR_{PHASE5_{DROP_{CFG}[7:0]}} \quad (58)$$

$$PHASE6_{ADD_{TH}} = \Delta_{LSB} \times MFR_{PHASE6_{ADD_{CFG}[7:0]}} \quad (59)$$

$$PHASE6_{DROP_{TH}} = \Delta_{LSB} \times MFR_{PHASE6_{DROP_{CFG}[7:0]}} \quad (60)$$

$$PHASE7_{ADD_{TH}} = \Delta_{LSB} \times MFR_{PHASE7_{ADD_{CFG}[7:0]}} \quad (61)$$

$$PHASE7_{DROP_{TH}} = \Delta_{LSB} \times MFR_{PHASE7_{DROP_{CFG}[7:0]}} \quad (62)$$

$$PHASE8_{ADD_{TH}} = \Delta_{LSB} \times MFR_{PHASE8_{ADD_{CFG}[7:0]}} \quad (63)$$

$$PHASE8_{DROP_{TH}} = \Delta_{LSB} \times MFR_{PHASE8_{DROP_{CFG}[7:0]}} \quad (64)$$

Where:

Δ_{LSB} is the minimum slew rate step [0.94 A].

MFR_PHASEn_ADD_CFG [7:0], MFR_PHASEn_DROP_CFG [7:0] are the dedicated PMBus™ configuration bits [0 A ~ 239.7A].

Default values are:

PHASE2_ADD_TH = 14 A

PHASE2_DROP_TH = 10 A

PHASE3_ADD_TH = 25 A

PHASE3_DROP_TH = 21 A

PHASE4_ADD_TH = 33 A

PHASE4_DROP_TH = 29 A

PHASE5_ADD_TH = 46 A

PHASE5_DROP_TH = 42 A

PHASE6_ADD_TH = 60 A

PHASE6_DROP_TH = 56 A

PHASE7_ADD_TH = 72 A

PHASE7_DROP_TH = 68 A

PHASE8_ADD_TH = 85 A

PHASE8_DROP_TH = 81 A

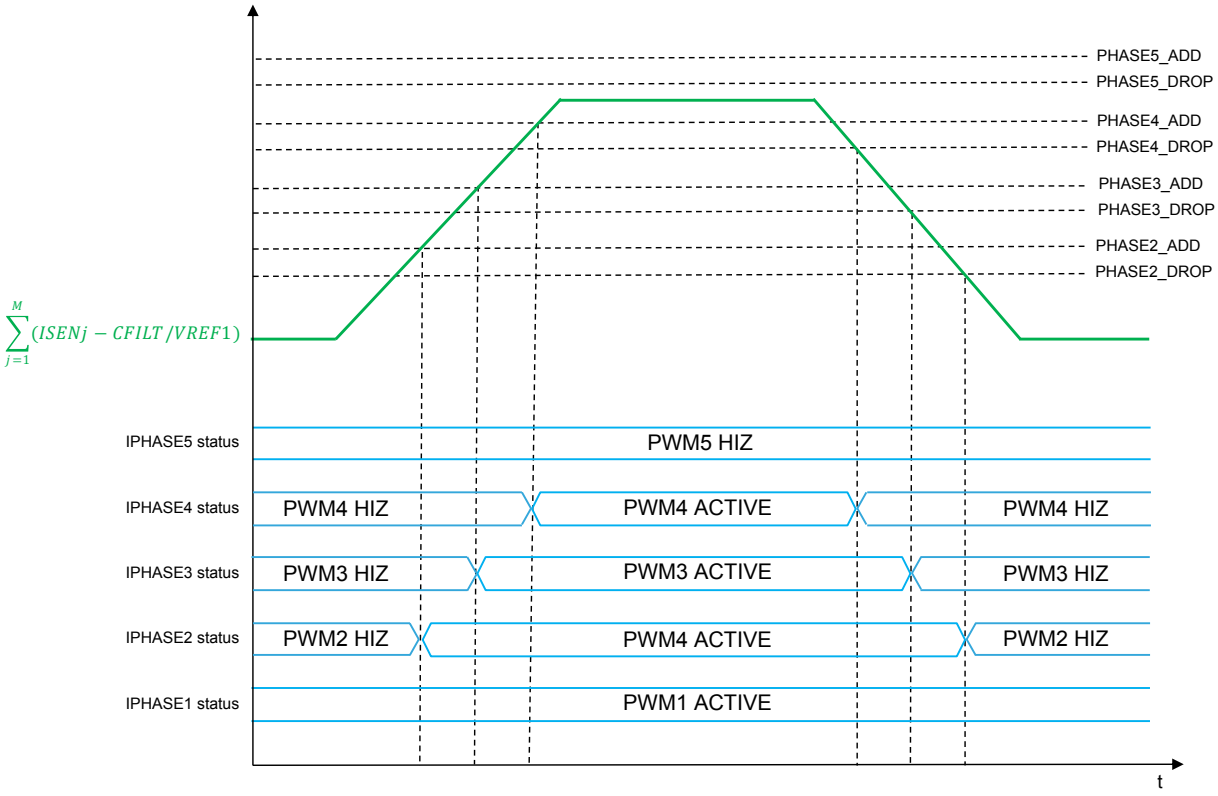
In case PHASEn_ADD_TH = 0x00 the dynamic phase shedding function is disabled, and no phase adds drop whit respect to phase assignment configuration is performed.

DPS DROP_DELAY value can be programmed through a dedicated PMBus™ register as follows:

Table 67. DPS drop delay configuration bit

PH_SHED_DELAY1	PH_SHED_DELAY1	Description
0	0	DROP DELAY = 8 PWM periods (default)
0	1	DROP DELAY = 16 PWM periods
1	0	DROP DELAY = 24 PWM periods
1	1	DROP DELAY = 32 PWM periods

Figure 73. **DPS timing diagram**



When DPS is active, a minimum number of active phases can be configured through a dedicated PMBus™ command as follows:

Table 68. **DPS minimum phase drop limit configuration bits**

NPH_PS02	NPH_PS01	NPH_PS00	Description
0	0	0	At least 1 active phase (default)
0	0	1	At least 1 active phase
0	1	0	At least 2 active phases
0	1	1	At least 3 active phases
1	0	0	At least 4 active phases
1	0	1	At least 5 active phases
1	1	0	At least 6 active phases
1	1	1	At least 7 active phases

DPS minimum phase number (NPH_PS) should be always lower than or equal to the phase number assigned to the loop (PHASE_CFG).

In case DPS minimum phase number is set higher than the assigned phase number, the NPH_PS configuration has the higher priority in defining the number of active phases.

Example: if NPH_PS = 0x4 for loop 1 while PHASE_CFG = 0x2, then loop 1 will have 4 active phases instead of 2.

During fast load increase DPS control is overridden to quickly support the current change. The DCO output period is monitored and if it falls below an adaptive threshold the controller instantly increases the number of active phases.

If $T_{DCO} \leq \frac{1}{N+1} T_{NOMINAL}$ occurs, the active phase number of the loop is increased by 1, independently of the DPS assertion.

Where:

N is the number of active phases.

$T_{NOMINAL}$ is the switching period programmed in TSWITCH.

Phase boost can be disabled by a dedicated PMBus™ bit as follows:

Table 69. Phase boosting enable bit

DISABLE_DPM_PROT	Description
0	Phase boosting enabled (default)
1	Phase boosting disabled

Note:

- *DPS disabling can be achieved by setting PHASEn_ADD_TH = 0x00 only while DPS enabling need to properly set both PHASEn_ADD_TH and PHASEn-DROP.*
- *For Loop 1:*
  - *PHASE2_ADD_TH is the current threshold above which phase 2 is added to phase 1*
  - *PHASE3_ADD_TH is the current threshold above which phase 3 is added to phase 1/2*
  - *PHASE4_ADD_TH is the current threshold above which phase 4 is added to phase 1/2/3*
  - *PHASE5_ADD_TH is the current threshold above which phase 5 is added to phase 1/2/3/4*
  - *PHASE6_ADD_TH is the current threshold above which phase 6 is added to phase 1/2/3/4/5*
  - *PHASE7_ADD_TH is the current threshold above which phase 7 is added to phase 1/2/3/4/5/6*
  - *PHASE8_ADD_TH is the current threshold above which phase 8 is added to phase 1/2/3/4/5/6/7*
- *For Loop 2:*
  - *PHASE8_ADD_TH is the current threshold above which phase 7 is added to phase 8*
  - *PHASE7_ADD_TH is the current threshold above which phase 6 is added to phase 8/7*
  - *PHASE6_ADD_TH is the current threshold above which phase 5 is added to phase 8/7/6*
- *PHASEn_DROP_TH is the current threshold below which a phase is dropped following the reverse scheme depicted above for the two loops.*
- *Unused phases shall be configured with PHASEn_ADD_TH = 0xFF.*
- *Unused loops or used loops with no DPM requirements shall be configured with PHASEn_ADD_TH = 0x00 on all assigned phases.*

Example 1:

PHASE_CFG=0x15

Loop 1 uses phases 1:5 (phase 6 unused)

Loop 2 uses phase 1_L2:2_L2

DPM is active on both loops

PHASE2_ADD_TH = Iload1

PHASE3_ADD_TH = Iload2

PHASE4_ADD_TH = Iload3

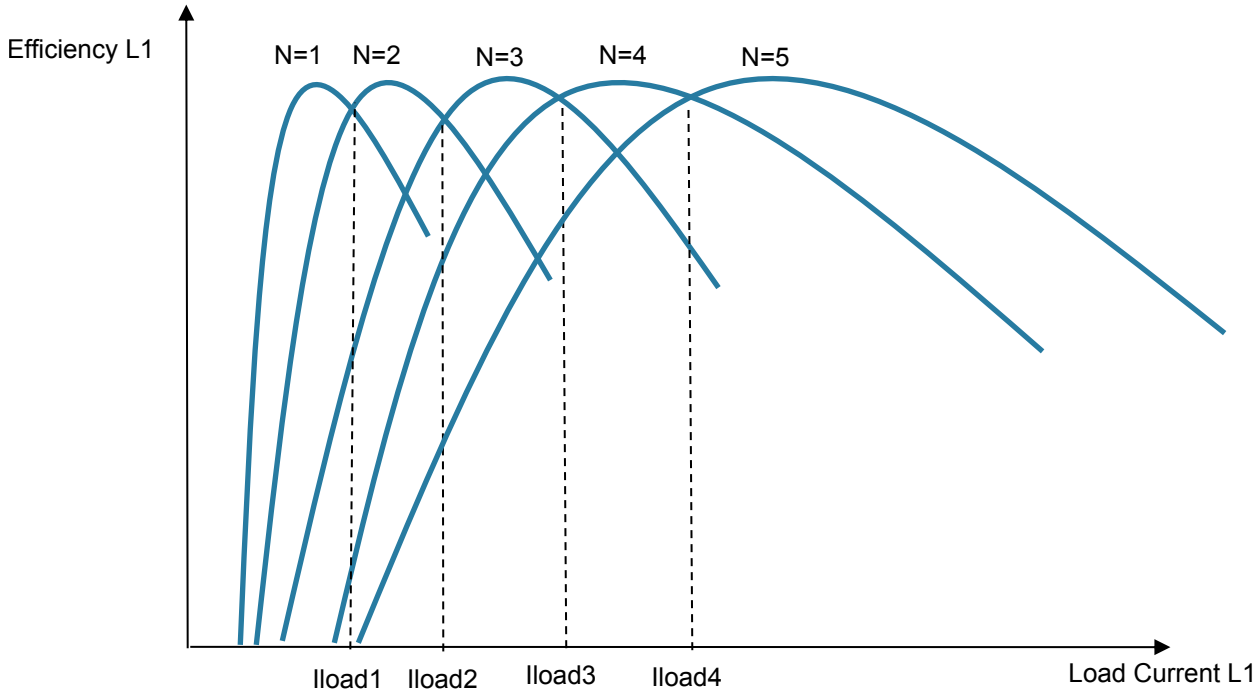
PHASE5_ADD_TH = Iload4

PHASE6_ADD_TH = 0xFF

PHASE7_ADD_TH = 0xFF

PHASE8_ADD_TH = 0xIload5

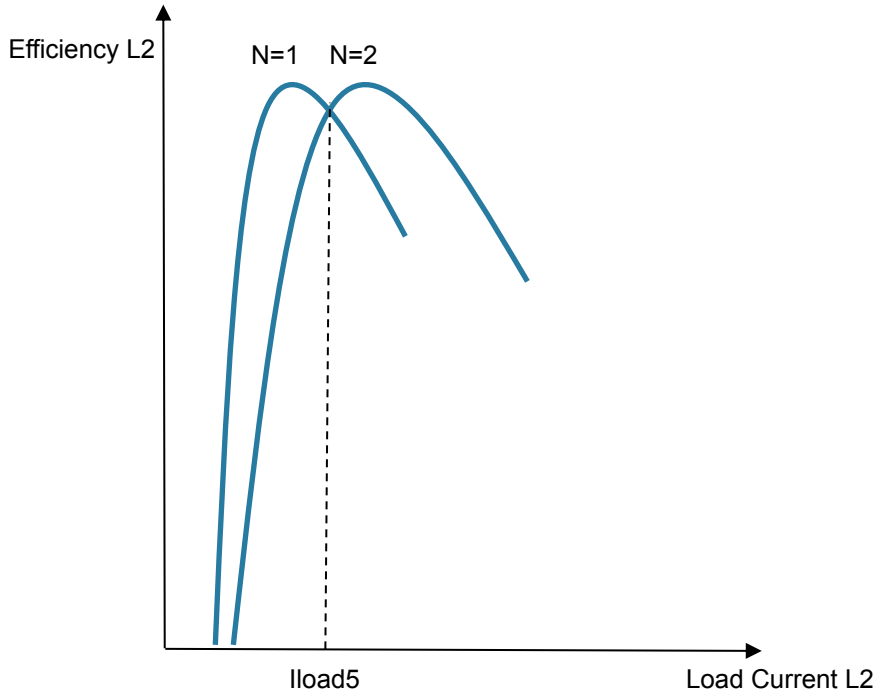
Figure 74. **DPM configuration efficiency-load current - Example 1**



Example 2:

PHASE_CFG = 0x15
Loop 1 uses phases 1:5 (phase 6 unused)
Loop 2 uses phase 1_L2:2_L2
DPM active on loop 2 disabled on Loop 1
PHASE2_ADD_TH = 0x00
PHASE3_ADD_TH = 0x00
PHASE4_ADD_TH = 0x00
PHASE5_ADD_TH = 0x00
PHASE6_ADD_TH = 0x00
PHASE7_ADD_TH = 0xFF
PHASE8_ADD_TH = 0xIload5

Figure 75. **DPM configuration efficiency-load current - Example 2**



3.14.7.2 *Active diode emulation (ADE)*

When operating in a single phase configuration under very light load condition, STPM098C allows a further efficiency boosting by forcing the controller to work in DCM (discontinuous current mode) and consequently reducing DrMOS conduction losses.

The n-th loop ADE activation can be disabled separately by means of a dedicated PMBus™ command as follows:

Table 70. **ADE disable bit**

CTRL_PFM_DIS	Description
0	ADE enabled (default)
1	ADE disabled

If ADE is disabled, when DPS reduces the number of active phases to 1, the controller will still works in CCM. CCM/DCM boundary condition is sensed by a dedicated zero-current comparator on ISENn which constantly monitors the current level.

If ISENn – CFILT/VREF1 ≤ ZC_OFFSET occurs for an interval longer than ZC_MASK_DELAY, the related PWM output is overridden to HIZ. PWM masking is removed at the next switching cycle.

Zero current detection threshold ZC_OFFSET can be offset with respect to zero level by means of two dedicated PMBus™ commands OFSZC<1:0> and GAINZC<3:0> as follows:

ZC_OFFSET = ZC_OFFSET (OFSZC) + ZC_OFFSET (GAINZC)

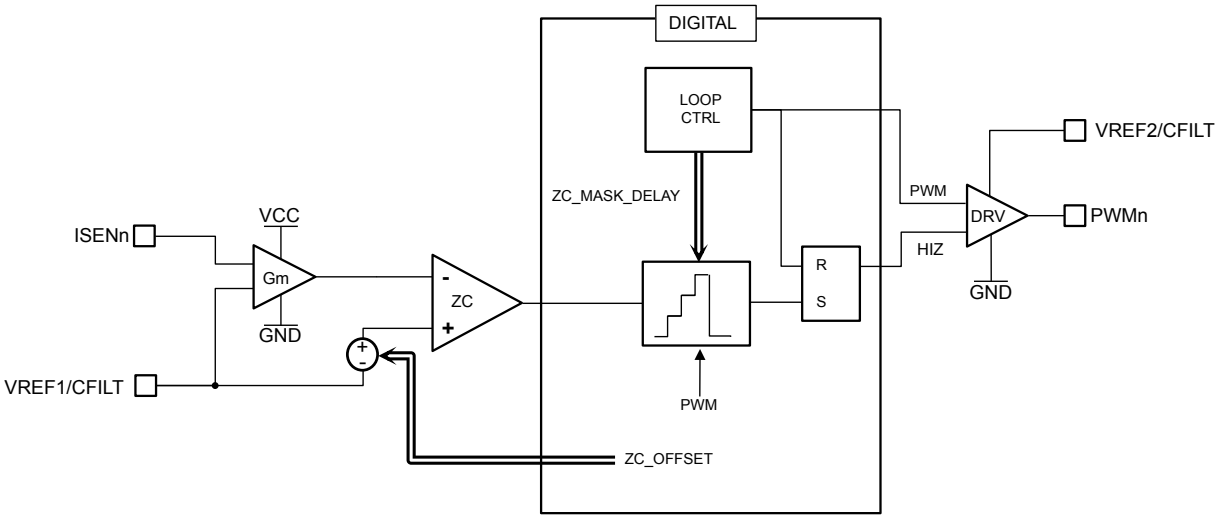
Table 71. **ZC offset1 configuration bit**

OFSZC1	OFSZC 0	Description
0	0	ZC_OFFSET = 0 mV (default)
0	1	ZC_OFFSET = 8 mV
1	0	ZC_OFFSET = 16 mV
1	1	ZC_OFFSET = 24 mV

Table 72. **ZC offset2 configuration bit**

GAINZC2	GAINZC1	GAINZC0	Description
0	0	0	ZC_OFFSET = -3.2 mV (default)
0	0	1	ZC_OFFSET = -9.6 mV
0	1	0	ZC_OFFSET = -16 mV
0	1	1	ZC_OFFSET = -22.4 mV
1	0	0	ZC_OFFSET = 22.4 mV
1	0	1	ZC_OFFSET = 16 mV
1	1	0	ZC_OFFSET = 9.6 mV
1	1	1	ZC_OFFSET = 3.2 mV

Figure 76. **Zero-current detection simplified block diagram**



Zero current detection masking time in terms of successive PWM periods can be configured by a dedicated PMBus™ bit ZC_MASK_DELAY<2:0>.

$$ZC_{MASK_{DELAY}} = ZC_{MASK_{DELAY_{lsb}}} \times \mathrm{ZC_{MASK_{DELAY[2:0]}}} \quad (65)$$

Where:

ZC_MASK_DELAY_lsb is the minimum masking step [25 ns].

ZC_MASK_DELAY [2:0] are the dedicated PMBus™ configuration bits [0 ~ 175 ns].

The default value is ZC_MASK_DELAY = 0x0.

This nonlinear control forces the DrMOS state according to control loop assertion while switch DrMOS to tristate as soon as phase current crosses the zero level, thus emulating an asynchronous rectification.

As a consequence of this behavior the loop controller reacts by linearly reducing the equivalent switching frequency that effectively results in lowered switching losses.

Figure 77. **ADE activation timing diagram**

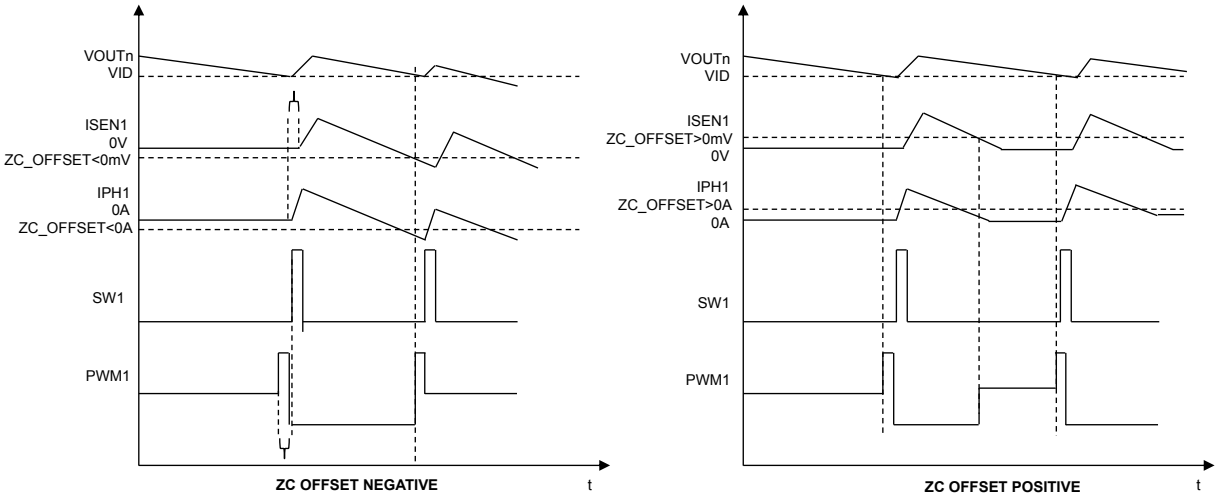
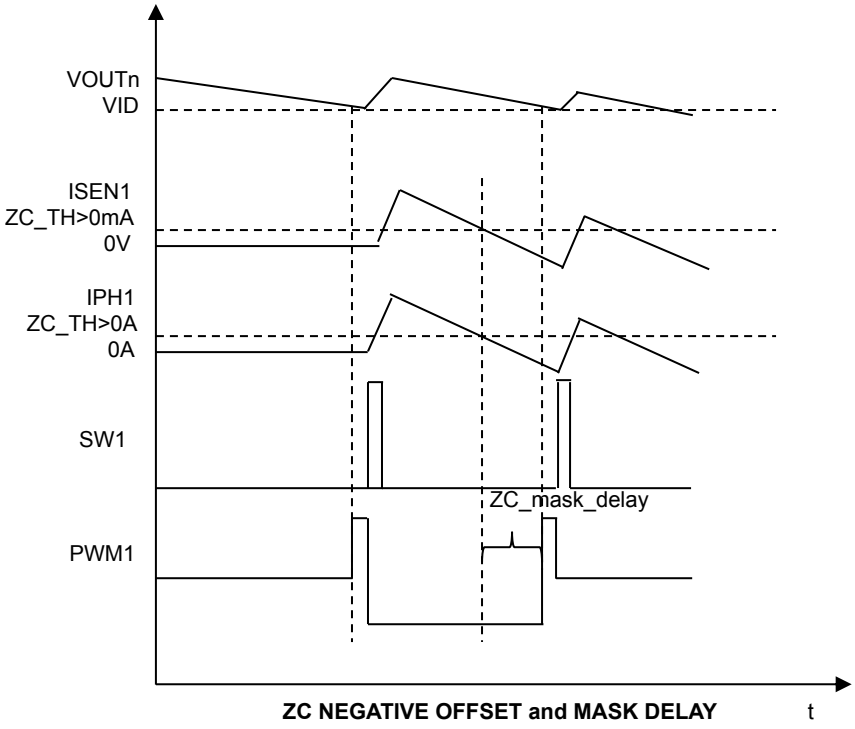


Figure 78. **ADE timing diagram with masking delay**



In order to prevent pulse skipping frequency reduction to enter the audible band, switching frequency clamp to 30 kHz can be applied by means of a dedicated PMBus™ command as follows:

Table 73. **ADE frequency clamp enable bit**

ULTRASONIC_ENA	Description
0	ADE frequency clamp disabled (default)
1	ADE frequency clamp enabled

3.15 Power system management bus interface (PMBus™)

STPM098C implements a standard 2-pin PMBus™ interface to access both IC configuration and status registers up to 400 kHz baud rate (up/down-stream).

3.15.1 Protocol description

3.15.1.1 Physical layer

Figure 79. **PMBus™ AC characteristics timing diagram**

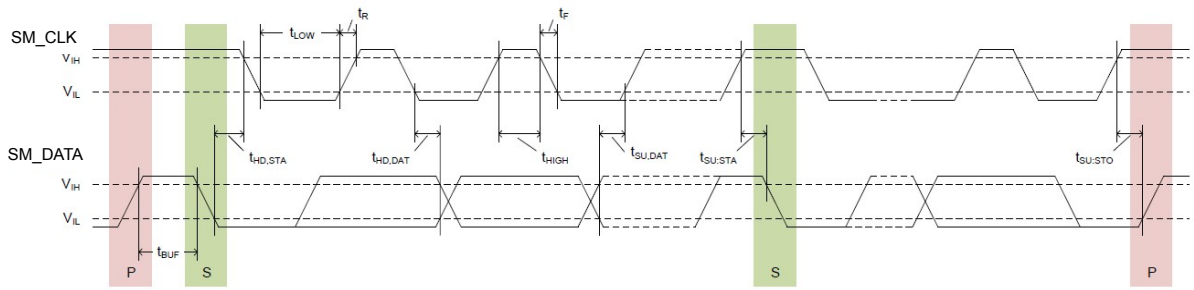


Table 74. **PMBus™ 100 kHz class AC characteristics**

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
PMBus™_fpmb	PMBus™ operating frequency		10	-	100	kHz	-
PMBus™_tbuf	Bus free time between STOP and START condition		4.7	-	-	µs	-
	Hold time after (REPEATED) START condition		4.0	-	-	µs	After this period the first clock is generated
PMBus™_tsusta	REPEATED START condition setup time		4.7	-	-	µs	-
PMBus™_tsusto	STOP condition setup time		4.0	-	-	µs	-
PMBus™_thddat	Data hold time		0	-	-	ns	-
PMBus™_tsudat	Data setup time		250	-	-	ns	-
PMBus™_timeout	Detect clock low timeout		25	-	35	ms	-
PMBus™_tlow	Clock low period		4.7	-	-	µs	-
PMBus™_thigh	Clock high period		4.0	-	50	µs	-
PMBus™_tlowsext	Cumulative clock low extend time (target device)		-	-	25	ms	-
PMBus™_tlowmext	Cumulative clock low extend time (controller device)		-	-	10	ms	-
PMBus™_tf	Clock/data fall time		-	-	300	ns	-
PMBus™_tr	Clock/data rise time		-	-	1000	ns	-

Table 75. **PMBus™ 400 kHz class AC characteristics**

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
PMBus™_fpmb	PMBus™ operating frequency		10	-	400	kHz	-
PMBus™_tbuf	Bus free time between STOP and START condition		1.3	-	-	µs	-

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
PMBus™_thdsta	Hold time after (REPEATED) START condition		0.6	-	-	µs	After this period the first clock is generated.
	REPEATED START condition setup time		0.6	-	-	µs	-
PMBus™_tsusto	STOP condition setup time		0.6	-	-	µs	-
PMBus™_thddat	Data hold time		300	-	-	ns	-
PMBus™_tsudat	Data setup time		100	-	-	ns	-
PMBus™_timeout	Detect clock low timeout		25	-	35	ms	-
PMBus™_tlow	Clock low period		1.3	-	-	µs	-
PMBus™_thigh	Clock high period		0.6	-	50	µs	-
PMBus™_tlowsext	Cumulative clock low extend time (target device)		-	-	25	ms	-
PMBus™_tlowmext	Cumulative clock low extend time (controller device)		-	-	10	ms	-
PMBus™_tf	Clock/data fall time		20	-	300	ns	-
PMBus™_tr	Clock/data rise time		20	-	300	ns	-
PMBus™_tspike	Noise spike suppression time		-	-	-	ns	-

3.15.1.2 *Network layer*

Target address assignment

STPM098C PMBus™ target address assignment can be defined through pin SM_ADDR by applying a defined voltage. SM_ADDR input voltage is digitized by a dedicated ADC and encoded in a 7-bit word among 8 possible addresses.

Note: SM_ADDR voltage is supposed to be programmed by means of a resistive partition from the VCC reference line. According to this concept target Address programming resistances can be retrieved by solving the following equations in sequence:

1. *Total resistance* $\rightarrow R_{TOT} = R_{ADDRH} + R_{ADDRL} = \frac{V_{CC}}{I_{VCC_{MAX}}}$

   Where Ivcc_max is the maximum current allowed to be sunk from VCC by resistive partition.

2. *Partition factor* $\rightarrow \alpha = \frac{R_{ADDRH}}{R_{ADDRL}} = \frac{V_{CC}}{SM_{ADDR}} - 1$

   Where SM_ADDR is the desired voltage at SM_ADDR pin.

Table 76. SM_ADDR voltage ADC electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
ADC input							
ADDR_adc_range	ADDR ADC voltage input range		0	-	5	V	-
ADDR_adc_ic	ADDR ADC input current	SM_ADDR = 5 V	20	30	40	µA	-
ADC input resolution							
ADDR _adc_resolution	ADDR ADC resolution		-	10	-	bits	Application information
ADDR_adc_lsb	ADDR ADC LSB		-	5.3	-	mV	Application information
ADC input accuracy							
ADDR_adc_total_err	ADDR ADC total error		-60	-	60	mV	-
ADC input dynamic characteristics							
ADDR_adc_in_sr	ADDR ADC sample rate	CLK_SSM_EN = 0	-	10	-	MHz	Application information
ADDR_adc_latency	ADDR ADC conversion latency		-	65	100	µs	Application information

Input voltage at SM_ADDR pin is encoded according to the following table:

Table 77. Target Address versus SM_ADD voltage

SM_ADDR	PMBus™ address [bin]	PMBus™ address [dec]
0.4739 ±40 mV	1011000	88
0.9017 ±70 mV	1011001	89
1.3123 ±100 mV	1011010	90
1.6611 ±130 mV	1011011	91
2.2883 ±170 mV	1011100	92
3.1153 ±220 mV	1011101	93
3.7523 ±250 mV	1011110	94
4.4464 ±280 mV	1011111	95

Note: SM_ADDR voltage ranges are not overlapping. Should the pin voltage fall between two adjacent ranges, the address the device is going to use cannot be predicted nor guaranteed in advance; however, once determined, it will not be changing until the next device power cycle, as expected.

Supported protocols

To access STPM098C's configuration and monitoring units, the PMBus™ interface supports the following list of command protocols:

- Send byte with PEC
- Read byte with PEC
- Write byte with PEC
- Read word with PEC
- Write word with PEC
- Read 32 with PEC
- Write 32 with PEC

3.16 Functional safety

3.16.1 Safe state

To reach the safety requirements of the system, the following safe state is supported by STPM098C:

SAFE-HIZ

When SAFE-HIZ is active the controller unit is disabled by forcing the PWM outputs in a tristate mode so that PWMn = HIZ [n = 1, 2, 3, 4, 5, 6, 7, 8].

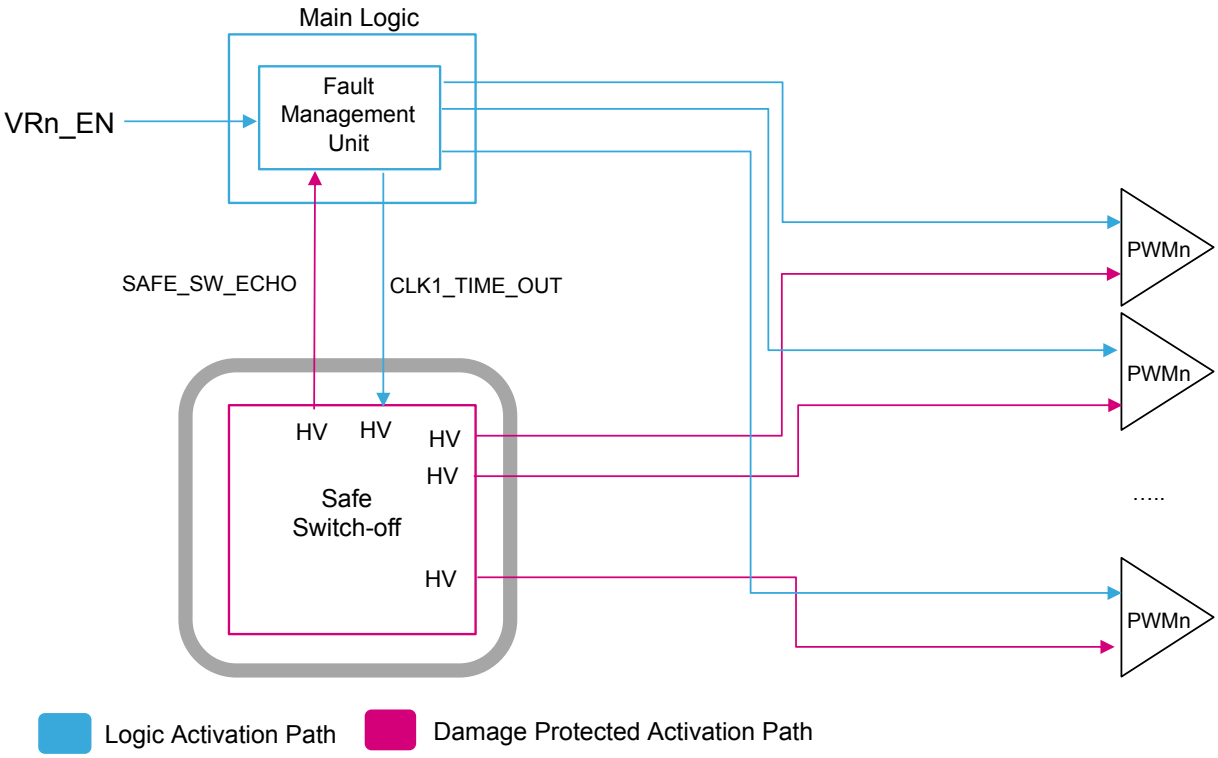
SAFE-HIZ is activated by default if the following conditions are verified:

- Latched fault detection
- Configurable fault with related FRC set to 1

3.16.2 Safe state activation

The safe state activation is established through two separate paths.

Figure 80. Safe states activation paths



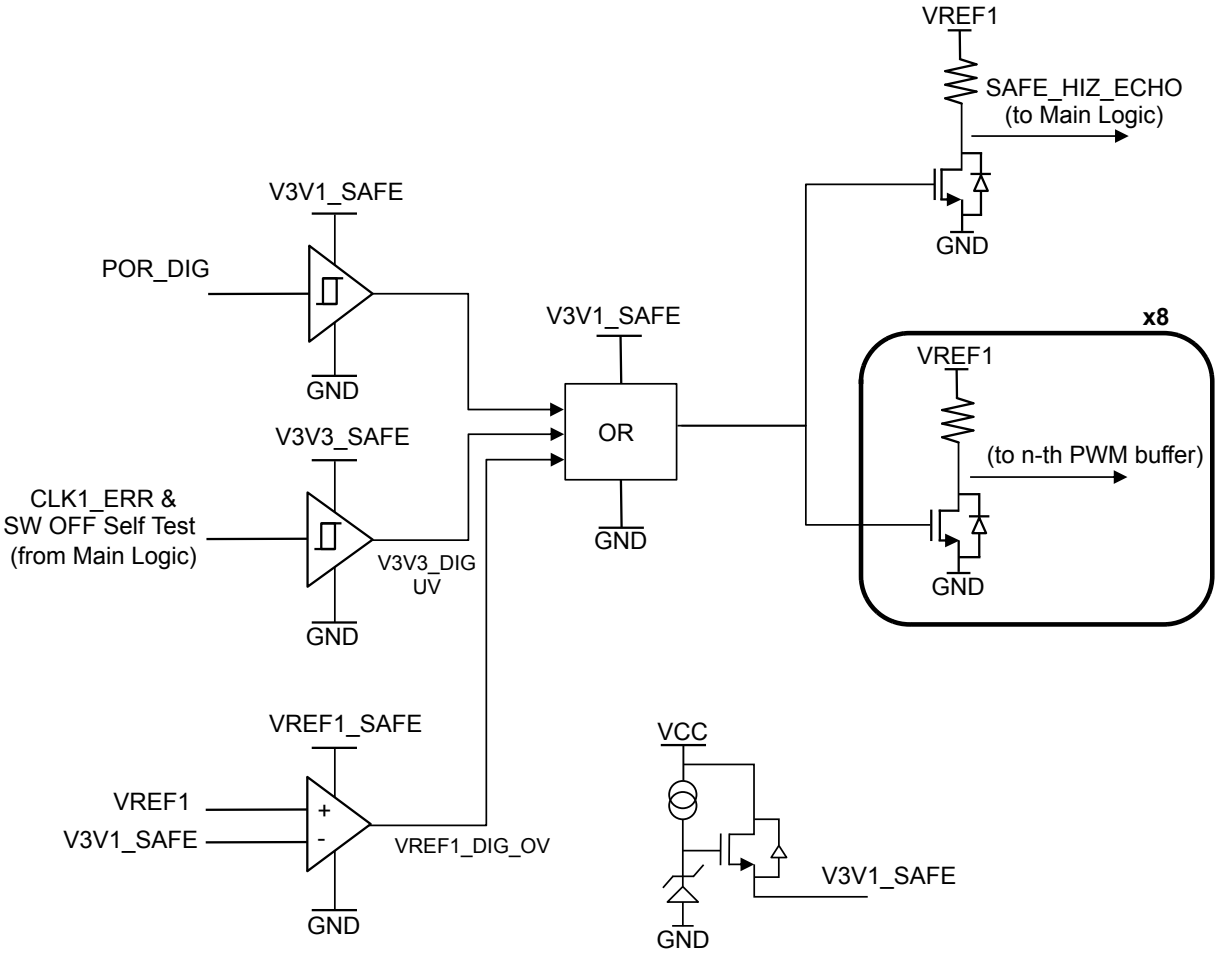
Logic activation path: safe state activation is carried out entirely by the main logic. This path is used to enter SAFE-HIZ state except if it is determined by CLK1_TIME_OUT and VREF1_UV/OV.

Damage protected activation path: in case of device failure where the internal main logic integrity is compromised, STPM098C implements an isolated safe switch off structure which allows it to activate through a separated path. This path is used to generate:

- VREF1_OV
- VREF1_UV
- CLK1_TIME_OUT

The safe state activation through the damage protected path is signaled by setting to '1' the dedicated PMBus™ read only register SAFE_HIZ_ECHO.

Figure 81. **Damage protected activation simplified structure**



4 Current consumption

Table 78. Mean current consumptions in loop operating mode

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
ISTBY_VCC1	Current consumption on VCC. No PWM switching.	VCC = 5 V -40 °C ≤ T_j ≤ 25 °C Default configuration and VR_EN1 = VR_EN2 = 0 V	50	70	100	mA
ISTBY_VCC2	Current consumption on VCC. No PWM switching.	VCC = 5 V 25°C ≤ T_j ≤ 150 °C Default configuration and VR_EN1 = VR_EN2 = 0 V	50	70	100	mA

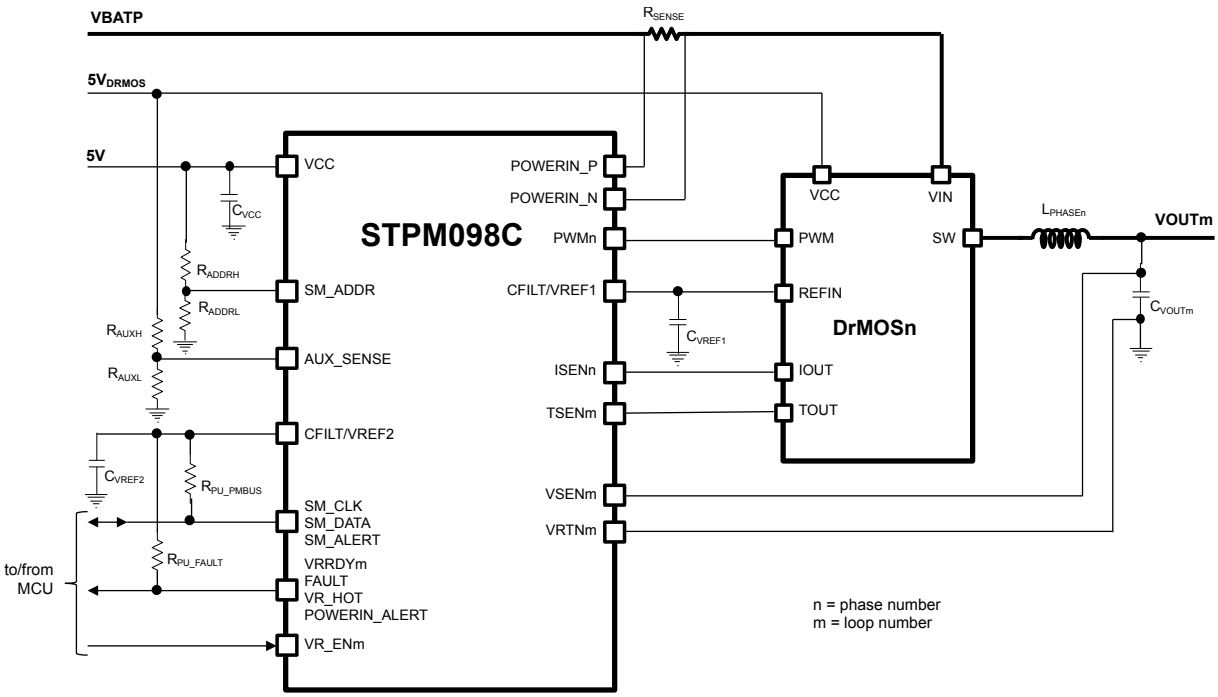
Note:

- *Current consumption on VCC when PWM are switching can be estimated by incrementing the STBY consumption by the extra current needed by the n-th switching PWM buffer to drive the external capacitive load.*
  $I_{PWMn} = \frac{C_{Load} f_{sw} VREF2}{CFILT}$
  Where fsw is the phase`s switching frequency and Cload is the input capacitance of DrMOS PWM pin.
- *Indicated current consumptions include only STPM098C related contribution strictly needed to its functional operation. As a consequence, they do not include consumption due to additional applicative elements connected to the device (example DrMOS REFIN loading, PMBus™ interface pull-up resistances, external resistive partitioning etc.)*

5 Application circuit

The following schematic is a reference application circuit for the STPM098C multiphase regulator; it shows the minimum required components for the device to operate. Power section details (DrMOS and its related components, output inductor and capacitors), are strongly dependent on the customer's system choice, as well as the number of phases assigned to each loop, so the proposed part numbers and values suggested are intended to be only indicative.

Figure 82. Reference application circuit



VBATP is the battery line protected against battery reverse events, as well as any other possible damaging disturbances that might occur, according to specific standards requirements. Methods for battery line protection are in charge of the system design. From the STPM098C point of view, VBATP line must not exceed POWERIN_P and POWERIN_N absolute maximum ratings.

5 V goes to VCC, which is the main supply line for STPM098C; in the proposed schematic it is separated from DrMOS main supply line but they could be possibly shared, according to system design needs. STPM098C's AUX_SENSE input can be used to monitor DrMOS dedicated supply line for diagnostic and safety purposes.

STPM098C fault lines, VR_EN and PMBus™ lines are to be connected to an automotive grade MCU. For safety architecture implementation, the same MCU could be used to also acquire other feedback signals coming from DrMOS, as instance, for temperature check or output voltage monitoring.

5.1 Bill of material

Table 79. Reference bill of material

Name	Min	Typ	Max	Unit	Minimum requirements	Notes
C_{VCC}	-	10	-	µF	6.3 V	To be placed close to the VCC pin
C_{VREF1}	-	4.7	-	µF	6.3 V	To be placed close to the VREF1 pin
C_{VFRE2}	-	4.7	-	µF	6.3 V	To be placed close to the VFRE2 pin
C_{VOUTm}	-	-	-	-	-	According to the customer's configuration
DrMOSn	-	-	-	-	-	STSHB50

Name	Min	Typ	Max	Unit	Minimum requirements	Notes
L_{PHASEn}	-	160	-	nH	I_{RMS_MIN} = 30 A	Shielded high current power inductor
R_{ADDRH}	-	4.7	-	kΩ	0.01 W	-
R_{ADDRL}	-	4.7	-	kΩ	0.01 W	-
R_{AUXH}	-	4.7	-	kΩ	0.01 W	-
R_{AUXL}	-	4.7	-	kΩ	0.01 W	-
R_{PU_FAULT}	-	4.7	-	kΩ	0.01 W	-
R_{PU_PMBUS}	-	4.7	-	kΩ	0.01 W	-
R_{SENSE}	-	1	-	mΩ	1%, 2 W	-

5.1.1 Output capacitors configuration example

As a reference example, next table shows output capacitors bill of material for a customer's application with the following characteristics:

Loop 1

- N. of phases: 6 (with dynamic phase shedding enabled)
- Output inductors: 160 nH
- Vout: 0.75 V
- I_{LOAD_MAX}: 180 A
- PWM frequency: 500 kHz

Loop 2

- N. of phases: 2 (with dynamic phase shedding enabled)
- Output inductors: 160 nH
- Vout: 0.75 V
- I_{LOAD_MAX}: 45 A
- PWM frequency: 500 kHz

For each control loop, capacitors are grouped in 2 banks to be placed, namely, close to output inductors and close to load.

Table 80. Output capacitors example BOM

		N.	Value [µF]	Requirements	Package	Total C [mF]
Loop 1	C_{VOUT1_1}	15	22	6.3 V, 10%	1206	4.745
		15	1	10 V, 10%	0402	
		20	220	4 V, 20%	1210	
	C_{VOUT1_2}	40	220	4 V, 20%	1210	8.839
		1	10	4 V, 20%	0603	
		29	1	10 V, 10%	0402	
Loop 2	C_{VOUT2_1}	8	220	4 V, 20%	1206	1.76
	C_{VOUT2_2}	4	10	4 V, 20%	0603	0.503
		2	220	4 V, 20%	1210	
		23	1	10 V, 10%	0402	

6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

6.1 VFQFN48+4L (7x7x0.9 mm exp. pad down) package information

Figure 83. **VFQFN48+4L (7x7x0.9 mm exp. pad down) package outline**

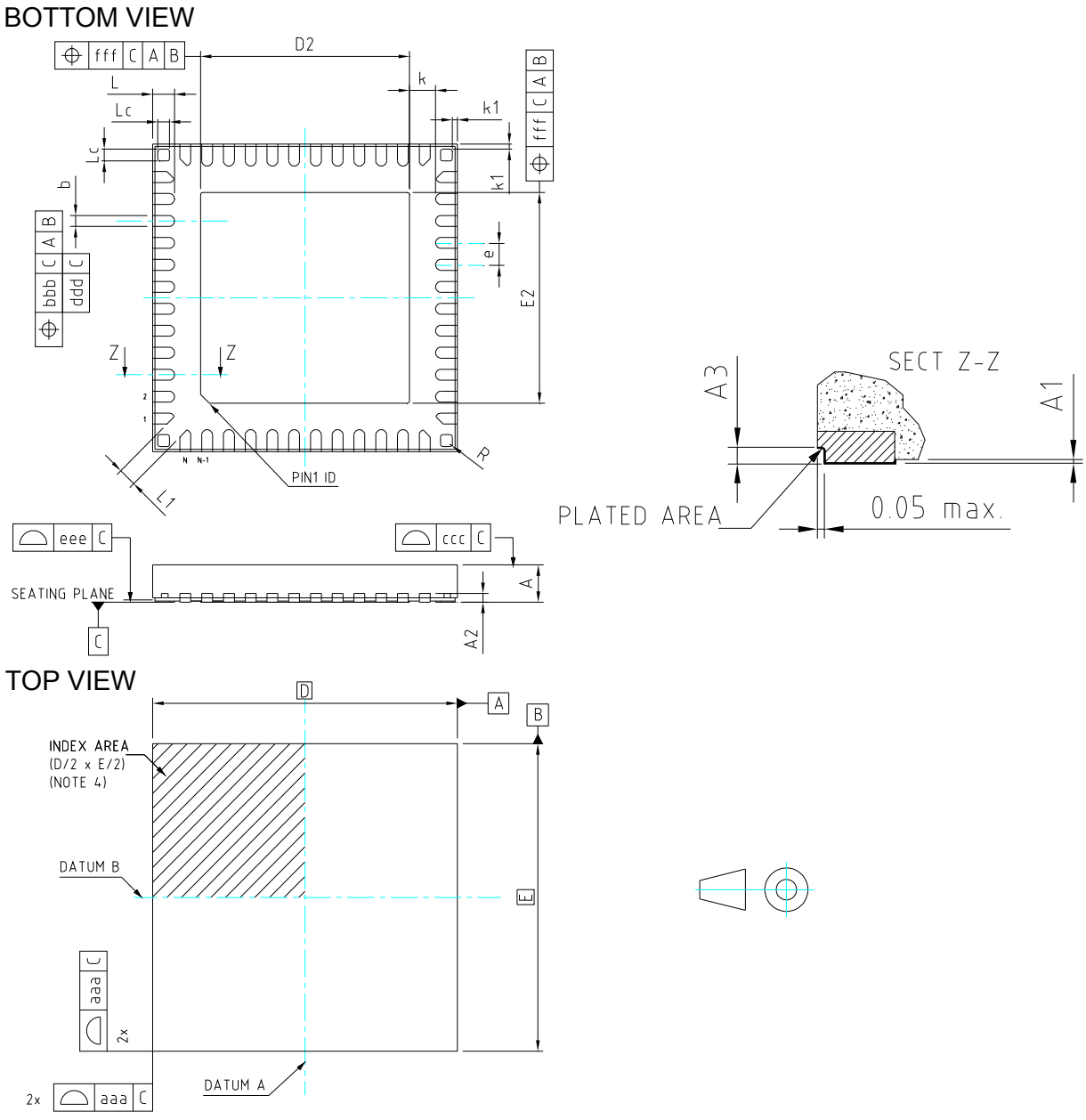


Table 81. **VFQFN48+4L (7x7x0.9 mm exp. pad down) package mechanical data**

Symbol	Dimensions in mm		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A2		0.2 REF	
A3	0.10	-	-
b	0.20	0.25	0.3
D	-	7.00	-
D2	5.30	5.40	5.50
e	-	0.5	-
E	-	7.00	-
E2	5.30	5.40	5.50
L	0.45	0.50	0.55
Lc	0.22	0.27	0.32
L1	0.35	-	-
k	0.25	-	-
k1	-	0.115	-
R	-	0.05	-
N		48+1	
Tolerance of form and position			
aaa		0.15	
bbb		0.10	
ccc		0.08	
ddd		0.05	
eee		0.10	
fff		0.10	
REF		-	

Revision history

Table 82. **Document revision history**

Date	Version	Changes
16-Jan-2024	1	Initial release.

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