MP5490

Fully Integrated Power Management Solution with 4-Channel IDACs and Multi-Channel ADCs with Negative Bias for Optical Modules

DESCRIPTION

The MP5490 is a complete power management solution that is well-suited for the transmitter optical subassembly (TOSA) of optical modules. The MP5490 integrates four high-accuracy current sources (IDx) for distributed feedback (DFB) laser diodes (LDs), and four negative voltage biases for an electro-absorption modulated laser (EML) bias. The MP5490 also provides 4-channel EML current measurements and monitoring photodetector (MPD) current measurements to simplify the design.

The integrated 6 channels of high-accuracy and low temperature coefficient analog-to-digital converters (ADCs) can be used to read the external current, voltage, and temperature to save microcontroller (MCU) resources.

All output rails can be adjusted via the I^2C bus or preset via the multi-page one-time programmable (MOTP) memory.

The MP5490 requires a minimal number of external components, and is available in a space-saving WLCSP-36 (3mmx4.25mm) package.

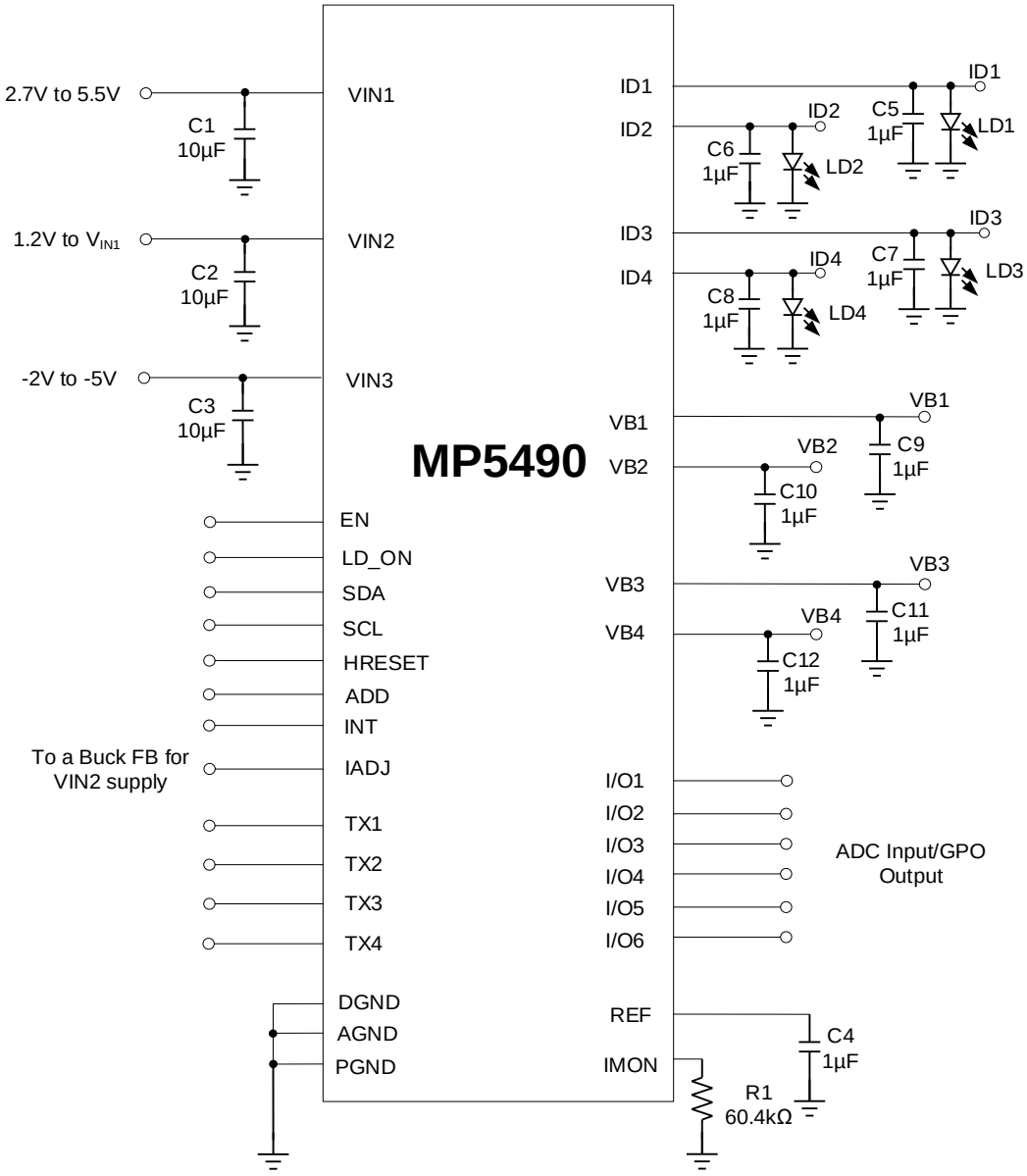
FEATURES

- 4-Channel, Configurable Accurate ID Current Source:
  - Up to 250mA per Channel
  - 10-Bit Digital-to-Analog Converter (DAC) for ID Current
- 4-Channel, Configurable Accurate Electro-Absorption Modulated Laser (EML) Bias Voltage:
  - Options to Range between -0.1V and -2.5V or -0.1V and -5V
  - Up to 60mA of Load Current per Channel
  - 10-Bit DAC for EML Bias Voltage
- 4-Channel Monitoring Photodetector (MPD) Measurement:
  - Range from 0mA to 5mA
- 6-Channel General-Purpose Input/Output (GPIO):
  - Supports Analog-to-Digital Converter (ADC) Input or GPO Output
  - Selectable Open-Drain or Push-Pull GPO
- High-Accuracy, 12-Bit ADC:
  - 0V to 2.5V External ADC Input
  - 4-Channel ID Voltage Measurement
  - 4-Channel EML Current Measurement
- System:
  - I^2C Control Interface
  - I^2C Hardware Reset via HRESET
  - Supply and Temperature Fault Alarms
  - Available in a WLCSP-36 (3mmx4.25mm) Package

APPLICATIONS

- Optical Modules

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP5490GC-0000	WLCSP-36 (3.0mmx4.25mm)	*See Below*	1
MP5490GC-xxxx**	WLCSP-36 (3.0mmx4.25mm)		

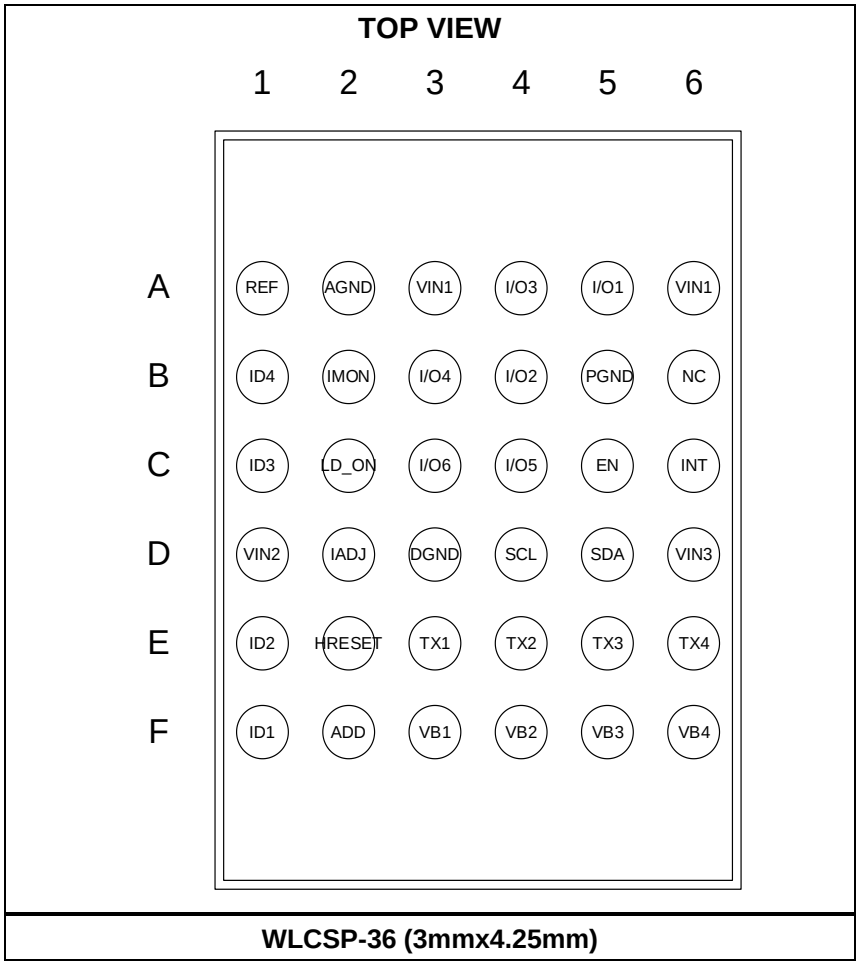
* For Tape & Reel, add suffix -Z (e.g. MP5490GC-xxxx-Z).

** “xxxx” is the configuration code identifier for the register setting stored in the MOTP. The default number is “0000” (MP5490GC-0000). Each “x” can be a hexadecimal value between 0 and F. Work with an MPS FAE to create this unique number, even if ordering the “0000” code.

TOP MARKING

BMF: Product code of MP5490GC
Y: Year code
WW: Week code
LLL: Lot number

PACKAGE REFERENCE



WLCSP-36 (3mmx4.25mm)

PIN FUNCTIONS

Pin #	Name	Description
A1	REF	**2.5V reference**. Bypass the REF pin with a 1μF ceramic capacitor connected to AGND.
A2	AGND	**Analog ground.**
A3, A6	VIN1	**Power supply input for analog and digital circuitry.** Bypass the VIN1 pin with a 10μF ceramic capacitor connected to AGND.
A4	I/O3	**ADC input or GPO output port 3.** This pin can be adjusted via the I²C.
A5	I/O1	**ADC input or GPO output port 1.** This pin can be adjusted via the I²C.
B1	ID4	**Channel 4 current source.** This pin's output current is controlled by the internal register.
B2	IMON	**Current reference setting pin.** Connect a high-accuracy resistor with a low temperature coefficient (60.4kΩ) to AGND.
B3	I/O4	**ADC input or GPO output port 4.** This pin can be adjusted via the I²C.
B4	I/O2	**ADC input or GPO output port 2.** This pin can be adjusted via the I²C.
B5	PGND	**Power ground.**
B6	NC	**No connection internally.**
C1	ID3	**Channel 3 current source.** This pin's output current is controlled by the internal register.
C2	LD_ON	**Channel 1–4 current source enable control.**
C3	I/O6	**ADC input or GPO output port 6.** This pin can be adjusted via the I²C.
C4	I/O5	**ADC input or GPO output port 5.** This pin can be adjusted via the I²C.
C5	EN	**Enable pin.** The EN pin controls all of the MP5490's analog circuits. The I²C interface and registers are not controlled by the EN pin.
C6	INT	**Interrupt pin.** Open drain output.
D1	VIN2	**Power supply for current source ID1–ID4.** Bypass the VIN2 pin with a 10μF ceramic capacitor connected to PGND.
D2	IADJ	**Adjustable interface**. Connect the IADJ pin to a buck converter's FB pin, then it can control the buck's output via the I²C. Float this pin if it is not used.
D3	DGND	**Digital ground.**
D4	SCL	**I²C clock signal input.**
D5	SDA	**I²C data pin.**
D6	VIN3	**Power supply for EML bias voltage VB1–VB4.** Bypass the VIN3 pin with a 10μF ceramic capacitor connected to PGND.
E1	ID2	**Channel 2 current source.** This pin's output current is controlled by the internal register.
E2	HRESET	**I²C interface hardware reset pin.** A high logic on this pin refreshes the I²C interface but maintains the I²C's register values.
E3	TX1	**Channel 1 MPD current measurement pin.** This pin senses the MPD current. It is internally powered by the negative bias source (VIN3).
E4	TX2	**Channel 2 MPD current measurement pin.** This pin senses the MPD current. It is internally powered by the negative bias source (VIN3).
E5	TX3	**Channel 3 MPD current measurement pin.** This pin senses the MPD current. It is internally powered by the negative bias source (VIN3).
E6	TX4	**Channel 4 MPD current measurement pin.** This pin senses the MPD current. It is internally powered by the negative bias source (VIN3).
F1	ID1	**Channel 1 current source.** This pin's output current is controlled by the internal register.
F2	ADD	**Address setting for I²C.** Connect one resistor from the ADD pin to AGND. A different resistor sets different I²C addresses.

PIN FUNCTIONS *(continued)*

Pin #	Name	Description
F3	VB1	**Channel 1 EML bias voltage.** This pin's output voltage is controlled by the internal register. This pin also requires a 1μF decoupling capacitor.
F4	VB2	**Channel 2 EML bias voltage.** This pin's output voltage is controlled by the internal register. This pin also requires a 1μF decoupling capacitor.
F5	VB3	**Channel 3 EML bias voltage.** This pin's output voltage is controlled by the internal register. This pin also requires a 1μF decoupling capacitor.
F6	VB4	**Channel 4 EML bias voltage.** This pin's output voltage is controlled by the internal register. This pin also requires a 1μF decoupling capacitor.

ABSOLUTE MAXIMUM RATINGS (1)

V_{IN1}, V_{IN2}..... -0.3V to +6.5V
V_{IN3}.....-6.5V to +0.3V
V_{B1}, V_{B2}, V_{B3}, V_{B4}.....V_{IN3} - 0.3V to +0.3V
T_{X1}, T_{X2}, T_{X3}, T_{X4}.....V_{IN3} - 0.3V to +0.3V
All other pins.....-0.3V to +6.25V
Continuous power dissipation (T_A = 25°C) (2) (4)
.....4.62W
Junction temperature (T_J)..... 150°C
Lead temperature.....260°C
Storage temperature..... -65°C to +150°C

ESD Ratings

Human body model (HBM) ..... ±2000V
Charged-device model (CDM).....±1000V

Recommended Operating Conditions (3)

Supply voltage (V_{IN1}).....2.7V to 5.5V
Supply voltage (V_{IN2}).....1.2V to V_{IN1}
Supply voltage (V_{IN3}).....-2V to -5V
IDx current source range.....0mA to 250mA
EML bias VB range.....-0.1V to -2.5V/-5V
MPD current sensor range.....0mA to 5mA
Operating junction temp (T_J).... -40°C to +125°C

Thermal Resistance θ_{JA} θ_{JC}

WLCSP-36 (3.0mmx4.25mm)
EV5490-C-00A (4).....27.....6.5.. °C/W
JESD51-7 (5) .....27.8 ....6.6.. °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on the EV5490-C-00A, a 4-layer PCB.
5) The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7 and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

ELECTRICAL CHARACTERISTICS

V_{IN1} = 3.3V, V_{IN2} = 1.8V, V_{IN3} = -3.3V, T_J = -40°C to 125°C (6), unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Supply						
VIN1 voltage (V_{IN1}) under-voltage lockout (UVLO) rising threshold	V_{IN1_R}		2.25	2.4	2.55	V
V_{IN1} UVLO hysteresis	V_{IN1_HYS}			200		mV
VIN2 voltage (V_{IN2}) UVLO rising threshold	V_{IN2_R}		0.8	0.9	1	V
V_{IN2} UVLO hysteresis	V_{IN2_HYS}			135		mV
VIN3 voltage (V_{IN3}) UVLO rising threshold	V_{IN3_R}		-1.9	-1.7	-1.5	V
V_{IN3} UVLO hysteresis	V_{IN3_HYS}			100		mV
Supply current	I_{IN1}	EN on, ID and EML on, no load		4.7	5.5	mA
		EN off		2.3	3	mA
Logic Input (EN, HRESET, and LD_ON pins)						
Input logic high voltage			0.8			V
Input logic low voltage					0.4	V
Internal pull-down resistor				1		MΩ
Analog Signals						
IADJ source current capability				15.5		µA
IADJ sink current capability				-15.5		µA
Reference voltage			2.485	2.5	2.515	V
IMON voltage			1.195	1.2	1.205	V
ID Current Source						
VIN2 to ID pin dropout voltage		Load = 250mA			400	mV
Discharge resistor		Pull LD_ON low		10		Ω
LD_ON turn-on delay (7)	t_{LD_ON}	From LD_ON high to IDx current starts to rise, SR bits = 01		30		µs
LD_ON turn-off delay (7)	t_{LD_OFF}	From LD_ON low to ID current start drop		2		µs
ID current slew rate		SR bits = 01		0.75		mA/µs
ID current accuracy		ID = 100mA	-1.5		+1.5	%
		ID = 250mA	-2		+2	%
Short-circuit protection (SCP) hiccup time period (7)		IDx short to PGND		80		ms
EML Bias Voltage						
EML current capability		Per channel	60			mA
VIN3 to VB pin dropout voltage		Load = 60mA			500	mV
Discharge resistor		Pull EN low		110		Ω
VB voltage slew rate		VB_EN bits on		7		mV/µs

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN1} = 3.3V, V_{IN2} = 1.8V, V_{IN3} = -3.3V, T_J = -40°C to 125°C (6), unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
EML bias voltage accuracy		VB = -1.2V, load = 1mA, T_J = 25°C	-1		+1	%
		VB = -1.2V, load = 1mA, T_J = -40°C to +85°C	-3		+3	%
Power supply rejection ratio (7)		500kHz, I_{BX} = 10mA, C_{BX} = 1µF		40		dB
		1000kHz, I_{BX} =10mA, C_{BX} = 1µF		20		dB
Internal over-current protection (OCP) threshold (7)		VBx short to PGND		150		mA
Interrupt (INT)						
INT pin output low voltage		Sink 5mA			0.4	V
INT pin leakage current		INT logic high, pull up to 3.3V			1	µA
Voltage Analog-to-Digital Converter (ADC) EC Parameters						
I/O input voltage range			0		2.5	V
I/O ADC offset		ADC input: 0.1V, 1.2V, and 2.4V	-7		+7	mV
ADC conversion time				25		µs
Thermal Warning and Shutdown						
Thermal shutdown entry threshold (7)	T_{SD}			160		°C
Thermal shutdown recovery threshold (7)				130		°C
Thermal warning threshold (7)	T_{WARN}			120		°C
Thermal warning hysteresis (7)	T_{WARN_HYS}			20		°C

Notes:

6) Not tested in production; guaranteed by over-temperature correlation.
7) Guaranteed by engineering sample characterization; not tested in production.

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN1} = 3.3V, V_{IN2} = 1.8V, V_{IN3} = -3.3V, T_J = 25°C, unless otherwise noted.

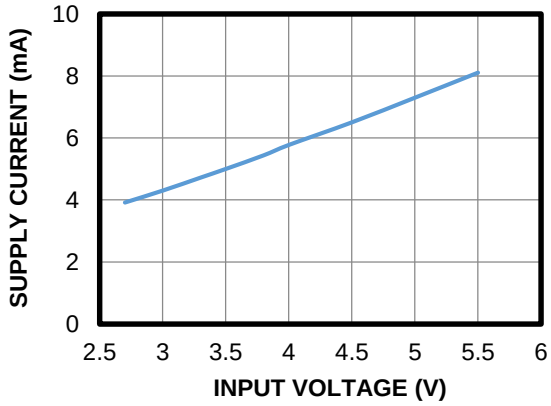
Parameter	Symbol	Condition	Min	Typ	Max	Units
I^2C Interface						
SCL, SDA input high voltage			1.2			V
SCL, SDA input low voltage					0.4	V
SDA output low voltage		Sink 5mA			0.4	V
I^2C clock frequency					400	kHz
SCL high time	t_{HIGH}		0.6			µs
SCL low time	t_{LOW}		1.3			µs
Data set-up	t_{SU_DAT}		0.1			µs
Data hold time	t_{HD_DAT}		0		0.9	µs
Set-up time for repeated start	t_{SU_STA}		0.6			µs
Hold time for (repeated) start	t_{HD_STA}		0.6			µs
Bus free time between a start and a stop command	t_{BUF}		1.3			µs
Set-up time for stop command	t_{SU_STO}		0.6			µs
Rise time of SCL and SDA	t_R		20 + 0. 1 x C_B		300	ns
Fall time of SCL and SDA	t_F		20 + 0. 1 x C_B		300	ns
Pulse width of suppressed Spike	t_{SP}		0		50	ns
Capacitance for each bus Line	C_B				400	pF

TYPICAL CHARACTERISTICS

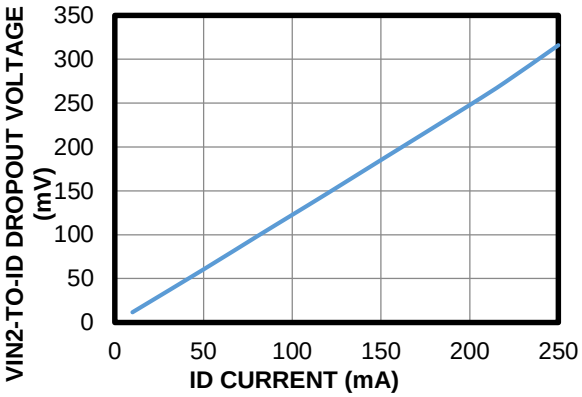
V_{IN1} = 3.3V, V_{IN2} = 1.8V, V_{IN3} = -3.3V T_A = 25°C, unless otherwise noted.

Supply Current vs. Input Voltage

EN on, ID and EML on, no load

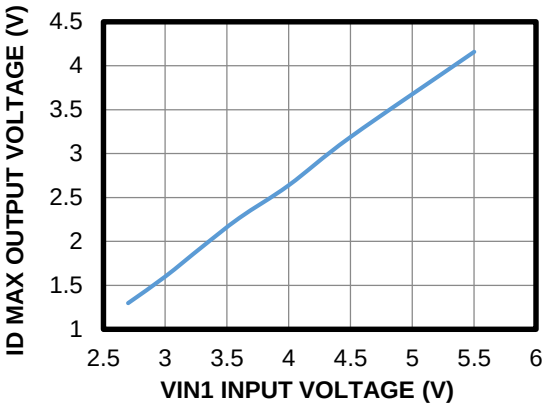


VIN2-to-ID Dropout Voltage vs. ID Current

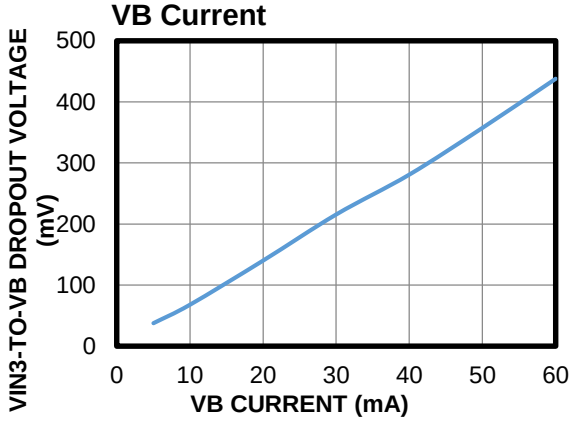


ID Max Output Voltage vs. VIN1 Input Voltage

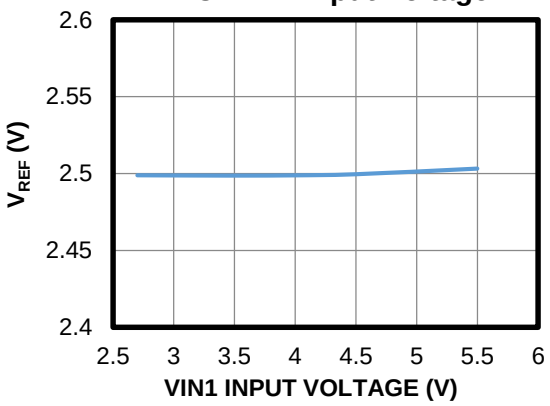
ID current = 250mA



VIN3-to-VB Dropout Voltage vs. VB Current



V_{REF} vs. VIN1 Input Voltage

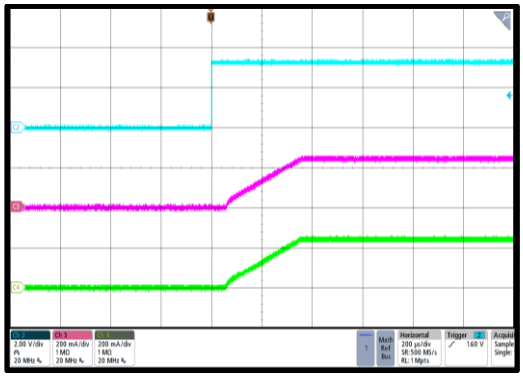


TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN1} = 3.3V, V_{IN2} = 1.8V, V_{IN3} = -3.3V, T_A = 25°C, unless otherwise noted.

Turn On via LD_ON

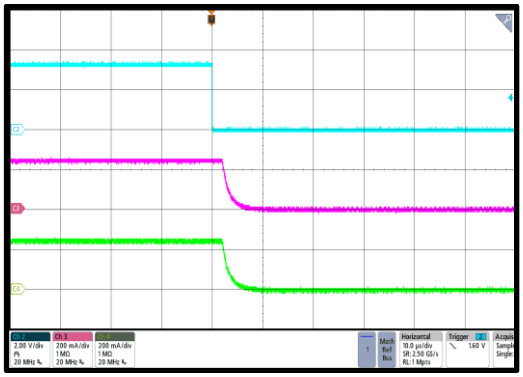
ID1 = ID3 = 250mA, SR bit = 01



200µs/div.

Turn Off via LD_ON

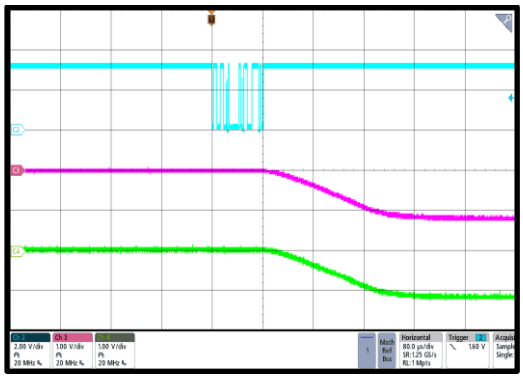
ID1 = ID3 = 250mA



10µs/div.

VB_EN Bit On

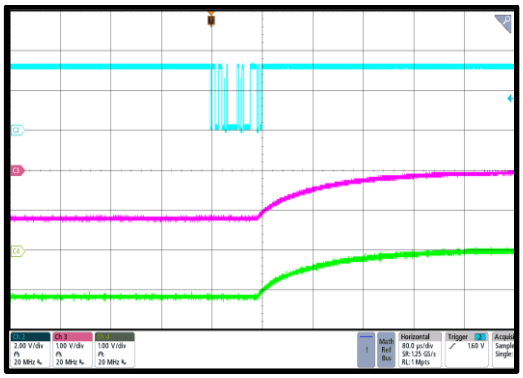
VB1 = VB3 = -1.2V



80µs/div.

VB_EN Bit Off

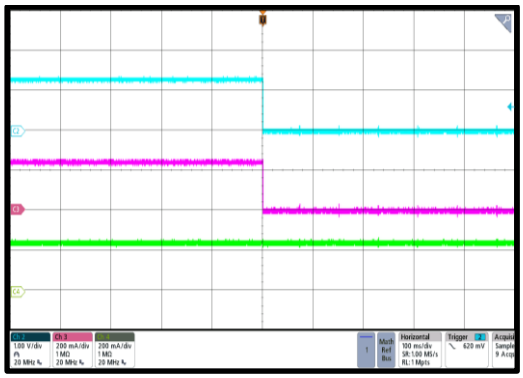
VB1 = VB3 = -1.2V



80µs/div.

ID SCP Entry

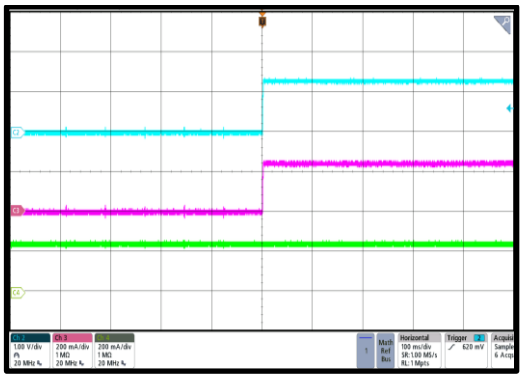
ID1 = ID3 = 250mA, auto-recovery mode



100ms/div.

ID SCP Recovery

ID1 = ID3 = 250mA, auto-recovery mode



100ms/div.

FUNCTIONAL BLOCK DIAGRAM

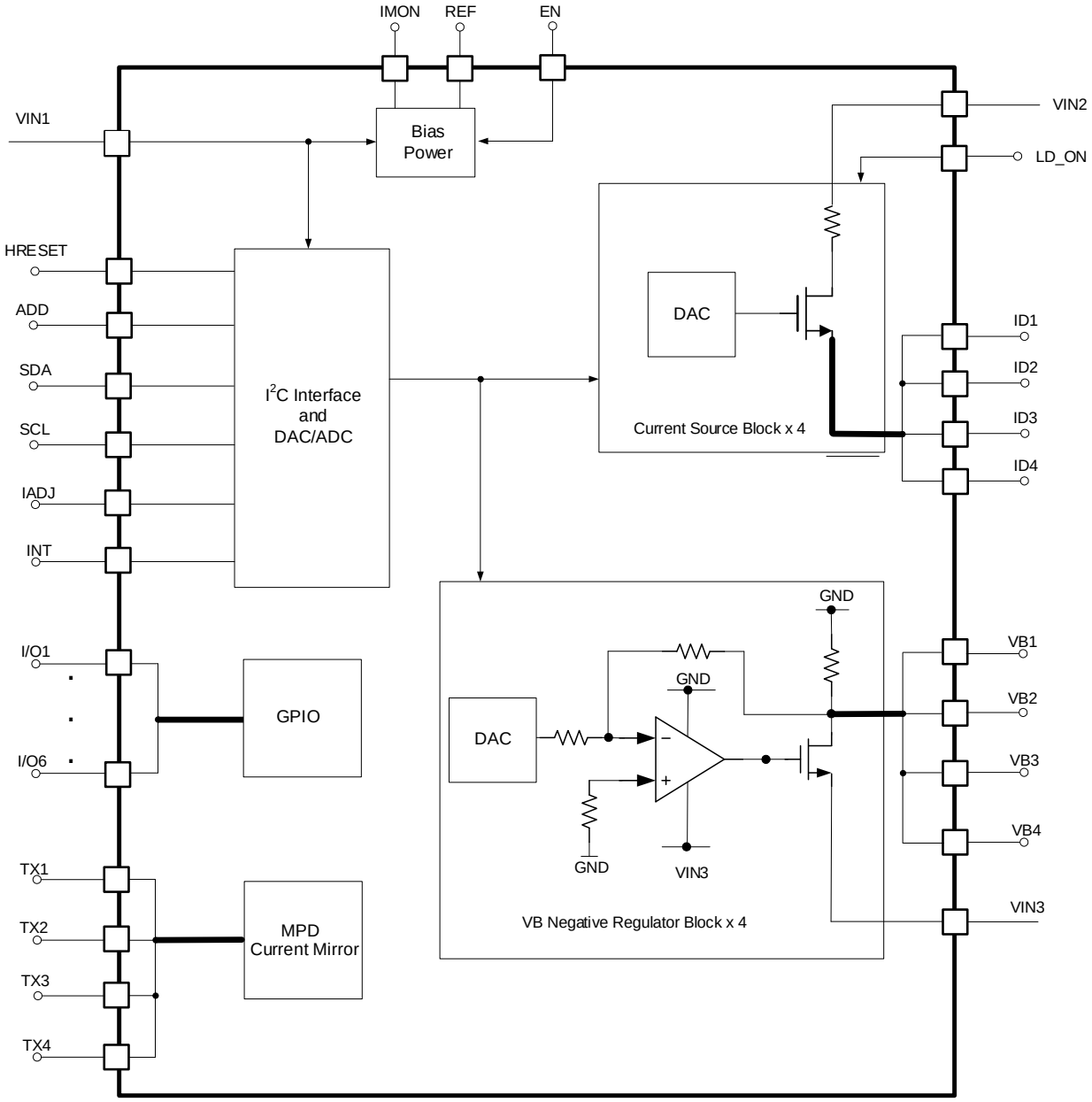


Figure 2: Functional Block Diagram

OPERATION

The MP5490 is a complete power management solution that is well-suited for the transmitter optical subassembly (TOSA) of optical modules. The MP5490 integrates four high-accuracy current sources (IDx) for distributed feedback (DFB) laser diodes (LDs), and four negative voltage biases for the electro-absorption modulated laser (EML) bias. The MP5490 also provides the EML current measurement to simplify the design.

The integrated 6-channel, high-accuracy and low temperature coefficient analog-to-digital converters (ADCs) can be used to read the external current, voltage, and temperature to save microcontroller (MCU) resources.

All output rails can be adjusted via the I²C bus or preset via the multi-page one-time programmable (MOTP) memory. The I²C interface provides adjustable default current/voltage scaling and powerful logic functions. See the Register Description section starting on page 17 for more details.

Power Supply and Enable (EN) Control

The MP5490 requires three external power sources. Its power-on status is determined by the external power source statuses on VIN1, VIN2, VIN3, and EN.

VIN1 supplies the internal bias and control circuit. VIN2 provides the power for the IDx output and GPO pull-up power. The VIN2 voltage (V_{IN2}) should not exceed the VIN1 voltage (V_{IN1}) in application. VIN3 provides the power for the EML bias and MPD current measurement circuit.

Enable control includes the EN pin and EN bit. The IDx current and EML bias start working when both are at high logic, but the I²C interface is not controlled by the EN pin and EN bit. The I²C is always active when V_{IN1} exceeds its under-voltage lockout (UVLO) threshold.

The ID block has an independent LD_ON pin that controls when IDx is on/off. The IDx outputs are active only when LD_ON is at a high logic (see Figure 3) The LD_ON pin can shut off the ID block within 2µs.

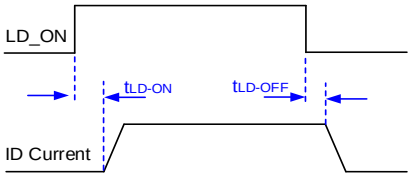


Figure 3: LD_ON Delay Time

High-Accuracy Current Source

The MP5490 integrates four high-accuracy current sources from ID1 to ID4. All channels are sourced powered from VIN2.

The ID power offers an accurate current source configured via the IDx registers (07h~0Eh), and based on 0.25mA/LSB. The MP5490 can support up to 250mA of current sourcing per channel.

The IDx pin's output voltage is limited by the voltage levels of VIN1 and VIN2. See the Typical Characteristics section on page 10 for more information.

High-Accuracy EML Bias

The MP5490 integrates four high-accuracy, negative voltage biases from VB1 to VB4. All channels are sourced power from VIN3.

The EML bias power offers an accurate negative voltage, which can be configured via the VBx registers (0Fh~16h), and is based on -2.5mV/LSB. The MP5490 can support up to a -2.5V bias voltage by default with 60mA of maximum current capability per channel. Set CTL0 (00h), bit D[6] to adjust the maximum bias voltage to -5V.

The VBx pin's output voltage is limited by the VIN3 voltage (V_{IN3}). See the Typical Characteristics section on page 10 for more information.

MPD Current Sensor

The MP5490 integrates four current sensors from TX1 to TX4. All channels are sourced powered internally from VIN3. Connect a non-positive voltage on the TXx pin. The MPD current is sensed and read out via the I²C.

ADC Input and GPO Function

The MP5490 integrates a high-accuracy, 12-bit analog-to-digital converter (ADC) from I/O1 to I/O6. The input range is between 0V and 2.5V.

This pin can also be reused as a general-purpose output (GPO). Open-drain or push-pull structures can be selected via GPO_PULL-UP (0Eh and 1Ah).

The output statuses can be configured via the I²C interface.

Overload and Short-Circuit Protection (SCP)

The IDx pin integrates laser short-circuit protection (SCP) circuitry. If the system senses the IDx output voltage is below 0.3V, the chip turns off the port for protection. After the protection is triggered, the MP5490 may recover after a while, or it may stay in latch-off mode, as selected via the PROTECT (11h or 29h) register. This protection is disabled during internal soft start. If the IDx pin opens without a laser diode connection, the output voltage rises up close to V_{IN2}. Ensure that all external components can operate at a safe state.

The EML bias has an internal current limit (typically 150mA). During over-current or short-circuit conditions, EML continuously outputs 150mA of current.

IADJ Function

The MP5490 offers an IADJ pin to assist an external buck converter providing an output voltage supply to the VIN2 pin by connecting the IADJ pin to an external switching regulator's FB pin (see Figure 4). The MP5490 can sink or source a configurable current (0.122μA/LSB) to adjust the buck's output voltage via the IADJ (36h) register. This function can provide a suitable V_{IN2} to improve efficiency.

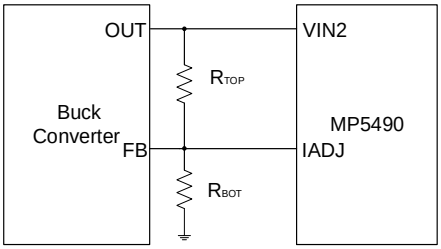


Figure 4: IADJ Application

Interrupt (INT)

The MP5490 offers an INT pin for an interrupt signal. The INT pin pulls low if any bit in the WARN1 (32h) or WARN2 (33h) register is triggered and the warning bit is not masked.

If the warning bit is cleared, the INT pin rises high again and waits for the next interrupt event. If a second interrupt event occurs while the INT pin is low, the INT pin does not change to high until all interrupt sources are cleared.

Temperature Sensor

The MP5490 offers the TEMP (64h/65h) registers to report the die temperature. The registers store the voltage from the internal temperature sensor. The least significant bit (LSB) is 0.074°C. The temperature (*T*) can be calculated with Equation (1):

$$T = n \times 0.074°C - 143\ (°C) \quad (1)$$

Where *n* is the register value in decimal format.

Thermal Warning and Shutdown

Thermal warning and shutdown prevent the part from operating at exceedingly high temperatures. When the silicon die temperature exceeds 120°C, the MP5490 sets the OT_WARN bit to 1. If the die temperature exceeds 160°C, the MP5490 sets the OT bit to 1, and the system initiates a shutdown. The device restarts when the temperature drops to 130°C.

Slave Address

To support multiple MP5490s through one I²C bus, use the ADD pin to configure the I²C address for each MP5490. Connect a resistor from the ADD pin to ground to set the slave address. Table 1 shows the ADD pin configurations with different resistor values.

Table 1: ADD Pin Configuration

R_{ADD}	I²C Slave Address	
43kΩ/short to GND	0x60	1100 000
75kΩ	0x62	1100 010
105kΩ	0x64	1100 100
130kΩ/float	0x66	1100 110

I²C INTERFACE

I²C Serial Interface Description

The I²C is a 2-wire, bidirectional serial interface, consisting of a data line (SDA) and a clock line (SCL). The lines are externally pulled to a bus voltage when they are idle. Connecting to the line, a master device generates the SCL signal and device address, and then arranges the communication sequence. The MP5490 interface is an I²C slave that can support fast mode (400kHz) communication. The I²C interface adds flexibility to the power supply solution. The output EML voltage, IDx current, or other parameters can be instantaneously controlled via the I²C interface. When the master sends the address as an 8-bit value, the 7-bit address should be followed by 0 or 1 to indicate a write or read operation, respectively.

Start and Stop Commands

The start and stop commands are signaled by the master device which signifies the beginning and the end of the I²C transfer. The start (S) command is defined as the SDA signal transitioning from high to low while the SCL is high. The stop (P) command is defined as the SDA signal transitioning from low to high while the SCL is high. Figure 5 shows the start and stop commands.

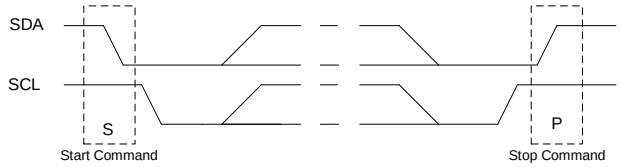


Figure 5: Start and Stop Commands

The master then generates the SCL clocks, then it transmits the device address and the read/write (R/W) direction bit on the SDA line.

Transfer Data

Data is transferred in 8-bit or 16-bit bytes by the SDA line. Each byte of data must be followed by an acknowledge (ACK) bit.

I²C Update Sequence

The MP5490 requires a start command, a valid I²C address, a register address byte, and a data byte for a single data update. After receiving each byte, the MP5490 acknowledges by pulling the SDA line low during the high period of a single clock pulse. A valid I²C address selects the MP5490. The MP5490 performs an update on the falling edge of the LSB byte.

Figure 6 shows an I²C example writing to a single register. Figure 7 shows an I²C example writing to multiple registers. Figure 8 on page 16 shows an I²C example reading a register.

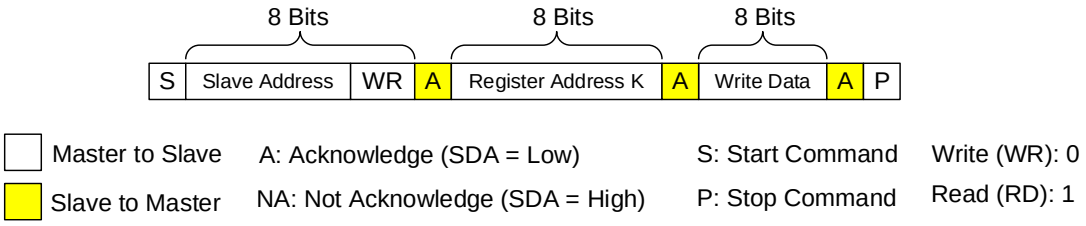


Figure 6: I²C Write Example (Write Single Register)

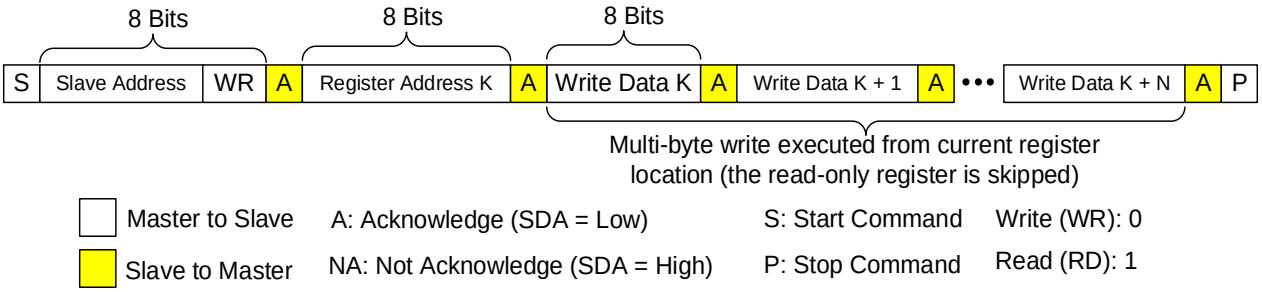


Figure 7: I²C Write Example (Write Multi-Register)

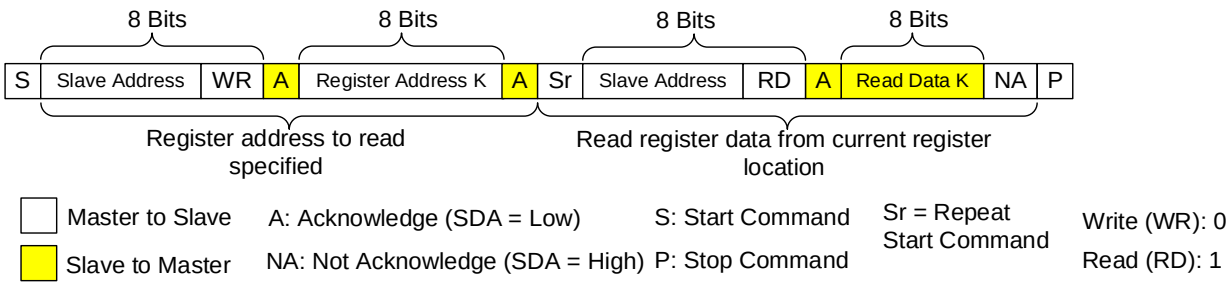


Figure 8: I²C Read Example (Read Single Register)

REGISER DESCRIPTION

MOTP E-Fuse Configure Table

Add.	Name	D7	D6	D5	D4	D3	D2	D1	D0
0x00	CTL0	SYSEN	VB_ GAIN	RESERVE D	DELAY_BASE_TIME		RESERVED	ADC_MODE	RESERVED
0x01	CTL1	ID_EN	ID_DELAY_SLOT			ID1_EN	ID2_EN	ID3_EN	ID4_EN
0x02	CTL2	VB_EN	VB_DELAY_SLOT			VB1_EN	VB2_EN	VB3_EN	VB4_EN
0x03	CTL3	I/O_EN	I/O1_EN	I/O2_EN	I/O3_EN	I/O4_EN	I/O5_EN	I/O6_EN	RESERVED
0x04	CTL4	TX_EN	TX1_EN	TX2_EN	TX3_EN	TX4_EN	RESERVED		
0x07	ID	MSB_8_BIT_OF_ID_CURRENT							
0x08		RESERVED			SLEW_RATE		RESERVED	LSB_2_BIT_OF_ID_ CURRENT	
0x09	VB	MSB_8_BIT_OF_VB_VOLTAGE							
0x0A		RESERVED						LSB_2_BIT_OF_VB_ VOLTAGE	
0x0C	I/O_ CONFIG	I/O1	I/O2	I/O3	I/O4	I/O5	I/O6	RESERVED	
0x0D	GPO CONFIG	GPO1	GPO2	GPO3	GPO4	GPO5	GPO6	RESERVED	
0x0E	GPO_ PULL-UP	PL1	PL2	PL3	PL4	PL5	PL6	RESERVED	
0x0F	THRES1	MSB_8_BIT_OF_EML(VB)_CURRENT_THRESHOLD							
0x10	THRES2	MSB_8_BIT_OF_ID_VOLTAGE_THRESHOLD							
0x11	PROTECT	ID_SCP_ MODE	RESERVED						

MOTP E-FUSE TABLE DESCRIPTION

CTL0 (00h)

Format: Unsigned binary

The CTL0 command enables the system and sets the VBx voltage range, IDx/VBx delay base time, and ADC mode.

Bits	Access	Bit Name	Default	Description
D[7]	R	SYSEN	0	Enables the system by default. If the VIN1 and EN pin's voltages exceed their ULVO thresholds and the SYSEN bit is set to 1, the MP5490 starts to work. This bit also starts the time sequencing slot. 0: Disabled 1: Enabled
D[6]	R	VB_GAIN	0	Sets the VB block's gain. 0: 1x Gain. The VB1–VB4 output is between -0.1V and -2.5V 1: 2x Gain. The VB1–VB4 output is between -0.1V and -5V. At the same time, its step is double that of the 1x gain
D[5]	R	RESERVED	0	Reserved.
D[4:3]	R	DELAY_BASE_TIME	00	Sets the Idx current source and EML bias voltage start-up time. Calculate the start-up delay based on DELAY_SLOT x multiplied by DELAY_BASE_TIME. D[4:3] / Delay Base Time (ms): 00 / 0.25; 01 / 0.5; 10 / 1; 11 / 2
D[2]	R	RESERVED	1	Reserved.

D[1]	R	ADC_MODE	0	Selects the ADC mode. 0: Single mode. The register data is a one-time sample 1: Average mode. The ADC transfers the average data (8 times) into the register
D[0]	R	RESERVED	0	Reserved.

Figure 9 shows the time delays set by DELAY_BASE_TIME.

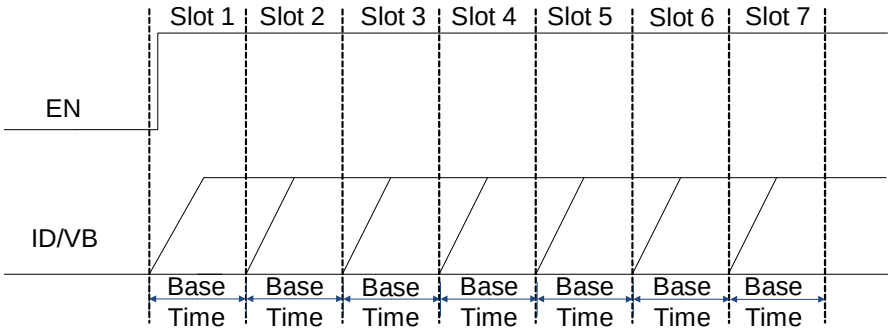


Figure 9: Time Delays

CTL1 (01h)

Format: Unsigned binary

The CTL1 command enables the ID block and sets the start-up delay slot.

Bits	Access	Bit Name	Default	Description
D[7]	R	ID_EN	0	Enables the ID block. This bit is masked if ID_DELAY_SLOT is not set to 000. 0: Disabled 1: Enabled
D[6:4]	R	ID_DELAY_SLOT	000	Sets the default Idx turn-on delay after the EN bit is set. All ID channels start up with the same delay slot. Calculate the start-up delay based on ID_DELAY_SLOT multiplied by DELAY_BASE_TIME.
D[3]	R	ID1_EN	1	Enables the ID1 output. 0: Disabled 1: Enabled
D[2]	R	ID2_EN	1	Enables the ID2 output. 0: Disabled 1: Enabled
D[1]	R	ID3_EN	1	Enables the ID3 output. 0: Disabled 1: Enabled
D[0]	R	ID4_EN	1	Enables the ID4 output. 0: Disabled 1: Enabled

D[6:4]	Slot	D[6:4]	Slot
000	Enable digital EN	100	Slot 4
001	Slot 1	101	Slot 5
010	Slot 2	110	Slot 6
011	Slot 3	111	Slot 7

Figure 10 shows the turn-on delays set by ID_DELAY_SLOT.

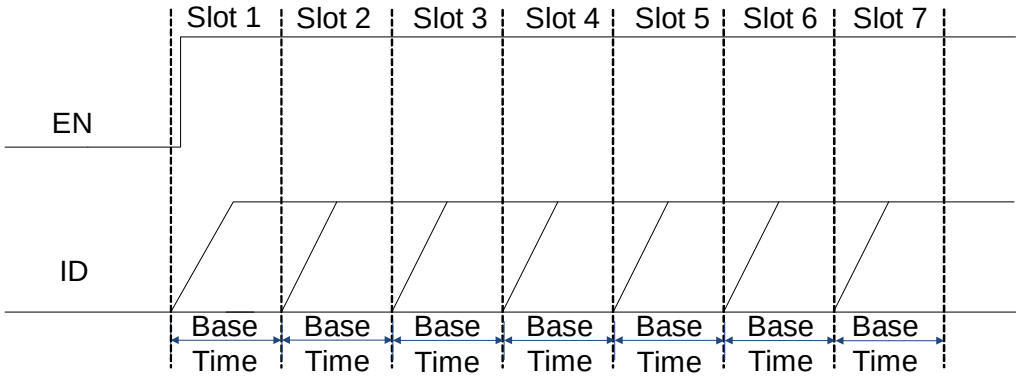


Figure 10: Time Delays

CTL2 (02h)

Format: Unsigned binary

The CTL2 command enables the VB block and sets the and start-up delay slot.

Bits	Access	Bit Name	Default	Description
D[7]	R	VB_EN	0	Enables the VB block. This bit is masked if VB_DELAY_SLOT is not equal to 000. 0: Disabled 1: Enabled
D[6:4]	R	VB_DELAY_SLOT	000	Sets the default VBx turn-on delay after the EN bit is set. All VB channels start up with the same delay slot. Calculate the start-up delay based on VB_DELAY_SLOT multiplied by DELAY_BASE_TIME.
D[3]	R	VB1_EN	1	Enables the VB1 output. 0: Disabled 1: Enabled
D[2]	R	VB2_EN	1	Enables the VB2 output. 0: Disabled 1: Enabled
D[1]	R	VB3_EN	1	Enables the VB3 output. 0: Disabled 1: Enabled
D[0]	R	VB4_EN	1	Enables the VB4 output. 0: Disabled 1: Enabled

D[6:4]	Slot	D[6:4]	Slot
000	Enable digital EN	100	Slot 4
001	Slot 1	101	Slot 5
010	Slot 2	110	Slot 6
011	Slot 3	111	Slot 7

Figure 11 shows the turn-on delays set by VB_DELAY_SLOT.

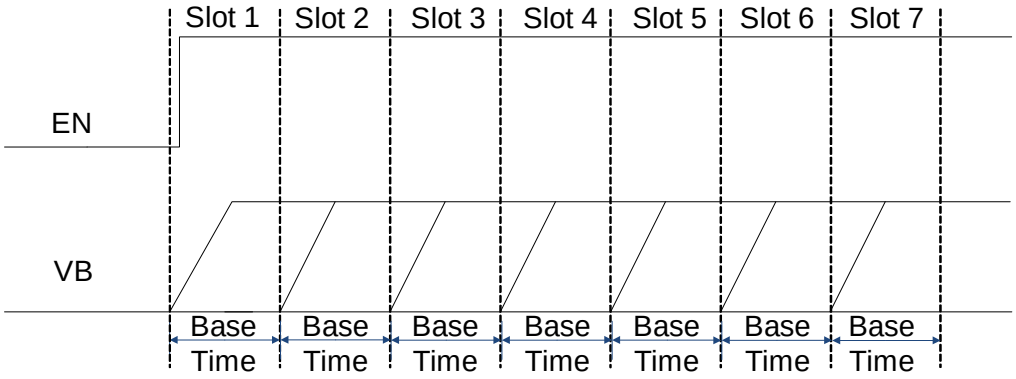


Figure 11: Time Delays

CTL3 (03h)

Format: Unsigned binary

The CTL3 command enables the I/Ox pins.

Bits	Access	Bit Name	Default	Description
D[7]	R	I/O_EN	0	Enables the I/O block. Each I/O port can operate after this bit is enabled. 0: Disabled 1: Enabled
D[6]	R	I/O1_EN	1	Enables the I/O1 output. 0: Disabled 1: Enabled
D[5]	R	I/O2_EN	1	Enables the I/O2 output. 0: Disabled 1: Enabled
D[4]	R	I/O3_EN	1	Enables the I/O3 output. 0: Disabled 1: Enabled
D[3]	R	I/O4_EN	1	Enables the I/O4 output. 0: Disabled 1: Enabled
D[2]	R	I/O5_EN	1	Enables the I/O5 output. 0: Disabled 1: Enabled
D[1]	R	I/O6_EN	1	Enables the I/O6 output. 0: Disabled 1: Enabled
D[0]	R	RESERVED	0	Reserved.

CTL4 (04h)

Format: Unsigned binary

The CTL4 command enables the TXx pin.

Bits	Access	Bit Name	Default	Description
D[7]	R	TX_EN	0	Enables the MPD current measurement block. Each TX port can operate after this bit is enabled. 0: Disabled 1: Enabled
D[6]	R	TX1_EN	1	Enables the TX1 output. 0: Disabled 1: Enabled
D[5]	R	TX2_EN	1	Enables the TX2 output. 0: Disabled 1: Enabled
D[4]	R	TX3_EN	1	Enables the TX3 output. 0: Disabled 1: Enabled
D[3]	R	TX4_EN	1	Enables the TX4 output. 0: Disabled 1: Enabled
D[2:0]	R	RESERVED	000	Reserved.

ID (07h)

Format: Unsigned binary

The ID (07h) command configures the 8 most significant bits (MSB) for the current of all 4 channels.

Bits	Access	Bit Name	Default	Description
D[7:0]	R	MSB_8_BIT_OF_ID_CURRENT	0000 0000	Sets the 8 MSB of the Idx output current. The range is between 0mA and 250mA by connecting 60.4kΩ from the IMON pin to AGND. These MOTP bits configure all 4 channels.

ID (08h)

Format: Unsigned binary

The ID (08h) command configures the 2 least significant bits (LSB) 2 bit for the current of all 4 channels, as well as the slew rate.

Bits	Access	Bit Name	Default	Description
D[7:5]	R	RESERVED	000	Reserved.
D[4:3]	R	SLEW RATE	01	Sets the Idx output current's rising slew rate. These MOTP bits configure all 4 channels. 00: 1.5mA/μs 01: 0.75mA/μs 10: 0.375mA/μs 11: 0.1875mA/μs
D[2]	R	RESERVED	0	Reserved.
D[1:0]	R	LSB_2_BIT_OF_ID_CURRENT	00	Sets the 2 LSB of the Idx output current. The range is between 0mA and 250mA by connecting 60.4kΩ from the IMON pin to AGND. These MOTP bits configure all 4 channels.

VB (09h)

Format: Unsigned binary

The VB (09h) command configures the 8 MSB for the EML biased voltage for all 4 channels.

Bits	Access	Bit Name	Default	Description
D[7:0]	R	MSB_8_BIT_OF_VB_VOLTAGE	0000 0000	Sets the 8 MSB of the EML bias voltage. The range is between -0.1V and -2.5V or -0.1V and -5V. These MOTP bits configure all 4 channels.

VB (0Ah)

Format: Unsigned binary

The VB (0Ah) command configures the 2 LSB for the EML biased voltage for all 4 channels.

Bits	Access	Bit Name	Default	Description
D[7:2]	R	RESERVED	0000 00	Reserved.
D[1:0]	R	MSB_2_BIT_OF_VB_VOLTAGE	00	Sets the 2 LSB of the EML bias voltage. The range is between -0.1V and -2.5V or -0.1V and -5V. These MOTP bits configure all 4 channels.

I/O_CONFIG (0Ch)

Format: Unsigned binary

The I/O_CONFIG command sets the I/Ox pin’s default function.

Bits	Access	Bit Name	Default	Description
D[7]	R	I/O1	0	Selects the I/O1 pin’s mode. 0: ADC input 1: GPO
D[6]	R	I/O2	0	Selects the I/O2 pin’s mode. 0: ADC input 1: GPO
D[5]	R	I/O3	0	Selects the I/O3 pin’s mode. 0: ADC input 1: GPO
D[4]	R	I/O4	0	Selects the I/O4 pin’s mode. 0: ADC input 1: GPO
D[3]	R	I/O5	0	Selects the I/O5 pin’s mode. 0: ADC input 1: GPO
D[2]	R	I/O6	0	Selects the I/O6 pin’s mode. 0: ADC input 1: GPO
D[1:0]	R	RESERVED	00	Reserved.

GPO_CONFIG (0Dh)

Format: Unsigned binary

The GPO_CONFIG command sets GPO pin's default output.

Bits	Access	Bit Name	Default	Description
D[7]	R	GPO1	0	Sets the I/O1 pin's default output if GPO mode is selected. 0: Output low 1: Output high
D[6]	R	GPO2	0	Sets the I/O2 pin's default output if GPO mode is selected. 0: Output low 1: Output high
D[5]	R	GPO3	0	Sets the I/O3 pin's default output if GPO mode is selected. 0: Output low 1: Output high
D[4]	R	GPO4	0	Sets the I/O4 pin's default output if GPO mode is selected. 0: Output low 1: Output high
D[3]	R	GPO5	0	Sets the I/O5 pin's default output if GPO mode is selected. 0: Output low 1: Output high
D[2]	R	GPO6	0	Sets the I/O6 pin's default output if GPO mode is selected. 0: Output low 1: Output high
D[1:0]	R	RESERVED	00	Reserved.

GPO_PULL-UP (0Eh)

Format: Unsigned binary

The GPO_PULL-UP command sets default structure of the GPO pin's output.

Bits	Access	Bit Name	Default	Description
D[7]	R	PL1	0	Sets the default structure of the I/O1 pin's output if GPO mode is selected. 0: Open-drain output 1: Push-pull output. Internally pull up to the VIN2 voltage when it outputs high
D[6]	R	PL2	0	Sets the default structure of the I/O2 pin's output if GPO mode is selected. 0: Open-drain output 1: Push-pull output. Internally pull up to the VIN2 voltage when it outputs high
D[5]	R	PL3	0	Sets the default structure of the I/O3 pin's output if GPO mode is selected. 0: Open-drain output 1: Push-pull output. Internally pull up to the VIN2 voltage when it outputs high

D[4]	R	PL4	0	Sets the default structure of the I/O4 pin's output if GPO mode is selected. 0: Open-drain output 1: Push-pull output. Internally pull up to the VIN2 voltage when it outputs high
D[3]	R	PL5	0	Sets the default structure of the I/O5 pin's output if GPO mode is selected. 0: Open-drain output 1: Push-pull output. Internally pull up to the VIN2 voltage when it outputs high
D[2]	R	PL6	0	Sets the default structure of the I/O6 pin's output if GPO mode is selected. 0: Open-drain output 1: Push-pull output. Internally pull up to the VIN2 voltage when it outputs high
D[1:0]	R	RESERVED	00	Reserved.

THRES1 (0Fh)

Format: Unsigned binary

The THRES1 command sets the EML (VB) current limit.

Bits	Access	Bit Name	Default	Description
D[7:0]	R	VB_CURRENT_ THRESHOLD	1111 1111	Sets the EML (VB) current limit. If the current on ID1–ID4 exceeds this threshold, the INT pin sends an alarm.

THRES2 (10h)

Format: Unsigned binary

The THRES2 command sets the Idx pin's voltage limit.

Bits	Access	Bit Name	Default	Description
D[7:0]	R	ID_VOLTAGE_ THRESHOLD	1111 1111	Sets the Idx pin's voltage limit. If the voltage on ID1–ID4 exceeds this threshold, the INT pin sends an alarm.

PROTECT (11h)

Format: Unsigned binary

The PROTECT command sets the Idx output protection mode.

Bits	Access	Bit Name	Default	Description
D[7]	R	ID_SCP_MODE	0	Sets the Idx output protection mode. If latch-off mode is enabled, the output can be re-enabled again by V_{IN1} under-voltage lockout (UVLO), V_{IN2} UVLO, the LD_ON pin's UVLO, EN pin UVLO, or the digital EN bits (including the ID_EN bit and respective Idx_EN bit). 0: Automatically recover after a protection is triggered 1: Latch-off after a protection is triggered
D[6:0]	R	RESERVED	000 0000	Reserved.

I²C REGISTER MAP

Add.	Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x00	CTL0	R/W	SYSEN	VB_ GAIN	RESERVE D	DELAY_BASE_ TIME		RESER VED	ADC_ MODE	RESER VED	0000 0100
0x01	CTL1	R/W	ID_EN	ID_DELAY_SLOT			ID1_EN	ID2_EN	ID3_EN	ID4_EN	0000 1111
0x02	CTL2	R/W	VB_EN	VB_DELAY_SLOT			VB1_EN	VB2_EN	VB3_EN	VB4_EN	0000 1111
0x03	CTL3	R/W	I/O_EN	I/O1_EN	I/O2_EN	I/O3_EN	I/O4_EN	I/O5_EN	I/O6_EN	RESER VED	0111 1110
0x04	CTL4	R/W	TX_EN	TX1_EN	TX2_EN	TX3_EN	TX4_EN	RESERVED			0111 1000
0x07	ID1	R/W	MSB_8_BIT_OF_ID1_CURRENT								0000 0000
0x08			RESERVED			SLEW_RATE		RESER VED	LSB_2_BIT_OF_ ID1_CURRENT		0000 1000
0x09	ID2	R/W	MSB_8_BIT_OF_ID2_CURRENT								0000 0000
0x0A		R/W	RESERVED			SLEW_RATE		RESER VED	LSB_2_BIT_OF_ID2 _CURRENT		0000 1000
0x0B	ID3	R/W	MSB_8_BIT_OF_ID3_CURRENT								0000 0000
0x0C		R/W	RESERVED			SLEW_RATE		RESER VED	LSB_2_BIT_OF_ ID3_CURRENT		0000 1000
0x0D	ID4	R/W	MSB_8_BIT_OF_ID4_CURRENT								0000 0000
0x0E		R/W	RESERVED			SLEW_RATE		RESER VED	LSB_2_BIT_OF_ ID4_CURRENT		0000 1000
0x0F	VB1	R/W	MSB_8_BIT_OF_VB1_VOLTAGE								0000 0000
0x10		R/W	RESERVED						LSB_2_BIT_OF_ VB1_VOLTAGE		0000 0000
0x11	VB2	R/W	MSB_8_BIT_OF_VB2_VOLTAGE								0000 0000
0x12		R/W	RESERVED						LSB_2_BIT_OF_ VB2_VOLTAGE		0000 0000
0x13	VB3	R/W	MSB_8_BIT_OF_VB3_VOLTAGE								0000 0000
0x14		R/W	RESERVED						LSB_2_BIT_OF_ VB3_VOLTAGE		0000 0000
0x15	VB4	R/W	MSB_8_BIT_OF_VB4_VOLTAGE								0000 0000
0x16		R/W	RESERVED						LSB_2_BIT_OF_ VB4_VOLTAGE		0000 0000
0x18	I/O CONFIG	R/W	I/O1	I/O2	I/O3	I/O4	I/O5	I/O6	RESERVED		0000 0000
0x19	GPO CONFIG	R/W	GPO1	GPO2	GPO3	GPO4	GPO5	GPO6	RESERVED		0000 0000
0x1A	GPO PULL-UP	R/W	PL1	PL2	PL3	PL4	PL5	PL6	RESERVED		0000 0000
0x1B	THRES1	R/W	MSB_8_BIT_OF_EML(VB)_CURRENT_THRESHOLD								1111 1111
0x1C	THRES2	R/W	MSB_8_BIT_OF_ID_VOLTAGE_THRESHOLD								1111 1111
0x1D	T_IO1_H	R/W	MSB_8_BIT_OF_I/O1_HIGH_THRESHOLD								1111 1111
0x1E	T_IO1_L	R/W	MSB_8_BIT_OF_I/O1_LOW_THRESHOLD								0000 0000
0x1F	T_IO2_H	R/W	MSB_8_BIT_OF_I/O2_HIGH_THRESHOLD								1111 1111
0x20	T_IO2_L	R/W	MSB_8_BIT_OF_I/O2_LOW_THRESHOLD								0000 0000
0x21	T_IO3_H	R/W	MSB_8_BIT_OF_I/O3_HIGH_THRESHOLD								1111 1111
0x22	T_IO3_L	R/W	MSB_8_BIT_OF_I/O3_LOW_THRESHOLD								0000 0000
0x23	T_IO4_H	R/W	MSB_8_BIT_OF_I/O4_HIGH_THRESHOLD								1111 1111
0x24	T_IO4_L	R/W	MSB_8_BIT_OF_I/O4_LOW_THRESHOLD								0000 0000
0x25	T_IO5_H	R/W	MSB_8_BIT_OF_I/O5_HIGH_THRESHOLD								1111 1111
0x26	T_IO5_L	R/W	MSB_8_BIT_OF_I/O5_LOW_THRESHOLD								0000 0000
0x27	T_IO6_H	R/W	MSB_8_BIT_OF_I/O6_HIGH_THRESHOLD								1111 1111
0x28	T_IO6_L	R/W	MSB_8_BIT_OF_I/O6_LOW_THRESHOLD								0000 0000
0x29	PROTECT	R/W	ID_ SCP_ MODE	RESERVED							0000 0000
0x2A	ADCM1	R/W	IVB1	IVB2	IVB3	IVB4	VID1	VID2	VID3	VID4	1111 1111
0x2B	ADCM2	R/W	TX1	TX2	TX3	TX4	I/O1	I/O2	I/O3	I/O4	1111 1111
0x2C	ADCM3	R/W	I/O5	I/O6	TEMP	VIN2	VIN3	RESERVED			1111 1000
0x2D	CONFIG	R/W	RESERVED		VB_DIS	ID_DIS	RESER VED	WARN_ REFRE SH	RESERVED		1111 0000
0x2E	STATUS 1	R	RESERVED		VB1_FLG	VB2_ FLG	VB3_ FLG	VB4_ FLG	ID1_FL G	ID2_FL G	0000 0000
0x2F	STATUS 2	R	ID3_ FLG	ID4_ FLG	TX1_FLG	TX2_ FLG	TX3_ FLG	TX4_ FLG	I/O1_ FLG	I/O2_ FLG	0000 0000

I²C REGISTER MAP *(continued)*

Add.	Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x30	STATUS 3	R	I/O3_ FLG	I/O4_ FLG	I/O5_FLG	I/O6_ FLG	LD_ON_ FLG	ID_OV	VIN2_ UV	VIN3_ UV	0000 0000
0x31	STATUS 4	R	GPO1_ OUTPUT	GPO2_ OUTPUT	GPO3_ OUTPUT	GPO4_ OUTPUT	GPO5_ OUTPUT	GPO6_ OUTPUT	RESERVED		0000 0000
0x32	WARN1	R	RESERVED		VB_OC	ID_OC	RESERVED		OT_ WARN	OT	0000 0000
0x33	WARN2	R	I/O1	I/O2	I/O3	I/O4	I/O5	I/O6	-		0000 0000
0x34	MASK	R/W	RESERVED		VB_OC_ MSK	ID_OC_ MSK	RESERVED		OT_ WARN_ MSK	OT_ MSK	0000 0000
0x36	IADJ	R/W	IADJ_PROGRAM								0000 0000
ADC Result											
0x40	VB1_ CURRENT	R	MSB_8_BIT_OF_VB1_CURRENT								
0x41		R	RESERVED				LSB_4_BIT_OF_VB1_CURRENT				
0x42	VB2_ CURRENT	R	MSB_8_BIT_OF_VB2_CURRENT								
0x43		R	RESERVED				LSB_4_BIT_OF_VB2_CURRENT				
0x44	VB3_ CURRENT	R	MSB_8_BIT_OF_VB3_CURRENT								
0x45		R	RESERVED				LSB_4_BIT_OF_VB3_CURRENT				
0x46	VB4_ CURRENT	R	MSB_8_BIT_OF_VB4_CURRENT								
0x47		R	RESERVED				LSB_4_BIT_OF_VB4_CURRENT				
0x48	ID1_ VOLTAGE	R	MSB_8_BIT_OF_ID1_VOLTAGE								
0x49		R	RESERVED				LSB_4_BIT_OF_ID1_VOLTAGE				
0x4A	ID2_ VOLTAGE	R	MSB_8_BIT_OF_ID2_VOLTAGE								
0x4B		R	RESERVED				LSB_4_BIT_OF_ID2_VOLTAGE				
0x4C	ID3_ VOLTAGE	R	MSB_8_BIT_OF_ID3_VOLTAGE								
0x4D		R	RESERVED				LSB_4_BIT_OF_ID3_VOLTAGE				
0x4E	ID4_ VOLTAGE	R	MSB_8_BIT_OF_ID4_VOLTAGE								
0x4F		R	RESERVED				LSB_4_BIT_OF_ID4_VOLTAGE				
0x50	TX1_ CURRENT	R	MSB_8_BIT_OF_TX1_CURRENT								
0x51		R	RESERVED				LSB_4_BIT_OF_TX1_CURRENT				
0x52	TX2_ CURRENT	R	MSB_8_BIT_OF_TX2_CURRENT								
0x53		R	RESERVED				LSB_4_BIT_OF_TX2_CURRENT				
0x54	TX3_ CURRENT	R	MSB_8_BIT_OF_TX3_CURRENT								
0x55		R	RESERVED				LSB_4_BIT_OF_TX3_CURRENT				
0x56	TX4_ CURRENT	R	MSB_8_BIT_OF_TX4_CURRENT								
0x57		R	RESERVED				LSB_4_BIT_OF_TX4_CURRENT				
0x58	I/O1_ VOLTAGE	R	MSB_8_BIT_OF_I/O1_VOLTAGE								
0x59		R	RESERVED				LSB_4_BIT_OF_I/O1_VOLTAGE				
0x5A	I/O2_ VOLTAGE	R	MSB_8_BIT_OF_I/O2_VOLTAGE								
0x5B		R	RESERVED				LSB_4_BIT_OF_I/O2_VOLTAGE				
0x5C	I/O3_ VOLTAGE	R	MSB_8_BIT_OF_I/O3_VOLTAGE								
0x5D		R	RESERVED				LSB_4_BIT_OF_I/O3_VOLTAGE				
0x5E	I/O4_ VOLTAGE	R	MSB_8_BIT_OF_I/O4_VOLTAGE								
0x5F		R	RESERVED				LSB_4_BIT_OF_I/O4_VOLTAGE				
0x60	I/O5_ VOLTAGE	R	MSB_8_BIT_OF_I/O5_VOLTAGE								
0x61		R	RESERVED				LSB_4_BIT_OF_I/O5_VOLTAGE				
0x62	I/O6_ VOLTAGE	R	MSB_8_BIT_OF_I/O6_VOLTAGE								
0x63		R	RESERVED				LSB_4_BIT_OF_I/O6_VOLTAGE				
0x64	TEMP	R	MSB_8_BIT_OF_TEMPERATURE								
0x65		R	RESERVED				LSB_4_BIT_OF_TEMPERATURE				
0x66	VIN2_ VOLTAGE	R	MSB_8_BIT_OF_VIN2_VOLTAGE								
0x67		R	RESERVED				LSB_4_BIT_OF_VIN2_VOLTAGE				
0x68	VIN3_ VOLTAGE	R	MSB_8_BIT_OF_VIN3_VOLTAGE								
0x69		R	RESERVED				LSB_4_BIT_OF_VIN3_VOLTAGE				

I²C REGISTER DESCRIPTION

CTL0 (00h)

Format: Unsigned binary

The CTL0 command enables the system and sets the VB voltage range, ID delay base time, and ADC mode.

Bits	Access	Bit Name	Default	Description
D[7]	R/W	SYSEN	0	Enables the system by default. If the VIN1 and EN pin's voltages exceed their ULVO thresholds and the SYSEN bit is set to 1, the MP5490 starts to work. This bit also starts the time sequencing slot. 0: Disabled 1: Enabled
D[6]	R/W	VB_GAIN	0	Sets the VB block's gain. 0: 1x Gain. The VB1–VB4 output is between -0.1V and -2.5V 1: 2x Gain. The VB1–VB4 output is between -0.1V and -5V. At the same time, its step is double that of the 1x gain
D[5]	R/W	RESERVED	0	Reserved.
D[4:3]	R/W	DELAY_BASE_TIME	00	Sets the Idx current source and EML bias voltage start-up time. Calculate the start-up delay based on DELAY_SLOT x multiplied by DELAY_BASE_TIME.
D[2]	R/W	RESERVED	1	Reserved.
D[1]	R/W	ADC_MODE	0	Selects the ADC mode. 0: Single mode. The register data is a one-time sample 1: Average mode. The ADC transfers the average data (8 times) into the register
D[0]	R/W	RESERVED	0	Reserved.

D[4:3]	Delay Base Time (ms)
00	0.25
01	0.5
10	1
11	2

Figure 12 shows the time delays set by DELAY_BASE_TIME.

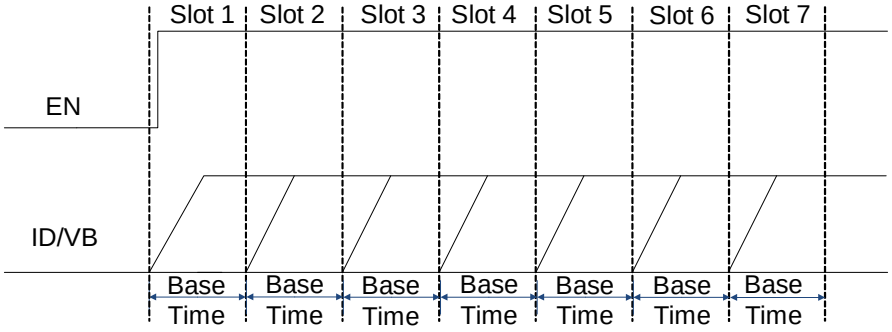


Figure 12: Time Delays

CTL1 (01h)

Format: Unsigned binary

The CTL1 command enables the ID block and sets the start-up delay slot.

Bits	Access	Bit Name	Default	Description
D[7]	R/W	ID_EN	0	Enables the ID block. This bit is masked if ID_DELAY_SLOT is not set to 000. 0: Disabled 1: Enabled
D[6:4]	R/W	ID_DELAY_SLOT	000	Sets the default Idx turn-on delay default value after the EN bit is set. All ID channels start up with the same delay slot. Calculate the start-up delay based on ID_DELAY_SLOT multiplied by DELAY_BASE_TIME.

D[6:4]	Slot	D[6:4]	Slot
000	Enable digital EN	100	Slot 4
001	Slot 1	101	Slot 5
010	Slot 2	110	Slot 6
011	Slot 3	111	Slot 7

D[3]	R/W	ID1_EN	1	Enables the ID1 output. 0: Disabled 1: Enabled
D[2]	R/W	ID2_EN	1	Enables the ID2 output. 0: Disabled 1: Enabled
D[1]	R/W	ID3_EN	1	Enables the ID3 output. 0: Disabled 1: Enabled
D[0]	R/W	ID4_EN	1	Enables the ID4 output. 0: Disabled 1: Enabled

Figure 13 shows the turn-on delays set by ID_DELAY_SLOT.

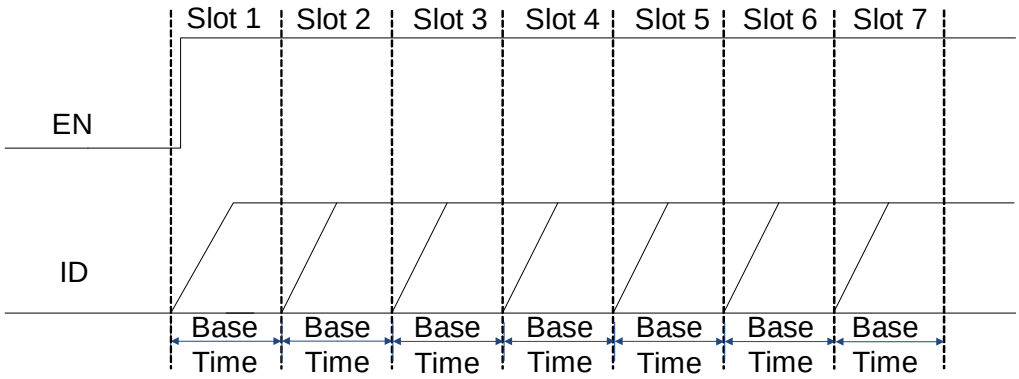


Figure 13: Time Delays

CTL2 (02h)

Format: Unsigned binary

The CTL2 command enables the VB bloc and sets the and start-up delay.

Bits	Access	Bit Name	Default	Description
D[7]	R/W	VB_EN	0	Enables the VB block. This bit is masked if VB_DELAY_SLOT is not equal to 000. 0: Disabled 1: Enabled
D[6:4]	R/W	VB_DELAY_SLOT	000	Sets the default VBx turn-on delay default value after the EN bit is set. All VB channels start up with the same delay slot. Calculate the start-up delay based on VB_DELAY_SLOT multiplied by DELAY_BASE_TIME.
D[3]	R/W	VB1_EN	1	Enables the VB1 output. 0: Disabled 1: Enabled
D[2]	R/W	VB2_EN	1	Enables the VB2 output. 0: Disabled 1: Enabled
D[1]	R/W	VB3_EN	1	Enables the VB3 output. 0: Disabled 1: Enabled
D[0]	R/W	VB4_EN	1	Enables the VB4 output. 0: Disabled 1: Enabled

D[6:4]	Slot	D[6:4]	Slot
000	Enable digital EN	100	Slot 4
001	Slot 1	101	Slot 5
010	Slot 2	110	Slot 6
011	Slot 3	111	Slot 7

Figure 14 shows the turn-on delays set by VB_DELAY_SLOT.

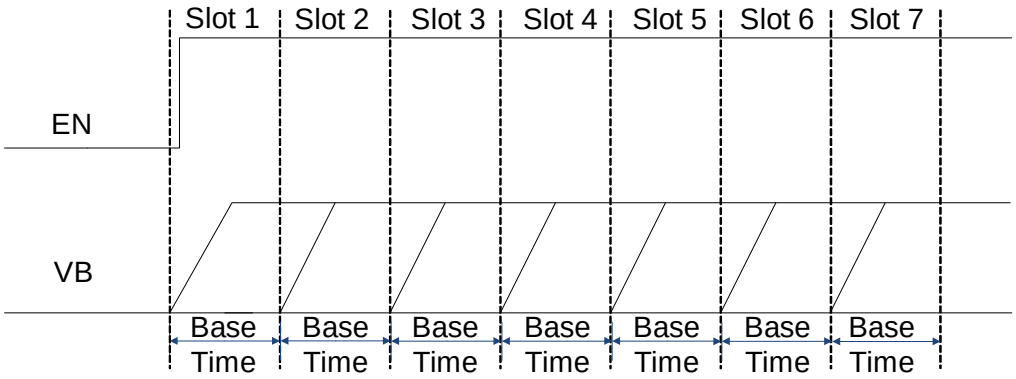


Figure 14: Time Delays

CTL3 (03h)

Format: Unsigned binary

The CTL3 command enables the I/Ox pins.

Bits	Access	Bit Name	Default	Description
D[7]	R/W	I/O_EN	0	Enables the I/O block. Each I/O port can operate after this bit is enabled. 0: Disabled 1: Enabled
D[6]	R/W	I/O1_EN	1	Enables the I/O1 output. 0: Disabled 1: Enabled
D[5]	R/W	I/O2_EN	1	Enables the I/O2 output. 0: Disabled 1: Enabled
D[4]	R/W	I/O3_EN	1	Enables the I/O3 output. 0: Disabled 1: Enabled
D[3]	R/W	I/O4_EN	1	Enables the I/O4 output. 0: Disabled 1: Enabled
D[2]	R/W	I/O5_EN	1	Enables the I/O5 output. 0: Disabled 1: Enabled
D[1]	R/W	I/O6_EN	1	Enables the I/O6 output. 0: Disabled 1: Enabled
D[0]	R/W	RESERVED	0	Reserved.

CTL4 (04h)

Format: Unsigned binary

The CTL4 command enables the TXx pin.

Bits	Access	Bit Name	Default	Description
D[7]	R/W	TX_EN	0	Enables the MPD current measurement block. Each TX port can operate after this bit is enabled. 0: Disabled 1: Enabled
D[6]	R/W	TX1_EN	1	Enables the TX1 output. 0: Disabled 1: Enabled
D[5]	R/W	TX2_EN	1	Enables the TX2 output. 0: Disabled 1: Enabled
D[4]	R/W	TX3_EN	1	Enables the TX3 output. 0: Disabled 1: Enabled

D[3]	R/W	TX4_EN	1	Enables the TX4 output. 0: Disabled 1: Enabled
D[2:0]	R/W	RESERVED	000	Reserved.

ID1 (07h/08h)

Format: Unsigned binary

The ID1 command sets the ID1 pin's current and slew rate.

ID1 (07h)

Bits	Access	Bit Name	Default	Description
D[7:0]	R/W	MSB_8_BIT_OF_ID1_CURRENT	0000 0000	Set the ID1 current from 0mA to 250mA via the ID1 registers (07h, bits D[7:0] and 08h, bits D[1:0]). Each step is 0.25mA.The current is 0.25mA x Decimal (the register value). Setting these registers to 00 may shutdown this IC or result in an offset current.

ID1 (08h)

Bits	Access	Bit Name	Default	Description
D[7:5]	R/W	RESERVED	000	Reserved.
D[4:3]	R/W	SLEW_RATE	01	Sets the ID1 slew rate. 00: 1.5mA/µs 01: 0.75mA/µs 10: 0.375mA/µs 11: 0.1875mA/µs
D[2]	R/W	RESERVED	0	Reserved.
D[1:0]	R/W	LSB_2_BIT_OF_ID1_CURRENT	00	Set the ID1 current from 0mA to 250mA via the ID1 registers (07h, bits D[7:0] and 08h, bits D[1:0]). Each step is 0.25mA.The current is 0.25mA x Decimal (the register value). Setting these registers to 00 may shutdown this IC or result in an offset current.

ID2 (09h/0Ah)

Format: Unsigned binary

The ID2 command sets the ID2 pin's current and slew rate.

ID2 (09h)

Bits	Access	Bit Name	Default	Description
D[7:0]	R/W	MSB_8_BIT_OF_ID2_CURRENT	0000 0000	Set the ID2 current from 0mA to 250mA via the ID2 registers (09h, bits D[7:0] and 0Ah, bits D[1:0]). Each step is 0.25mA.The current is 0.25mA x Decimal (the register value). Setting these registers to 00 may shutdown this IC or result in an offset current.

ID2 (0Ah)

Bits	Access	Bit Name	Default	Description
D[7:5]	R/W	RESERVED	000	Reserved.
D[4:3]	R/W	SLEW_RATE	01	Sets the ID2 pin's slew rate. 00: 1.5mA/μs 01: 0.75mA/μs 10: 0.375mA/μs 11: 0.1875mA/μs
D[2]	R/W	RESERVED	0	Reserved.
D[1:0]	R/W	LSB_2_BIT_OF_ID2_CURRENT	00	Set the ID2 current from 0mA to 250mA via the ID2 registers (09h, bits D[7:0] and 0Ah, bits D[1:0]). Each step is 0.25mA.The current is 0.25mA x Decimal (the register value). Setting these registers to 00 may shutdown this IC or result in an offset current.

ID3 (0Bh/0Ch)

Format: Unsigned binary

The ID3 command sets the ID3 pin's current and slew rate.

ID3 (0Bh)

Bits	Access	Bit Name	Default	Description
D[7:0]	R/W	MSB_8_BIT_OF_ID3_CURRENT	0000 0000	Set the ID3 current from 0mA to 250mA via the ID3 registers (0Bh, bits D[7:0] and 0Ch, bits D[1:0]). Each step is 0.25mA.The current is 0.25mA x Decimal (the register value). Setting these registers to 00 may shutdown this IC or result in an offset current.

ID3 (0Ch)

Bits	Access	Bit Name	Default	Description
D[7:5]	R/W	RESERVED	000	Reserved.
D[4:3]	R/W	SLEW_RATE	01	Sets the ID3 pin's slew rate. 00: 1.5mA/μs 01: 0.75mA/μs 10: 0.375mA/μs 11: 0.1875mA/μs
D[2]	R/W	RESERVED	0	Reserved.
D[1:0]	R/W	LSB_2_BIT_OF_ID3_CURRENT	00	Set the ID3 current from 0mA to 250mA via the ID3 registers (0Bh, bits D[7:0] and 0Ch, bits D[1:0]). Each step is 0.25mA.The current is 0.25mA x Decimal (the register value). Setting these registers to 00 may shutdown this IC or result in an offset current.

ID4 (0Dh/0Eh)

Format: Unsigned binary

The ID4 command sets the ID4 pin's current and slew rate.

ID4 (0Dh)

Bits	Access	Bit Name	Default	Description
D[7:0]	R/W	MSB_8_BIT_OF_ID4_CURRENT	0000 0000	Set the ID4 current from 0mA to 250mA via the ID4 registers (0Dh, bits D[7:0] and 0Eh, bits D[1:0]). Each step is 0.25mA.The current is 0.25mA x Decimal (the register value). Setting these registers to 00 may shutdown this IC or result in an offset current.

ID4 (0Eh)

Bits	Access	Bit Name	Default	Description
D[7:5]	R/W	RESERVED	000	Reserved.
D[4:3]	R/W	SLEW_RATE	01	Sets the ID4 pin's slew rate. 00: 1.5mA/µs 01: 0.75mA/µs 10: 0.375mA/µs 11: 0.1875mA/µs
D[2]	R/W	RESERVED	0	Reserved.
D[1:0]	R/W	LSB_2_BIT_OF_ID4_CURRENT	00	Set the ID4 current from 0mA to 250mA via the ID4 registers (0Dh, bits D[7:0] and 0Eh, bits D[1:0]). Each step is 0.25mA.The current is 0.25mA x Decimal (the register value). Setting these registers to 00 may shutdown this IC or result in an offset current.

VB1 (0Fh/10h)

Format: Unsigned binary

The VB1 command sets the VB1 pin's voltage.

VB1 (0Fh)

Bits	Access	Bit Name	Default	Description
D[7:0]	R/W	MSB_8_BIT_OF_VB1_VOLTAGE	0000 0000	Sets the VB1 pin's voltage from -0.1V to -2.5V or -0.1V to -5V, which is determined by the VB_GAIN bit. The VB1 voltage is set via the VB1 registers (0Fh, bits D[7:0], and 10h, bits D[1:0]). If VB_GAIN = 0, each step is -2.5mV, and the VB1 voltage = -2.5mV x Decimal (register value). If VB_GAIN = 1, each step is -5mV, and the VB1 voltage = -5mV x Decimal (register value).

VB1 (10h)

Bits	Access	Bit Name	Default	Description
D[7:2]	R/W	RESERVED	0000 00	Reserved.

D[1:0]	R/W	LSB_2_BIT_OF_ VB1_VOLTAGE	00	Sets the VB1 pin's voltage from -0.1V to -2.5V or -0.1V to -5V, which is determined by the VB_GAIN bit. The VB1 voltage is set via the VB1 registers (0Fh, bits D[7:0], and 10h, bits D[1:0]). If VB_GAIN = 0, each step is -2.5mV, and the VB1 voltage = -2.5mV x Decimal (register value). If VB_GAIN = 1, each step is -5mV, and the VB1 voltage = -5mV x Decimal (register value).

VB2 (11h/12h)

Format: Unsigned binary

The VB2 command sets the VB2 pin's voltage.

VB2 (11h)

Bits	Access	Bit Name	Default	Description
D[7:0]	R/W	MSB_8_BIT_OF_ VB2_VOLTAGE	0000 0000	Sets the VB2 pin's voltage from -0.1V to -2.5V or -0.1V to -5V, which is determined by the VB_GAIN bit. The VB2 voltage is set via the VB2 registers (11h, bits D[7:0], and 12h, bits D[1:0]). If VB_GAIN = 0, each step is -2.5mV, and the VB2 voltage = -2.5mV x Decimal (register value). If VB_GAIN = 1, each step is -5mV, and the VB2 voltage = -5mV x Decimal (register value).

VB2 (12h)

Bits	Access	Bit Name	Default	Description
D[7:2]	R/W	RESERVED	0000 00	Reserved.
D[1:0]	R/W	LSB_2_BIT_OF_ VB2_VOLTAGE	00	Sets the VB2 pin's voltage from -0.1V to -2.5V or -0.1V to -5V, which is determined by the VB_GAIN bit. The VB2 voltage is set via the VB2 registers (11h, bits D[7:0], and 12h, bits D[1:0]). If VB_GAIN = 0, each step is -2.5mV, and the VB2 voltage = -2.5mV x Decimal (register value). If VB_GAIN = 1, each step is -5mV, and the VB2 voltage = -5mV x Decimal (register value).

VB3 (13h/14h)

Format: Unsigned binary

The VB3 command sets the VB3 pin's voltage.

VB3 (13h)

Bits	Access	Bit Name	Default	Description
D[7:0]	R/W	MSB_8_BIT_OF_ VB3_VOLTAGE	0000 0000	Sets the VB3 pin's voltage from -0.1V to -2.5V or -0.1V to -5V, which is determined by the VB_GAIN bit. The VB3 voltage is set via the VB3 registers (13h, bits D[7:0], and 14h, bits D[1:0]). If VB_GAIN = 0, each step is -2.5mV, and the VB3 voltage = -2.5mV x Decimal (register value). If VB_GAIN = 1, each step is -5mV, and the VB3 voltage = -5mV x Decimal (register value).

VB3 (14h)

Bits	Access	Bit Name	Default	Description
D[7:2]	R/W	RESERVED	0000 00	Reserved.
D[1:0]	R/W	LSB_2_BIT_OF_ VB3_VOLTAGE	00	Sets the VB3 pin's voltage from -0.1V to -2.5V or -0.1V to -5V, which is determined by the VB_GAIN bit. The VB3 voltage is set via the VB3 registers (13h, bits D[7:0], and 14h, bits D[1:0]). If VB_GAIN = 0, each step is -2.5mV, and the VB3 voltage = -2.5mV x Decimal (register value). If VB_GAIN = 1, each step is -5mV, and the VB3 voltage = -5mV x Decimal (register value).

VB4 (15h/16h)

Format: Unsigned binary

The VB4 command sets VB4 voltage.

VB4 (15h)

Bits	Access	Bit Name	Default	Description
D[7:0]	R/W	MSB_8_BIT_OF_ VB4_VOLTAGE	0000 0000	Sets the VB4 pin's voltage from -0.1V to -2.5V or -0.1V to -5V, which is determined by the VB_GAIN bit. The VB4 voltage is set via the VB4 registers (15h, bits D[7:0], and 16h, bits D[1:0]). If VB_GAIN = 0, each step is -2.5mV, and the VB4 voltage = -2.5mV x Decimal (register value). If VB_GAIN = 1, each step is -5mV, and the VB4 voltage = -5mV x Decimal (register value).

VB4 (16h)

Bits	Access	Bit Name	Default	Description
D[7:2]	R/W	RESERVED	0000 00	Reserved.
D[1:0]	R/W	LSB_2_BIT_OF_ VB4_VOLTAGE	00	Sets the VB4 pin's voltage from -0.1V to -2.5V or -0.1V to -5V, which is determined by the VB_GAIN bit. The VB4 voltage is set via the VB4 registers (15h, bits D[7:0], and 16h, bits D[1:0]). If VB_GAIN = 0, each step is -2.5mV, and the VB4 voltage = -2.5mV x Decimal (register value). If VB_GAIN = 1, each step is -5mV, and the VB4 voltage = -5mV x Decimal (register value).

I/O_CONFIG (18h)

Format: Unsigned binary

The I/O_CONFIG command sets the I/Ox pin's function.

Bits	Access	Bit Name	Default	Description
D[7]	R/W	I/O1	0	Sets the I/O1 pin's mode selection. 0: ADC input 1: GPO
D[6]	R/W	I/O2	0	Sets the I/O2 pin's mode selection. 0: ADC input 1: GPO

D[5]	R/W	I/O3	0	Sets the I/O3 pin's mode selection. 0: ADC input 1: GPO
D[4]	R/W	I/O4	0	Sets the I/O4 pin's mode selection. 0: ADC input 1: GPO
D[3]	R/W	I/O5	0	Sets the I/O5 pin's mode selection. 0: ADC input 1: GPO
D[2]	R/W	I/O6	0	Sets the I/O6 pin's mode selection. 0: ADC input 1: GPO
D[1:0]	R/W	RESERVED	00	Reserved.

GPO_CONFIG (19h)

Format: Unsigned binary

The GPO_CONFIG command sets the output status for the I/O1~I/O6 pins.

Bits	Access	Bit Name	Default	Description
D[7]	R/W	GPO1	0	Sets the I/O1 pin's default output if GPO mode is selected. 0: Output low 1: Output high
D[6]	R/W	GPO2	0	Sets the I/O2 pin's default output if GPO mode is selected. 0: Output low 1: Output high
D[5]	R/W	GPO3	0	Sets the I/O3 pin's default output if GPO mode is selected. 0: Output low 1: Output high
D[4]	R/W	GPO4	0	Sets the I/O4 pin's default output if GPO mode is selected. 0: Output low 1: Output high
D[3]	R/W	GPO5	0	Sets the I/O5 pin's default output if GPO mode is selected. 0: Output low 1: Output high
D[2]	R/W	GPO6	0	Sets the I/O6 pin's default output if GPO mode is selected. 0: Output low 1: Output high
D[1:0]	R/W	GPO1	00	Reserved.

GPO_PULL-UP (1Ah)

Format: Unsigned binary

The GPO_PULL-UP command sets the default structure of the I/Ox pin's output.

Bits	Access	Bit Name	Default	Description
D[7]	R/W	PL1	0	Sets the default structure of the I/O1 pin's output if GPO mode is selected. 0: Open-drain output 1: Push-pull output. Internally pull up to the VIN2 voltage when it outputs high
D[6]	R/W	PL2	0	Sets the default structure of the I/O2 pin's output if GPO mode is selected. 0: Open-drain output 1: Push-pull output. Internally pull up to the VIN2 voltage when it outputs high
D[5]	R/W	PL3	0	Sets the default structure of the I/O3 pin's output if GPO mode is selected. 0: Open-drain output 1: Push-pull output. Internally pull up to the VIN2 voltage when it outputs high
D[4]	R/W	PL4	0	Sets the default structure of the I/O4 pin's output if GPO mode is selected. 0: Open-drain output 1: Push-pull output. Internally pull up to the VIN2 voltage when it outputs high
D[3]	R/W	PL5	0	Sets the default structure of the I/O5 pin's output if GPO mode is selected. 0: Open-drain output 1: Push-pull output. Internally pull up to the VIN2 voltage when it outputs high
D[2]	R/W	PL6	0	Sets the default structure of the I/O6 pin's output if GPO mode is selected. 0: Open-drain output 1: Push-pull output. Internally pull up to the VIN2 voltage when it outputs high
D[1:0]	R/W	RESERVED	00	Reserved.

THRESHOLD1 (1Bh)

Format: Unsigned binary

The THRESHOLD1 command sets the EML (VBx) current limit.

Bits	Access	Bit Name	Default	Description
D[7:0]	R/W	CURRENT_ THRESHOLD	1111 1111	Sets the EML (VB) current limit threshold. When the monitored VB1–VB4 current exceeds this threshold based on the 8 MSB from the ADC, the INT pin sends an alarm. This threshold's step (230.4μA). For example, to set a 30mA current limit, set these bits to = BIN (30mA/230.4μA) = 1000 0010.

THRESHOLD2 (1Ch)

Format: Unsigned binary

The THRESHOLD2 command sets the Idx pin's voltage limit.

Bits	Access	Bit Name	Default	Description
D[7:0]	R/W	ID_VOLTAGE_ THRESHOLD	1111 1111	Sets the Idx pin's voltage limit. When the monitored ID1–ID4 voltage exceeds this threshold based on the 8 MSB from the ADC, the INT pin sends an alarm. This threshold's step (14.656mV). For example, to set a 2V voltage limit, set these bits = BIN (2V/14.656mV) = 1000 1000.

THRESHOLD_IO1_HIGH (1Dh)

Format: Unsigned binary

The THRESHOLD_IO1_HIGH command sets the high threshold for the I/O1 port.

Bits	Access	Bit Name	Default	Description
D[7:0]	R/W	T_IO1_H	1111 1111	Sets the high threshold for the I/O1 port when ADC mode is active. If the I/O1 port is set to ADC mode and the monitored I/O1 voltage exceeds the threshold based on the 8 MSB from the ADC, the INT pin sends an alarm This threshold's step (9.76mV). For example, to set a 2V over-voltage (OV) limit, configure these bits = BIN (2V/9.76mV) = 1100 1101.

THRESHOLD_IO1_LOW (1Eh)

Format: Unsigned binary

The THRESHOLD_IO1_LOW command sets the low threshold for the I/O1 port.

Bits	Access	Bit Name	Default	Description
D[7:0]	R/W	T_IO1_L	0000 0000	Sets the low threshold for the I/O1 port when ADC mode is active. If the I/O1 port is set to ADC mode and the monitored I/O1 voltage falls below the threshold based on the 8 MSB from the ADC, the INT pin sends an alarm. This threshold's step (9.76mV). For example, to set a 0.1V under-voltage (UV) limit, configure these bits = BIN (0.1V/9.76mV) = 0000 1010.

THRESHOLD_IO2_HIGH (1Fh)

Format: Unsigned binary

The THRESHOLD_IO2_HIGH command sets the high threshold for the I/O2 port.

Bits	Access	Bit Name	Default	Description
D[7:0]	R/W	T_IO2_H	1111 1111	Sets the high threshold for the I/O2 port when ADC mode is active. If the I/O2 port is set to ADC mode and the monitored I/O2 voltage exceeds the threshold based on the 8 MSB from the ADC, the INT pin sends an alarm This threshold's step (9.76mV).

THRESHOLD_IO2_LOW (20h)

Format: Unsigned binary

The THRESHOLD_IO2_LOW command sets the low threshold for the I/O2 port.

Bits	Access	Bit Name	Default	Description
D[7:0]	R/W	T_IO2_L	0000 0000	Sets the low threshold for the I/O2 port when ADC mode is active. If the I/O2 port is set to ADC mode and the monitored I/O2 voltage falls below the threshold based on the 8 MSB from the ADC, the INT pin sends an alarm This threshold's step (9.76mV).

THRESHOLD_IO3_HIGH (21h)

Format: Unsigned binary

The THRESHOLD_IO3_HIGH command sets the high threshold for the I/O3 port.

Bits	Access	Bit Name	Default	Description
D[7:0]	R/W	T_IO3_H	1111 1111	Sets the high threshold for the I/O3 port when ADC mode is active. If the I/O3 port is set to ADC mode and the monitored I/O3 voltage exceeds the threshold based on the 8 MSB from the ADC, the INT pin sends an alarm This threshold's step (9.76mV).

THRESHOLD_IO3_LOW (22h)

Format: Unsigned binary

The THRESHOLD_IO3_LOW command sets the low threshold of I/O3 port.

Bits	Access	Bit Name	Default	Description
D[7:0]	R/W	T_IO3_L	0000 0000	Sets the low threshold for the I/O3 port when ADC mode is active. If the I/O3 port is set to ADC mode and the monitored I/O3 voltage falls below the threshold based on the 8 MSB from the ADC, the INT pin sends an alarm This threshold's step (9.76mV).

THRESHOLD_IO4_HIGH (23h)

Format: Unsigned binary

The THRESHOLD_IO4_HIGH command sets the high threshold for the I/O4 port.

Bits	Access	Bit Name	Default	Description
D[7:0]	R/W	T_IO4_H	1111 1111	Sets the high threshold for the I/O4 port when ADC mode is active. If the I/O4 port is set to ADC mode and the monitored I/O4 voltage exceeds the threshold based on the 8 MSB from the ADC, the INT pin sends an alarm This threshold's step (9.76mV).

THRESHOLD_IO4_LOW (24h)

Format: Unsigned binary

The THRESHOLD_IO4_LOW command sets the low threshold for the I/O4 port.

Bits	Access	Bit Name	Default	Description
D[7:0]	R/W	T_IO4_L	0000 0000	Sets the low threshold for the I/O4 port when ADC mode is active. If the I/O4 port is set to ADC mode and the monitored I/O4 voltage falls below the threshold based on the 8 MSB from the ADC, the INT pin sends an alarm This threshold's step (9.76mV).

THRESHOLD_IO5_HIGH (25h)

Format: Unsigned binary

The THRESHOLD_IO5_HIGH command sets the high threshold for the I/O5 port.

Bits	Access	Bit Name	Default	Description
D[7:0]	R/W	T_IO5_H	1111 1111	Sets the high threshold for the I/O5 port when ADC mode is active. If the I/O5 port is set to ADC mode and the monitored I/O5 voltage exceeds the threshold based on the 8 MSB from the ADC, the INT pin sends an alarm This threshold's step (9.76mV).

THRESHOLD_IO5_LOW (26h)

Format: Unsigned binary

The THRESHOLD_IO5_LOW command sets the low threshold for the I/O5 port.

Bits	Access	Bit Name	Default	Description
D[7:0]	R/W	T_IO5_L	0000 0000	Sets the low threshold for the I/O5 port when ADC mode is active. If the I/O5 port is set to ADC mode and the monitored I/O5 voltage falls below the threshold based on the 8 MSB from the ADC, the INT pin sends an alarm This threshold's step (9.76mV).

THRESHOLD_IO6_HIGH (27h)

Format: Unsigned binary

The THRESHOLD_IO6_HIGH command sets the high threshold for the I/O6 port.

Bits	Access	Bit Name	Default	Description
D[7:0]	R/W	T_IO6_H	1111 1111	Sets the high threshold for the I/O6 port when ADC mode is active. If the I/O6 port is set to ADC mode and the monitored I/O6 voltage exceeds the threshold based on the 8 MSB from the ADC, the INT pin sends an alarm This threshold's step (9.76mV).

THRESHOLD_IO6_LOW (28h)

Format: Unsigned binary

The THRESHOLD_IO6_LOW command sets the low threshold for the I/O6 port.

Bits	Access	Bit Name	Default	Description
D[7:0]	R/W	T_IO6_L	0000 0000	Sets the low threshold for the I/O6 port when ADC mode is active. If the I/O6 port is set to ADC mode and the monitored I/O6 voltage falls below the threshold based on the 8 MSB from the ADC, the INT pin sends an alarm This threshold's step (9.76mV).

PROTECT (29h)

Format: Unsigned binary

The PROTECT command sets the Idx short-circuit protection (SCP) mode.

Bits	Access	Bit Name	Default	Description
D[7]	R/W	ID_SCP_MODE	0	Sets the Idx protection mode when the laser triggers SCP. If latch-off mode is enabled, the output can be re-enabled again by V_{IN1} under-voltage lockout (UVLO), V_{IN2} UVLO, the LD_ON pin's UVLO, EN pin UVLO, or the digital EN bits (including the ID_EN bit and respective Idx_EN bit). 0: Auto-recovery 1: Latch-off
D[6:0]	R/W	RESERVED	000 0000	Reserved.

ADCM1 (2Ah)

Format: Unsigned binary

The ADCM1 command enables the ADCs for the VBx current and Idx voltage.

Bits	Access	Bit Name	Default	Description
D[7]	R/W	IVB1	1	ADC manager. The high bit enables the current ADC for VB1. 0: Disabled 1: Enabled
D[6]	R/W	IVB2	1	ADC manager. The high bit enables the current ADC for VB2. 0: Disabled 1: Enabled
D[5]	R/W	IVB3	1	ADC manager. The high bit enables the current ADC for VB3. 0: Disabled 1: Enabled
D[4]	R/W	IVB4	1	ADC manager. The high bit enables the current ADC for VB4. 0: Disabled 1: Enabled
D[3]	R/W	VID1	1	ADC manager. The high bit enables the voltage ADC for ID1. 0: Disabled 1: Enabled
D[2]	R/W	VID2	1	ADC manager. The high bit enables the voltage ADC for ID2. 0: Disabled 1: Enabled
D[1]	R/W	VID3	1	ADC manager. The high bit enables the voltage ADC for ID3. 0: Disabled 1: Enabled
D[0]	R/W	VID4	1	ADC manager. The high bit enables the voltage ADC for ID4. 0: Disabled 1: Enabled

ADCM2 (2Bh)

Format: Unsigned binary

The ADCM2 command enables the ADCs for the TXx current and I/O1–I/O4 ports.

Bits	Access	Bit Name	Default	Description
D[7]	R/W	TX1	1	ADC manager. The high bit enables the current ADC for TX1. 0: Disabled 1: Enabled
D[6]	R/W	TX2	1	ADC manager. The high bit enables the current ADC for TX2. 0: Disabled 1: Enabled
D[5]	R/W	TX3	1	ADC manager. The high bit enables the current ADC for TX3. 0: Disabled 1: Enabled
D[4]	R/W	TX4	1	ADC manager. The high bit enables the current ADC for TX4. 0: Disabled 1: Enabled
D[3]	R/W	I/O1	1	ADC manager. The high bit enables the ADC input for I/O1. This bit is auto-disabled in GPO mode. 0: Disabled 1: Enabled
D[2]	R/W	I/O2	1	ADC manager. The high bit enables the ADC input for I/O2. This bit is auto-disabled in GPO mode. 0: Disabled 1: Enabled
D[1]	R/W	I/O3	1	ADC manager. The high bit enables the ADC input for I/O3. This bit is auto-disabled in GPO mode. 0: Disabled 1: Enabled
D[0]	R/W	I/O4	1	ADC manager. The high bit enables the ADC input for I/O4. This bit is auto-disabled in GPO mode. 0: Disabled 1: Enabled

ADCM3 (2Ch)

Format: Unsigned binary

The ADCM3 command enables the ADCs for the I/O5–I/O6 ports, TEMP, VIN2, and VIN3.

Bits	Access	Bit Name	Default	Description
D[7]	R/W	I/O5	1	ADC manager. The high bit enables the ADC input for I/O5. This bit is auto-disabled in GPO mode. 0: Disabled 1: Enabled
D[6]	R/W	I/O6	1	ADC manager. The high bit enables the ADC input for I/O6. This bit is auto-disabled in GPO mode. 0: Disabled 1: Enabled

D[5]	R/W	TEMP	1	ADC manager. The high bit enables the temperature ADC. 0: Disabled 1: Enabled
D[4]	R/W	VIN2	1	ADC manager. The high bit enables the voltage ADC for VIN2. 0: Disabled 1: Enabled
D[3]	R/W	VIN3	1	ADC manager. The high bit enables the voltage ADC for VIN3. 0: Disabled 1: Enabled
D[2:0]	R/W	RESERVED	000	Reserved.

CONFIG (2Dh)

Format: Unsigned binary

The CONFIG command enables the VB/ID discharge functions and refreshes the I^2C.

Bits	Access	Bit Name	Default	Description
D[7:6]	R/W	RESERVED	11	Reserved.
D[5]	R/W	VB_DISCHARGE	1	Enables the VB discharge feature. 0: Do not discharge 1: Discharge when VBx is disabled
D[4]	R/W	ID_DISCHARGE	1	Enables the ID discharge feature. 0: Do not discharge 1: Discharge when Idx is disabled
D[3]	R/W	RESERVED	0	Reserved.
D[2]	R/W	WARN_REFRESH	0	Refreshes all I^2C codes to their default values. 0: Do not refresh 1: Forced refresh then auto-recover to 0
D[1:0]	R/W	RESERVED	00	Reserved.

STATUS1 (2Eh)

Format: Unsigned binary

The STATUS1 command enables the operation status of VB1–VB4, ID1, and ID2.

Bits	Access	Bit Name	Default	Description
D[7:6]	R	RESERVED	00	Reserved.
D[5]	R	VB1_FLG	0	Enables VB1 operation. 0: Disabled 1: Enabled
D[4]	R	VB2_FLG	0	Enables VB2 operation. 0: Disabled 1: Enabled
D[3]	R	VB3_FLG	0	Enables VB3 operation. 0: Disabled 1: Enabled

D[2]	R	VB4_FLG	0	Enables VB4 operation. 0: Disabled 1: Enabled
D[1]	R	ID1_FLG	0	Enables ID1 operation. 0: Disabled 1: Enabled
D[0]	R	ID2_FLG	0	Enables ID2 operation. 0: Disabled 1: Enabled

STATUS2 (2Fh)

Format: Unsigned binary

The STATUS2 command enables the operation status of ID3, ID4, TX1–TX4, I/O1, and I/O2.

Bits	Access	Bit Name	Default	Description
D[7]	R	ID3_FLG	0	Enables ID3 operation. 0: Disabled 1: Enabled
D[6]	R	ID4_FLG	0	Enables ID4 operation. 0: Disabled 1: Enabled
D[5]	R	TX1_FLG	0	Enables TX1 measurement operation. 0: Disabled 1: Enabled
D[4]	R	TX2_FLG	0	Enables TX2 measurement operation. 0: Disabled 1: Enabled
D[3]	R	TX3_FLG	0	Enables TX3 measurement operation. 0: Disabled 1: Enabled
D[2]	R	TX4_FLG	0	Enables TX4 measurement operation. 0: Disabled 1: Enabled
D[1]	R	I/O1_FLG	0	Enables I/O1 port operation. 0: Disabled 1: Enabled
D[0]	R	I/O2_FLG	0	Enables I/O2 port operation. 0: Disabled 1: Enabled

STATUS3 (30h)

Format: Unsigned binary

The STATUS3 command enables the operation status of I/O3–I/O6, LD_ON, IDOV, VIN2_UV, and VIN3_UV.

Bits	Access	Bit Name	Default	Description
D[7]	R	I/O3_FLG	0	Enables I/O3 port operation. 0: Disabled 1: Enabled
D[6]	R	I/O4_FLG	0	Enables I/O4 port operation. 0: Disabled 1: Enabled
D[5]	R	I/O5_FLG	0	Enables I/O5 port operation. 0: Disabled 1: Enabled
D[4]	R	I/O6_FLG	0	Enables I/O6 port operation. 0: Disabled 1: Enabled
D[3]	R	LD_ON_FLG	0	Enables LD_ON EN operation. 0: Disabled 1: Enabled
D[2]	R	ID_OV	0	Indicates the Idx voltage over-voltage (OV) status. If any Idx channel's output voltage exceeds the ID voltage threshold, this bit is set to 1. 0: No OV status 1: There is an OV status
D[1]	R	VIN2_UV	0	Indicates the V_{IN2} under-voltage lockout (UVLO) status. 0: There is a UVLO status 1: No UVLO status
D[0]	R	VIN3_UV	0	Indicates the V_{IN3} UVLO status. 0: There is a UVLO status 1: No UVLO status

STATUS4 (31h)

Format: Unsigned binary

The STATUS4 command monitors the I/Ox status.

Bits	Access	Bit Name	Default	Description
D[7]	R	GPO1_OUTPUT	0	Indicates the GPO1 status when GPO mode is selected. If ADC mode is selected, do not use this bit. 0: Output low 1: Output high
D[6]	R	GPO2_OUTPUT	0	Indicates the GPO2 status when GPO mode is selected. If ADC mode is selected, do not use this bit. 0: Output low 1: Output high

D[5]	R	GPO3_OUTPUT	0	Indicates the GPO3 status when GPO mode is selected. If ADC mode is selected, do not use this bit. 0: Output low 1: Output high
D[4]	R	GPO4_OUTPUT	0	Indicates the GPO4 status when GPO mode is selected. If ADC mode is selected, do not use this bit. 0: Output low 1: Output high
D[3]	R	GPO5_OUTPUT	0	Indicates the GPO5 status when GPO mode is selected. If ADC mode is selected, do not use this bit. 0: Output low 1: Output high
D[2]	R	GPO6_OUTPUT	0	Indicates the GPO6 status when GPO mode is selected. If ADC mode is selected, do not use this bit. 0: Output low 1: Output high
D[1:0]	R	RESERVED	00	Reserved.

WARN1 (32h)

Format: Unsigned binary

The WARN1 command monitors status of ID_OC, OT_WARN, OT and VB_OC.

Bits	Access	Bit Name	Default	Description
D[7:6]	R	RESERVED	00	Reserved.
D[5]	R	VB_OC	0	Indicates whether there is a VBx over-current (OC) warning. If any VBx channel triggers the EML (VB) current threshold this bit is set to 1. This bit controls the INT pin. 0: No OC warning 1: There is an OC warning
D[4]	R	ID_OC	0	Indicates the Idx OC warning status. If any Idx voltage drops below 0.3V, this bit is set to 1. This bit controls the INT pin. 0: Good 1: Not good
D[3:2]	R	RESERVED	00	Reserved.
D[1]	R	OT_WARN	0	Indicates whether there is an over-temperature (OT) warning. This bit controls the INT pin. 0: No OT warning 1: There is an OT warning
D[0]	R	OT	0	Indicates whether there is an OT fault. This bit controls the INT pin. 0: No OT fault 1: There is an OT fault

WARN2 (33h)

Format: Unsigned binary

The WARN2 command monitors the over-voltage (OV) and under-voltage (UV) statuses of I/O1–I/O6.

Bits	Access	Bit Name	Default	Description
D[7]	R	I/O1	0	Indicates whether the OV or UV threshold has been reached for I/O1 when it is an ADC port. The bit is set to 1 if a related condition occurs and controls the INT pin. 0: No OV or UV status 1: There is an OV or UV status
D[6]	R	I/O2	0	Indicates whether the OV or UV threshold has been reached for I/O2 when it is an ADC port. The bit is set to 1 if a related condition occurs and controls the INT pin. 0: No OV or UV status 1: There is an OV or UV status
D[5]	R	I/O3	0	Indicates whether the OV or UV threshold has been reached for I/O3 when it is an ADC port. The bit is set to 1 if a related condition occurs and controls the INT pin. 0: No OV or UV status 1: There is an OV or UV status
D[4]	R	I/O4	0	Indicates whether the OV or UV threshold has been reached for I/O4 when it is an ADC port. The bit is set to 1 if a related condition occurs and controls the INT pin. 0: No OV or UV status 1: There is an OV or UV status
D[3]	R	I/O5	0	Indicates whether the OV or UV threshold has been reached for I/O5 when it is an ADC port. The bit is set to 1 if a related condition occurs and controls the INT pin. 0: No OV or UV status 1: There is an OV or UV status
D[2]	R	I/O6	0	Indicates whether the OV or UV threshold has been reached for I/O6 when it is an ADC port. The bit is set to 1 if a related condition occurs and controls the INT pin. 0: No OV or UV status 1: There is an OV or UV status
D[1:0]	R	RESERVED	0	Reserved.

MASK (34h)

Format: Unsigned binary

The MASK command masks off the INT pin’s behavior.

Bits	Access	Bit Name	Default	Description
D[7:6]	R/W	RESERVED	00	Reserved.
D[5]	R/W	VB_OC_MSK	0	Masks the VB_OC bit and controls the INT pin. 0: Not masked 1: Masked
D[4]	R/W	ID_OC_MSK	0	Masks the ID_OC bit and controls the INT pin. 0: Not masked 1: Masked

D[3:2]	R/W	RESERVED	00	Reserved.
D[1]	R/W	OT_WARN_MSK	0	Masks the OT_WARN bit and controls the INT pin. 0: Not masked 1: Masked
D[0]	R/W	OT_MSK	0	Masks the OT and controls the INT pin. 0: Not masked 1: Masked

IADJ (36h)

Format: Unsigned binary

The IADJ command sets the IADJ pin's sink/source current.

Bits	Access	Bit Name	Default	Description
D[7]	R/W	IADJ_PROGRAM	0	0: Source current from the MP5490 to the buck's FB resistor divider to regulate the buck's output voltage lower 1: Sink current from the buck's FB resistor divider to ground through the MP5490's IADJ pin. This can regulate buck's output voltage to exceed the voltage set by the FB resistor divider
D[6:0]	R/W		000 0000	Bits D[6:0] of this command set the IADJ current. Each step is 0.122μA. When selecting the source: The IADJ current is 0.122μA x Decimal (register value). The buck converter's output can be calculated with the following equation: $\left(1+\frac{R_{TOP}}{R_{BOT}}\right) x\ V_{FB} - R_{TOP}\ x\ IADJ$ Where R_{TOP} and R_{BOT} are the buck converter's feedback resistors, and V_{FB} is the buck's reference voltage. When selecting the sink: The IADJ current is 15.5μA – 0.122μA x decimal (register value). The buck converter's output can be calculated with the following equation: $\left(1+\frac{R_{TOP}}{R_{BOT}}\right) x\ V_{FB} + R_{TOP}\ x\ IADJ$

VB1_CURRENT (40h/41h)

Format: Direct

The VB1_CURRENT command monitors the VB1 current's ADC value.

VB1_CURRENT (40h)

Bits	Access	Bit Name	Default	Description
D[7:0]	R	MSB_8_BIT_OF_ VB1_CURRENT	0000 0000	The VB1 current is stored in the VB1_CURRENT registers (40h, bits D[7:0], and 41h, bits D[3:0]). Each step is 14.4μA. The current is 14.4μA x Decimal (register value).

VB1_CURRENT (41h)

Bits	Access	Bit Name	Default	Description
D[7:4]	R	RESERVED	0000	Reserved.
D[3:0]	R	LSB_4_BIT_OF_ VB1_CURRENT	0000	The VB1 current is stored in the VB1_CURRENT registers (40h, bits D[7:0], and 41h, bits D[3:0]). Each step is 14.4μA. The current is 14.4μA x Decimal (register value).

VB2_CURRENT (42h/43h)

Format: Direct

The VB2_CURRENT command monitors the VB2 current's ADC value.

VB2_CURRENT (42h)

Bits	Access	Bit Name	Default	Description
D[7:0]	R	MSB_8_BIT_OF_ VB2_CURRENT	0000 0000	The VB2 current is stored in the VB2_CURRENT registers (42h, bits D[7:0], and 43h, bits D[3:0]). Each step is 14.4μA. The current is 14.4μA x Decimal (register value).

VB2_CURRENT (43h)

Bits	Access	Bit Name	Default	Description
D[7:4]	R	RESERVED	0000	Reserved.
D[3:0]	R	LSB_4_BIT_OF_ VB2_CURRENT	0000	The VB2 current is stored in the VB2_CURRENT registers (42h, bits D[7:0], and 43h, bits D[3:0]). Each step is 14.4μA. The current is 14.4μA x Decimal (register value).

VB3_CURRENT (44h/45h)

Format: Direct

The VB3_CURRENT command monitors the VB3 current's ADC value.

VB3_CURRENT (44h)

Bits	Access	Bit Name	Default	Description
D[7:0]	R	MSB_8_BIT_OF_ VB3_CURRENT	0000 0000	The VB3 current is stored in the VB3_CURRENT registers (44h, bits D[7:0], and 45h, bits D[3:0]). Each step is 14.4μA. The current is 14.4μA x Decimal (register value).

VB3_CURRENT (45h)

Bits	Access	Bit Name	Default	Description
D[7:4]	R	RESERVED	0000	Reserved.
D[3:0]	R	LSB_4_BIT_OF_ VB3_CURRENT	0000	The VB3 current is stored in the VB3_CURRENT registers (44h, bits D[7:0], and 45h, bits D[3:0]). Each step is 14.4μA. The current is 14.4μA x Decimal (register value).

VB4_CURRENT (46h/47h)

Format: Direct

The VB4_CURRENT command monitors the VB4 current's ADC value.

VB4_CURRENT (46h)

Bits	Access	Bit Name	Default	Description
D[7:0]	R	MSB_8_BIT_OF_ VB4_CURRENT	0000 0000	The VB4 current is stored in the VB4_CURRENT registers (46h, bits D[7:0], and 47h, bits D[3:0]). Each step is 14.4μA. The current is 14.4μA x Decimal (register value).

VB4_CURRENT (47h)

Bits	Access	Bit Name	Default	Description
D[7:4]	R	RESERVED	0000	Reserved.
D[3:0]	R	LSB_4_BIT_OF_ VB4_CURRENT	0000	The VB4 current is stored in the VB4_CURRENT registers (46h, bits D[7:0], and 47h, bits D[3:0]). Each step is 14.4μA. The current is 14.4μA x Decimal (register value).

ID1_VOLTAGE (48h/49h)

Format: Direct

The ID1_VOLTAGE command monitors the ID1 voltage's ADC value.

ID1_VOLTAGE (48h)

Bits	Access	Bit Name	Default	Description
D[7:0]	R	MSB_8_BIT_OF_ ID1_VOLTAGE	0000 0000	The ID1 voltage is stored in the ID1_VOLTAGE registers (48h, bits D[7:0], and 49h, bits D[3:0]). Each step is 0.916mV. The voltage is 0.916mV x Decimal (register value).

ID1_VOLTAGE (49h)

Bits	Access	Bit Name	Default	Description
D[7:4]	R	RESERVED	0000	Reserved.
D[3:0]	R	LSB_4_BIT_OF_ ID1_VOLTAGE	0000	The ID1 voltage is stored in the ID1_VOLTAGE registers (48h, bits D[7:0], and 49h, bits D[3:0]). Each step is 0.916mV. The voltage is 0.916mV x Decimal (register value).

ID2_VOLTAGE (4Ah/4Bh)

Format: Direct

The ID2_VOLTAGE command monitors the ID2 voltage's ADC value.

ID2_VOLTAGE (4Ah)

Bits	Access	Bit Name	Default	Description
D[7:0]	R	MSB_8_BIT_OF_ ID2_VOLTAGE	0000 0000	The ID2 voltage is stored in the ID2_VOLTAGE registers (4Ah, bits D[7:0], and 4Bh, bits D[3:0]). Each step is 0.916mV. The voltage is 0.916mV x Decimal (register value).

ID2_VOLTAGE (4Bh)

Bits	Access	Bit Name	Default	Description
D[7:4]	R	RESERVED	0000	Reserved.
D[3:0]	R	LSB_4_BIT_OF_ ID2_VOLTAGE	0000	The ID2 voltage is stored in the ID2_VOLTAGE registers (4Ah, bits D[7:0], and 4Bh, bits D[3:0]). Each step is 0.916mV. The voltage is 0.916mV x Decimal (register value).

ID3_VOLTAGE (4Ch/4Dh)

Format: Direct

The ID3_VOLTAGE command monitors ID3 voltage ADC value.

ID3_VOLTAGE (4Ch)

Bits	Access	Bit Name	Default	Description
D[7:0]	R	MSB_8_BIT_OF_ ID3_VOLTAGE	0000 0000	The ID3 voltage is stored in the ID3_VOLTAGE registers (4Ch, bits D[7:0], and 4Dh, bits D[3:0]). Each step is 0.916mV. The voltage is 0.916mV x Decimal (register value).

ID3_VOLTAGE (4Dh)

Bits	Access	Bit Name	Default	Description
D[7:4]	R	RESERVED	0000	Reserved.
D[3:0]	R	LSB_4_BIT_OF_ ID3_VOLTAGE	0000	The ID3 voltage is stored in the ID3_VOLTAGE registers (4Ch, bits D[7:0], and 4Dh, bits D[3:0]). Each step is 0.916mV. The voltage is 0.916mV x Decimal (register value).

ID4_VOLTAGE (4Eh/4Fh)

Format: Direct

The ID4_VOLTAGE command monitors the ID4 voltage's ADC value.

ID4_VOLTAGE (4Eh)

Bits	Access	Bit Name	Default	Description
D[7:0]	R	MSB_8_BIT_OF_ ID4_VOLTAGE	0000 0000	The ID4 voltage is stored in the ID4_VOLTAGE registers (4Eh, bits D[7:0], and 4Fh, bits D[3:0]). Each step is 0.916mV. The voltage is 0.916mV x Decimal (register value).

ID4_VOLTAGE (4Fh)

Bits	Access	Bit Name	Default	Description
D[7:4]	R	RESERVED	0000	Reserved.
D[3:0]	R	LSB_4_BIT_OF_ ID4_VOLTAGE	0000	The ID4 voltage is stored in the ID4_VOLTAGE registers (4Eh, bits D[7:0], and 4Fh, bits D[3:0]). Each step is 0.916mV. The voltage is 0.916mV x Decimal (register value).

TX1_CURRENT (50h/51h)

Format: Direct

The TX1_CURRENT command monitors the TX1 current's ADC value.

TX1_CURRENT (50h)

Bits	Access	Bit Name	Default	Description
D[7:0]	R	MSB_8_BIT_OF_ TX1_CURRENT	0000 0000	The TX1 current is stored in the TX1_CURRENT registers (50h, bits D[7:0], and 51h, bits D[3:0]). Each step is 1.16μA. The current is 1.16μA x Decimal (register value).

TX1_CURRENT (51h)

Bits	Access	Bit Name	Default	Description
D[7:4]	R	RESERVED	0000	Reserved.
D[3:0]	R	LSB_4_BIT_OF_ TX1_CURRENT	0000	The TX1 current is stored in the TX1_CURRENT registers (50h, bits D[7:0], and 51h, bits D[3:0]). Each step is 1.16μA. The current is 1.16μA x Decimal (register value).

TX2_CURRENT (52h/53h)

Format: Direct

The TX2_CURRENT command monitors the TX2 current's ADC value.

TX2_CURRENT (52h)

Bits	Access	Bit Name	Default	Description
D[7:0]	R	MSB_8_BIT_OF_ TX2_CURRENT	0000 0000	The TX2 current is stored in the TX2_CURRENT registers (52h, bits D[7:0], and 53h, bits D[3:0]). Each step is 1.16μA. The current is 1.16μA x Decimal (register value).

TX2_CURRENT (53h)

Bits	Access	Bit Name	Default	Description
D[7:4]	R	RESERVED	0000	Reserved.
D[3:0]	R	LSB_4_BIT_OF_ TX2_CURRENT	0000	The TX2 current is stored in the TX2_CURRENT registers (52h, bits D[7:0], and 53h, bits D[3:0]). Each step is 1.16μA. The current is 1.16μA x Decimal (register value).

TX3_CURRENT (54h/55h)

Format: Direct

The TX3_CURRENT command monitors the TX3 current's ADC value.

TX3_CURRENT (54h)

Bits	Access	Bit Name	Default	Description
D[7:0]	R	MSB_8_BIT_OF_ TX3_CURRENT	0000 0000	The TX3 current is stored in the TX3_CURRENT registers (54h, bits D[7:0], and 55h, bits D[3:0]). Each step is 1.16μA. The current is 1.16μA x Decimal (register value).

TX3_CURRENT (55h)

Bits	Access	Bit Name	Default	Description
D[7:4]	R	RESERVED	0000	Reserved.
D[3:0]	R	LSB_4_BIT_OF_ TX3_CURRENT	0000	The TX3 current is stored in the TX3_CURRENT registers (54h, bits D[7:0], and 55h, bits D[3:0]). Each step is 1.16μA. The current is 1.16μA x Decimal (register value).

TX4_CURRENT (56h/57h)

Format: Direct

The TX4_CURRENT command monitors the TX4 current's ADC value.

TX4_CURRENT (56h)

Bits	Access	Bit Name	Default	Description
D[7:0]	R	MSB_8_BIT_OF_ TX4_CURRENT	0000 0000	The TX4 current is stored in the TX4_CURRENT registers (56h, bits D[7:0], and 57h, bits D[3:0]). Each step is 1.16μA. The current is 1.16μA x Decimal (register value).

TX4_CURRENT (57h)

Bits	Access	Bit Name	Default	Description
D[7:4]	R	RESERVED	0000	Reserved.
D[3:0]	R	LSB_4_BIT_OF_ TX4_CURRENT	0000	The TX4 current is stored in the TX4_CURRENT registers (56h, bits D[7:0], and 57h, bits D[3:0]). Each step is 1.16μA. The current is 1.16μA x Decimal (register value).

I/O1_VOLTAGE (58h/59h)

Format: Direct

The I/O1_VOLTAGE command monitors the I/O1 voltage's ADC value.

I/O1_VOLTAGE (58h)

Bits	Access	Bit Name	Default	Description
D[7:0]	R	MSB_8_BIT_OF_ I/O1_VOLTAGE	0000 0000	The I/O1 voltage is stored in the I/O1_VOLTAGE registers (58h, bits D[7:0], and 59h, bits D[3:0]).Each step is 0.61mV. The voltage is 0.61mV x Decimal (register value).

I/O1_VOLTAGE (59h)

Bits	Access	Bit Name	Default	Description
D[7:4]	R	RESERVED	0000	Reserved.
D[3:0]	R	LSB_4_BIT_OF_ I/O1_VOLTAGE	0000	The I/O1 voltage is stored in the I/O1_VOLTAGE registers (58h, bits D[7:0], and 59h, bits D[3:0]).Each step is 0.61mV. The voltage is 0.61mV x Decimal (register value).

I/O2_VOLTAGE (5Ah/5Bh)

Format: Direct

The I/O2_VOLTAGE command monitors the I/O2 voltage's ADC value.

I/O2_VOLTAGE (5Ah)

Bits	Access	Bit Name	Default	Description
D[7:0]	R	MSB_8_BIT_OF_ I/O2_VOLTAGE	0000 0000	The I/O2 voltage is stored in the I/O2_VOLTAGE registers (5Ah, bits D[7:0], and 5Bh, bits D[3:0]). Each step is 0.61mV. The voltage is 0.61mV x Decimal (register value).

I/O2_VOLTAGE (5Bh)

Bits	Access	Bit Name	Default	Description
D[7:4]	R	RESERVED	0000	Reserved.
D[3:0]	R	LSB_4_BIT_OF_ I/O2_VOLTAGE	0000	The I/O2 voltage is stored in the I/O2_VOLTAGE registers (5Ah, bits D[7:0], and 5Bh, bits D[3:0]). Each step is 0.61mV. The voltage is 0.61mV x Decimal (register value).

I/O3_VOLTAGE (5Ch/5Dh)

Format: Direct

The I/O3_VOLTAGE command monitors the I/O3 voltage's ADC value.

I/O3_VOLTAGE (5Ch)

Bits	Access	Bit Name	Default	Description
D[7:0]	R	MSB_8_BIT_OF_ I/O3_VOLTAGE	0000 0000	The I/O3 voltage is stored in the I/O3_VOLTAGE registers (5Ch, bits D[7:0], and 5Dh, bits D[3:0]). Each step is 0.61mV. The voltage is 0.61mV x Decimal (register value).

I/O3_VOLTAGE (5Dh)

Bits	Access	Bit Name	Default	Description
D[7:4]	R	RESERVED	0000	Reserved.
D[3:0]	R	LSB_4_BIT_OF_ I/O3_VOLTAGE	0000	The I/O3 voltage is stored in the I/O3_VOLTAGE registers (5Ch, bits D[7:0], and 5Dh, bits D[3:0]). Each step is 0.61mV. The voltage is 0.61mV x Decimal (register value).

I/O4_VOLTAGE (5Eh/5Fh)

Format: Direct

The I/O4_VOLTAGE command monitors the I/O4 voltage's ADC value.

I/O4_VOLTAGE (5Eh)

Bits	Access	Bit Name	Default	Description
D[7:0]	R	MSB_8_BIT_OF_ I/O4_VOLTAGE	0000 0000	The I/O4 voltage is stored in the I/O4_VOLTAGE registers (5Eh, bits D[7:0], and 5Fh, bits D[3:0]). Each step is 0.61mV. The voltage is 0.61mV x Decimal (register value).

I/O4_VOLTAGE (5Fh)

Bits	Access	Bit Name	Default	Description
D[7:4]	R	RESERVED	0000	Reserved.
D[3:0]	R	LSB_4_BIT_OF_ I/O4_VOLTAGE	0000	The I/O4 voltage is stored in the I/O4_VOLTAGE registers (5Eh, bits D[7:0], and 5Fh, bits D[3:0]). Each step is 0.61mV. The voltage is 0.61mV x Decimal (register value).

I/O5_VOLTAGE (60h/61h)

Format: Direct

The I/O5_VOLTAGE command monitors the I/O5 voltage's ADC value.

I/O5_VOLTAGE (60h)

Bits	Access	Bit Name	Default	Description
D[7:0]	R	MSB_8_BIT_OF_ I/O5_VOLTAGE	0000 0000	The I/O5 voltage is stored in the I/O5_VOLTAGE registers (60h, bits D[7:0], and 61h, bits D[3:0]). Each step is 0.61mV. The voltage is 0.61mV x Decimal (register value).

I/O5_VOLTAGE (61h)

Bits	Access	Bit Name	Default	Description
D[7:4]	R	RESERVED	0000	Reserved.
D[3:0]	R	LSB_4_BIT_OF_ I/O5_VOLTAGE	0000	The I/O5 voltage is stored in the I/O5_VOLTAGE registers (60h, bits D[7:0], and 61h, bits D[3:0]). Each step is 0.61mV. The voltage is 0.61mV x Decimal (register value).

I/O6_VOLTAGE (62h/63h)

Format: Direct

The I/O6_VOLTAGE command monitors the I/O6 voltage's ADC value.

I/O6_VOLTAGE (62h)

Bits	Access	Bit Name	Default	Description
D[7:0]	R	MSB_8_BIT_OF_ I/O6_VOLTAGE	0000 0000	The I/O6 voltage is stored in the I/O6_VOLTAGE registers (62h, bits D[7:0], and 63h, bits D[3:0]). Each step is 0.61mV. The voltage is 0.61mV x Decimal (register value).

I/O6_VOLTAGE (63h)

Bits	Access	Bit Name	Default	Description
D[7:4]	R	RESERVED	0000	Reserved.
D[3:0]	R	LSB_4_BIT_OF_ I/O6_VOLTAGE	0000	The I/O6 voltage is stored in the I/O6_VOLTAGE registers (62h, bits D[7:0], and 63h, bits D[3:0]). Each step is 0.61mV. The voltage is 0.61mV x Decimal (register value).

TEMP (64h/65h)

Format: Direct

The TEMP command monitors temperature ADC value.

TEMP (64h)

Bits	Access	Bit Name	Default	Description
D[7:0]	R	MSB_8_BIT_OF_ TEMPERATURE	0000 0000	The temperature is stored in the TEMP registers (64h, bits D[7:0], and 65h, bits D[3:0]). Each step is 0.074°C. The temperature is 0.074 x Decimal (register value) – 143°C.

TEMP (65h)

Bits	Access	Bit Name	Default	Description
D[7:4]	R	RESERVED	0000	Reserved.
D[3:0]	R	LSB_4_BIT_OF_ TEMPERATURE	0000	The temperature is stored in the TEMP registers (64h, bits D[7:0], and 65h, bits D[3:0]). Each step is 0.074°C. The temperature is 0.074 x Decimal (register value) – 143°C.

VIN2_VOLTAGE (66h/67h)

Format: Direct

The VIN2_VOLTAGE command monitors the VIN2 voltage's ADC value.

VIN2_VOLTAGE (66h)

Bits	Access	Bit Name	Default	Description
D[7:0]	R	MSB_8_BIT_OF_ VIN2_VOLTAGE	0000 0000	The VIN2 voltage is stored in the VIN2_VOLTAGE registers (66h, bits D[7:0], and 67h, bits D[3:0]). Each step is 1.52mV. The voltage is 1.52mV x Decimal (register value).

VIN2_VOLTAGE (67h)

Bits	Access	Bit Name	Default	Description
D[7:4]	R	RESERVED	0000	Reserved.
D[3:0]	R	LSB_4_BIT_OF_ VIN2_VOLTAGE	0000	The VIN2 voltage is stored in the VIN2_VOLTAGE registers (66h, bits D[7:0], and 67h, bits D[3:0]). Each step is 1.52mV. The voltage is 1.52mV x Decimal (register value).

VIN3_VOLTAGE (68h/69h)

Format: Direct

The VIN3_VOLTAGE command monitors the VIN3 voltage's ADC value.

VIN3_VOLTAGE (68h)

Bits	Access	Bit Name	Default	Description
D[7:0]	R	MSB_8_BIT_OF_ VIN3_VOLTAGE	0000 0000	The VIN3 voltage is stored in the VIN3_VOLTAGE registers (68h, bits D[7:0], and 69h, bits D[3:0]). Each step is -1.58mV. The voltage is -1.58mV x Decimal (register value).

VIN3_VOLTAGE (69h)

Bits	Access	Bit Name	Default	Description
D[7:4]	R	RESERVED	0000	Reserved.
D[3:0]	R	LSB_4_BIT_OF_ VIN3_VOLTAGE	0000	The VIN3 voltage is stored in the VIN3_VOLTAGE registers (68h, bits D[7:0], and 69h, bits D[3:0]). Each step is -1.58mV. The voltage is -1.58mV x Decimal (register value).

APPLICATION INFORMATION

Selecting the Output Capacitor

The output capacitors (C5~C12) help to reduce noise. It is recommended to use 1µF ceramic capacitors for the best performance.

Selecting the Input Capacitor

For stable operation, decoupling capacitors (C1, C2, and C3) are required between the VIN1, VIN2, and VIN3 to GND pins. It is recommended to add a 10µF ceramic capacitor to the VIN1, VIN2, and VIN3 pins.

IMON Setting

The MP5490 can set 0.25mA/LSB for the Idx output, and it supports up to 250mA of current sourcing with a 60.4kΩ resistor connected from IMON to AGND.

Design Example

Table 2 lists a design example following the application guidelines for the specifications below.

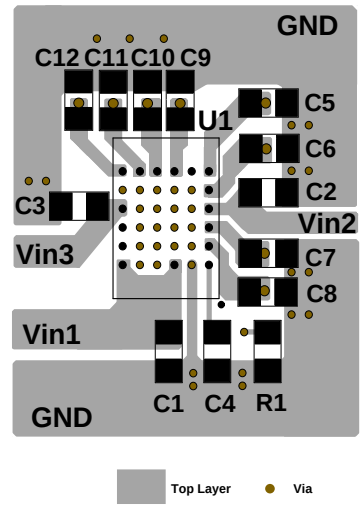
Table 2: Design Example

V_{IN1}	3.3V
V_{IN2}	1.8V
V_{IN3}	-3.3V
ID1–ID4	100mA
VB1–VB4	-1.2V

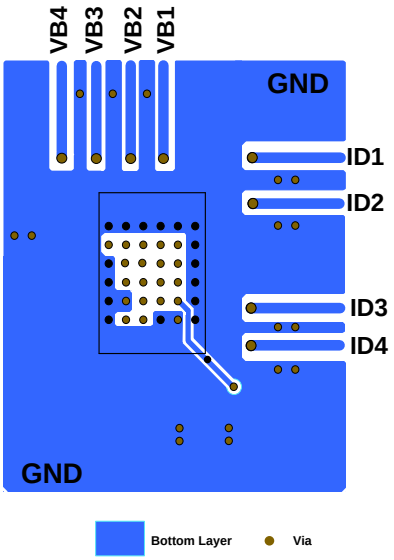
PCB Layout Guidelines

PCB layout is critical for ripple rejection and thermal performance. For the best results, refer to Figure 15 and follow the guidelines below:

1. Place the input capacitors (C1 and C4) as close as possible to the VIN1/REF and AGND pins.
2. Place the output capacitors (C2 and C5–C8) as close as possible to the VIN2/ID1–ID4 and PGND pins.
3. Place the output capacitor (C3 and C9–C12) as close as possible to the VIN3/VB1–VB4 and PGND pins.
4. Connect the input and output capacitors' GND to the PGND pins with a short and wide trace.



Top Layer



Bottom Layer

Figure 15: Recommended PCB Layout

TYPICAL APPLICATION CIRCUIT

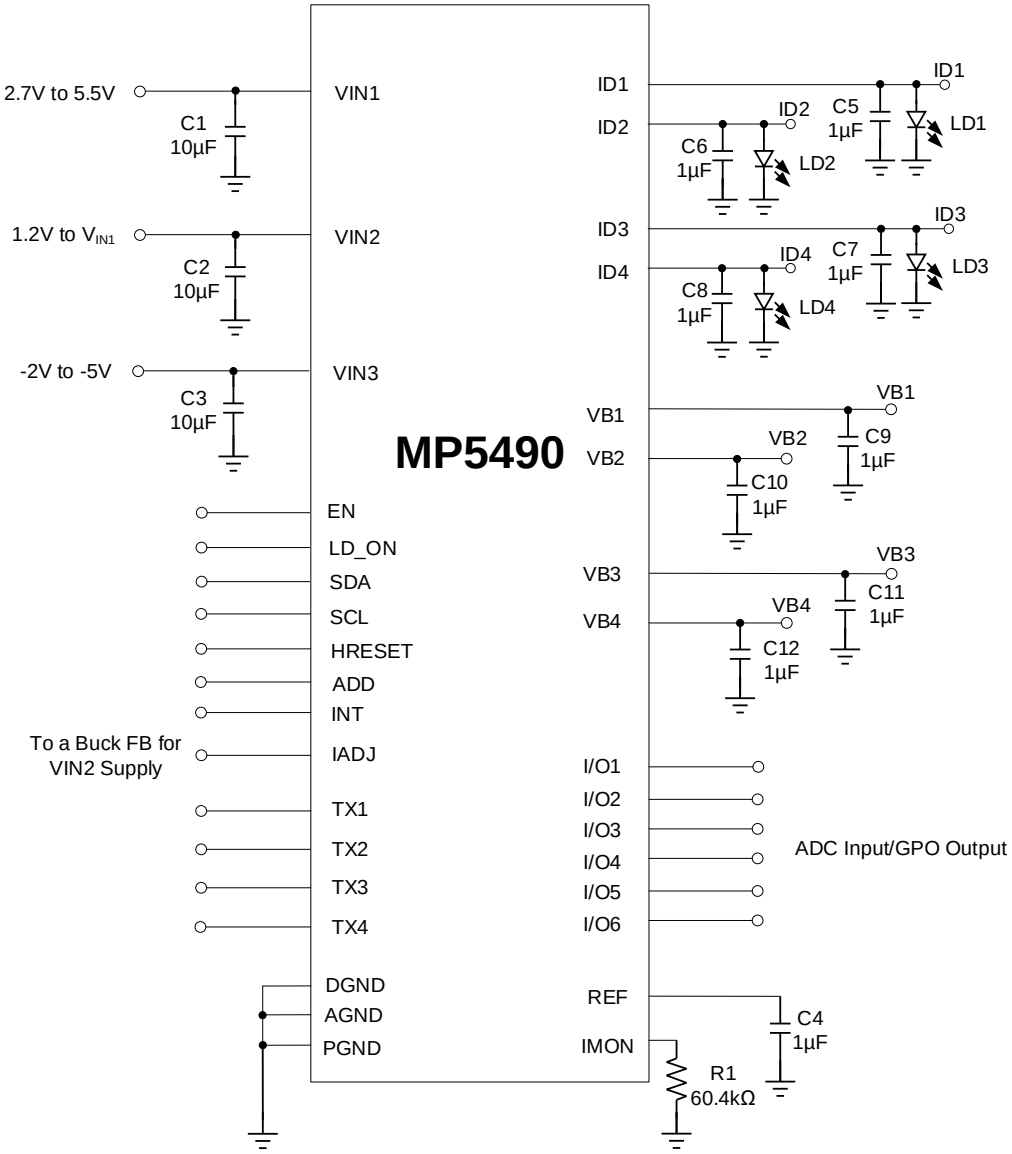
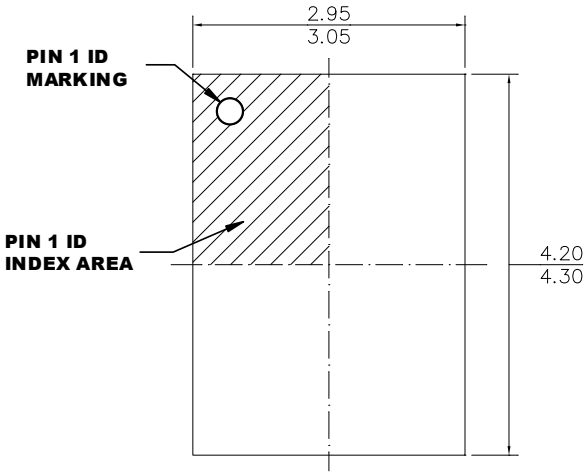


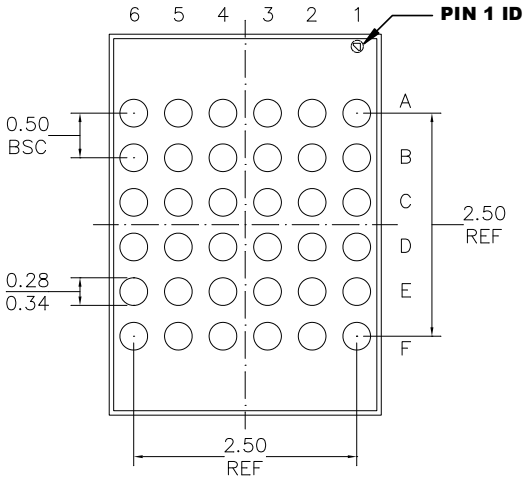
Figure 16: Typical Application Circuit

PACKAGE INFORMATION

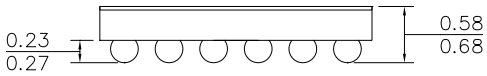
WLCSP-36 (3mmx4.25mm)



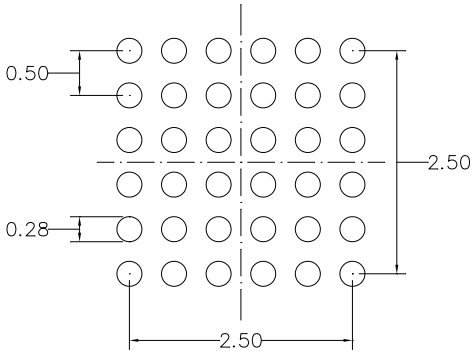
TOP VIEW



BOTTOM VIEW



SIDE VIEW

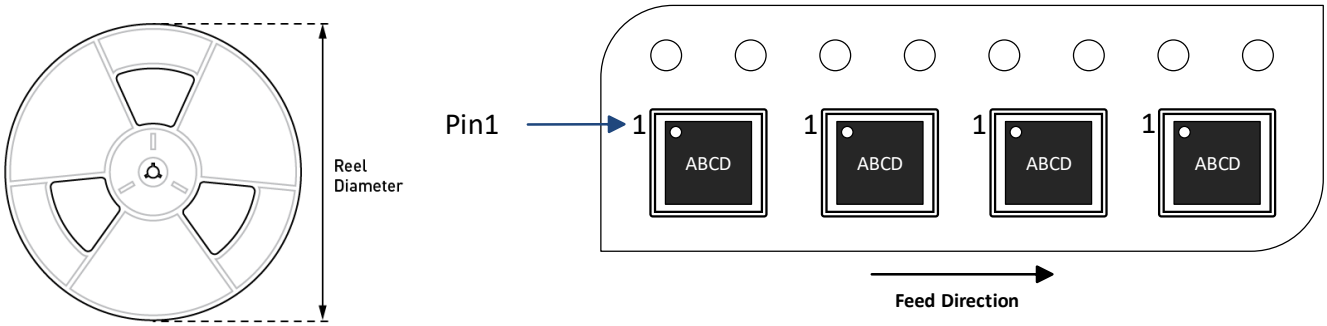


RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) BALL COPLANARITY SHALL BE 0.05 MILLIMETER MAX.
3) JEDEC REFERENCE IS MO-211.
4) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP5490GC-xxxx-Z	WLCSP-36 (3mmx4.25mm)	5000	N/A	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	5/10/2024	Initial Release	-