EV2724-RH-00A

I²C-Controlled, Single-Cell, 2.2A, NVDC Buck Charger with USB Type-C Sink Mode Evaluation Board

DESCRIPTION

The EV2724-RH-00A is an evaluation board designed to demonstrate the capabilities of the MP2724, a highly integrated, 2.2A, switch-mode battery management device for single-cell Li-ion or Li-polymer batteries. The narrow-voltage DC (NVDC) power path management (PPM) structure provides a low-impedance power path, which optimizes charging efficiency, reduces battery charging time, and extends battery life during discharging.

The MP2724 supports USB Type-C sink mode to detect the current capability of a USB Type-C adapter. USB Battery Charging Specification 1.2 (BC1.2) and non-standard adapter detection are also supported by the input source type identification algorithm.

The I²C interface offers complete operating control, charging parameter configuration, and status/interrupt monitoring.

The MP2724 supports a fully customizable JEITA profile with configurable temperature windows and actions.

The EV2724-RH-00A supports input sources up to 6.3V. It also supports boost mode and USB on-the-go (OTG) operation by supplying a voltage between 5V and 5.35V at the IN pin.

PERFORMANCE SUMMARY

Parameters	Conditions	Value
Input voltage (V_{IN}) supply		4V to 6.3V
Battery voltage (V_{BATT})		0V to 4.6V
Charge current (I_{CC})		0A to 2.2A
Input current (I_{IN})		0A to 3.2A
Boost output current (I_{BOOST_OUT})		0A to 3A

EVALUATION BOARD
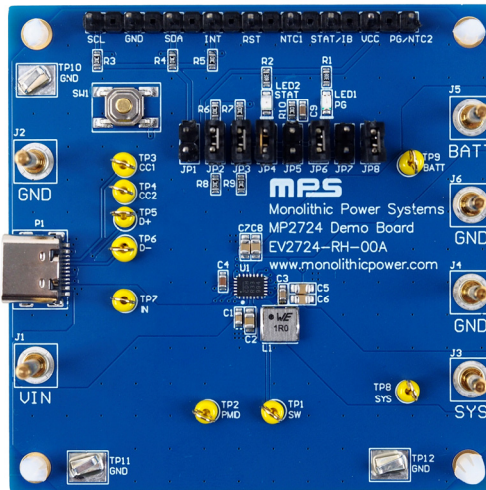
LxWxH (6.3cmx6.3cmx1.3cm)

Board Number	MPS IC Number
EV2724-RH-00A	MP2724GRH

QUICK START GUIDE

The EV2724-RH-00A evaluation board is designed to evaluate the MP2724. The EV2724-RH-00A layout accommodates most commonly used capacitors. The default function of this board is preset for charger mode, and the charge-full voltage is preset to 4.2V for a single-cell Li-ion battery.

Table 1 shows the EV2724-RH-00A's input and output connections.

Table 1: Input and Output Connections

Connectors	Description
J1, VIN	Positive input source terminal
J2, GND	Negative input source terminal
J3, SYS	Positive system load terminal
J4, GND	Negative system load terminal
J5, BATT	Positive battery pack terminal
J6, GND	Negative battery pack terminal
P1	USB Type-C connector
SCL, SDA, GND	I^{2}C connector

Table 2 shows the EV2724-RH-00A's jumper set-ups.

Table 2: Jumper Installations

| Jumper	Description	Default
JP1	I^{2}C pull-up to VCC.	Off
JP2	NTC1 on-board resistor divider.	On
JP3	NTC2 on-board resistor divider.	On
JP4	LED indication for STAT/IB.	On
JP5	IB resistor for STAT/IB. JP4 and JP5 should not be installed simultaneously.	Off
JP6	LED indication for PG/NTC2.	On
JP7	NTC2 connection to PG/NTC2. JP6 and JP7 should not be installed simultaneously.	Off
JP8	BATTSNS connection to BATT.	On

Evaluation Board Set-Up

1. The MP2724 evaluation software must be properly installed on the computer.

2. Prepare the USB-to-I^{2}C communication interface (EVKT-USBI2C-02) (see Figure 1).

Figure 1: USB-to-I^{2}C Communication Interface

3. Configure the test set-up for the MP2724 (see Figure 2 on page 3).
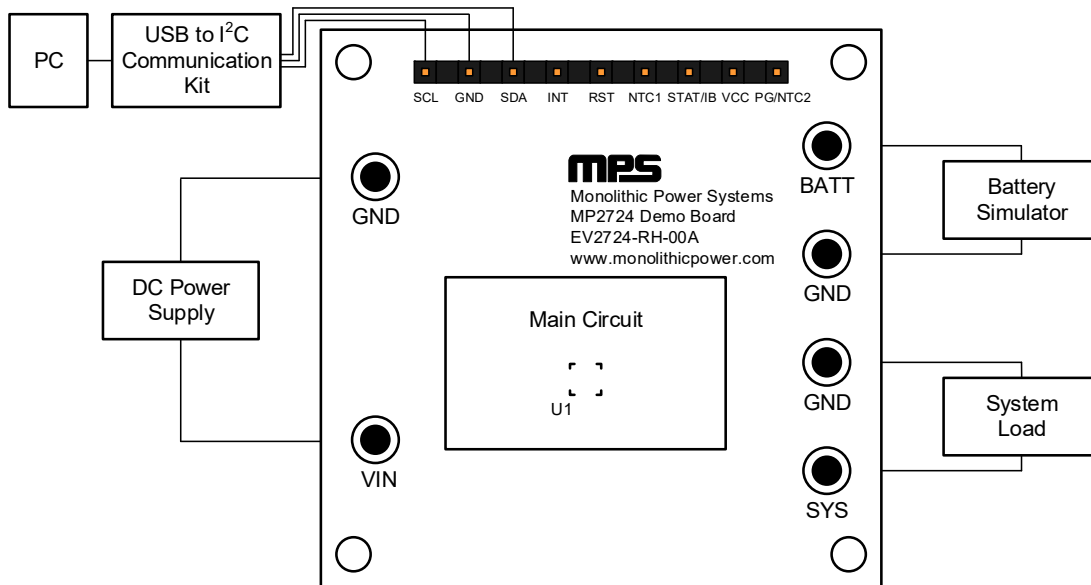
Figure 2: Measurement Equipment Set-Up

Start-Up Procedure

1. Set the battery simulator output to 3.8V, with the charge/discharge current limit set at 5A, then turn off the battery simulator.

2. Connect the battery simulator terminals to:
   a. Positive (+): BATT
   b. Negative (-): GND

3. Set the DC power source output to 5V, with the output current limit set at 5A, then turn off the DC power source.

4. Connect the DC power source terminals to:
   a. Positive (+): VIN
   b. Negative (-): GND

5. Connect the system load (typically an e-load device) terminals to:
   a. Positive (+): SYS
   b. Negative (-): GND

6. Set the system load to 0A.

7. Turn on the battery simulator.

8. Turn on the DC power source.

9. If necessary, turn on the system load.

10. Launch the MP2724 evaluation software. Figure 3 on page 4 shows the GUI's main window.

Figure 3: MP2724 Evaluation Software

GUI Operating Instructions

1. Ensure that all the connections are successful, including the connection between the USB-to-I²C communication interface and the EV2724-RH-00A. Successful connections are indicated in green on the lower left side of the GUI window (see Figure 3). The GUI is ready to run once all of the connections are successful.

2. Once the connections are successful, click the "Read All" button to update the GUI to the default settings.

3. After modifying the settings via the GUI, click the "Update All" button to write the settings to the MP2724's registers.
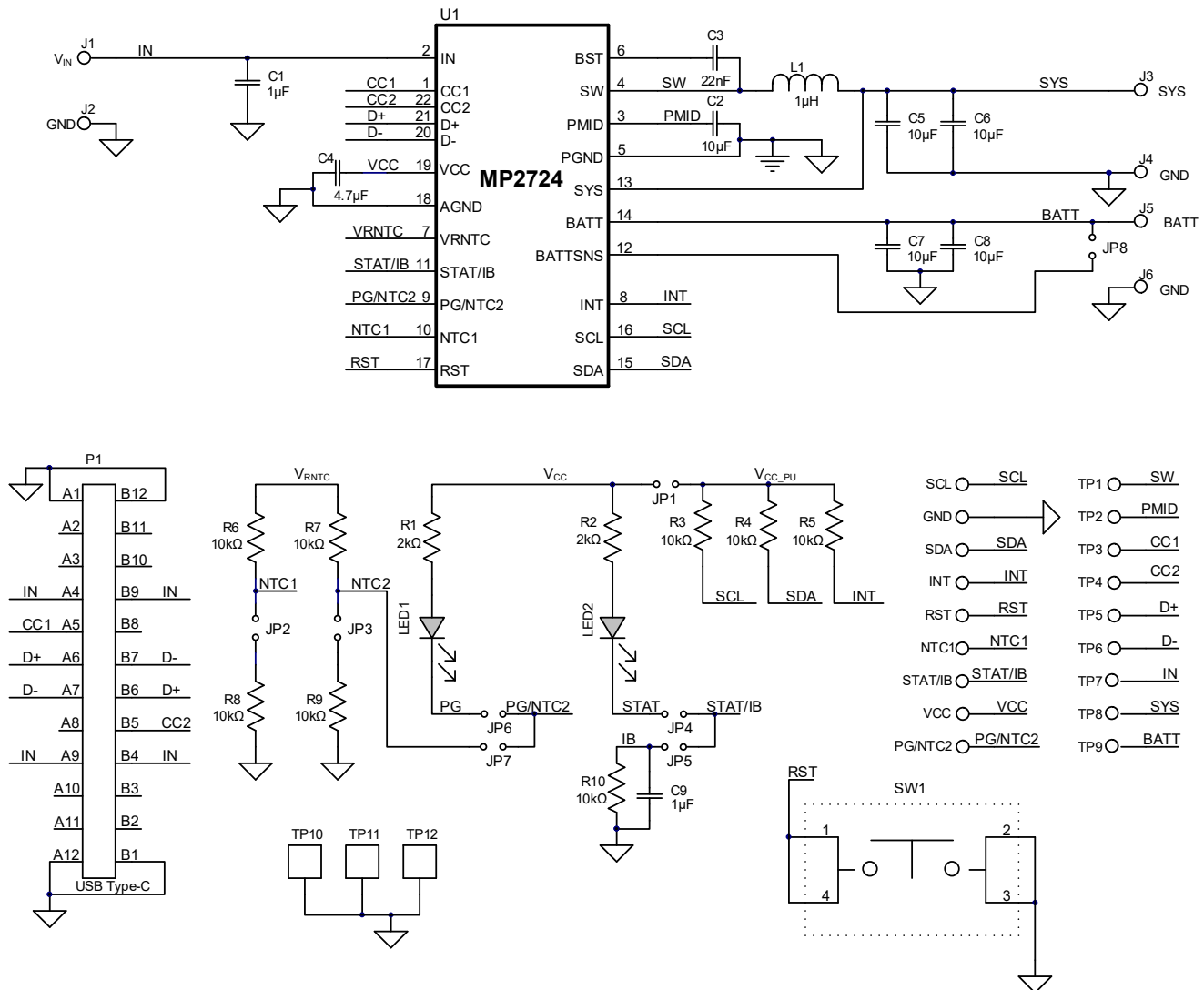
EVALUATION BOARD SCHEMATIC

Figure 4: Evaluation Board Schematic

EV2724-RH-00A BILL OF MATERIALS

| Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
1	C1	1μF	Ceramic capacitor, 25V, X7R	0603	Murata	GRM188R71E105K A12D
1	C2	10μF	Ceramic capacitor, 25V, X5R	0805	Murata	GRM21BR61E106K A73
1	C3	22nF	Ceramic capacitor, 100V, X7R	0603	Murata	GRM188R72A223K AC4D
1	C4	4.7μF	Ceramic capacitor, 16V, X7R	0603	Murata	GRM188R61C475K AAJD
4	C5, C6, C7, C8	10μF	Ceramic capacitor, 16V, X5R	0805	Murata	GRM21BR61C106K E15L
1	C9	1μF	Ceramic capacitor, 16V, X7R	0603	Murata	GRM188R71C105K A12D
1	L1	1μH	Inductor, R_{DC} = 12mΩ, I_{SAT} = 9A	SMD	Wurth	78438356010
2	R1, R2	2kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-072KL
3	R3, R4, R5	10kΩ	Film resistor, 5%	0603	Yageo	RC0603JR-0710K
5	R6, R7, R8, R9, R10	10kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-0710KL
1	LED1	Red	Red LED	0805	Bright LED	F3D02R-4A
1	LED2	Green	Green LED	0805	Bright LED	F3D02HG-1A
1	SW1	4mmx 10mm	Push button	SMD	Any	
1	P1	5A	Type-C connector	SMD	Any	
6	J1, J2, J3, J4, J5, J6	2mm	Connector	DIP	Any	
9	TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9	1mm	Test point, yellow	DIP	Any	
3	TP10, TP11, TP12	2.8mmx 3.8mm	Test point, ground	SMD	Any	
9	GND, INT, NTC1, PG/NTC2, RST, SCL, SDA, STAT/IB, VCC	2.54mm	Row connector	DIP	Any	
8	JP1, JP2, JP3, JP4, JP5, JP6, JP7, JP8	2.54mm	Row connector	DIP	Any	
5	JP2, JP3, JP4, JP6, JP8	2.54mm	Shunt	DIP	Any	
1	U1	MP2724	I^{2}C-controlled, single-cell, 2.2A, NVDC buck charger with USB Type-C sink mode	QFN-22 (2.5mmx 3.5mm)	MPS	MP2724GRH

PCB LAYOUT
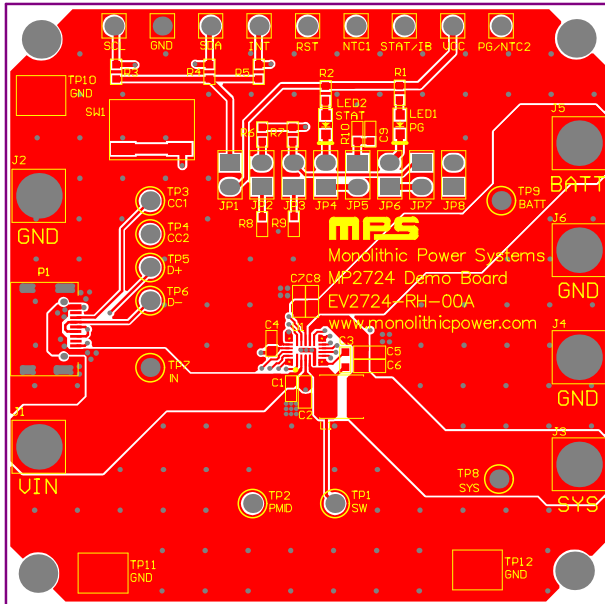
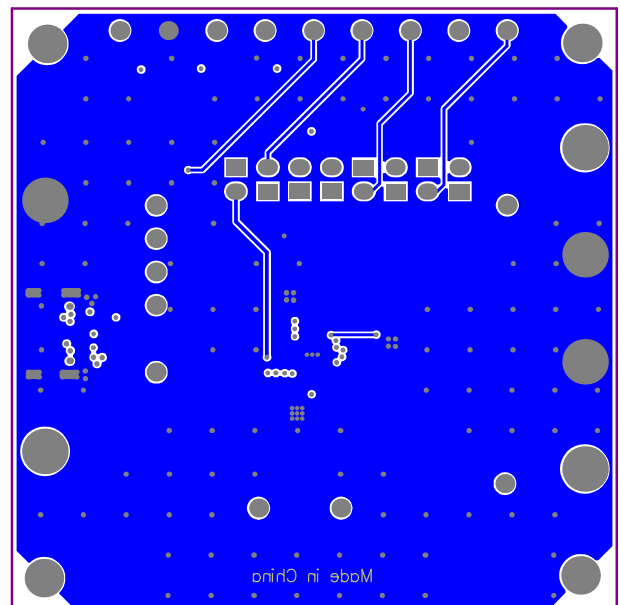Figure 5: Top Layer
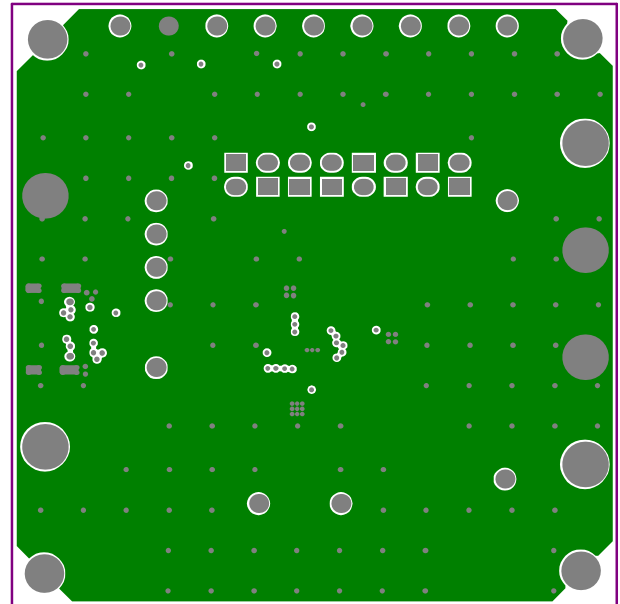
Figure 6: Mid-Layer 1
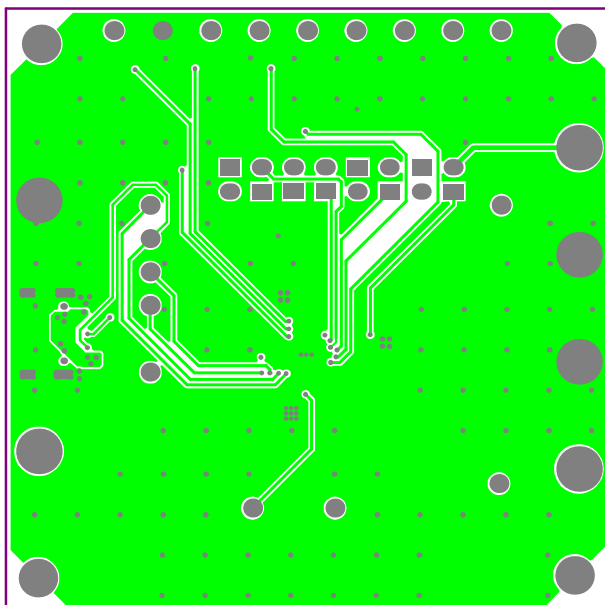
Figure 7: Mid-Layer 2

Figure 8: Bottom Layer

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	11/10/2023	Initial Release	-