MP2193

3A, 2.5V to 5.5V, Synchronous Step-Down Converter with 25µA I_Q in a WLCSP Package

DESCRIPTION

The MP2193 is a monolithic, step-down switch-mode converter with built-in, internal power MOSFETs. The MP2193 achieves 3A of continuous output current (I_{OUT}) from a 2.5V to 5.5V input voltage (V_{IN}) range, with excellent load and line regulation. The output voltage (V_{OUT}) can be regulated to as low as 0.6V.

Constant-on-time (COT) control provides fast transient response and eases loop stabilization. Fault protections include cycle-by-cycle current limiting and thermal shutdown.

The MP2193 is ideal for a wide range of applications, including high-performance DSPs, wireless power, portable and mobile devices, and other low-power systems.

The MP2193 requires a minimal number of readily available, standard external components, and is available in an ultra-small WLCSP-6 (0.85mmx1.25mm) package.

FEATURES

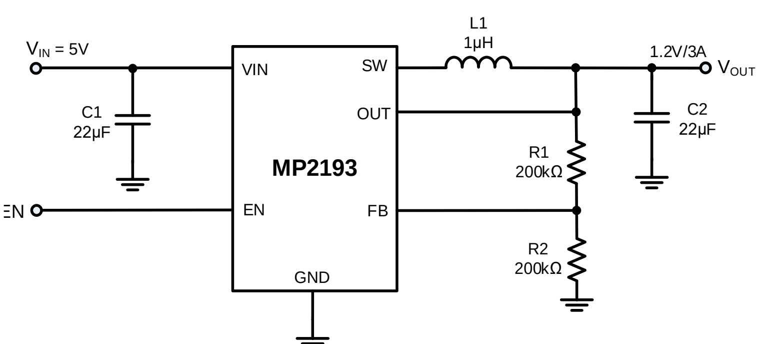
- Low 25µA Quiescent Current (I_Q)
- 1.1MHz Switching Frequency (f_{SW})
- EN for Power Sequencing
- 1% Feedback (FB) Accuracy
- Wide 2.5V to 5.5V Operating Input Voltage (V_{IN}) Range
- Output Voltage (V_{OUT}) Adjustable from 0.6V
- Up to 3A Output Current (I_{OUT})
- 65mΩ and 35mΩ Internal Power MOSFETs
- 100% Duty Cycle
- Output Discharge
- V_{OUT} Over-Voltage Protection (OVP)
- Short-Circuit Protection (SCP) with Hiccup Mode
- Available in a WLCSP-6 (0.85mmx1.25mm) Package

MPL Optimized Performance with MPS Inductor MPL-AL4020 Series

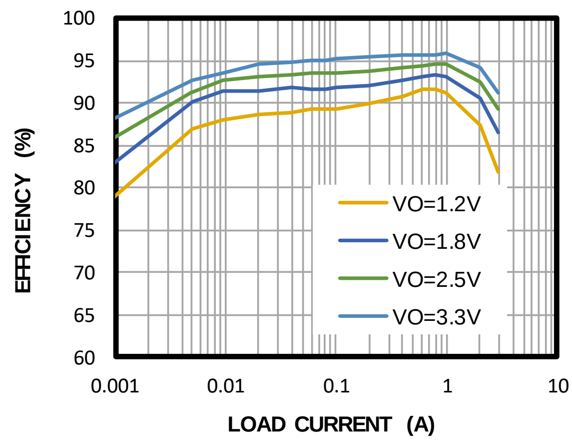
APPLICATIONS

- Solid State Drives (SSDs)
- Portable Instruments
- Battery-Powered Devices
- Multi-Function Printers

TYPICAL APPLICATION



Efficiency vs. Output Current
V_{IN} = 5V, L = 1µH, DCR = 10.1mΩ



ORDERING INFORMATION

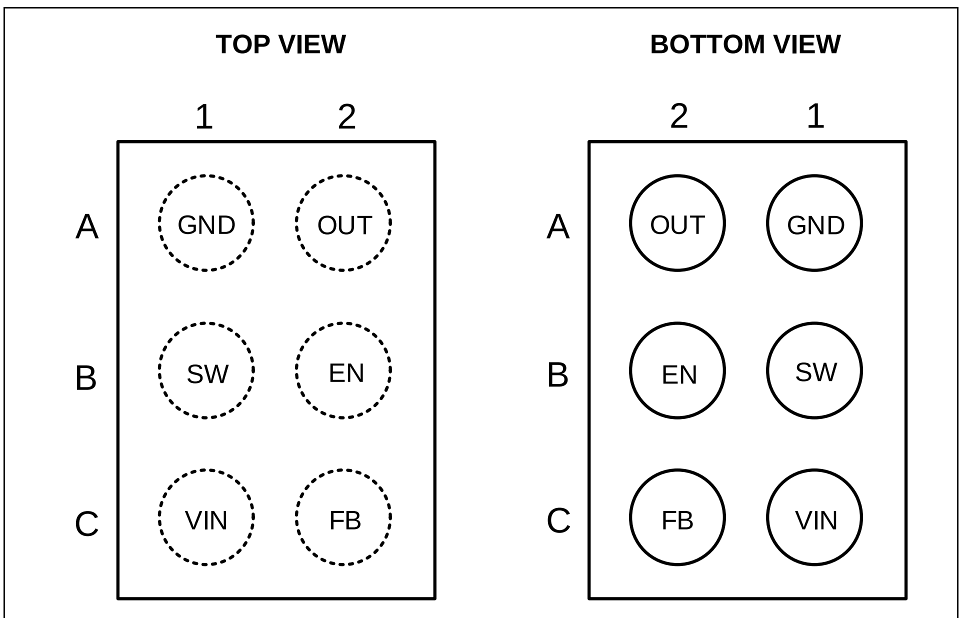
Part Number*	Package	Top Marking	V_{OUT} Range	MSL Rating
MP2193GC	WLCSP-6 (0.85mmx1.25mm)	*See Below*	Adjustable	1

* For Tape & Reel, add suffix -Z (e.g. MP2193GC-Z).

TOP MARKING

KA: Product code of MP2193GC
Y: Year code
LLL: Lot number

PACKAGE REFERENCE



WLCSP-6 (0.85mmx1.25mm)

PIN FUNCTIONS

Pin #	Name	Description
A1	GND	**Power ground.**
A2	OUT	**Output sense.** The OUT pin is the voltage power rail and input sense pin for the output voltage (V_{OUT}). Output capacitors (C_{OUT}) are required to reduce the V_{OUT} ripple.
B1	SW	**Output switching node.** The SW pin is the internal, high-side (HS) P-channel MOSFET's drain. Connect the inductor to SW to complete the converter.
B2	EN	**On/off control.**
C1	VIN	**Supply voltage.** The MP2193 operates from a 2.5V to 5.5V unregulated input voltage (V_{IN}). A decoupling capacitor is required to prevent large voltage spikes at the input.
C2	FB	**Feedback (FB).** Connect an external resistor divider from the output to GND, tapped to the FB pin, to set V_{OUT}.

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) 6.5V
V_{SW} .... -0.3V (-5V for <10ns) to
…………………………….+6.5V (10V for <10ns)
All other pins ....-0.3V to +6.5V
Junction temperature ....150°C
Lead temperature ....260°C
Continuous power dissipation (T_A = 25°C) (2) (4)
.... 1.39W
Storage temperature .... -65°C to +150°C

ESD Ratings

Human body model (HBM) .... ±2000V
Charged device model (CDM)……………………
……………………………………+1000V, -1500V

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) ....2.5V to 5.5V
Operating junction temp (T_J) .... -40°C to +125°C

Thermal Resistance	θ_{JA}	$\theta_{JC(TOP)}$	
EVL2193-C-00A (4)	90	30	°C/W
WLCSP-6 (5)	141	2	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, which may cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on the EVL2193-C-00A evaluation board, a 2-layer PCB.
5) Measured on JESD51-7, a 4-layer PCB. The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values are calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

ELECTRICAL CHARACTERISTICS

V_{IN} = 3.6V, T_J = -40°C to +125°C [6], typical value is tested at T_J = 25°C, over-temperature limit is guaranteed by characterization, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input voltage (V_{IN}) range			2.5		5.5	V
Under-voltage lockout (UVLO) rising threshold				2.3	2.45	V
UVLO hysteresis threshold				135		mV
Feedback (FB) voltage	V_{FB}	T_J = 25°C, 2.5V ≤ V_{IN} ≤ 5.5V, I_{OUT} = 1.5A	594	600	606	mV
		T_J = -40°C to +125°C, I_{OUT} = 1.5A	591	600	609	
FB current	I_{FB}	V_{FB} = 0.63V		50	100	nA
P-channel MOSFET on resistance	$R_{DS(ON)\_P}$	V_{IN} = 5V		65		mΩ
N-channel MOSFET on resistance	$R_{DS(ON)\_N}$	V_{IN} = 5V		35		mΩ
Switch leakage		V_{EN} = 0V, V_{IN} = 6V, V_{SW} = 0V and 6V, T_J = 25°C		0	1	µA
P-channel MOSFET peak current limit			4		6	A
N-channel MOSFET valley current limit				3.5		A
Zero-current detection (ZCD)				50		mA
On time	t_{ON}	V_{IN} = 5V, V_{OUT} = 1.2V		220		ns
		V_{IN} = 3.6V, V_{OUT} = 1.2V		300		
Switching frequency	f_{SW}	V_{OUT} = 1.2V, I_{OUT} = 0.5A		1100		kHz
Minimum off time	$t_{MIN-OFF}$			100		ns
Minimum on time [7]	t_{MIN-ON}			60		ns
Soft-start time	t_{SS-ON}	V_{OUT} rising from 10% to 90%		0.6		ms
EN turn-on delay		EN on to SW active		150		µs
EN input logic low voltage					0.4	V
EN input logic high voltage			1.2			V
Output discharge resistor	R_{DIS}	V_{EN} = 0V, V_{OUT} = 1.2V		200		Ω
EN input current		V_{EN} = 2V		1.2		µA
		V_{EN} = 0V		0		µA
Shutdown supply current shutdown		V_{EN} = 0V, T_J = 25°C		0	1	µA
Quiescent supply current, adjustable version		V_{EN} = 2V, V_{FB} = 0.63V, V_{IN} = 5V, T_J = 25°C		25	30	µA

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 3.6V, T_J = -40°C to +125°C (6), typical value is tested at T_J = 25°C, over-temperature limit is guaranteed by characterization, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Output over-voltage (OV) threshold	V_{OVP}		112	117	122	% of V_{FB}
V_{OUT} over-voltage protection (OVP) hysteresis	V_{OVP_HYS}			13		% of V_{FB}
OVP delay				12		µs
Low-side (LS) current		Current flowing from SW to GND		1.5		A
Absolute V_{IN} OVP		After V_{OUT} OVP is enabled		6.2		V
Absolute V_{IN} OVP hysteresis				400		mV
Thermal shutdown (7)				160		°C
Thermal hysteresis (7)				30		°C

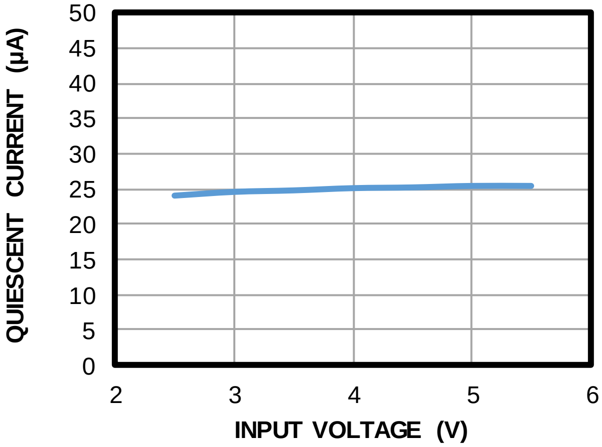
Notes:

6) Not tested in production. Guaranteed by over-temperature correlation.
7) Guaranteed by engineering sample characterization.

TYPICAL CHARACTERISTICS

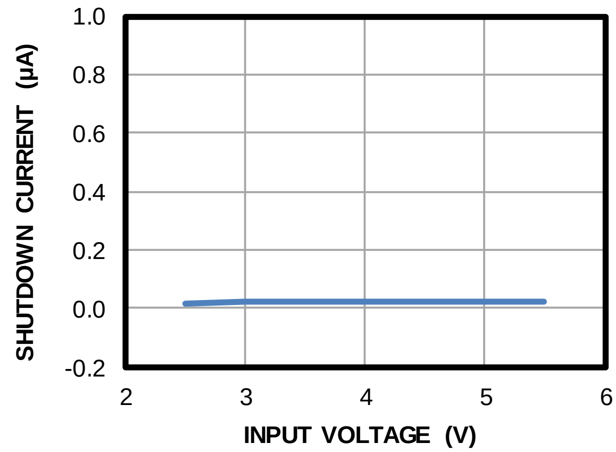
V_{IN} = 3.6V, V_{OUT} = 1.2V, L = 1µH, C_{OUT} = 22µF, T_A = 25°C, unless otherwise noted.

Quiescent Current vs. Input Voltage



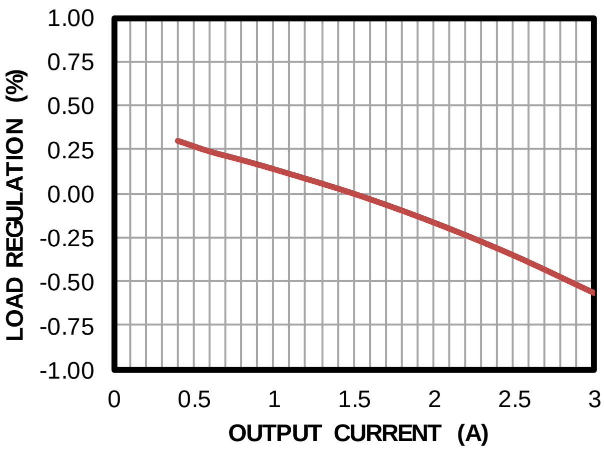
Shutdown Current vs. Input Voltage

V_{EN} = 0V

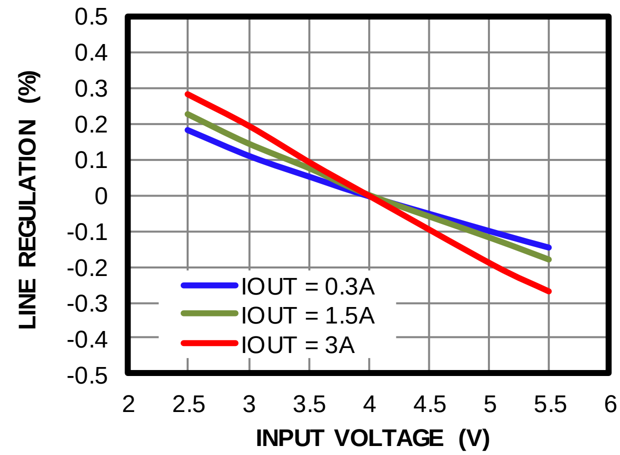


Load Regulation

V_{OUT} = 1.2V

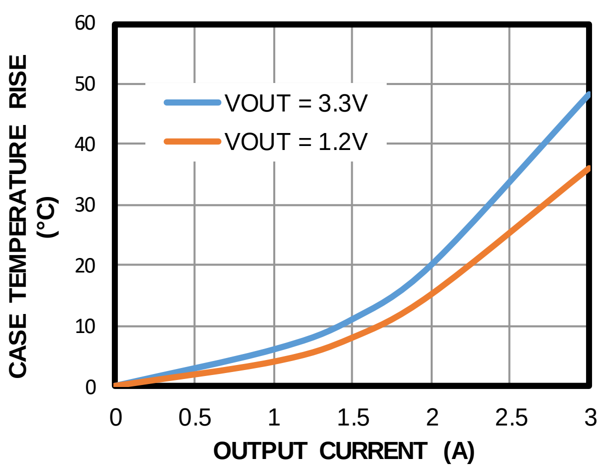


Line Regulation



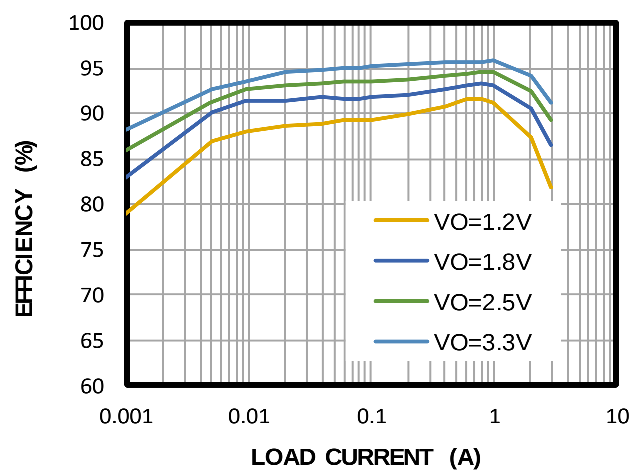
Case Temperature Rise vs. Output Current

V_{IN} = 5V



Efficiency vs. Output Current

V_{IN} = 5V, L = 1µH, DCR = 10.1mΩ

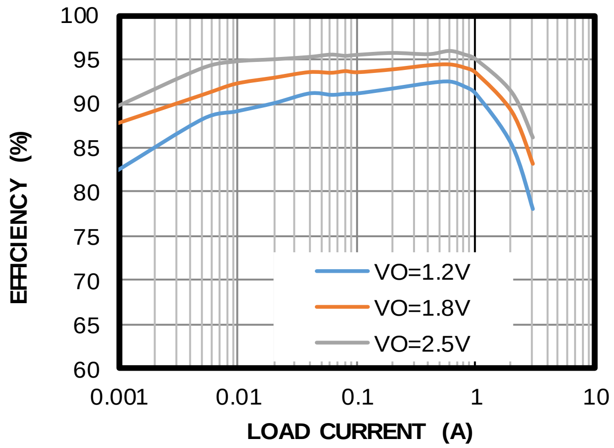


TYPICAL PERFORMANCE CHARACTERISTICS

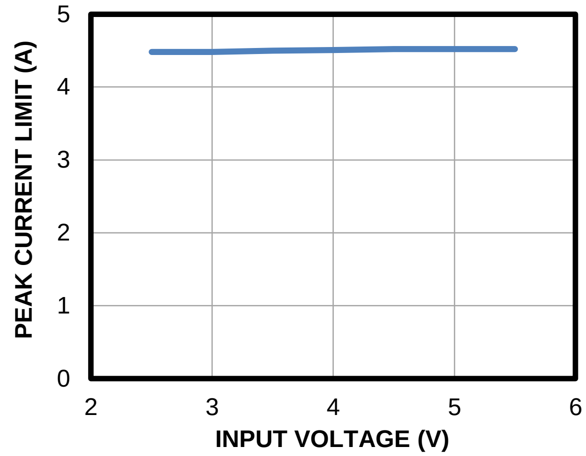
V_{IN} = 5V, V_{OUT} = 1.2V, L = 1μH, C_{OUT} = 22μF, T_A = 25°C, unless otherwise noted.

Efficiency vs. Output Current

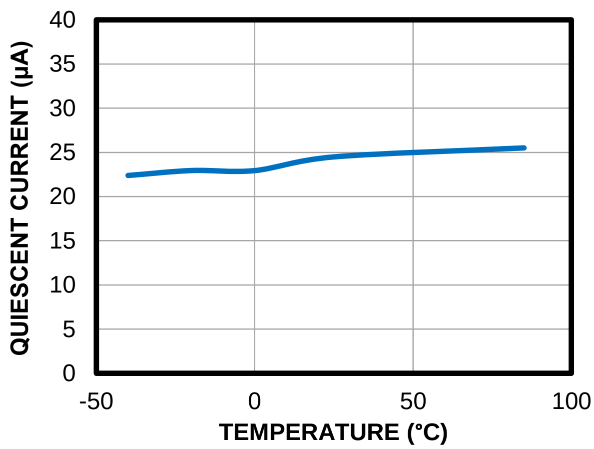
V_{IN} = 3.6V, L = 1μH, DCR = 10.1mΩ



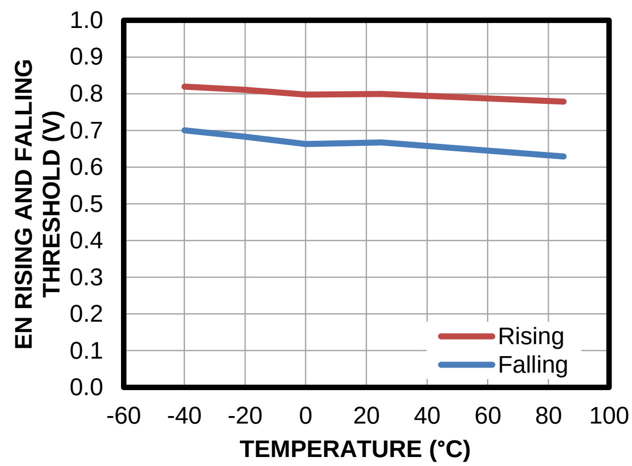
Peak Current Limit vs. Input Voltage



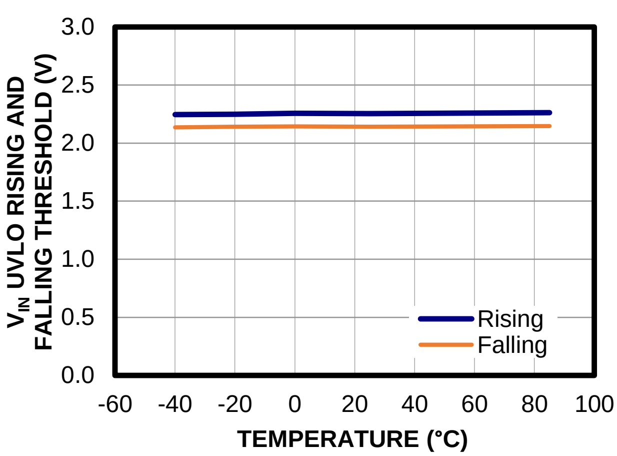
Quiescent Current vs. Temperature



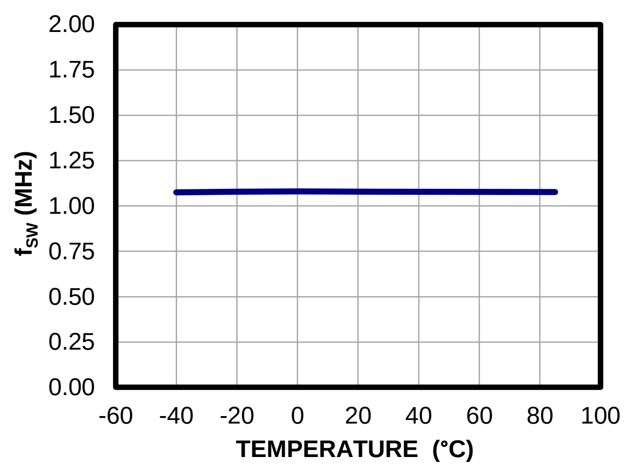
EN Rising and Falling Threshold vs. Temperature



V_{IN} UVLO Rising and Falling Threshold vs. Temperature



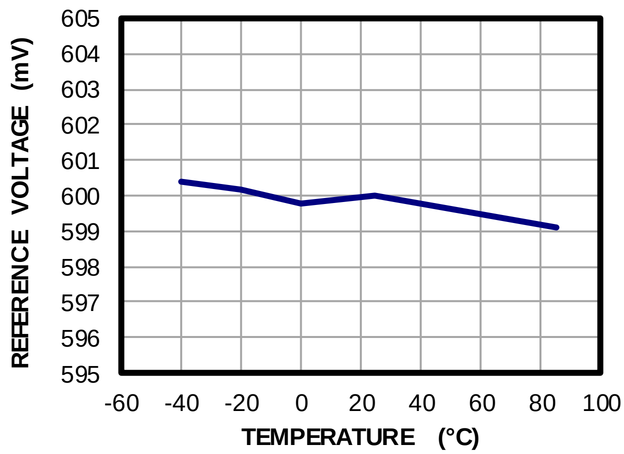
Switching Frequency vs. Temperature



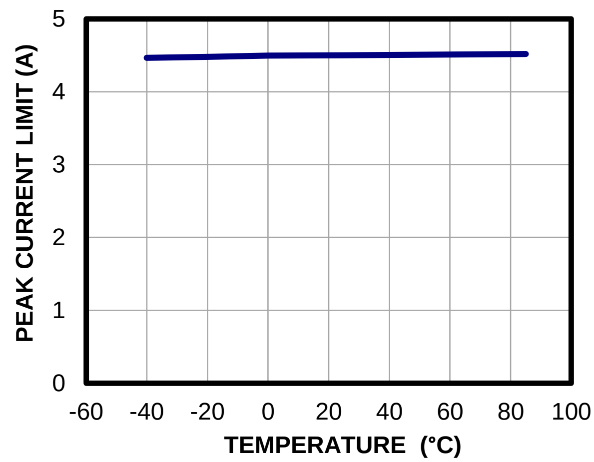
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1.2V, L = 1μH, C_{OUT} = 22μF, T_A = 25°C, unless otherwise noted.

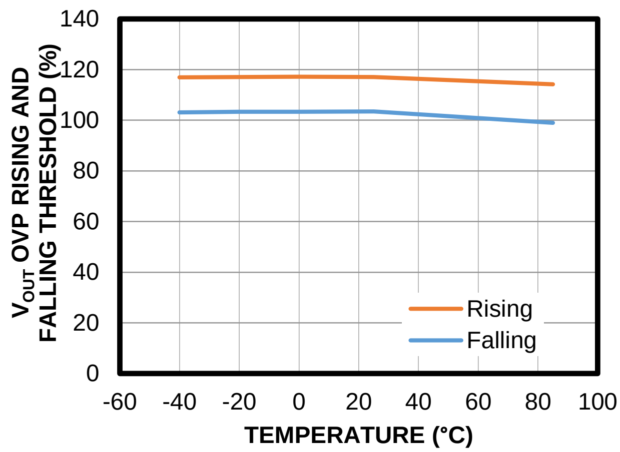
Reference Voltage vs. Temperature



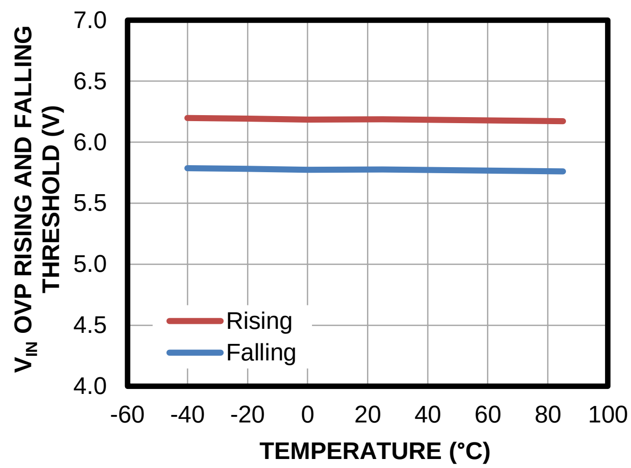
Peak Current Limit vs. Temperature



V_{OUT} OVP Rising and Falling Threshold vs. Temperature

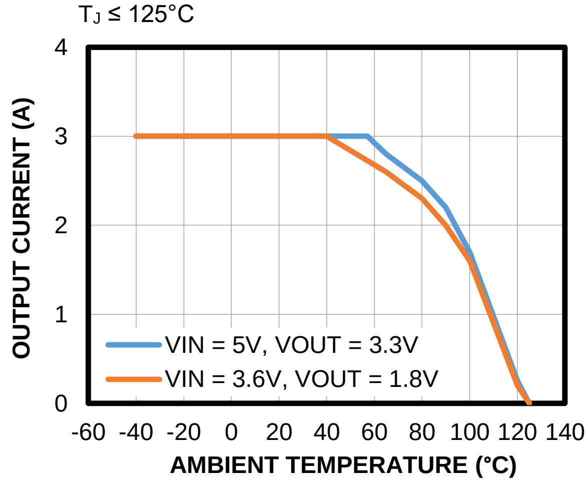


V_{IN} OVP Rising and Falling Threshold vs. Temperature



Output Current Derating vs. Ambient Temperature

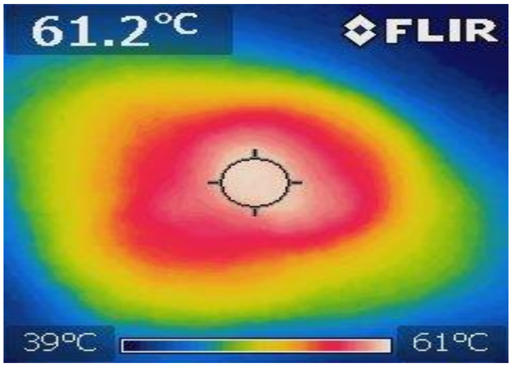
$T_J \leq 125°C$



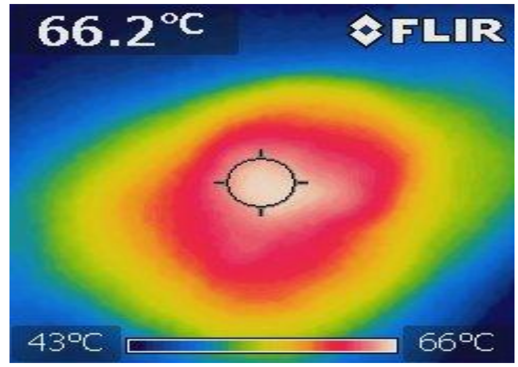
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1.2V, L = 1μH, C_{OUT} = 22μF, T_A = 25°C, unless otherwise noted.

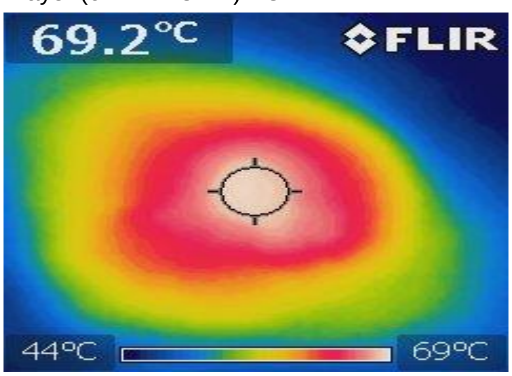
Thermal Image
V_{IN} = 5V, V_{OUT} = 1.2V, I_{OUT} = 3A,
2-layer (64mmx48mm) PCB



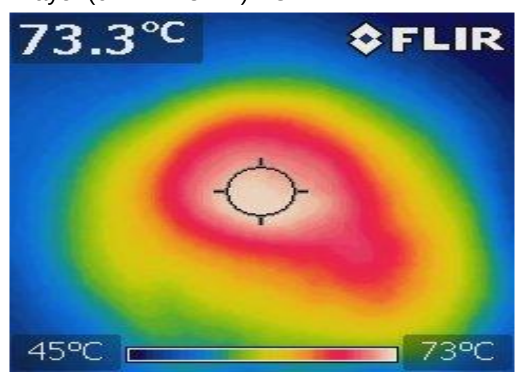
Thermal Image
V_{IN} = 5V, V_{OUT} = 1.8V, I_{OUT} = 3A,
2-layer (64mmx48mm) PCB



Thermal Image
V_{IN} = 5V, V_{OUT} = 2.5V, I_{OUT} = 3A,
2-layer (64mmx48mm) PCB



Thermal Image
V_{IN} = 5V, V_{OUT} = 3.3V, I_{OUT} = 3A,
2-layer (64mmx48mm) PCB

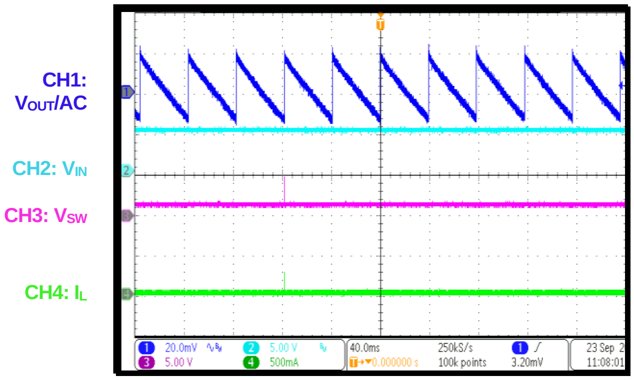


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1.2V, L = 1µH, C_{OUT} = 22µF, T_A = 25°C, unless otherwise noted.

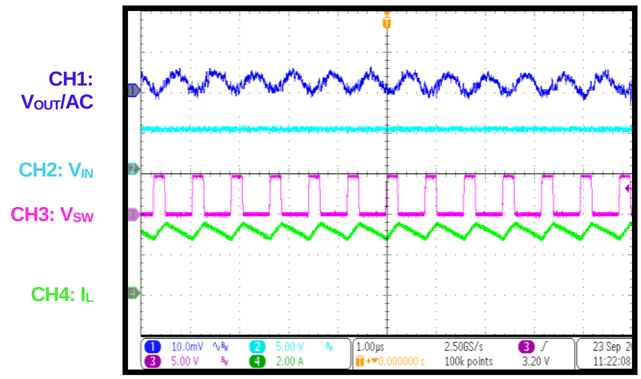
Steady State

I_{OUT} = 0A



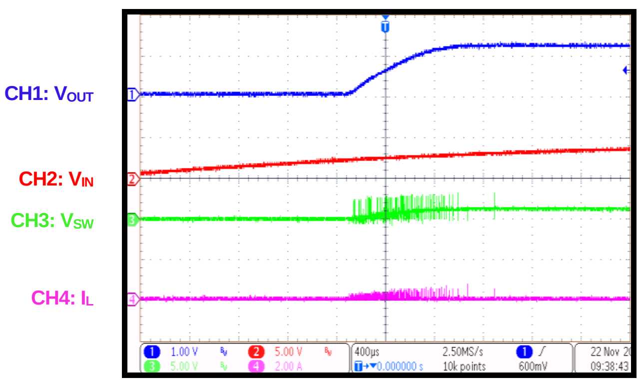
Steady State

I_{OUT} = 3A



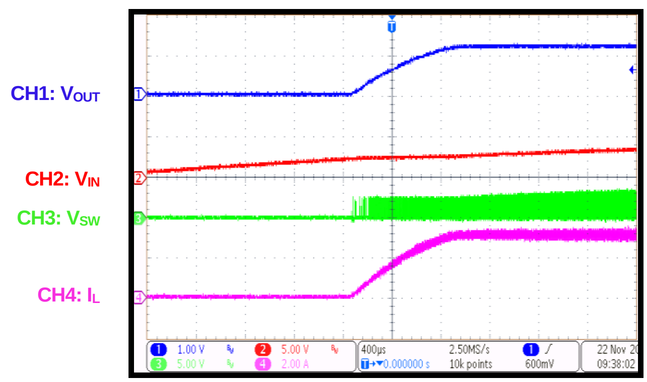
Start-Up through VIN

I_{OUT} = 0A



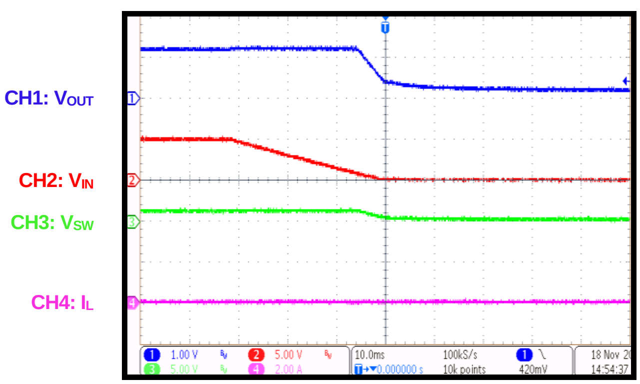
Start-Up through VIN

I_{OUT} = 3A



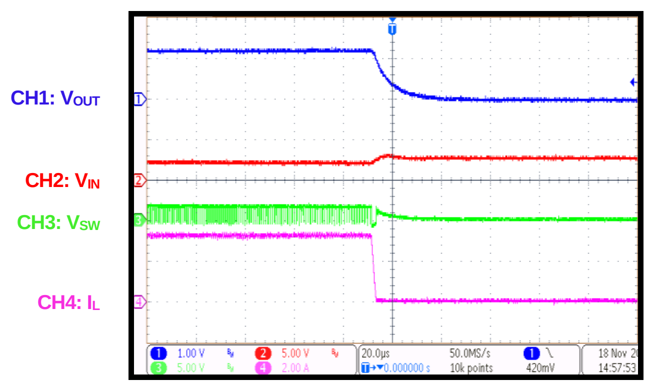
Shutdown through VIN

I_{OUT} = 0A



Shutdown through VIN

I_{OUT} = 3A

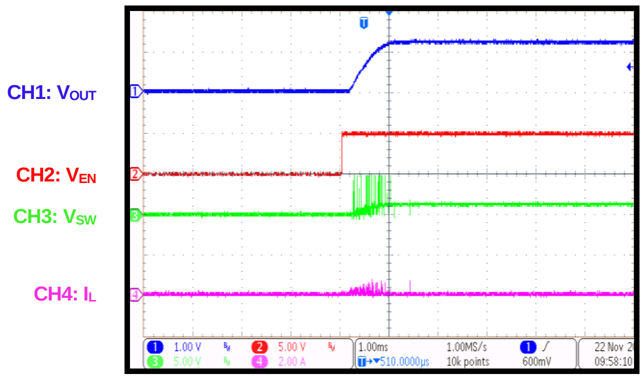


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1.2V, L = 1µH, C_{OUT} = 22µF, T_A = 25°C, unless otherwise noted.

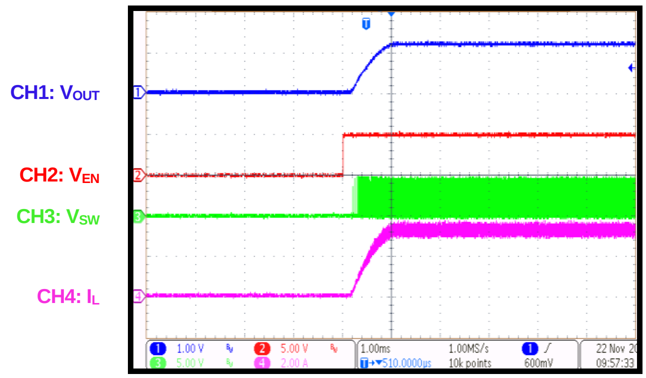
Start-Up through EN

I_{OUT} = 0A



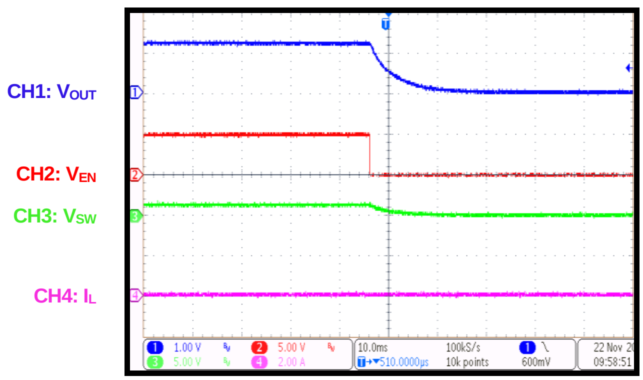
Start-Up through EN

I_{OUT} = 3A



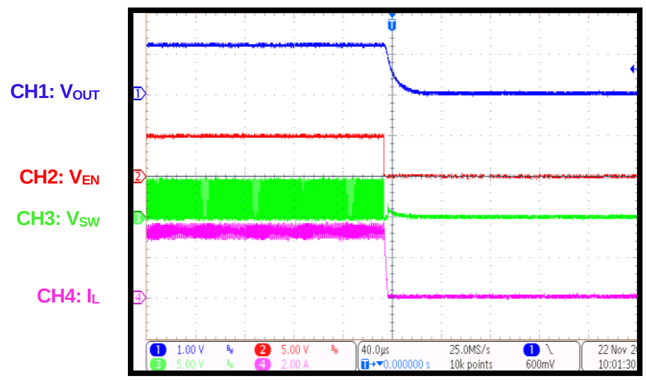
Shutdown through EN

I_{OUT} = 0A



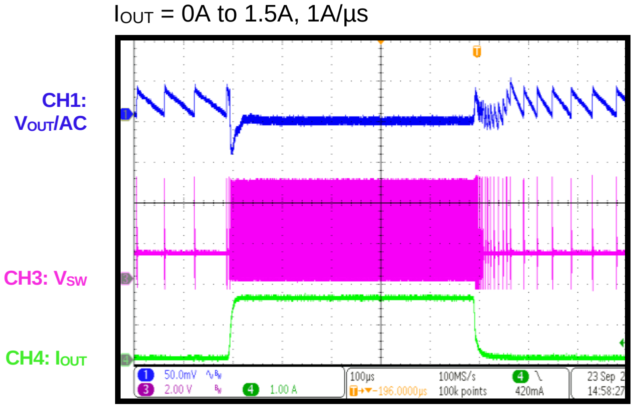
Shutdown through EN

I_{OUT} = 3A



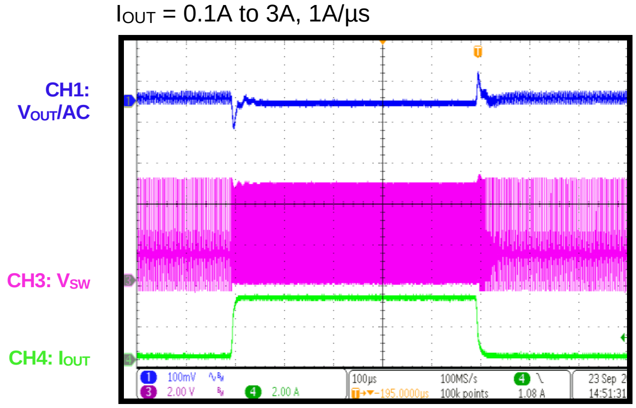
Load Transient

I_{OUT} = 0A to 1.5A, 1A/µs



Load Transient

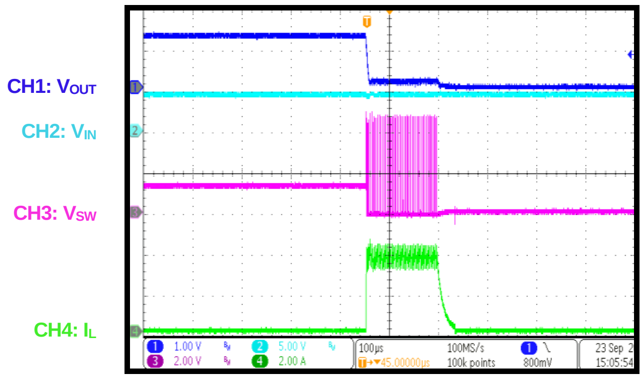
I_{OUT} = 0.1A to 3A, 1A/µs



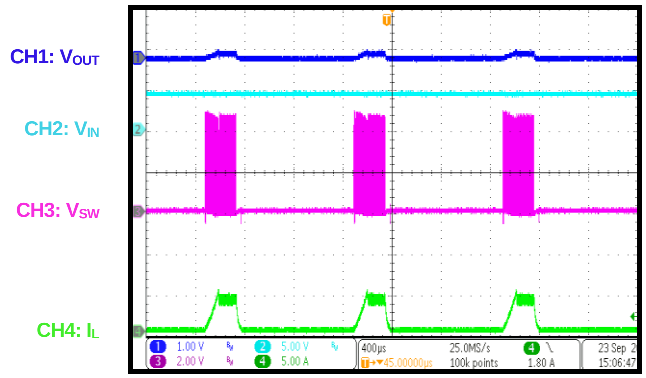
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1.2V, L = 1µH, C_{OUT} = 22µF, T_A = 25°C, unless otherwise noted.

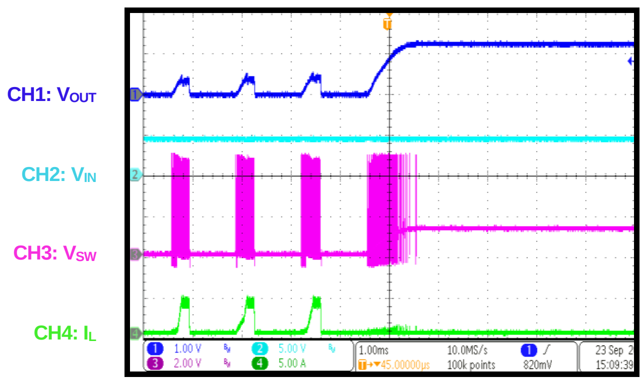
Short-Circuit Entry



Short-Circuit State



Short-Circuit Recovery



FUNCTIONAL BLOCK DIAGRAM

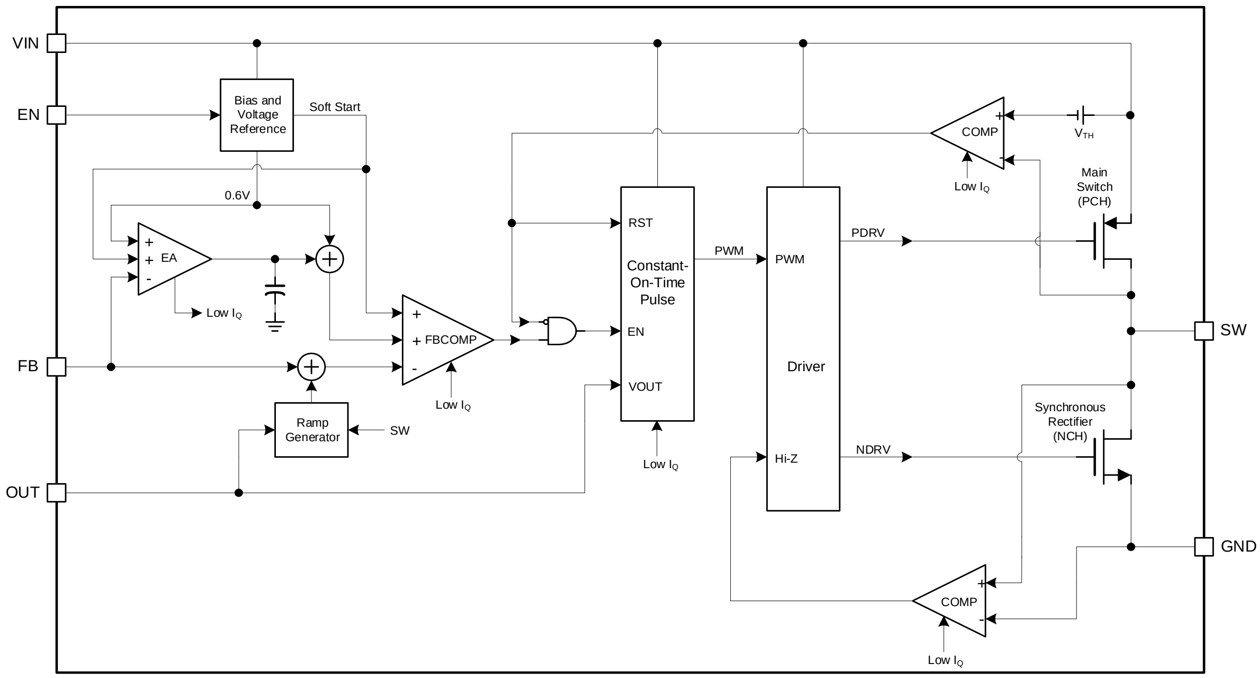


Figure 1: Functional Block Diagram

OPERATION

The MP2193 uses constant-on-time (COT) control with input voltage (V_{IN}) feed-forward to stabilize the switching frequency (f_{SW}) across the entire V_{IN} range. The MP2193 achieves 3A of continuous output current (I_{OUT}) from a 2.5V to 5.5V V_{IN} range, with excellent load and line regulation. The output voltage (V_{OUT}) can be regulated to as low as 0.6V.

Constant-On-Time (COT) Control

When compared to fixed-frequency pulse-width modulation (PWM) control, COT control offers a simpler control loop and faster transient response. By using V_{IN} feed-forward, the MP2193 maintains a fairly constant f_{SW} across the entire V_{IN} and V_{OUT} ranges. The switching pulse on time (t_{ON}) can be estimated using Equation (1):

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \times 0.91\mu s \quad (1)$$

To prevent inductor current (I_L) runaway during the load transient, the MP2193 has a fixed minimum off time of 100ns.

Sleep Mode

The MP2193 offers sleep mode to achieve high efficiency under extremely light loads. In sleep mode, most of the circuit blocks are turned off except for the error amplifier (EA) and PWM comparator. This reduces the operating current to a minimal value (see Figure 2).

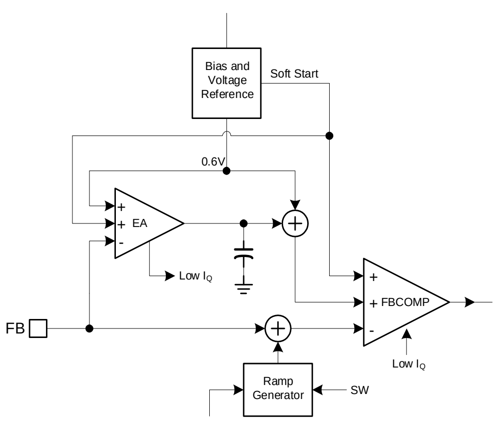


Figure 2: Operation Blocks in Sleep Mode

When the load becomes lighter, the V_{OUT} ripple (ΔV_{OUT}) increases, which then drives the EA output (EAO) lower. When the EAO reaches the internal low threshold, it is clamped at that level, and the MP2193 enters sleep mode.

During sleep mode, the feedback (FB) voltage (V_{FB}) valley is regulated to the internal reference voltage (V_{REF}). Therefore, the average V_{OUT} in sleep mode slightly exceeds V_{OUT} during discontinuous conduction mode (DCM) or continuous conduction mode (CCM). The on-time pulse in sleep mode is longer than the on-time pulse in DCM or CCM. Figure 3 shows the relationship between the average V_{FB} and internal V_{REF} in sleep mode.

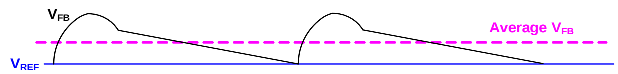


Figure 3: Average V_{FB} in Sleep Mode

When the MP2193 is in sleep mode, the average V_{OUT} exceeds internal V_{REF}. The EAO remains low and is clamped in sleep mode. When the load increases, the PWM switching period decreases to regulate V_{OUT}. ΔV_{OUT} drops relative to the PWM switching period. Once the EAO exceeds the internal low threshold, the MP2193 exits sleep mode and enters either DCM or CCM, depending on the load. In DCM or CCM, the EA regulates the average V_{OUT} to internal V_{REF} (see Figure 4).

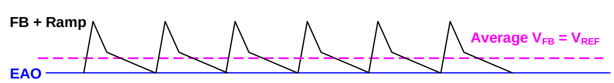


Figure 4: DCM Control

Due to the EA's clamping response time, there is always a loading hysteresis when entering or exiting sleep mode.

Advanced Asynchronous Modulation (AAM) Mode during Light-Load Operation

The MP2193 uses advanced asynchronous modulation (AAM) power-save mode and a zero-current detection (ZCD) circuit for light-load operation.

The MP2193 uses AAM power-save mode for light loads (see Figure 5 on page 15). The AAM current (I_{AAM}) is set internally. The SW on-pulse time is determined by the on-time generator and AAM comparator.

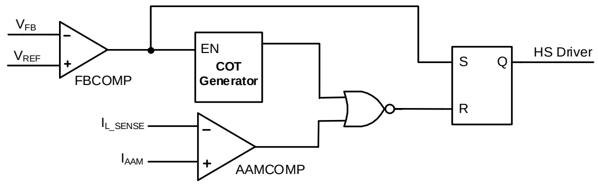
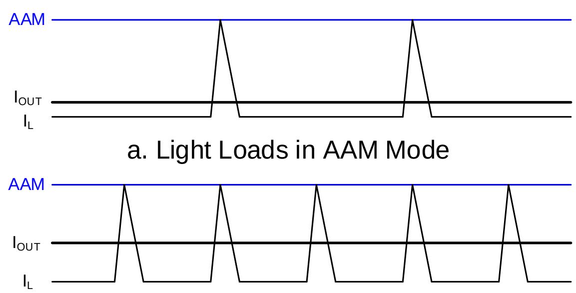


Figure 5: Simplified AAM Control Logic

Under light-load conditions, the SW on-time pulse is the longer pulse. If the AAM comparator pulse is longer than the on-time generator, then the operation mode is controlled by the AAM comparator (see Figure 6).

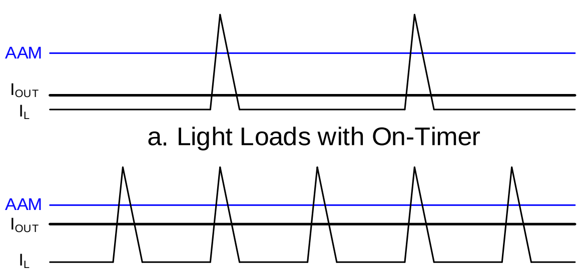


a. Light Loads in AAM Mode

b. Increasing Load in AAM Mode

Figure 6: The AAM Comparator Controls t_{ON}

If the AAM comparator pulse is shorter than the on-time generator, then the operation mode is controlled by the on-time generator (see Figure 7).



a. Light Loads with On-Timer

b. Increasing Loads with On-Timer

Figure 7: The On-Timer Controls t_{ON}

Figure 8 shows the when the AAM threshold decreases, t_{ON} increases gradually.

For CCM, I_{OUT} must exceed at least 50% of the AAM threshold. The AAM threshold is typically below I_L during normal duty cycles.

The MP2193 uses ZCD to determine whether I_L has started reversing. When I_L reaches the ZCD threshold, the low-side MOSFET (LS-FET) turns off.

AAM mode and the ZCD circuit enables the MP2193 to work in DCM under light loads, even if V_{OUT} is close to V_{IN}.

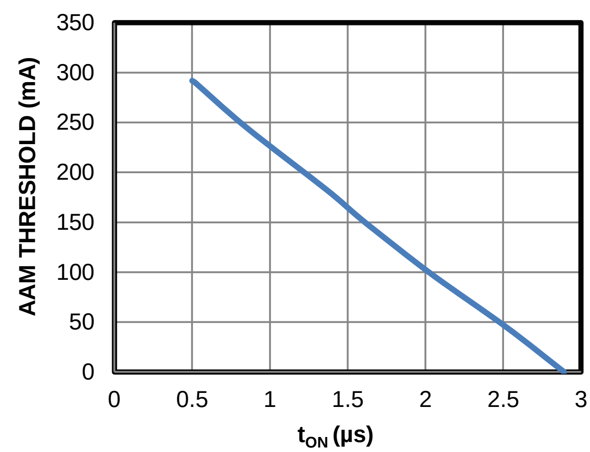


Figure 8: AAM Threshold Decreases as t_{ON} Increases

Enable (EN)

If V_{IN} exceeds the under-voltage lockout (UVLO) threshold (typically 2.3V), the MP2193 can be enabled by pulling EN above 1.2V. Leave EN floating or pull EN down to ground to disable the MP2193. There is an internal 1MΩ resistor connected from EN to ground.

When the device is disabled, the part enters output discharge mode automatically. The device's internal discharge MOSFET provides a resistive discharge path for the output capacitor (C_{OUT}).

Soft Start (SS)

The MP2193 has built-in soft start (SS) that ramps up V_{OUT} at a controlled slew rate to avoid overshooting during start-up. The soft-start time (t_{SS-ON}) is typically about 0.6ms.

Current Limit

The MP2193 has a typical 6A (max) high-side MOSFET (HS-FET) current limit (I_{LIMIT}). When the HS-FET reaches its I_{LIMIT}, the MP2193 remains in hiccup mode until the current drops. This prevents I_L from continuing to rise and damaging components.

Short Circuit and Recovery

If the MP2193 reaches its I_{LIMIT}, it enters short-circuit protection (SCP) and then attempts to recover with hiccup mode. The MP2193 disables the output power stage, discharges the SS capacitor (C_{SS}), and attempts to SS again automatically. If the short-circuit condition remains after SS is complete, the MP2193 repeats this cycle until the short circuit is removed and the output rises back to the regulation level.

V_{OUT} Over-Voltage Protection (OVP)

The MP2193 monitors V_{FB} to detect over-voltage (OV) conditions. If V_{FB} exceeds 117% of the target voltage, then the controller enters a dynamic regulation period. During this period, the LS-FET remains on until the low-side (LS) current drops to -1.5A. This discharges the output to keep it within the normal range. If the OV condition still remains, the LS-FET turns on again after a 1μs time delay. Once V_{FB} drops below 104% of V_{REF}, the MP2193 exits this regulation period. If the dynamic regulation cannot limit the increasing V_{OUT} and the input exceeds the 6.2V OVP threshold, then the MP2193 stops switching until V_{IN} drops below 5.7V. Once V_{IN} drops below 5.7V, the MP2193 resumes normal operation.

APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider sets V_{OUT} (see the Typical Application Circuit section on page 19). Select a FB resistor (R1) that reduces V_{OUT} leakage current. It is recommended for R1 to be between 100kΩ and 200kΩ. There is no strict requirement for the FB resistor. Select R1 to exceed 10kΩ. R2 can then be calculated using Equation (2):

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.6} - 1} \quad (2)$$

Figure 9 shows the FB circuit.

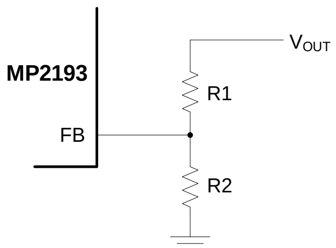


Figure 9: FB Network

Table 1 lists the recommended resistor values for common output voltages.

Table1: Resistor Values for Common Output Voltages

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)
1	200 (1%)	300 (1%)
1.2	200 (1%)	200 (1%)
1.8	200 (1%)	100 (1%)
2.5	200 (1%)	63.2 (1%)
3.3	200 (1%)	44.2 (1%)

Selecting the Inductor

MPL **Optimized Performance with MPS Inductor MPL-AL4020 Series**

Most applications work best with a 1µH to 2.2µH inductor. Select an inductor with a DC resistance below 50mΩ to optimize efficiency.

A high-frequency, switch-mode power supply with a magnetic device has strong EMI. Do not use unshielded power inductors. Metal alloy or multiplayer chip power inductors are ideal shielded inductors because they can effectively reduce EMI.

Table 2 lists some recommended power inductors.

Table 2: Power Inductor Selection

Part Number	Inductance	Manufacturer
MPL-AL4020-1R0	1µH	MPS
74437324010	1µH	Wurth

For most designs, the inductance (L_1) can be estimated using Equation (3):

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}} \quad (3)$$

Where ΔI_L is the inductor ripple current.

Choose I_L to be approximately 30% of the maximum load current. The maximum inductor peak current ($I_{L(MAX)}$) can be calculated using Equation (4):

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (4)$$

Selecting the Input Capacitor

The step-down converter has a discontinuous input current (I_{IN}), and requires a capacitor to supply AC current to the converter while maintaining the DC V_{IN}. Use low-ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, a 22µF capacitor is sufficient. Higher output voltages may require a 44µF capacitor to increase system stability.

The input capacitor (C_{IN}) requires an adequate ripple current rating since it absorbs the input switching current. The C_{IN} RMS current (I_{C1}) can be estimated using Equation (5):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (5)$$

The worst-case scenario occurs at V_{IN} = 2 x V_{OUT}, which can be calculated using Equation (6):

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (6)$$

For simplification, choose C_{IN} with an RMS current rating that exceeds half of the maximum load current.

C_{IN} can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality, 0.1μF ceramic capacitor as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at the input. The V_{IN} ripple caused by the capacitance (ΔV_{IN}) can be estimated using Equation (7):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (7)$$

Selecting the Output Capacitor

C_{OUT} (C2) stabilizes DC V_{OUT}. Low-ESR ceramic capacitors are recommended to limit ΔV_{OUT}. ΔV_{OUT} can be estimated using Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_{SW} \times C2}\right) \quad (8)$$

Where L_1 is the inductance, and R_{ESR} is the C_{OUT} equivalent series resistance (ESR).

When using ceramic capacitors, the capacitance dominates the impedance at f_{SW} and causes the majority of ΔV_{OUT}. For simplification, ΔV_{OUT} can be estimated using Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (9)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at f_{SW}. For simplification, ΔV_{OUT} can be estimated using Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (10)$$

C_{OUT} characteristics also affect the stability of the regulation system.

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. Poor layout design can result in poor line or load regulation and stability issues. For the best results, refer to Figure 10 and follow the guidelines below:

1. Place the high-current paths (GND, VIN, and SW) as close as possible to the device with short, direct, and wide traces.
2. Place C_{IN} as close to VIN and GND as possible.
3. Place the external FB resistors next to the FB pin.
4. Keep the switching node (SW) short, and route it away from the FB network.
5. Keep the V_{OUT} sense line as short as possible, and away from the power inductor (especially the surrounding inductor).

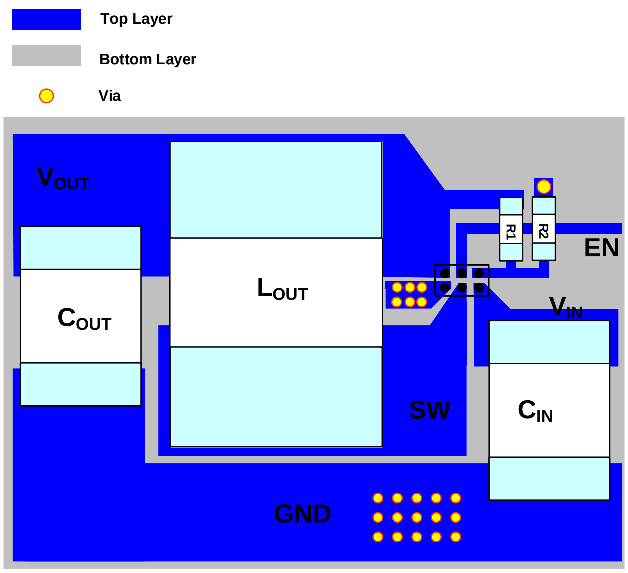


Figure 10: Recommended PCB Layout

TYPICAL APPLICATION CIRCUIT (8)

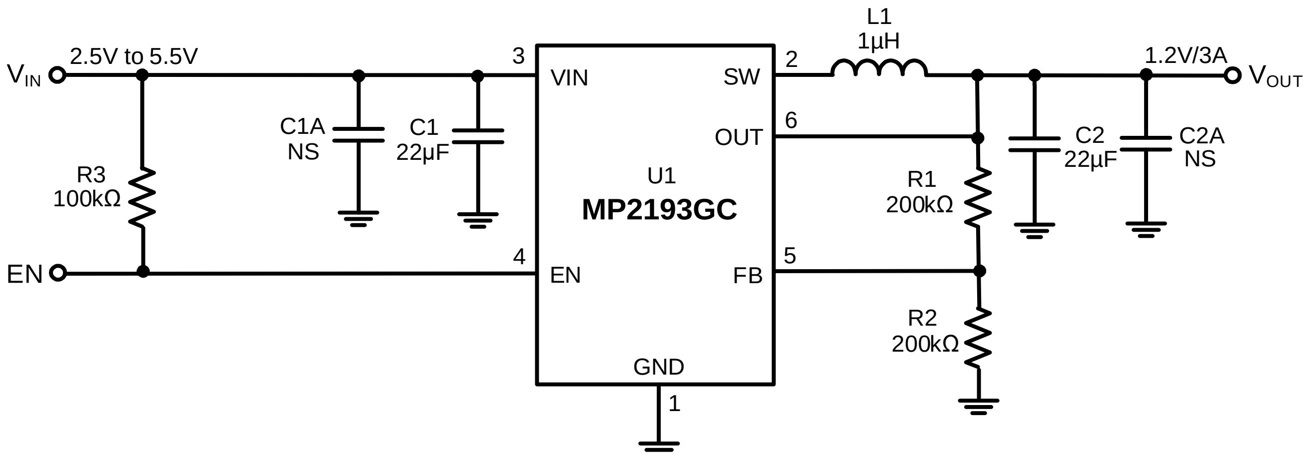


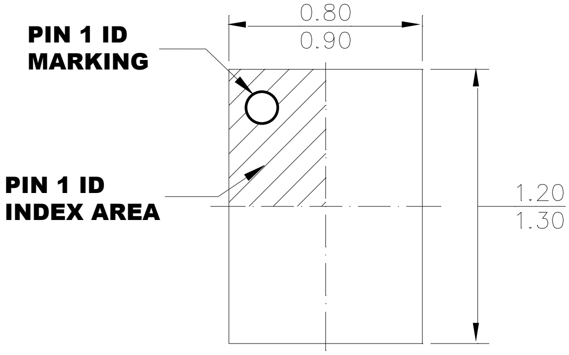
Figure 11: Typical Application Circuit

Note:

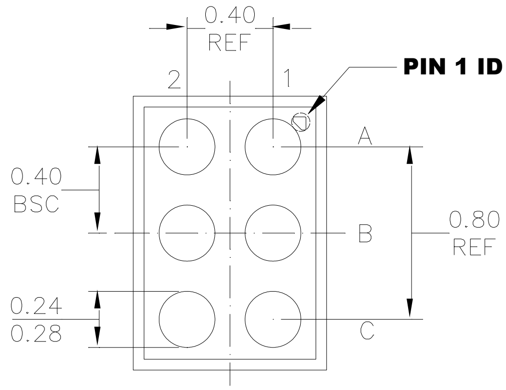
8) For applications where V_{IN} < 3.3V, additional input capacitors may be required.

PACKAGE INFORMATION

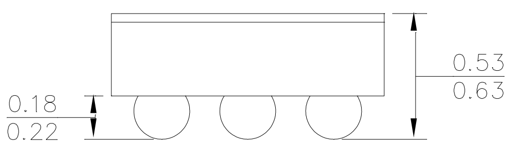
WLCSP-6 (0.85mmx1.25mm)



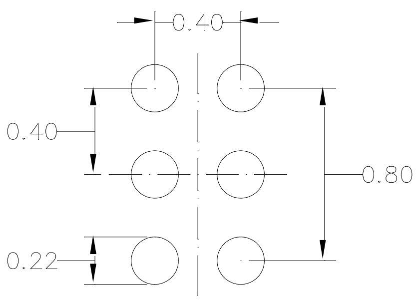
TOP VIEW



BOTTOM VIEW



SIDE VIEW

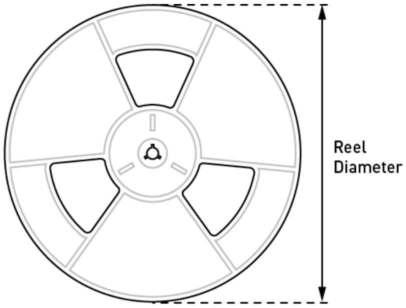


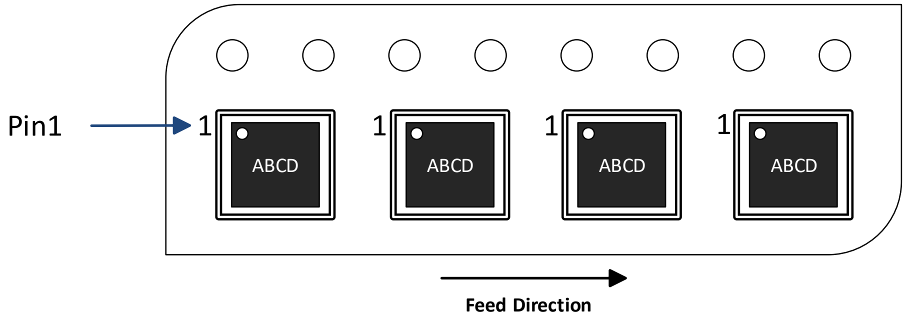
RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) BALL COPLANARITY SHALL BE 0.05 MILLIMETER MAX.
3) JEDEC REFERENCE IS MO-211.
4) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION





Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP2193GC-Z	WLCSP-6 (0.85mmx1.25mm)	3000	N/A	7in	8mm	4mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	5/2/2022	Initial Release	-
1.1	12/7/2023	Updated Figure 10	18