PXIe-5105 Features

2025-04-10

Contents

NI 5105

PXIe, 60 MHz, 8-Channel, 12-Bit PXI Oscilloscope

- 8 channels, simultaneously sampled
- 12-bit vertical resolution
- 60 MS/s real-time sampling rate
- 60 MHz bandwidth and antialias filter
- 16 MB, 128 MB, or 512 MB of memory
- NI-TClk synchronization

Related concepts:

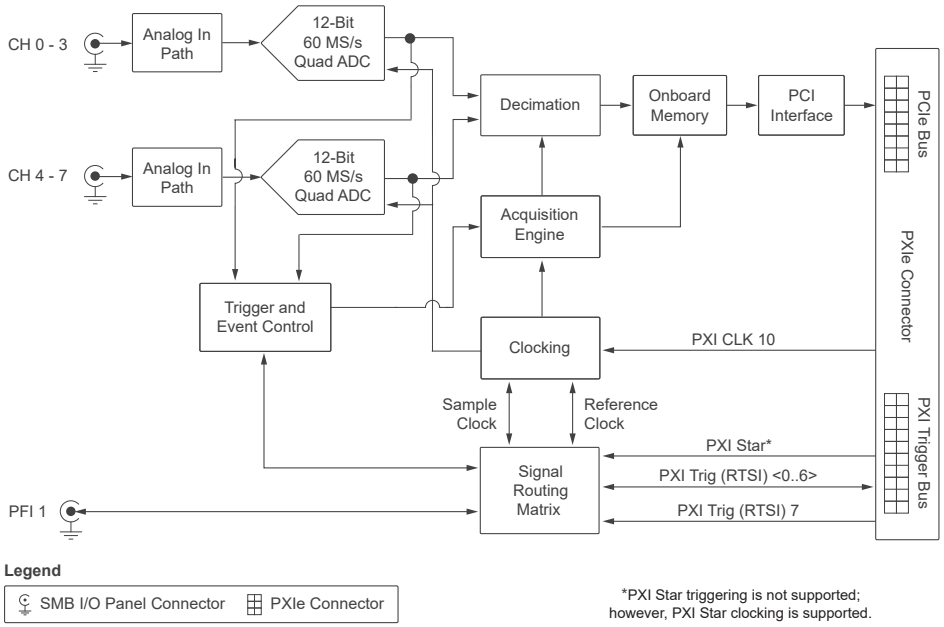
- SMC-Based Device Synchronization

Related information:

- Features Supported by NI-SCOPE Instruments

NI PXIe-5105 Block Diagram

The following figure shows a detailed block diagram of the NI PXIe-5105.

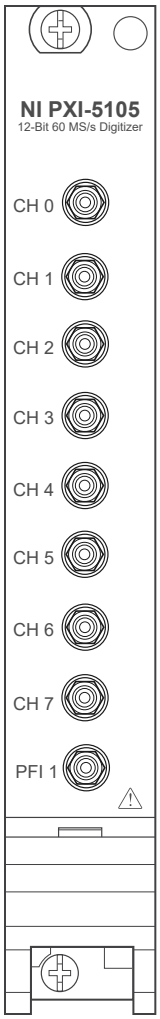


NI PXIe-5105 Front Panel

The following figure shows the front panel of the NI PXIe-5105. Descriptions of the connectors are shown below.

Connectors

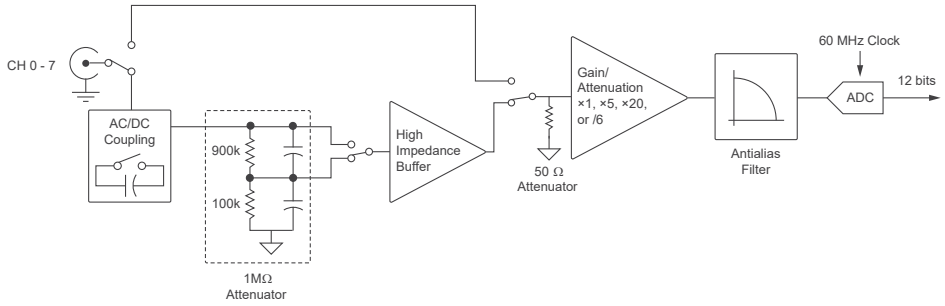
The NI 5105 has the following connectors on the front panel.



Connector	Description	Function
CH 0 through CH 7	Standard SMB connector	Analog input connection; digitizes data and triggers acquisitions
PFI 1	Standard SMB connector	Multipurpose PFI line for trigger in/out, external clock in, reference clock in/out, and timebase out.

NI 5105 Input Signal Conditioning

The NI 5105 has eight independent input channels. Each channel provides the choice of a 50 Ω input impedance path or a 1 MΩ input impedance path, as shown in the following diagram.



The 50 Ω path is optimized for flatness, distortion, dynamic range, and noise because the active circuitry in the signal path is minimized. High-performance communications measurements can take advantage of the large SFDR and 12-bit dynamic range of the 50 Ω path.

The 1 MΩ path provides the traditional oscilloscope input impedance and loading characteristics for numerous general-purpose measurement applications.

Note The ground on the device inputs is connected to the chassis ground.

Related information:

- SFDR

NI 5105 Input Ranges

The following table shows the NI 5105 input ranges for both the 50 Ω and 1 MΩ input paths.

50 Ω Input Path	1 MΩ Input Path
0.05 V_{pk-pk}	0.05 V_{pk-pk}
0.2 V_{pk-pk}	0.2 V_{pk-pk}
1 V_{pk-pk}	1 V_{pk-pk}
6 V_{pk-pk}	6 V_{pk-pk}
—	30 V_{pk-pk}

NI 5105 AC/DC Coupling

You can select AC or DC input coupling for the 1 MΩ input path. Select AC-coupling if the input signal has a DC component that you want to reject, provided that you are not concerned about low-frequency flatness.

The 50 Ω input path is always DC-coupled.

Related information:

- Input Coupling

NI 5105 Input Impedance

You can set the NI 5105 analog input impedance to either 50 Ω or 1 MΩ. The 50 Ω path provides slightly better noise and distortion performance because the high impedance buffer for the 1 MΩ path is bypassed. The 1 MΩ path is required in applications that require minimal loading.

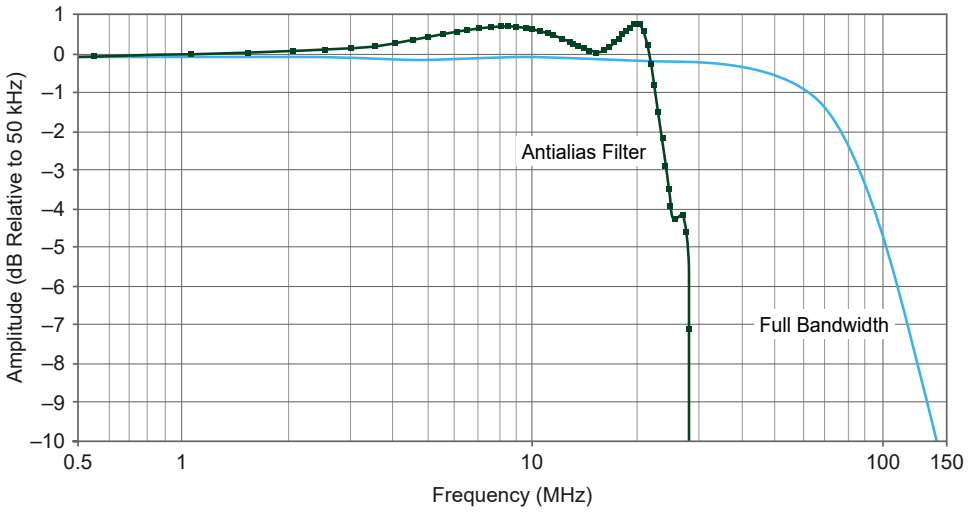
Protection

The 50 Ω inputs of the NI 5105 are protected by an overvoltage protection circuit. If an overvoltage event is large and sudden enough, however, the protection circuits might not have enough time to react before permanent damage occurs. It is therefore important that you observe the specified maximum signal input levels, especially when the inputs are set for 50 Ω.

NI 5105 Antialias Filter

The NI 5105 provides a bandwidth-limiting filter, the 24 MHz antialias filter. The primary purpose of the antialias filter is to minimize aliasing effects caused by signals greater than Nyquist applied to the 60 MS/s ADC. Refer to the hardware specifications document for more information on this filter.

A typical response with the antialias filter is shown in the following figure.

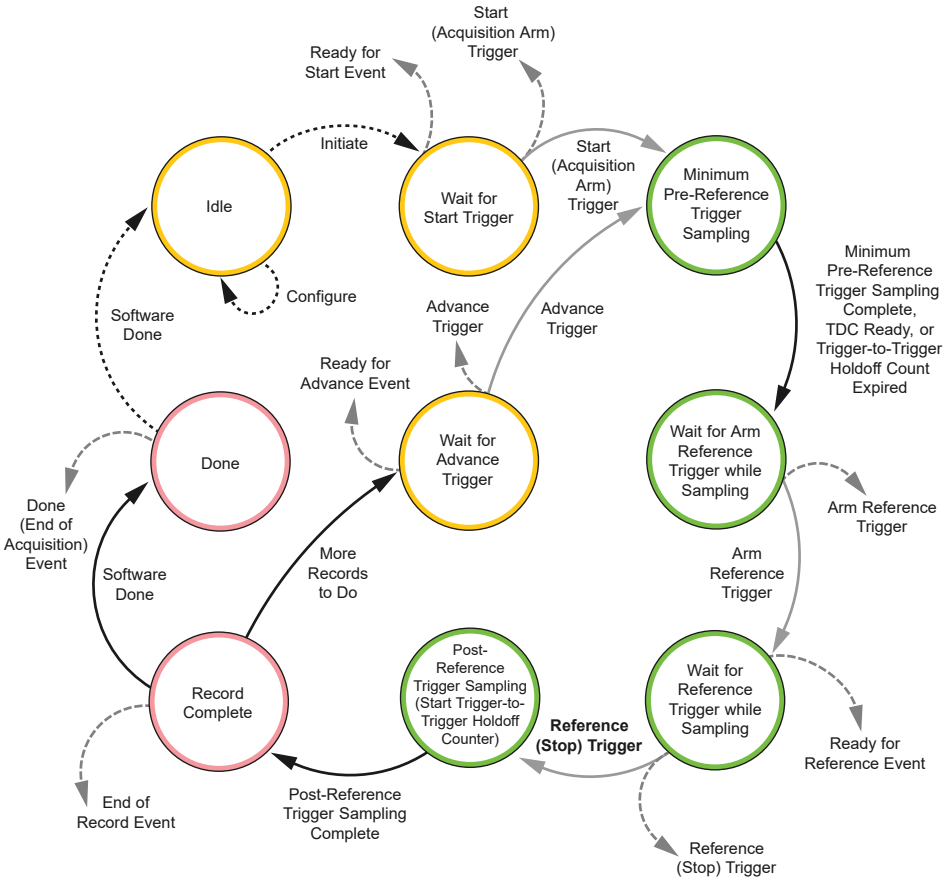


Related information:

- Aliasing
- Nyquist Theorem

SMC-Based Digitizers Acquisition Engine State Diagram

The following figure shows the acquisition engine state diagram for SMC-Based digitizers.



Note The **Reference (Stop) Trigger** is the same as the trigger level input of any traditional benchtop oscilloscope. To configure a digitizer to behave as a traditional benchtop oscilloscope, configure only this trigger using the **niScope Configure Trigger** function.

Arrow Color	Indication
Blue	State transitions always caused by software
Black	State transitions caused by the internal state machine of the device
Red	Output signals
Orange	User-configurable state transitions caused by software or hardware

NI SMC-based digitizers can be in any of the following basic states during the course of operation.

Idle—The module is not sampling a waveform. All the session attributes can be programmed in this state. In this state, the attributes have not necessarily been applied to hardware yet, so the hardware configuration of the module may not match the session attribute values. Also, the module remains configured as it was the last time a session was committed. When initiate is called on the module, all the attributes are programmed to the hardware. If the computer has just been reset, or `niScope_ResetDevice` has just been called, the module is in the Idle state.

Wait for Start Trigger—On initiating an acquisition, the module transitions to this state. If the Start (Acquisition Arm) Trigger Source is configured to Immediate, the module immediately transitions out of this state and generates a Start Trigger Event. If the Start Trigger Source has been configured for software or hardware trigger from one of the available sources, the module remains in this state until the configured trigger occurs. When the module recognizes a trigger condition, it transitions out of this state on the next clock cycle and generates a Start Trigger Event. The default Start Trigger Source is Immediate.

Minimum Pre-Reference Trigger Sampling—The module can transition into this state two ways: receiving the Start (Acquisition Arm) Trigger from the Start (Acquisition Arm) Trigger Source or receiving the Advance Trigger from the Advance Trigger Source. Transitioning into this state depends on the previous state of the module. While in this state, the module samples according to the session attributes configured. The module remains in this state until three conditions are satisfied: the minimum Pre-Reference Trigger sampling completes, the TDC is ready, and the trigger-to-trigger holdoff count has expired. The minimum Pre-Reference Trigger sampling is at least the user-configured Minimum Record Length multiplied by the user-configured Reference Position. The first time through this state, the trigger-to-trigger holdoff does not have an effect. When the three conditions have been satisfied, the module transitions out of this state on the next clock cycle.

Wait for Arm Reference Trigger while Sampling—After the module finishes the Minimum Pre-Reference Trigger Sampling state, the module transitions into this state. While in this state, the module continues to acquire Pre-Reference Trigger samples according to the session attributes configured. If the Arm Reference Trigger Source is configured to Immediate, the module transitions out of this state on the next clock edge. If the Arm Reference Trigger Source has been configured for a software trigger or a hardware trigger from one of the available sources, the module remains in this state until the configured trigger occurs. When the module recognizes a trigger condition,

the module transitions out of this state. The default Arm Reference Trigger Source is Immediate.

Wait for Reference Trigger while Sampling—After the module receives Arm Reference Trigger from the Arm Reference Trigger Source, the module transitions into this state. If the Reference Trigger Source has been configured for a software or hardware trigger from one of the available sources, the module remains in this state until the configured trigger occurs. When the module recognizes a trigger condition, the module transitions out of this state. The default Reference Trigger Source is Immediate.

Post-Reference Trigger Sampling—After the module receives the Reference (Stop) Trigger, the module transitions into this state. At the beginning of this state, the module starts a trigger-to-trigger holdoff counter. This holdoff counter corresponds to the user-configurable **Trigger Holdoff** attribute and is used in the Minimum Pre-Reference Trigger Sampling State. You can use the **Trigger Holdoff** attribute to delay the module from looking for a Reference Trigger between records. At the same time, the trigger-to-trigger holdoff counter is started, the module begins sampling Post-Reference Trigger samples according to the session attributes configured. When the Post-Reference Trigger sampling is completed, the module transitions out of this state.

Record Complete—After the module completes Post-Reference Trigger sampling, the module transitions into this state. The module leaves this state after the current record has been stored in the onboard memory. Upon leaving this state, the module outputs an End of Record Event.

Wait for Advance Trigger—After the module has completed a record and determines that there are still more records to complete, the module transitions into this state. If the Advance Trigger Source is configured to immediate, the module transitions out of this state on the next clock edge. If the Advance Trigger Source has been configured for software or hardware trigger from one of the available sources, the module remains in this state until the configured trigger occurs. Upon the module recognizing a trigger condition, the module transitions out of this state. The default Advance Trigger Source is Immediate.

Done—After the module completes a record and determines that all the records are done, it transitions into this state. Upon entering this state, the module outputs the End of Acquisition Event, which is a temporary state. The software transitions the module out of this state and back to the Idle state when you call either Fetch or Check

Status.

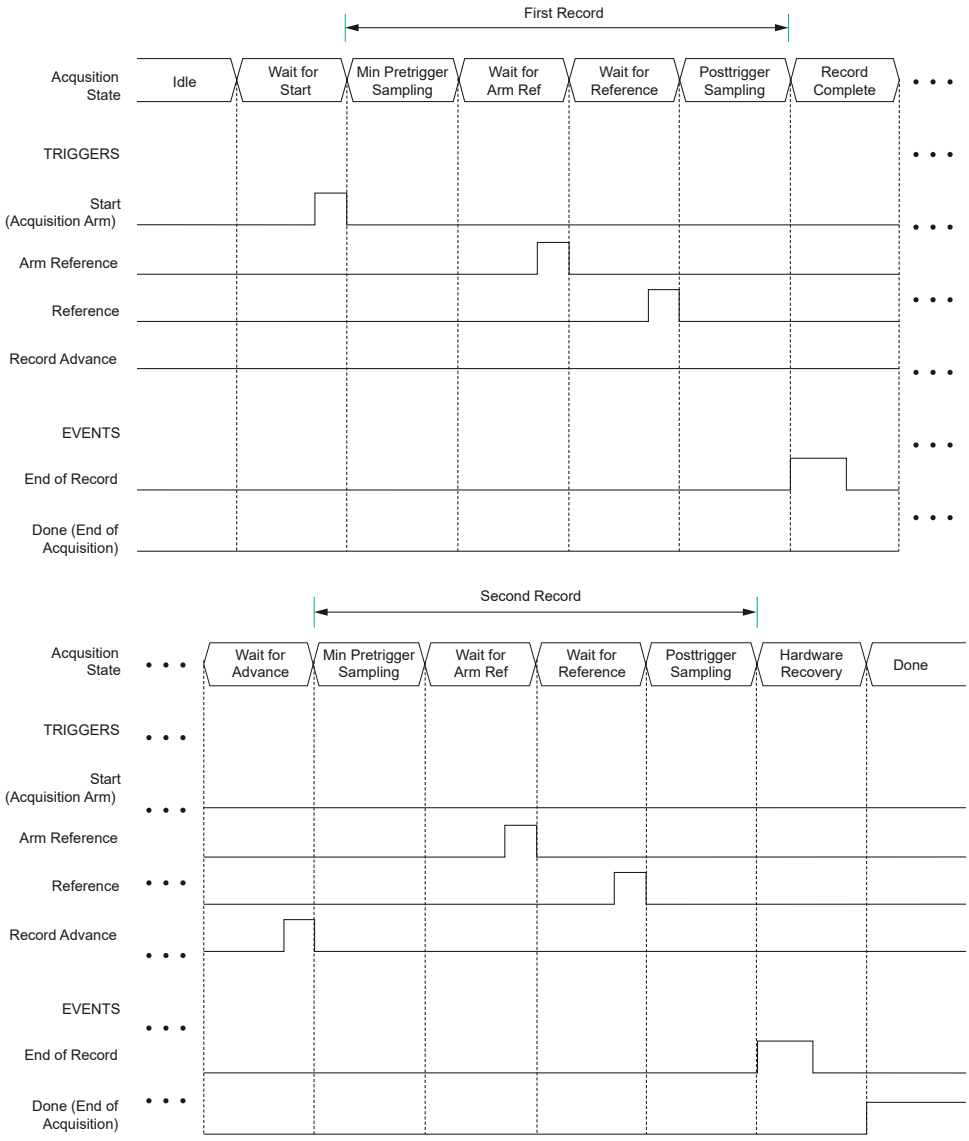
Related information:

- Triggering
- Trigger Types

SMC-Based Digitizers Timing Diagram

SMC-Based digitizers (NI 5105/5114/5122/5124/5142/5152/5153/5154/5160/5162/5622/5922) support multirecord acquisitions, which allow the capture of multiple triggered waveforms without software intervention. In this mode, the digitizer automatically begins storing a new record to onboard memory a short time after finishing the previous record. The number of records and record size are both configurable.

The following timing diagram illustrates how SMC-based digitizers react to the user-configurable input triggers during a multirecord acquisition.



Each state prefixed by Wait for is a state in which an input trigger can be configured. This trigger tells the digitizer when to transition out of that particular state. The hardware is only sensitive to a particular trigger when in that trigger's appropriate Wait for state. For example, the hardware is not sensitive to a high level on the Advance Trigger until it enters the Wait for the Advance trigger state.

Note The trigger signals in the timing diagram assume active high level triggers.

The exportable events are also shown in the timing diagram. The End of Record Event is generated once per record when the digitizer has acquired all of its pre- and post-

Reference Trigger samples. This signal can be used for handshaking between devices in a system. The Done Event asserts when all of the records have been completed, but it does not assert if the acquisition is aborted or times out.

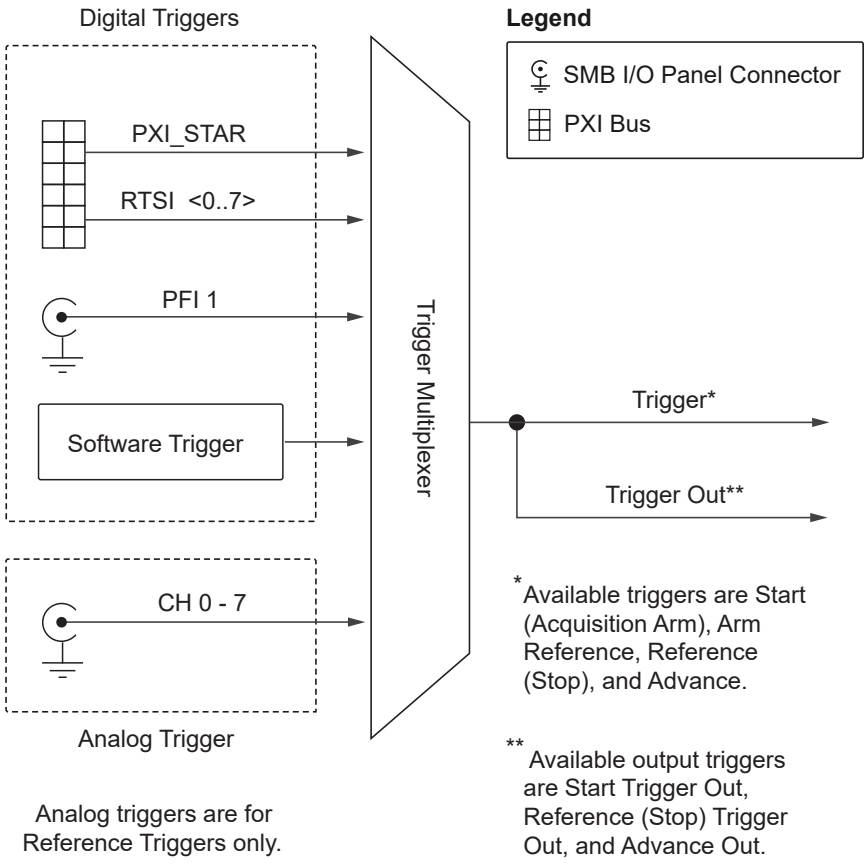
NI PXIe-5105 Routing Matrix

The following table shows the signals available for export from the NI PXIe-5105, and the lines to which they can be routed.

Source	**Destination**	
	PXI_Trig <0..6>(PXI Bus)	**PFI 1**
Exported Clocks		
Reference Clock (External)	—	√
Sample Clock (Full Rate)	—	√
Triggers		
Acquisition Arm (Start) Trigger	√	√
Reference (Stop) Trigger	√	√
Events		
End of Record Event	√	√
End of Acquisition Event	√	√
Ready for Start Event	√	√
Ready for Reference Event	√	√
Ready for Advance Event	√	√

NI PXIe-5105 Trigger Sources

The following figure shows the trigger sources for the NI PXIe-5105.



NI 5105 Trigger Types

The NI 5105 supports the following trigger types: edge, hysteresis, immediate, digital, software, and window triggers.

The NI 5105 uses the predecimated digitized data from the input channel ADC when performing an analog trigger on any of the channels. This behavior ensures a level and time trigger accuracy of 1 timebase clock period. Because the trigger detector circuit is after the ADC, there is a 24- to 30-sample delay when you export an analog trigger to another device.

Related information:

- Edge Triggers
- Hysteresis Triggers
- Immediate Triggers
- Digital Triggers

- Software Triggers
- Window Triggers

NI 5105 Trigger Holdoff

For the NI 5105, the holdoff timer is started by the Reference Trigger. When the current record finishes and the minimum number of pretrigger samples for the next record have been acquired, the holdoff timer is evaluated. If the timer has expired, the digitizer arms its Reference Trigger circuit. If the timer has not expired, the digitizer continues pretrigger sampling until the timer expires, and then arms its Reference Trigger circuit. Holdoff is applied for each Reference Trigger during a multirecord acquisition.

Related information:

- Trigger Holdoff

NI 5105 Trigger Delay

Trigger delay, which is specified in seconds, is achieved by adding the appropriate number of posttrigger samples to the record while keeping the allocated onboard memory equal to the record size you request. NI-SCOPE then corrects the trigger time by the delay you specify. To determine the maximum delay for a particular actual sample rate, use the following formula:

Max trigger delay in seconds = $[(2^{32} - 1) - \text{requested posttrigger samples}] \times (1/\text{actual sample rate})$

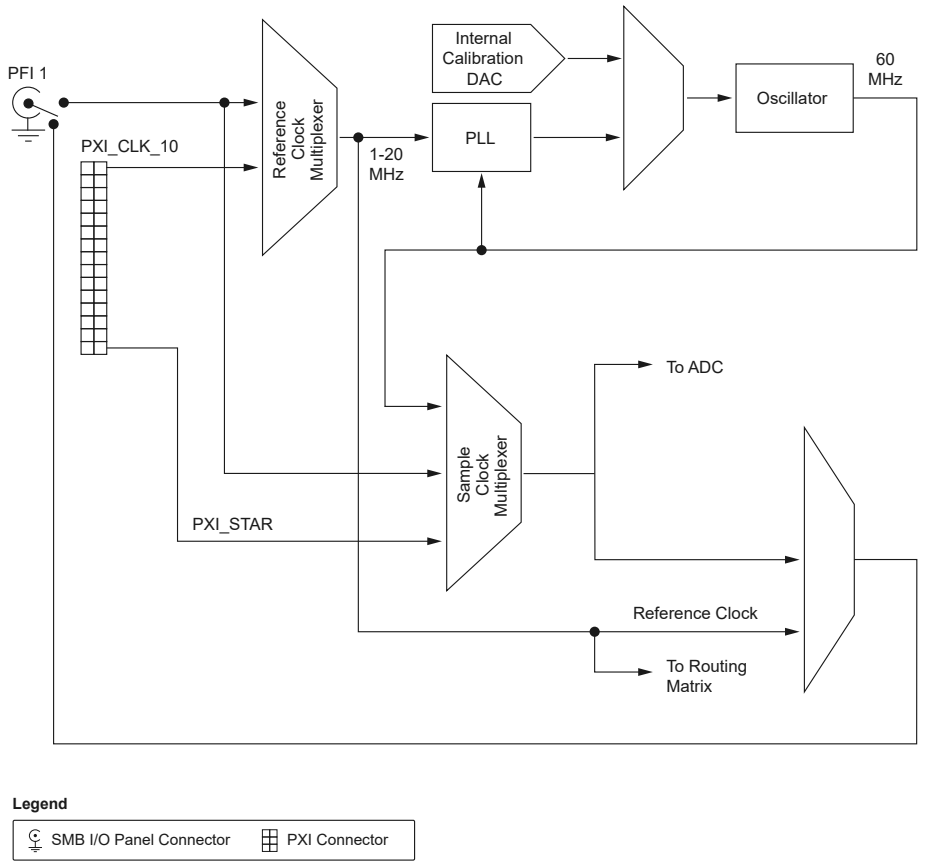
Note The maximum trigger delay changes when you use an external sample clock, and when you sample at rates other than full rate while using the internal sample clock.

Related information:

- Trigger Delay

PXIe-5105 Clocking

The clock circuitry on the PXIe-5105 offers versatile clocking options with its ability to use either the internal 60 MHz sample clock or to accept an external sample clock that you provide. You can also use the phase-locked loop (PLL) circuit on the PXIe-5105 to phase lock the internal 60 MHz sample clock with the PXI 10 MHz reference or with an external reference clock that you provide. The following diagram shows the clocking options of the PXIe-5105.



Sample Clock

The sample clock is sent to the ADC of each channel and to the input timing engine. The PXIe-5105 can decimate its sample clock (internal or external) by an integer divisor. When using an external clock, you can use decimation to achieve rates below the external clock frequency.

Internal Sample Clock

The PXIe-5105 has an onboard voltage controlled crystal oscillator (VCXO) running at 60 MHz. When using the onboard 60 MHz oscillator, you can choose either free-run mode or PLL mode. In free-run mode, the sample clock is the calibrated 60 MHz frequency of the VCXO. In PLL mode, the device phase locks its 60 MHz sample clock to the supplied reference clock. The PLL mode is useful when synchronizing the PXIe-5105 with other devices in a measurement system.

External Sample Clock

Some applications may require sampling at specific intervals that cannot be achieved by using the internal 60 MHz clock. In these cases, the PXIe-5105 can accept an external sample clock. External clocking also provides a method to synchronize the digitizer to other devices in a measurement system by distributing a common clock to multiple devices. An external sample clock can be supplied to the digitizer from the front panel connector or by routing the signal on the PXI backplane over the PXI star trigger line. Refer to the hardware specifications document for external sample clock requirements.

Reference Clock

The reference clock is used in the PXIe-5105 phase-locked loop (PLL) circuit to synchronize the sample clock to the reference clock. The PXIe-5105 can accept a reference clock from its front panel PFI 1 connector as well as from PXI_CLK10. This reference clock can be any frequency from 5 MHz to 20 MHz (in 1 MHz increments) if it is provided to PFI 1. The PXI_CLK10 is always a 10 MHz clock. The frequency stability of the sample clock matches that of the PLL reference clock when the two are phase locked. In turn, phase locking synchronizes clocks of multiple devices that are phase locked to the same reference clock. The default setting for the PXIe-5105 reference clock is `None`, or no reference clock is used.

Note Locking to a reference clock is not valid when using an external sample clock.

Exporting Clocks

The PFI 1 connector on the PXIe-5105 can be used for exporting the 60 MHz internal sample clock (full rate) or the reference clock when phase-locked to PXI_CLK10.

Related information:

- Reference Clock/Phase-Lock Loop
- PXI Star Trigger Line

NI 5105 Onboard Memory

The NI 5105 allocates at least 256 bytes of onboard memory for each record in a single multirecord acquisition. Samples are stored in this buffer before transfer to the host computer. Thus the minimum size for a buffer in the onboard memory is approximately 128 12-bit samples. Software allows you to specify buffers of less than these minimum buffer sizes but only the specified number of points are transferred from onboard memory into the host computer memory.

The total number of samples that can be stored depends on the acquisition memory size option. The maximum number of records in a single multirecord acquisition is determined by the the size of the memory option divided by 256 bytes (128 samples), as shown in the following equation:

$$[(\text{Record length}^* \times 2^\dagger \times \text{number of enabled channels}) + 480^\ddagger] \text{ rounded up to nearest 128 bytes}$$

Note: The maximum number of records is 100,000.

*samples

†bytes/sample

‡bytes

The memory options are 16 MB, 128 MB, or 512 MB, and the available memory is divided among all enabled channels.

Triggering and Memory Usage

During an acquisition, samples are stored in a circular buffer that is continually rewritten until a trigger is received. After the trigger is received, the NI 5105 continues to acquire posttrigger samples if you have specified a posttrigger sample count. The acquired samples are placed into onboard memory. The number of posttrigger or

pretrigger samples is only limited by the amount of onboard memory.

SMC-Based Device Synchronization

SMC-based digitizers are built on the National Instruments Synchronization and Memory Core (SMC) technology and therefore support TClk synchronization. Refer to the NI-TClk Synchronization Help for more information.

Related information:

- National Instruments Synchronization and Memory Core (SMC)
- NI-TClk Synchronization Help
- Features Supported by NI-SCOPE Instruments

SMC-Based Digitizers Multiple-Record Acquisition

SMC-based digitizers support multiple-record acquisition, which allows the capture of multiple triggered waveforms without software intervention. In this mode, the digitizer automatically begins a new acquisition in a new memory record soon after finishing the previous record. Multiple-record acquisitions can quickly acquire numerous triggered waveforms because they allow hardware rearming of the digitizer. Between each record, there is a dead time during which no triggers are accepted. During this time, the device sets up for the next record, as it transitions through the subsequent states of the SMC-Based Digitizers Acquisition Engine State Diagram. There is also a holdoff between the last trigger in a record and the trigger of a new record. This means that the minimum time between triggers is the greater of either:

- The between-record dead time plus the time per record, or
- The user-specified holdoff time (by default, the holdoff time = 0 s).

To increase the minimum time between triggers, use the trigger holdoff feature. For more information, refer to the SMC-Based Digitizers Acquisition Engine State Diagram.

Some digitizers specify a minimum rearm time. Minimum rearm time is the minimum time between reference triggers as the record length approaches a minimum (for example, record length = 1 sample).

The number of records that can be acquired varies depending on the memory option of the device. Depending on the digitizer, NI-SCOPE limits to approximately 100,000 records that can be configured without fetching during the acquisition. However, if an application allows for fetching records while they are being acquired, NI-SCOPE allows more records to be configured. Refer to Acquiring More Records Than Fit in Digitizer Memory for more information.

Related concepts:

- SMC-Based Digitizers Acquisition Engine State Diagram

Related information:

- Acquiring More Records Than Fit in Digitizer Memory
- Features Supported by NI-SCOPE Instruments
- Making Multiple-Record Acquisitions

NI 5105 Calibration

Every measurement instrument performs within its specifications over some finite temperature range and time period. If the temperature changes and time exceed those specified, and your application requires tight specifications, calibration is required.

For example, if the accuracy of a digitizer is specified as ±(1% of input + 10 mV), and you apply 5 V to the input, the error is:

1% of 5 V + 10 mV = 60 mV for temperature range 18-28 °C

This example demonstrates the traditional method of specifying accuracy. The problem with the traditional method is that in a system environment, temperature is not easily controlled. When a system is composed of multiple integrated instruments, the system is subject to temperature rise caused by inherent compromises in air circulation and other factors. Self-heating from surrounding equipment, uncontrolled manufacturing floor environment, and dirty fan filters are among these factors.

If the ambient temperature is outside of the 18-28 °C range, you may need to know exactly what the measurement accuracy is to compensate for this temperature

variation. With the traditional method, the only way to get the specified accuracy outside of the 18-28 °C range is to externally calibrate the system at the desired temperature. However, an external calibration is time-consuming and expensive and is infrequently done, so the specified accuracy is rarely obtained. You can learn more about external calibration at ni.com/calibration. In the example, if the ambient temperature of the digitizer is 48 °C, assuming the Tempco (TC) error is specified as

TC = (0.1% of input +1 mV)/ °C (a typical number is 10% of accuracy/ °C)

The additional error is

20 °C x TC = ±(2% of input + 20 mV) or 120 mV

The total error is three times the specified error (180 mV in the example above, versus 60 mV if temperature effect is ignored) due to the 48 °C ambient temperature.

Self-Calibration

To eliminate errors caused by changing temperatures, NI-SCOPE provides a highly repeatable self-calibration function.

For the NI 5105, this self-calibration capability yields the following benefits:

- Corrects for DC gain and offset errors within the digitizer by comparison to a precision, high-stability internal voltage reference. This is done for all ranges and all filter paths (enabled/disabled).
- Calibrates trigger timing to ensure accurate trigger timing and time-stamping.
- Calibrate the digital clock manager (DCM)
- Takes approximately 50 seconds to complete.

When to Self-Calibrate

For optimum performance, use self-calibration when the digitizer is placed in a new system, any time the temperature changes more than 5 °C from the previous self-calibration, or 90 days after the previous self-calibration. The result is a product that yields full performance over its operating temperature range and two-year calibration cycle for DC accuracy, AC response, and trigger level/timing. When the two-year calibration interval expires, an external calibration is required.

The NI 5105 has a temperature sensor that monitors temperature variations. The previous self-calibration time and date can also be read. Unless temperature variations are a serious problem, self-calibration is not recommended more than once per day.

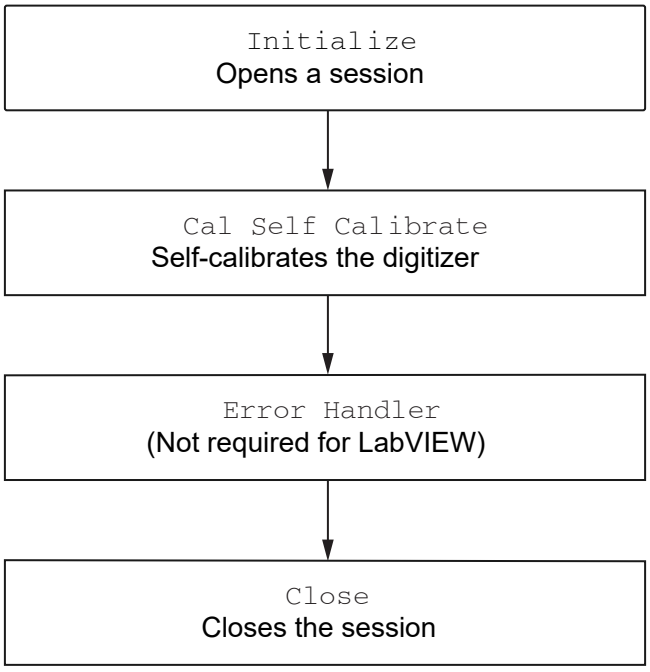
Input Connections During Self-Calibration

The NI 5105 internal circuitry is automatically isolated from the input during self-calibration. However, problems may occur if high-voltage, high-frequency signals (in excess of 500 V/µs slew rate) are present during self-calibration.

When in doubt, disconnect the inputs as directed. If you are absolutely certain that the maximum slew rate of the input signal is below 500 V/µs, then it is acceptable to leave the input signal connected during self-calibration.

Programming Flow

The following diagram shows the typical programming flow for self-calibration.



NI-SCOPE provides the `Calibrate` example, which you can find by using the shortcut at **Start»All Programs»National Instruments»NI-SCOPE»Examples**.

Summary of Calibration Options

A summary of the calibration options available and when to use them is shown in the following table.

Calibration	Impact	When	Notes
External calibration	Calibrate time drift of onboard reference	Every 2 years	Calibrates and verifies to full specifications
Self-calibration	Offset and gain Trigger timing	90 days, or when temperature changes >5 °C	Ensures range to range matching Ensures trigger accuracy
No calibration	None, within 2 year calibration cycle or if temperature stays within ±5 C	High accuracy not required outside of 5 °C	If self-calibration is not used, derate the accuracy using the specified Tempco

Related information:

- Calibration