PXIe-5164 Specifications

2025-04-23

Contents

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Definitions

Warranted specifications describe the performance of a model under stated operating conditions and are covered by the model warranty.

Characteristics describe values that are relevant to the use of the model under stated operating conditions but are not covered by the model warranty.

- ***Typical*** specifications describe the performance met by a majority of models.
- ***Nominal*** specifications describe an attribute that is based on design, conformance testing, or supplemental testing.

Conditions

Specifications are valid under the following conditions unless otherwise noted.

- All vertical ranges
- All bandwidths and bandwidth limit filters
- Sample rate set to 1 GS/s
- Onboard Sample Clock locked to onboard Reference Clock
- The PXIe-5164 is warmed up for 15 minutes at ambient temperature
- Calibration IP is used properly when using LabVIEW Instrument Design Libraries for Reconfigurable Oscilloscopes (instrument design libraries) to create FPGA bitfiles. Refer to the ***NI Reconfigurable Oscilloscopes Help*** for more information about the calibration API.

Warranted specifications are valid under the following conditions unless otherwise noted.

- Ambient temperature range of 0 °C to 50 °C
- Calibration cycle is maintained
- The PXI Express chassis fan speed is set to HIGH, the foam fan filters are removed if

present, and the empty slots contain PXI chassis slot blockers and filler panels. For more information about cooling, refer to the ***Maintain Forced-Air Cooling Note to Users*** available at ni.com/manuals.

- External calibration performed at 23 °C ±3 °C
- Within ±5 °C of temperature at last self-calibration as reported by onboard temperature sensor

Typical specifications are valid under the following conditions unless otherwise noted.

- Ambient temperature range of 0 °C to 50 °C

PXIe-5164 Front Panel

Figure 1. PXIe-5164 Front Panel

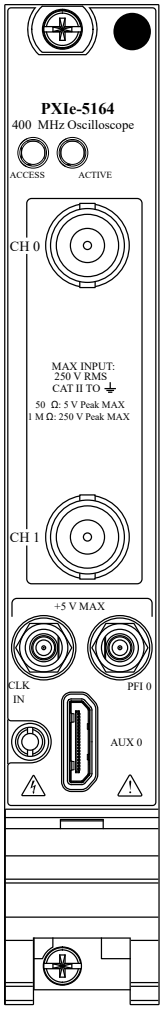


Table 1. Connectors

Signal	Connector Type	Description
CH 0 and CH 1	BNC female	Analog input connection; digitizes data and triggers acquisitions.
CLK IN	SMB	Imports an external reference clock or sample clock to the oscilloscope.
PFI 0	SMB	PFI line for digital trigger input/output, probe compensation.
AUX 0	MHDMR	Reference clock input, reference clock output, bidirectional digital PFI, and 3.3 V power output.

PXIe-5164 Pinout

Use the pinout to connect to terminals on the PXIe-5164.

Figure 1. PXIe-5164 AUX 0 Connector Pinout

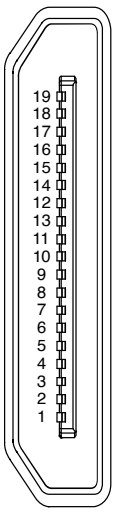


Table 2. AUX 0 Connector Pin Assignments

Pin	Signal	Signal Description
1	GND	Ground reference for signals
2	CLK IN	Used to import an external Reference Clock or Sample Clock
3	GND	Ground reference for signals
4	GND	Ground reference for signals
5	CLK OUT	Used to export the Reference Clock

Pin	Signal	Signal Description
6	GND	Ground reference for signals
7	GND	Ground reference for signals
8	AUX 0/PFI 0	Bidirectional PFI line
9	AUX 0/PFI 1	Bidirectional PFI line
10	GND	Ground reference for signals
11	AUX 0/PFI 2	Bidirectional PFI line
12	AUX 0/PFI 3	Bidirectional PFI line
13	GND	Ground reference for signals
14	AUX 0/PFI 4	Bidirectional PFI line
15	AUX 0/PFI 5	Bidirectional PFI line
16	AUX 0/PFI 6	Bidirectional PFI line
17	AUX 0/PFI 7	Bidirectional PFI line
18	+3.3 V	+3.3 V power (200 mA maximum)
19	GND	Ground reference for signals

PXIe-5164 SCB-19 Pinout

You can use the SCB-19 connector block to connect digital signals to the AUX 0 connector on the PXIe-5164 front panel. Refer to the following figure and table for information about the SCB-19 signals when connected to the AUX 0 front panel connector.

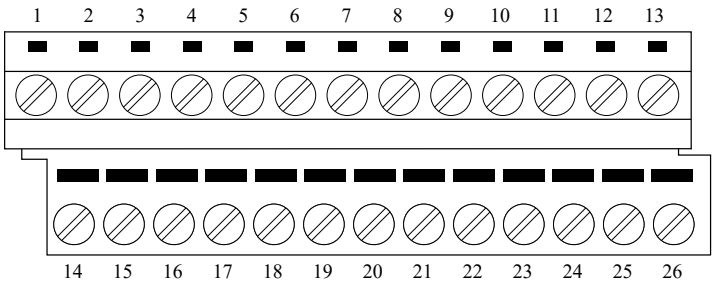


Table 3. SCB-19 Signal Descriptions

Pin	Signal	Signal Description
1	PFI 0	Bidirectional PFI line
2	PFI 1	Bidirectional PFI line
3	PFI 2	Bidirectional PFI line
4	PFI 3	Bidirectional PFI line
5	NC	No connection
6	CLK IN	Used to import an external reference clock or sample clock
7	NC	No connection
8	CLK OUT	Used to export the reference clock
9	PFI 4	Bidirectional PFI line
10	PFI 5	Bidirectional PFI line
11	PFI 6	Bidirectional PFI line
12	PFI 7	Bidirectional PFI line
13	+3.3 V	+3.3 V power (200 mA maximum)
14 to 26	GND	Ground reference for signals

PXIe-5164 AUX 0 Breakout Cable to 6 BNCs Pinout

You can use the AUX 0 Breakout Cable to 6 BNCs to connect digital signals to the AUX 0 connector on the PXIe-5164 front panel. Refer to the following figure and table for information about the AUX 0 Breakout Cable to 6 BNCs signals when connected to the AUX 0 front panel connector.

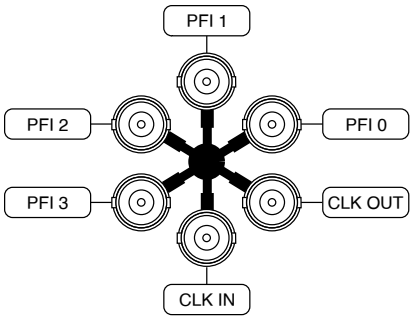


Table 4. AUX 0 Breakout Cable to 6 BNCs Signal Descriptions

Signal	Connector Type	Description
CLK IN	BNC female	Used to import an external reference clock
CLK OUT		Used to export the reference clock
PFI 0		Bidirectional PFI line
PFI 1		Bidirectional PFI line
PFI 2		Bidirectional PFI line
PFI 3		Bidirectional PFI line

Vertical

Analog Input

Number of channels	Two (simultaneously sampled)
Input type	Referenced single-ended
Connectors	BNC, ground referenced

Impedance and Coupling

Input impedance	50 Ω ±1.25%, typical

	1 MΩ ±0.5%, typical
Input capacitance (1 MΩ)	20.2 pF ±2.5 pF, typical
Input coupling	AC DC

Figure 1. 50 Ω Voltage Standing Wave Ratio (VSWR)

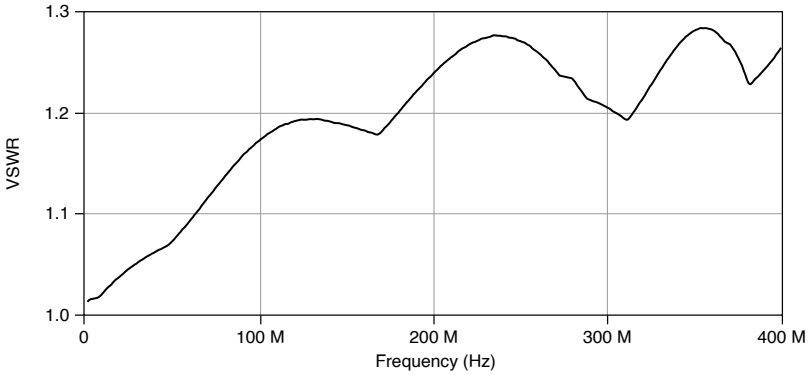
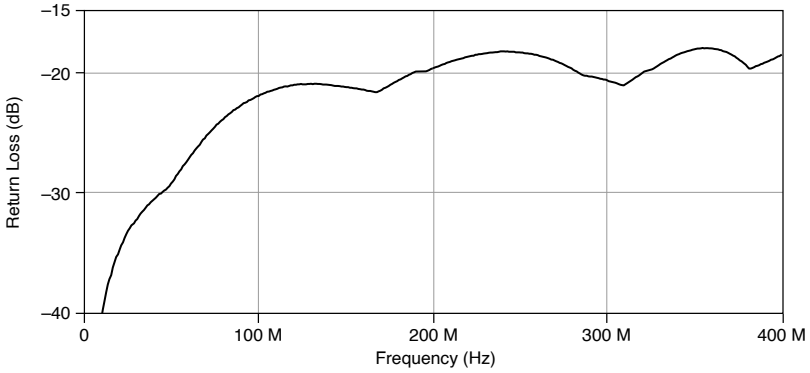


Figure 1. 50 Ω Input Return Loss



Voltage Levels

50 Ω FS input range (V_{pk-pk})	0.25 V 0.5 V 1 V

	2.5 V 5 V

Table 5. 1 MΩ FS Input Range and Vertical Offset Range

Input Range (V_{pk-pk})	Vertical Offset Range[1] (V)
0.25 V	±5
0.5 V	±5
1 V	±5
2.5 V	±10 or ±248.75
5 V	±10 or ±247.5
10 V	±10 or ±245
25 V	±50 or ±237.5
50 V	±50 or ±225
100 V	±50 or ±200

Maximum input overload	
50 Ω	|Peaks| ≤5 V
1 MΩ [2] [2]	250 V RMS

Notice Signals exceeding the maximum input overload may cause damage to the device.

1. For input ranges between 2.5 V_{pk-pk} and 100 V_{pk-pk}, two offset ranges are possible. The driver software automatically picks the offset range that provides the highest resolution and accuracy.
2. Derate above 500 kHz at 20 dB/dec until 5 MHz, then derate at 10 dB/dec.

Accuracy

Resolution	14 bits
DC accuracy[3][3],4[4]	
50 Ω	±+(0.5% × |***Reading***|) + (0.2% of FS)+, warranted
1 MΩ	±[(0.65% × |***Reading*** - ***Vertical Offset***|) + (0.4% × |***Vertical Offset***|) + (0.2% of FS) + 0.15 mV], warranted
DC drift[5][5]	±[(0.015% × |***Reading*** - ***Vertical Offset***|) + (0.001% × |***Vertical Offset***|) + (0.009% of FS)] per °C, nominal
AC amplitude accuracy[3]	±0.2 dB at 50 kHz, warranted

Table 6. Crosstalk 50 Ω, Nominal

Frequency	Level
1 MHz	-100 dB
10 MHz	-100 dB
100 MHz	-85 dB
400 MHz	-65 dB

3. Within ± 5 °C of self-calibration temperature.
4. Applies after averaging data for 8.5 ms
5. Used to calculate errors when on board temperature changes more than ±5 °C from the self-calibration temperature.

Table 7. Crosstalk 1 MΩ, Nominal

Frequency	Level	
	0.25 V_{pk-pk} to 10 V_{pk-pk}	25 V_{pk-pk} to 100 V_{pk-pk}
1 MHz	-85 dB	-70 dB
10 MHz	-85 dB	-70 dB
100 MHz	-75 dB	-55 dB
300 MHz	-60 dB	-40 dB

Note Crosstalk measurements were measured on one channel with a test signal applied to another channel, with the same range setting on both channels.

Bandwidth and Transient Response

Bandwidth (-3 dB)[6]	
50 Ω	400 MHz, warranted
1 MΩ [7]	300 MHz 285 MHz, warranted
Bandwidth-limiting filters[6]	
Low-pass filters	20 MHz [8] 30 MHz [8] 150 MHz

6. Normalized to 50 kHz.
7. Verified using a 50 Ω source and 50 Ω feedthrough terminator.
8. Only available in NI-SCOPE.

High-pass filters[8]	90 Hz 450 Hz
Passband amplitude flatness[6]	
50 Ω	±0.5 dB from 50 kHz to 330 MHz, warranted
1 MΩ [7]	±0.7 dB from 50 kHz to 200 MHz, warranted
AC-coupling cutoff (-3 dB)[9][9]	
50 Ω	40 kHz
1 MΩ [7]	7.5 Hz
Rise/fall time[10][10]	
50 Ω	1 ns
1 MΩ [7]	1.5 ns

9. Verified using a 50 Ω source.
10. 50% FS input pulse.

Figure 1. 50 Ω Full Bandwidth Frequency Response, 1 V_{pk-pk}, Measured

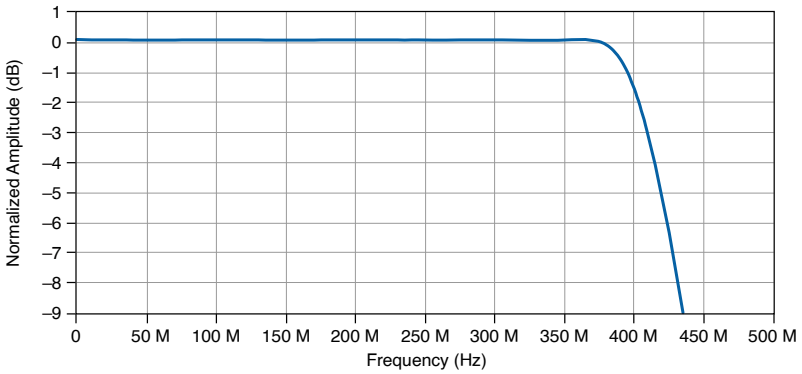


Figure 1. 50 Ω Full Bandwidth Frequency Response Zoomed, 1 V_{pk-pk}, Measured

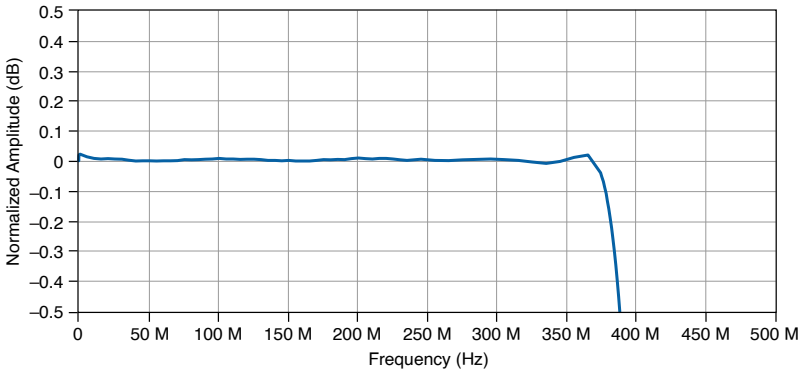


Figure 1. 50 Ω 150 MHz Bandwidth Frequency Response, 1 V_{pk-pk}, Measured

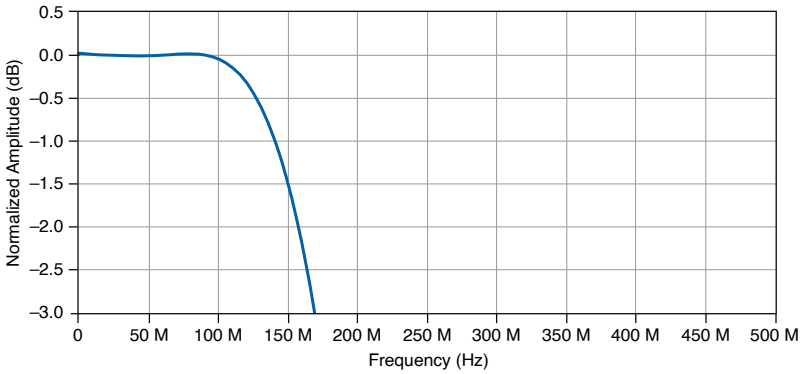


Figure 1. 1 MΩ Full Bandwidth Frequency Response, 1 V_{pk-pk}, Measured

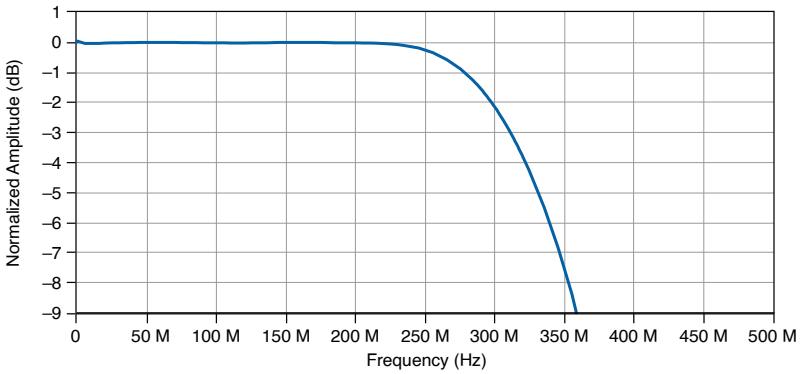


Figure 1. 1 MΩ Full Bandwidth Frequency Response Zoomed, 1 V_{pk-pk}, Measured

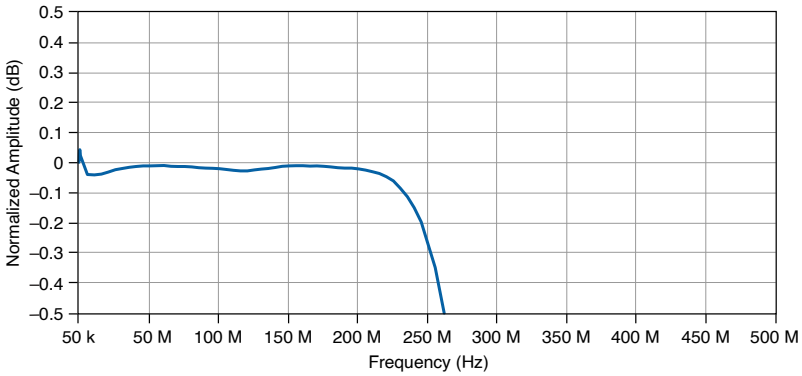
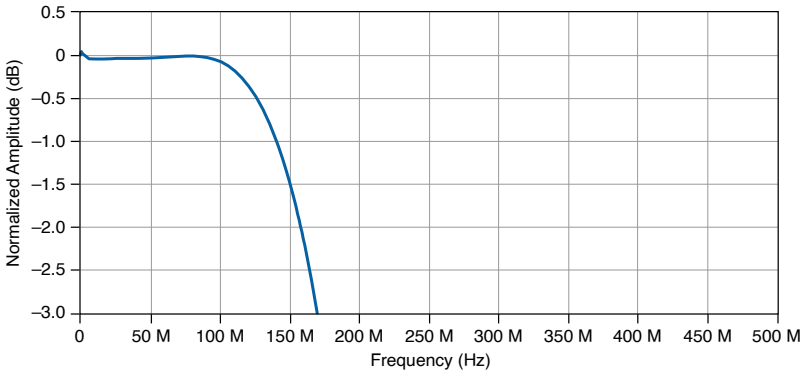


Figure 1. 1 MΩ 150 MHz Bandwidth Frequency Response, 1 V_{pk-pk}, Measured



Spectral Characteristics

50 Ω Spectral Characteristics Excludes ADC Interleaving spurs. 1

Table 8. Spurious-Free Dynamic Range (SFDR)[11]

Input Range (V_{pk-pk})	<100 MHz, Full Bandwidth (dBc)	>100 MHz to <350 MHz, Full Bandwidth (dBc)
0.25 V	-70	-66
0.5 V	-73	-65
1 V	-74	-66
2.5 V	-71	-63
5 V	-69	-60

11. -1 dBFS input signal corrected to FS. 1 kHz resolution bandwidth.

Table 9. Total Harmonic Distortion (THD)[12][12]

Input Range (V_{pk-pk})	<100 MHz, Full Bandwidth (dBc)	>100 MHz to <350 MHz, Full Bandwidth (dBc)
0.25 V	-70	-62
0.5 V	-73	-61
1 V	-73	-62
2.5 V	-70	-62
5 V	-70	-60

Table 10. Effective Number of Bits (ENOB)[11]

Input Range (V_{pk-pk})	<350 MHz, Full Bandwidth	<100 MHz, 150 MHz Filter	<10 MHz, 20 MHz, and/or 30 MHz Filter
0.25 V	9.4	10.7	11.6
0.5 V	9.5	10.9	11.7
1 V	9.5	11.0	11.8
2.5 V	9.6	11.1	11.9
5 V	9.5	11.0	11.8

1 MΩ Spectral Characteristics Excludes ADC Interleaving spurs. , Verified using a 50 Ω source and 50 Ω feedthrough terminator. 5

Table 11. Spurious-Free Dynamic Range (SFDR)[11]

Input Range (V_{pk-pk})	<100 MHz, Full Bandwidth (dBc)	>100 MHz to <250 MHz, Full Bandwidth (dBc)
0.25 V	-61	-57
0.5 V	-56	-50
1 V	-49	-43
2.5 V	-59	-55

12. -1 dBFS input signal corrected to FS. Includes the second through the fifth harmonics.

Input Range (V_{pk-pk})	<100 MHz, Full Bandwidth (dBc)	>100 MHz to <250 MHz, Full Bandwidth (dBc)
5 V	-53	-47

Table 12. Total Harmonic Distortion (THD)[12]

Input Range (V_{pk-pk})	<50 MHz, Full Bandwidth (dBc)	50 MHz to 250 MHz, Full Bandwidth (dBc)
0.25 V	-73	-58
0.5 V	-68	-50
1 V	-62	-43
2.5 V	-70	-56
5 V	-64	-48

Table 13. Effective Number of Bits (ENOB)[11]

Input Range (V_{pk-pk})	<250 MHz, Full Bandwidth	<100 MHz, 150 MHz Filter	<10 MHz, 20 Mhz, and/or 30 MHz Filter
0.25 V	8.8	9.6	10.5
0.5 V	8.1	9.8	11.1
1 V	7.0	9.0	11.5
2.5 V	8.6	9.5	10.4
5 V	7.7	9.5	11.1

Figure 1. 50 Ω Single-Tone Spectrum, 1 V_{pk-pk}Input Range, 150 MHz Filter, 9.9 MHz Input Tone at

-1 dBFS, Measured

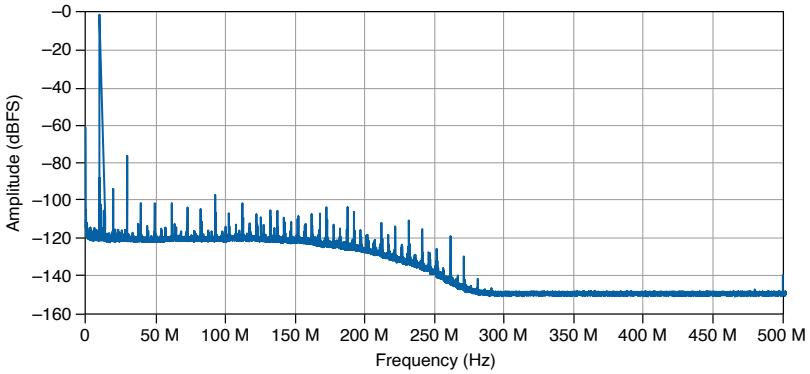


Figure 1. 50 Ω Single-Tone Spectrum, 1 $V_{pk\text{-}pk}$ Input Range, Full Bandwidth, 9.9 MHz Input Tone at -1 dBFS, Measured

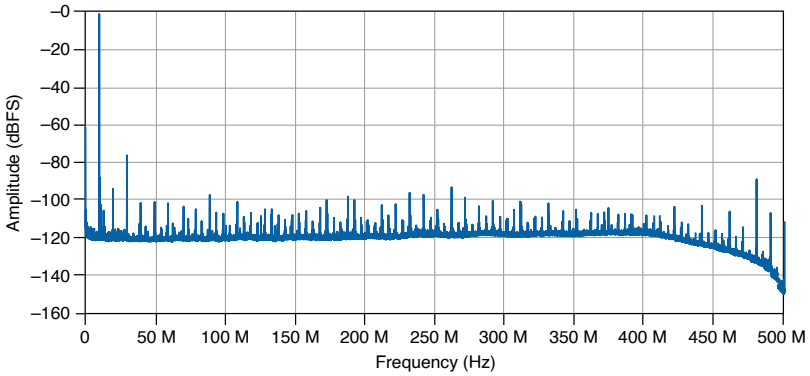


Figure 1. 50 Ω Single-Tone Spectrum, 1 $V_{pk\text{-}pk}$ Input Range, Full Bandwidth, 99.9 MHz Input Tone at -1 dBFS, Measured

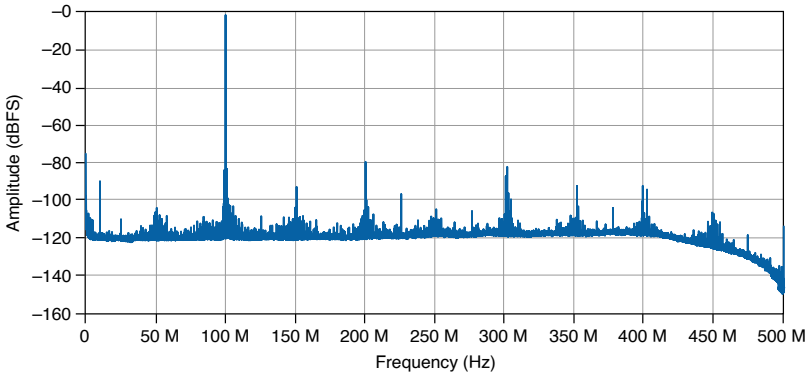


Figure 1. 1 MΩ Single-Tone Spectrum, 1 $V_{pk\text{-}pk}$ Input Range, 150 MHz Filter, 9.9 MHz Input Tone at

-1 dBFS, Measured

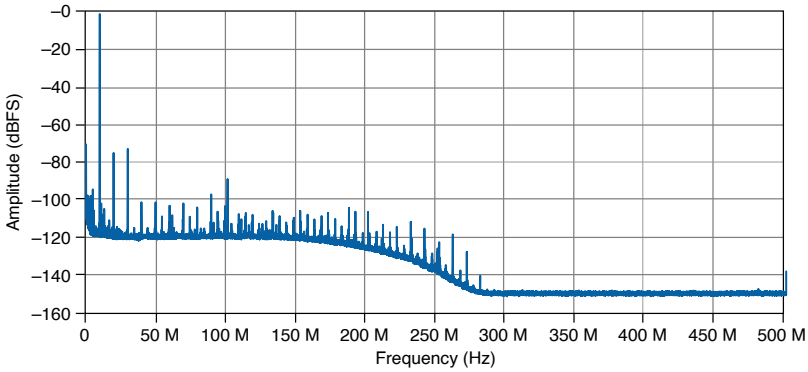
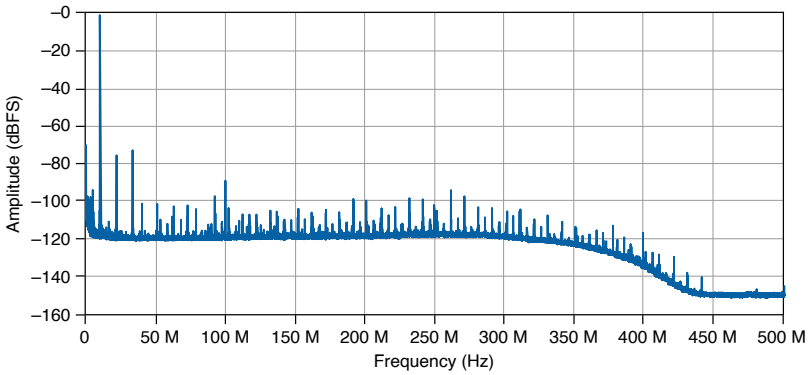


Figure 1. 1 MΩ Single-Tone Spectrum, 1 V_{pk-pk} Input Range, Full Bandwidth, 9.9 MHz Input Tone at -1 dBFS, Measured



Noise[13]

50 Ω RMS Noise

Table 14. RMS Noise (Full Bandwidth), Warranted

Input Range (V_{pk-pk})	RMS Noise (% of Full Scale)
0.25 V	0.045
0.5 V	0.040
1 V	0.035
2.5 V	0.030
5 V	0.030

13. Verified with 50 Ω terminator connected directly to BNC input.

Table 15. RMS Noise (150 MHz Filter), Typical

Input Range (V_{pk-pk})	RMS Noise (% of Full Scale)
0.25 V	0.018
0.5 V	0.018
1 V	0.017
2.5 V	0.017
5 V	0.014

Figure 1. 50 Ω Channel 0 Average Noise Density, 1 V_{pk-pk}Range, Measured

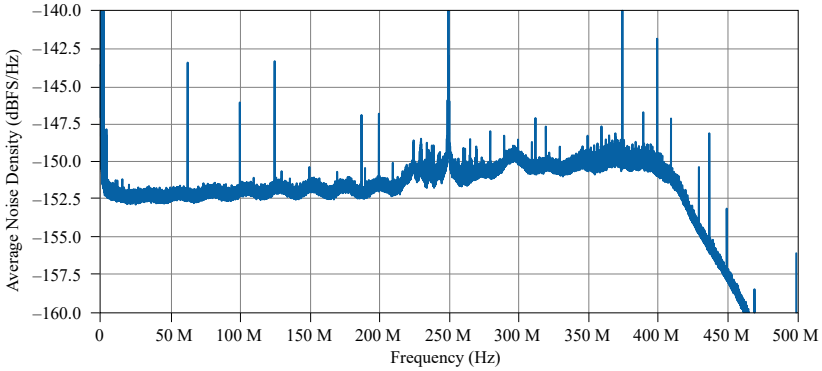
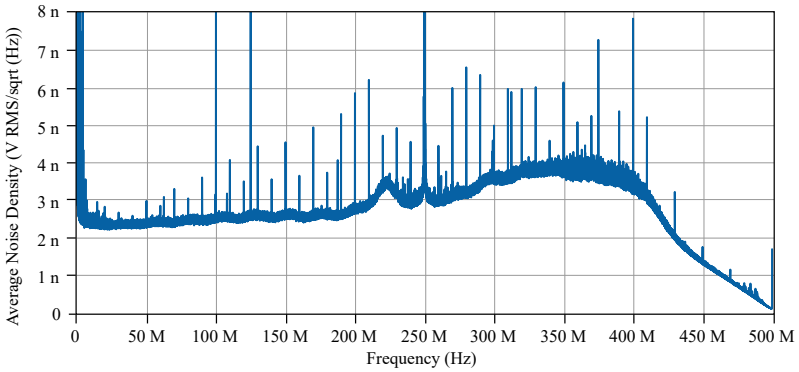


Figure 1. 50 Ω Channel 0 Average Noise Density, 0.25 V_{pk-pk} Range, Measured



1 MΩ RMS Noise

Table 16. RMS Noise (Full Bandwidth)

Input Range (V_{pk-pk})	RMS Noise (% of Full Scale), Warranted
0.25 V	0.110
0.5 V	0.060

Input Range (V_{pk-pk})	RMS Noise (% of Full Scale), Warranted
1 V	0.050
2.5 V	0.100
5 V	0.060
10 V	0.050
25 V	0.080
50 V	0.060
100 V	0.050

Table 17. RMS Noise (150 MHz Filter), Typical

Input Range (V_{pk-pk})	RMS Noise (% of Full Scale)
0.25 V	0.070
0.5 V	0.050
1 V	0.030
2.5 V	0.100
5 V	0.050
10 V	0.030
25 V	0.060
50 V	0.040
100 V	0.030

Horizontal

Sample Clock

Sources	
Internal	Onboard clock (internal VCTCXO)
External	CLK IN (front panel SMB connector)

	PXIe-DSTAR_A (backplane connector)
Sample rate range, real-time[14]	15.259 kS/s to 1 GS/s
Timebase frequency	1.0 GHz
Timebase accuracy	
Phase-locked to onboard clock	±5 ppm, warranted
Phase-locked to external clock	Equal to the external clock accuracy
Sample clock jitter[15]	500 fs RMS

Phase-Locked Loop (PLL) Reference Clock

Sources	
Internal	Onboard clock (internal VCTCXO) PXI_CLK10 (backplane connector)
External (10 MHz)	CLK IN (front panel SMB connector) AUX 0 CLK IN (front panel MHDMR connector)
Duty cycle tolerance	45% to 55%, typical

14. Divide by n decimation from 1.0 GS/s used for all rates less than 1.0 GS/s. For more information about the sample clock and decimation, refer to the ***NI High-Speed Digitizers Help***.
15. Integrated from 100 Hz to 10 MHz. Includes the effects of the converter aperture uncertainty and the clock circuitry jitter. Excludes trigger jitter.

External Sample Clock

Source	CLK IN (front panel SMB connector)
Impedance	50 Ω
Coupling	AC
Frequency	1.0 GHz
Input voltage range, when configured as a sample clock	632 mV_{pk-pk} to 5 V_{pk-pk} (0 dBm to 18 dBm), typical
Maximum input overload, when configured as a sample clock	6 V_{pk-pk}
Duty cycle tolerance	45% to 55%, typical

External Reference Clock In

Sources	CLK IN (front panel SMB connector) AUX 0 CLK IN (front panel MHDMR connector)
Impedance	50 Ω
Coupling	AC

Frequency[16]	10 MHz
Input voltage range, when configured as a reference clock	623 mV_{pk-pk} to 5 V_{pk-pk} (0 dBm to 18 dBm), typical
Maximum input overload, when configured as a reference clock	6 V_{pk-pk}

Reference Clock Out

Source	PXI_CLK10 (backplane connector)
Destination	AUX 0 CLK OUT (front panel MHDMR connector)
Output impedance	50 Ω
Logic type	3.3 V CMOS
Maximum current drive	±12 mA

Trigger

Supported triggers	Reference (stop) trigger Reference (arm) trigger Start trigger

16. The PLL reference clock must be accurate to ±25 ppm.

	Advance trigger
Trigger types	Edge Window Hysteresis Digital Immediate Software
Trigger sources	CH 0 CH 1 SMB PFI 0 AUX 0 PFI <0..7> PXI_Trig <0..6> Software
Trigger delay	from 0 ns to 2.25×10^{15} ns $((2^{51} - 1) \times$ ***Sample Clock Period*** ns)
Dead time	496 ns
Hold off	From dead time to 1.84×10^{19} ns $((2^{64} - 1) \times$ ***Sample Clock Period*** ns)

For more information about triggers, refer to ***Triggering*** in ***NI-SCOPE***.

Related information:

- Triggering

Analog Trigger

Sources		CH 0 CH 1
Time resolution		
Interpolator enabled[17]	***Sample Clock Period*** / 1024 = 0.977 ps	
Interpolator disabled	Sample clock period (1 ns)	
Trigger filters		
Low Frequency (LF) Reject		100 kHz
High Frequency (HF) Reject		100 kHz
Trigger accuracy[18][18]		0.5% of FS
Trigger jitter[18]		15 ps RMS
Minimum threshold duration[19]		Sample clock period

17. Requires NI-SCOPE.
18. Analog triggers. For input frequencies less than 250 MHz.
19. Data must exceed each corresponding trigger threshold for at least the minimum duration to ensure analog triggering.

Digital Trigger

Sources	PFI 0 (front panel SMB connector) AUX 0 PFI <0..7> (front panel MHDMR connector) PXI_Trig <0..6> (backplane connector)
Time resolution	8 ns
Approximate trigger delay difference between analog edge trigger and digital trigger source[20]	1275 ns, nominal

Related information:

- Characterizing Setup to Account for Delay on Digital Trigger

Programmable Function Interface

Connectors	AUX 0 PFI <0..7> (front panel MHDMR connector) PFI 0 (front panel SMB connector)
Direction	Bidirectional per channel

20. This value is approximate because changes to the digital trigger routing or the analog signal path affect propagation delay. You can compensate for the delay difference by adjusting the NI-SCOPE trigger delay value. Add an additional 80 ns trigger delay when passing a trigger between PXIe-5164 modules. With the same hardware and software configuration, the trigger delay difference is consistent within the timing resolution across modules of the same model. For more information about the trigger delay difference, refer to ***Characterizing Setup to Account for Delay on Digital Trigger***.

Direction control latency	125 ns
As an Input (Trigger)	
Destination	FPGA diagram Start trigger (acquisition arm) Reference (stop) trigger Arm Reference Trigger Advance trigger
Input impedance	49.9 kΩ
V_{IH}	2 V, typical
V_{IL}	0.8 V, typical
Recommended input range	3.3 V
Maximum input overload	0 to 3.3 V 5 V tolerant
Maximum frequency	50 MHz
Minimum pulse width	10 ns
As an Output (Event)	

Sources	FPGA diagram Ready for Start Start trigger (acquisition arm) Ready for Reference Reference (stop) trigger End of Record Ready for Advance Advance trigger Done (end of acquisition) Probe Compensation[21]
Output impedance	50 Ω
Logic type	3.3 V CMOS
Maximum current drive	12 mA
Maximum frequency	50 MHz
Minimum pulse width	10 ns

21. 1 kHz, 50% duty cycle square wave, SMB PFI 0 only.

AUX 0 Connector Specifications

Connector	MHDMR
Voltage output	3.3 V ±10%
Maximum current drive on +3.3 V	200 mA
Output impedance on +3.3 V	<1 Ω

Waveform Specifications

Onboard memory size[22]	1.5 GB
Minimum record length	1 sample
Number of pretrigger samples	Zero up to (***Record Length*** - 1)
Number of posttrigger samples	Zero up to ***Record Length***
Maximum number of records in onboard memory[23]	4,194,304 for 1.5 GB

22. Onboard memory is shared among all enabled channels.
23. You can exceed these numbers if you fetch records while acquiring data. For more information, refer to the ***NI High-Speed Digitizers Help***.

Table 18. Examples of Allocated Onboard Memory Per Record (1.5 GB Onboard Memory)

Channels	Bytes per Sample	Max Records per Channel	Record Length	Allocated Onboard Memory per Record
1	2	4,194,304	1	384
1	2	671,088	1,000	2,400
1	2	79,137	10,000	20,352
1	2	1	805,306,192	1,610,612,736
2	2	4,194,304	1	384
2	2	364,722	1,000	4,416
2	2	39,850	10,000	33,216
2	2	1	402,653,096	1,610,612,736

Memory Sanitization

For information about memory sanitization, refer to the letter of volatility for your device, which is available at ni.com/manuals.

FPGA

FPGA model	Xilinx Kintex-7 XC7K410T FPGA
Xilinx Kintex-7 XC7K410T FPGA Resources	
Slice registers	508,400
Slice look-up tables (LUT)	254,200
DSPs	1,540

18 Kb block RAMs	1,590

Note Note that some of these resources are consumed by the logic necessary to operate the device and integrate with software, and are thus out of the control of users.

Calibration

External Calibration

External calibration yields the following benefits:

- Corrects for gain and offset errors of the onboard references used in self-calibration.
- Adjusts timebase accuracy.
- Compensates the 1 MΩ ranges.
- Corrects the frequency response for all ranges.

All calibration constants are stored in nonvolatile memory.

Self-Calibration

Self-calibration is done on software command. The calibration corrects for the following aspects:

- Gain
- Offset
- Interleaving spurs
- Intermodule synchronization errors

Refer to the ***NI High-Speed Digitizers Help*** for information about when to self-calibrate the device.

Calibration Specifications

Interval for external calibration	2 years
Warm-up time[24]	15 minutes

Software

Driver Software

This device was first supported in NI-SCOPE16.1 and NI LabVIEW Instrument Design Libraries for Reconfigurable Oscilloscopes16.1. NI LabVIEW Instrument Design Libraries for Reconfigurable Oscilloscopes is an IVI-compliant driver that allows you to configure, control, and calibrate the device. NI-SCOPE provides application programming interfaces for many development environments.

Application Software

NI-SCOPE provides programming interfaces, documentation, and examples for the following application development environments:

- LabVIEW
- LabWindows™/CVI™
- Measurement Studio
- Microsoft Visual C/C++
- .NET (C# and VB.NET)

Interactive Soft Front Panel and Configuration

When you install NI-SCOPE on a 64-bit system, you can monitor, control, and record

24. Warm-up begins after the chassis and controller or PC is powered, the device is recognized by the host, and the device is configured using the instrument design libraries or NI-SCOPE. Running an included sample project or running self-calibration using MAX will configure the device and start warm-up. Self-calibration is recommended following the specified warm-up time. In some RIO applications, the power consumed by the module can be significantly higher than the default image for the module. In these cases, you can improve performance by loading your image and configuring the device before warm-up time begins.

measurements from the PXIe-5164 using InstrumentStudio.

InstrumentStudio is a software-based front panel application that allows you to perform interactive measurements on several different device types in a single program.

Note InstrumentStudio is supported only on 64-bit systems. If you are using a 32-bit system, use the NI-SCOPE–specific soft front panel instead of InstrumentStudio.

Interactive control of the PXIe-5164 was first available via InstrumentStudio in NI-SCOPE18.1 and via the NI-SCOPE SFP in NI-SCOPE16.1. InstrumentStudio and the NI-SCOPE SFP are included on the NI-SCOPE media.

NI Measurement & Automation Explorer (MAX) also provides interactive configuration and test tools for the PXIe-5164. MAX is included on the driver media.

Synchronization

Channel-to-channel skew, between the channels of a PXIe-5164	
Channel-to-channel skew (full bandwidth)	
50 Ω	<100 ps
1 MΩ	<150 ps

Synchronization with the NI-TClk API

NI-TClk is an API that enables system synchronization of supported PXI modules in one or more PXI chassis, which you can use with the PXIe-5164 and NI-SCOPE. NI-TClk installs with NI-SCOPE.

NI-TClk uses a shared Reference Clock and triggers to align the Sample Clocks of PXI modules and synchronize the distribution and reception of triggers. These signals are routed through the PXI chassis backplane without external cable connections between

PXI modules in the same chassis.

Module-to-module skew, between PXIe-5164 modules using NI-TClk [25]	
NI-TClk synchronization without manual adjustment [26] [26]	
Skew, Peak-to-Peak [27] [27]	300 ps
NI-TClk synchronization with manual adjustment [26]	
Skew after manual adjustment	≤10 ps
Sample Clock delay/adjustment resolution	3.5 ps

Related information:

- NI-TClk Overview

Bus Interface

Form factor	PXI Express (x8 Gen 2)

25. Although you can use NI-TClk to synchronize non-identical modules, these specifications apply only to synchronizing identical modules. Specifications are valid under the following conditions:

    - All modules installed in the same PXI Express chasses.
    - NI-TClk used to align the sample clocks of each module.
    - All parameters set to identical values for each module.
    - Self-calibration completed.
    - Ambient temperature within ±1 °C of self-calibration.

    For other configurations, including multi-chassis systems, contact NI Technical Support at ***ni.com/support***.
26. Manual adjustment is the process of minimizing synchronization jitter and skew by adjusting Trigger Clock (TClk) signals using the instrument driver.
27. Caused by clock and analog delay differences. Tested with a PXIe-1082 chassis with maximum slot to slot skew of 100 ps.

Slot compatibility	PXI Express or hybrid
DMA channels	32

Power Requirements

+3.3 V DC	6.5 W
+12 V DC	18.5 W
Total power[28]	25 W
Total maximum power allowed[29]	38.25 W

Physical

Dimensions	3U, one-slot, PXI Express Gen 2 x8 module 21.26 cm × 12.88 cm × 2.0 cm (8.37 in × 5.07 in × 0.787 in)
Weight	460 g (16.2 oz)

28. Power consumed depends on the FPGA image and driver software used. This specification represents the maximum power for the NI-SCOPE use case or typical value when using the Instrument Design Libraries (IDL).
29. Maximum allowable power when using a custom LabVIEW FPGA image.

Environmental Characteristics

Temperature	
Operating	0 °C to 50 °C
Storage	-40 °C to 71 °C
Humidity	
Operating	10% to 90%, noncondensing
Storage	5% to 95%, noncondensing
Pollution Degree	2
Maximum altitude	4,600 m (570 mbar) (at 25 °C ambient temperature)
Shock and Vibration	
Operating vibration	5 Hz to 500 Hz, 0.3 g RMS
Non-operating vibration	5 Hz to 500 Hz, 2.4 g RMS
Operating shock	30 g, half-sine, 11 ms pulse